

Article

# A Highly Sensitive CMOS Digital Hall Sensor for Low Magnetic Field Applications

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Received: 22 December 2011; in revised form: 20 January 2012 / Accepted: 21 January 2012 /

Published: 15 February 2012

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**Abstract:** Integrated CMOS Hall sensors have been widely used to measure magnetic fields. However, they are difficult to work with in a low magnetic field environment due to their low sensitivity and large offset. This paper describes a highly sensitive digital Hall sensor fabricated in 0.18  $\mu\text{m}$  high voltage CMOS technology for low field applications. The sensor consists of a switched cross-shaped Hall plate and a novel signal conditioner. It effectively eliminates offset and low frequency 1/f noise by applying a dynamic quadrature offset cancellation technique. The measured results show the optimal Hall plate achieves a high current related sensitivity of about 310 V/AT. The whole sensor has a remarkable ability to measure a minimum  $\pm 2$  mT magnetic field and output a digital Hall signal in a wide temperature range from  $-40$  °C to 120 °C.

**Keywords:** Hall sensor; CMOS technology; dynamic offset cancellation; chopped technique

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## 1. Introduction

Presently, Hall magnetic field sensors are widely established for their great applications in industrial control systems, intelligent instruments, and consumer electronic products, *etc.* They are used not only for direct measurement of magnetic fields, but also for non-direct measurements, like speed or position, *etc.* Hall devices can be realized in standard integrated circuit processes such as the bipolar or

CMOS technologies. Compared to bipolar Hall devices, CMOS Hall devices exhibit the following advantages: high reliability, small size, low cost and compatibility with other CMOS technologies [1–4]. Unfortunately, integrated CMOS Hall sensors also suffer from a lot of non-idealities [2–4]. First of all, their magnetic field sensitivity is very low. For instance, in a linear or angular position Hall sensor, the value of magnetic field is usually 5 mT at one cm distance from a magnet which has a magnetic field of around 0.1 T. Under this magnetic field, the CMOS Hall device gives a weak output signal of hundreds of micro-volts. Second, its offset is rather high. A CMOS Hall device is very vulnerable to process fluctuation, temperature drift and package-induced stress. These negative factors induce serious offset voltage and low frequency 1/f noise which may be large enough to obscure the Hall signal. In addition, CMOS operational amplifiers (OP-AMPs) used for Hall signal conditioning have poor performance in terms of offset and 1/f noise compared to bipolar OP-AMPs. For example, the typical value of the offset of a CMOS OP-AMP is as large as  $\pm 2$  mV [5].

Therefore, the low magnetic sensitivity and the large offset of Hall sensors limit both the minimum value of the magnetic field that can be measured as well as the accuracy of the measurements. So far the techniques used to reduce the offset and 1/f noise from the electronic circuits, can be mainly divided into auto-zero (AZ), correlated double sampling (CDS) and chopper stabilization (CHS) techniques [6]. Compared with the AZ and CDS, the CHS technique can effectively eliminate the offset and 1/f noise of the electronics without requiring any low-pass filtering [7–9]. It transposes the signal to a higher frequency, where there is no low frequency 1/f noise, and then demodulates it back to the baseband after amplification. However, the CHS technique only effectively removes the offset and 1/f noise of the amplifiers, but it cannot satisfactorily suppress the external input offset and 1/f noise. In order to eliminate these non-ideal factors simultaneously, a quasi-chopped technique for dynamic offset cancellation, *i.e.*, the so-called spinning current technique, has been widely employed in Hall sensors [9,10].

This paper deals with a highly sensitive digital Hall sensor fabricated in 0.18  $\mu\text{m}$  high voltage (HV) CMOS technology for low magnetic field applications. A new chopper stabilized instrumental chain is employed to perform the dynamic offset cancellation, which mainly consists of an optimal switched Hall plate, and a novel and simple signal conditioner. In particular, the proposed signal conditioner features a switched hysteresis comparator to replace the sample-hold circuit and Schmitt trigger of conventional signal conditioner, which further reduces the size and cost of the proposed Hall sensor.

This paper is arranged as follows: first, the design and optimization of the CMOS horizontal Hall plate is briefly introduced. Further, the structure of an analog front-end with the dynamic offset cancellation is described in detail. Then, the simulation and experimental results are presented and discussed. Finally, conclusions are drawn.

## 2. Cross-Shaped Hall Plate

The cross-shaped Hall plate as a horizontal Hall device has been broadly used due to its relatively high sensitivity and low offset. The structure of the CMOS cross-shaped Hall plate is schematically shown in Figure 1. It is fabricated in an N-well diffusion area which is built in a P-type substrate, with four N+ doped terminals [11–13]. The 90° rotation symmetrical structure makes it well suitable for spinning current use where the biasing and sensing terminals are periodically permuted. In order

to reduce the  $1/f$  noise and carrier surface losses, a shallow P+ top layer often covers the surface of the N-well. The P+ top layer and P-type substrate are usually connected to ground. When a voltage  $V$  or current  $I$  bias is supplied via one pair of terminals and a perpendicular magnetic field  $B_Z$  is applied to the device surface, the Hall voltage  $V_H$  appears on the other pair of terminals due to the Hall effect. Considering the geometry of a real Hall plate,  $V_H$  can be expressed with the current related sensitivity  $S_I$  [13]:

$$V_H = S_I I B_Z, \quad (1)$$

with  $S_I = G \mu_H R_{square} = \frac{G \cdot r_H}{q n_{NW} t_{NW}}$ .  $S_I$  is determined by the geometrical correction factor  $G$ , the Hall mobility  $\mu_H$  or the Hall factor  $r_H$ , the doping concentration  $n_{NW}$  of the N-well, and the effective depth of the N-well  $t_{NW}$ .

Equation (1) can be rewritten with the voltage related sensitivity  $S_V$ :

$$V_H = S_V V B_Z, \quad (2)$$

with  $S_V = \frac{S_I}{R_{square} N_{square}} = \frac{G}{2 \frac{L}{W} + \frac{2}{3}} \mu_H$ ,  $L$  and  $W$  are the finger length and finger width of the

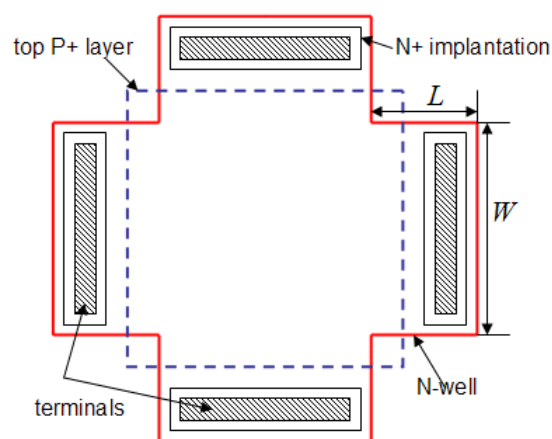
cross-shaped Hall plate, respectively.

For a cross-shaped Hall plate, the geometrical correction factor can be calculated by [13]:

$$G = 1 - 5.0267 \frac{\theta_H}{\tan(\theta_H)} e^{-\frac{\pi W + L}{2 W}} \quad (3)$$

where  $\theta_n$  is the Hall angle, equal to  $\tan^{-1}(\mu_H B)$ .

**Figure 1.** Top view of a conventional cross-shape Hall plate.



Equation (1) means that  $S_I$  is inversely proportional to the carrier concentration of the N-well. Therefore, a Hall device fabricated by a standard CMOS process has a low sensitivity due to high N-well doping concentration. In order to improve the current related sensitivity, we select a HV CMOS process to fabricate the Hall plate as it can provide an obviously lower N-well doping level than the standard CMOS process, despite a relatively deep N-well depth. On the other hand, the geometrical

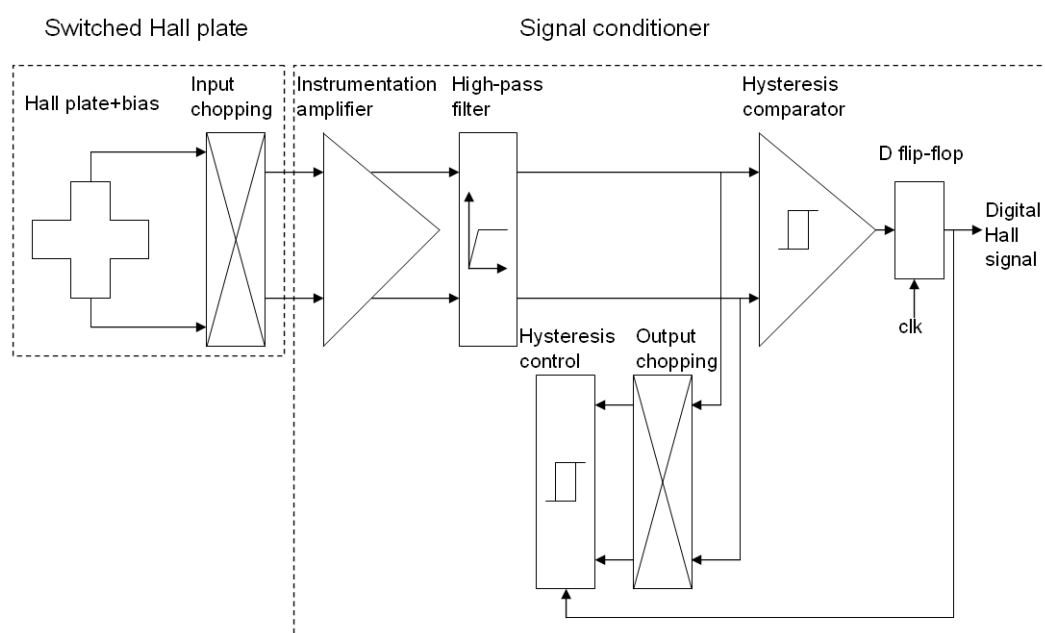
correction factor should also be enhanced, which is determined by the ratio of finger length  $L$  to finger width  $W$  in terms of Equation (3). In order to improve the voltage related sensitivity without reducing the current related sensitivity too much, an optimal cross geometry ( $W/L = 2$ ) has been reasonably selected in the layout design.

It is well known that CMOS Hall devices seriously suffer from a large offset. One of the main origins of offset comes from the mask-misalignment, which can be minimized by designing a Hall device with an appropriate and symmetric layout. In fact, the masks defining the terminals and N-well implant active layer of the Hall plate could be shifted or rotated relative to each other during photolithography. Any misalignment between terminals mask and the N-well mask will result in an offset, even in the absence of magnetic field. However, the smaller terminals designed within the N-well could lead to a larger masks misalignment. In the layout design, an optimized cross-shaped Hall plate structure is developed. Compared to the conventional Hall plate, the length of terminals reaches a maximum allowable value in the N-well for a given technology. Thus, the effect of the masks misalignment on the offset can be greatly reduced.

### 3. Front-End Signal Conditioning

The block diagram of the new chopper stabilized instrumental chain is illustrated in Figure 2. At first, applying the spinning current technique, the output and supply terminals of Hall plate are periodically interchanged so that the useful Hall signals are separated from the offset and  $1/f$  noise through input chopping modulation. Then, the modulated signals are amplified by a differential instrumentation amplifier. After this amplification, two high-pass filters remove the unwanted offset and  $1/f$  noise. Finally, the output signal passing through the filters is demodulated and the digital Hall signal is generated by a switched hysteresis comparator.

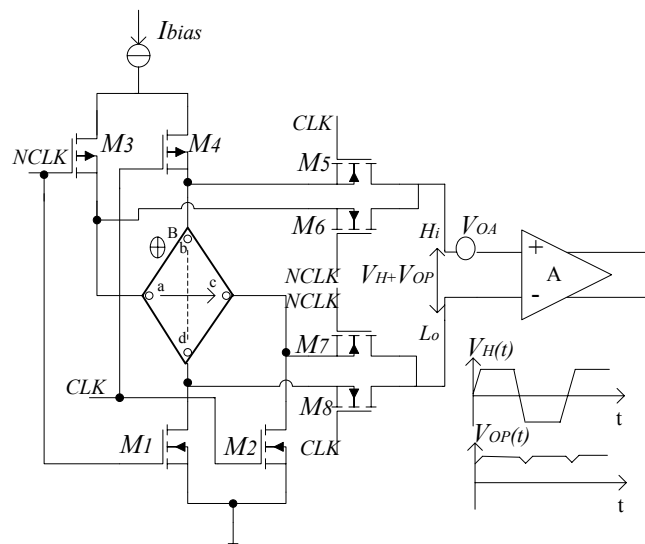
**Figure 2.** Block diagram of the new chopper stabilized instrumental chain.



### 3.1. Switched Hall plate

Figure 3 shows the switched Hall plate in Figure 2. Since the  $90^\circ$  rotation symmetrical Hall plate can be considered as a distributed resistive Wheatstone bridge from a dc point of view, the dynamic offset cancellation can be achieved by the spinning current method [3,4]. By periodical supply and output terminals permutation, the quadrature states are generated. One pair of complementary clocks of 100 kHz produce  $0^\circ$  and  $90^\circ$  states respectively. When CLK is high level, M2, M3, M5, and M8 turn on. The terminal *a* and terminal *c* of the Hall plate are connected to power and ground. Then current flows from terminal *a* to terminal *c*, and Hall signal appears between terminal *b* and terminal *d*. When NCLK is high level, M1, M4, M6 and M7 turn on, so there is a current flowing from terminal *b* to terminal *d*. Accordingly, a Hall signal is present between terminal *c* and terminal *a*. Thus, if the change of the magnetic field is much slower than the clock frequency, the differential output Hall voltage  $V_H$  periodically changes its polarities with the same magnitude in the course of current spinning. On the contrary, the differential output offset voltage  $V_{OP}$  always keeps the same magnitude and a constant polarity, as the same imbalance occurs in adjacent branches of the equivalent Wheatstone bridge network. It is important to note that the offset  $V_{OA}$  of the instrumentation amplifier becomes indistinguishable from  $V_{OP}$ . Consequently, a demodulation should be performed to extract the Hall signal and eliminate the Hall offset and the instrumentation amplifier's offset simultaneously by the following signal conditioner at no extra cost.

**Figure 3.** Switched Hall plate.



### 3.2. Signal Conditioner

The traditional signal conditioners execute sample-and-hold (S/H) and adding functions to remove offset without using low-pass filters [3,8]. First, the two differential outputs of the instrumentation amplifier are sampled and hold by S/H circuits during  $0^\circ$  and  $90^\circ$  states respectively. Next, the outputs of S/H circuits input the summing OP-AMP. Finally, the offset can be cancelled out by the summing OP-AMP. However, this signal conditioner layout requires four completely differential S/H circuits and a summing OP-AMP, thus it requires too large a chip size to fabricate four S/H capacitances. Moreover, the circuit structure is much more complicated. Later, a simplified circuit configuration was

proposed [14]. Here, a capacitance clocked by sampling clock is used to realize the adding function, taking place of a summing OP-AMP. Further, it only needs two S/H capacitances, and the total number of capacitances decreases from four to three. Nevertheless, this circuit requires four-phase different clocks, and the timing relationship in the circuit is much more complex.

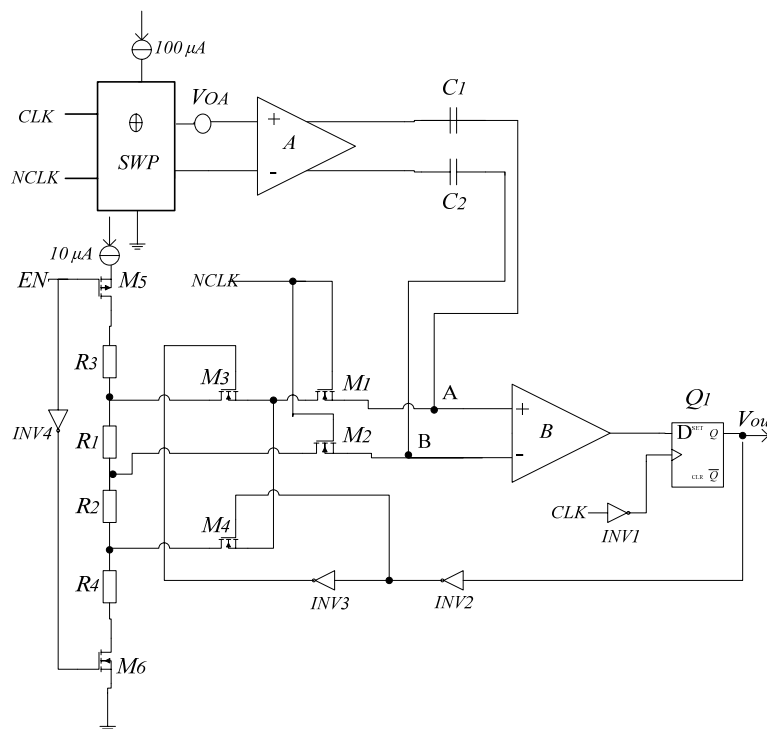
In this work, we propose a signal conditioner based on a high-pass filtering—demodulation configuration, as shown in Figure 4. Here, the switched Hall plate is represented by block SWP. EN is the enable signal and high level is effective. Compared to other similar signal conditioners [15,16], the proposed signal conditioner has a simpler structure. In addition to the instrumentation amplifier A, it only consists of two high-pass filters and a switched hysteresis comparator B. The circuit properly works as follows: during the  $0^\circ$  state, the differential input voltage of the instrumentation amplifier is:

$$V_i(0^\circ) = V_H + |V_{OP}(0^\circ)| + |V_{OA}| \quad (4)$$

During the  $90^\circ$  state, the differential input voltage of the instrumentation amplifier changes to:

$$V_i(90^\circ) = -V_H + |V_{OP}(90^\circ)| + |V_{OA}| \quad (5)$$

**Figure 4.** Signal conditioner of the digital Hall sensor.



After it is amplified by the instrumentation amplifier, the Hall signal can pass through the high-pass filters, but the offset and  $1/f$  noise are blocked. It is important to notice that a simple passive first order high-pass filter is sufficient to perfectly cancel the offset and  $1/f$  noise. The cut-off frequency of the high-pass filter has to be higher than the  $1/f$  noise frequency, which is typically between 500 Hz and 1 kHz, so a first order high-pass filter with 2 kHz cut-off frequency can achieve this requirement. The cut-off frequency is determined by  $1/C_1R_{AB}$  or  $1/C_2R_{AB}$ , where  $R_{AB}$  is the equivalent resistance between the points A and B. In order to obtain low  $1/f$  noise performance,  $C_1$  and  $C_2$  are set to 10 pF.

When NCLK is high level, switches M1 and M2 turn on, then, the differential input voltage of the comparator B is clamped to:

$$V_{AB} = V_{th} \quad (6)$$

where  $V_{th}$  is a trigger threshold level and its polarity is controlled by the feedback Hall output signal. When the Hall output signal is high level, switch M3 turns on and  $V_{th}$  is equal to  $V_{R1}$  (the current of 10  $\mu$ A flowing across resistor  $R_1$ ). Otherwise, switch M4 turns on, then  $V_{th}$  becomes  $-V_{R2}$  (the current of 10  $\mu$ A flowing across resistor  $R_2$ ). We selected  $R_1 = R_2 = R_3 = R_4 = 2$  K to make  $V_{th} = \pm 20$  mV. At the moment, the cut-off frequency of the high-pass filters is much higher than the chopping frequency of 100 KHz, hence both Hall signal and offset and 1/f noise are blocked.

When NCLK is low level, switches M1 and M2 turn off. At this time, the cut-off frequency of the high-pass filters becomes less than 100 kHz but higher than 2 kHz. Thus, only the Hall signal can pass through the high-pass filters. Since the amount of electric charge on the capacitances C1 and C2 remains unchanged, the differential input voltage of the comparator B changes to:

$$V_{AB} = 2A_u V_H + V_{th} \quad (7)$$

where,  $A_u$  is the voltage gain of the instrumentation amplifier A, and the residual offset voltage is neglected.

First assume that the initial state is  $V_A > V_B$ , so the output voltage of comparator B is a high level. At this time,  $V_{th}$  is equal to  $V_{R1}$ . When  $2A_u V_H$  reversely increases more than  $|V_{R1}|$ , the comparator B outputs a low level and  $V_{th}$  becomes  $-V_{R2}$ . Only when the value of  $2A_u V_H$  forward increases more than  $|V_{R2}|$ , the output becomes a high level. In order to output a standard CMOS level, a D flip-flop (DFF) is used.

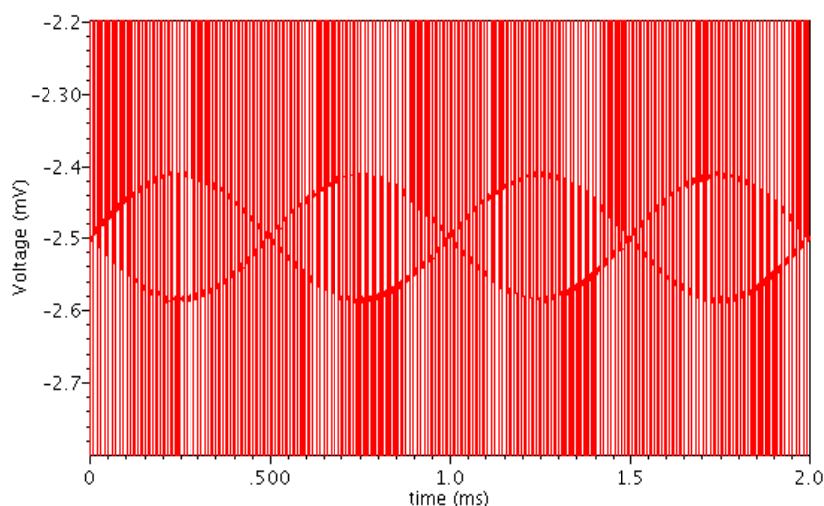
Therefore, the proposed signal conditioner not only effectively eliminates the offset and 1/f noise, but also realizes the hysteresis characteristics of a digital Hall sensor without a Schmitt trigger. Meanwhile, the whole signal conditioner only needs two capacitances, which further make the chip cost-effective.

#### 4. Circuit Simulations

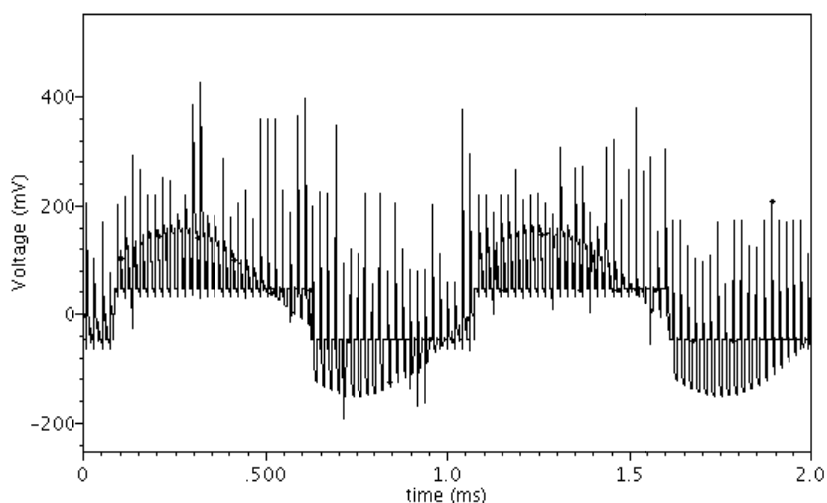
A SPICE simulation of the front-end chopper stabilized instrumental chain was performed with 100 kHz chopping clock frequency using a Cadence spectre simulator. The simulation model parameters of the devices were derived from the X-FAB 0.18  $\mu$ m HV CMOS technology. The Hall plate is modeled by an equivalent simulation model written in Verilog-A language [13]. The Hall plate model produces a 1 kHz sinusoidal Hall output signal of 80  $\mu$ V and a dc output offset of 2.5 mV when the input bias current is 100  $\mu$ A and the perpendicular magnetic field is 2.5 mT. After the Hall plate output signals are modulated at 100 kHz by applying the spinning current technique, they are fed into the instrumentation amplifier for amplification. Figure 5 illustrates the transient voltage waveform between the differential inputs of the instrumentation amplifier. Unfortunately, some parasitic spikes are obviously observed during commutations. These spikes are generated by the various non-idealities of the switches, including charge injection, clock feed-through and parasitic capacitances of Hall plate and switches. Although a dummy switch can reduce the charge injection, it will increase the complexity of the spinning current circuit. Since the RC time of the spikes is dominated by the

resistance of the Hall device and the parasitic capacitances, the best method to suppress these spikes is to reduce the parasitic capacitances. Therefore, we properly reduce the size of the switches without increasing the on-resistance too much and we employ a small Hall plate to reduce the parasitic capacitances in our design. Figure 6 shows the transient simulation voltage waveform at the differential inputs of the comparator B. It is clearly observed that the high-frequency Hall signal is demodulated into the original low-frequency signal and the offset is effectively eliminated by the high-pass filters. The digital Hall output signal waveform is shown in Figure 7. It can be seen that when the input Hall signal changes polarity, that is the magnetic field changes direction, the DFF output level changes synchronously. The simulation results also show that when the amplitude of the input Hall signal increases to 0.15 mV the signal conditioner can even cancel a maximum input Hall offset of 10 mV, which means that the signal conditioner can tolerate a larger offset if the Hall signal becomes larger. The simulated results indicate the improved signal conditioner has a remarkable ability to suppress the large offset and amplify the weak Hall signal.

**Figure 5.** Simulated transient voltage waveform between the differential inputs of the instrumentation amplifier.

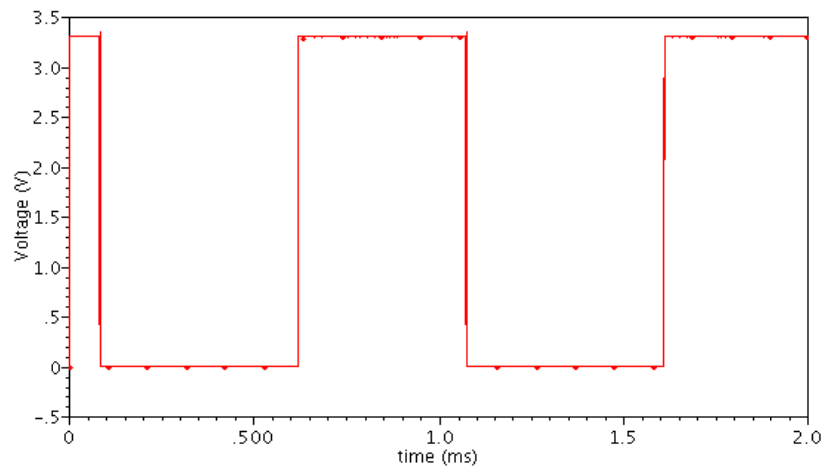


**Figure 6.** Simulated transient voltage waveform between the differential inputs of the comparator.





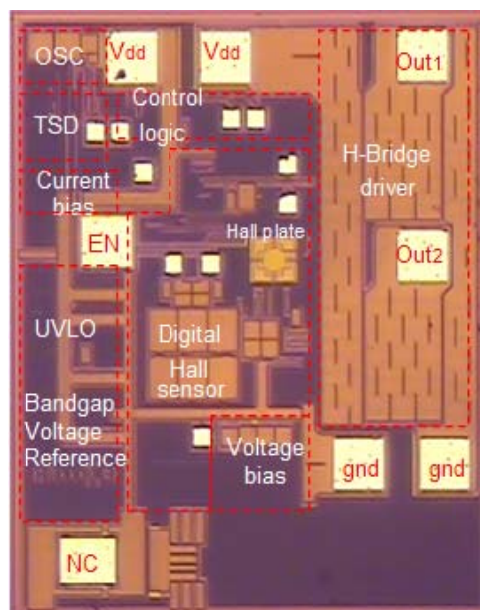
**Figure 7.** Simulated digital Hall output signal of the signal conditioner.



## 5. Experimental Results

A highly sensitive digital Hall sensor using the dynamic offset cancellation technique was implemented in a monolithic brushless DC motor driver chip based on the X-FAB 0.18  $\mu\text{m}$  HV CMOS process for detecting magnetic pole position. A microphotograph of the driver chip is shown in Figure 8. The cross-shaped Hall plate measuring  $64 \times 64 \mu\text{m}^2$  is situated in the central region of the chip. The spinning current circuit and the signal conditioner are located close to the Hall device. In addition, the single-chip motor driver also integrates other important functional blocks such as control logic, H-bridge driver, oscillator, bandgap voltage reference, thermal shutdown (TSD) and under voltage lockout (UVLO) protection, *etc.*

**Figure 8.** Microphotograph of the digital Hall sensor die.



Firstly, the performances of the single Hall device were tested by using a special Hall effect measuring instrument NDWH-648. The instrument can achieve a Hall voltage resolution of  $1 \mu\text{V}$ , providing a sufficiently high measuring accuracy over the measuring temperature range from 77 K to

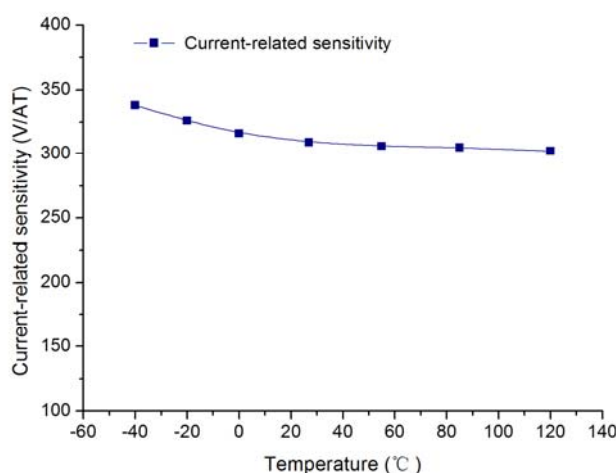
400 K. When the Hall plate is biased with 100  $\mu\text{A}$  DC current, the current related sensitivity was measured at room temperature. A comparison of the current related sensitivity has been made between the proposed Hall device and the reported CMOS Hall devices, as shown in Table 1.

**Table 1.** Comparison of the current related sensitivity between the proposed single Hall device and the reported Hall devices.

	Current Related Sensitivity	Technology
This work	310 V/AT	0.18 $\mu\text{m}$ HV CMOS
[7]	90 V/AT	0.35 $\mu\text{m}$ CMOS
[16]	95 V/AT	0.35 $\mu\text{m}$ CMOS
[17]	180 V/AT	0.8 $\mu\text{m}$ CMOS

It is obvious that a higher sensitivity of about 310 V/AT is achieved in this work. Figure 9 shows the thermal drift of the current related sensitivity within an industrial temperature range of  $-40\text{ }^{\circ}\text{C}$ – $120\text{ }^{\circ}\text{C}$ .

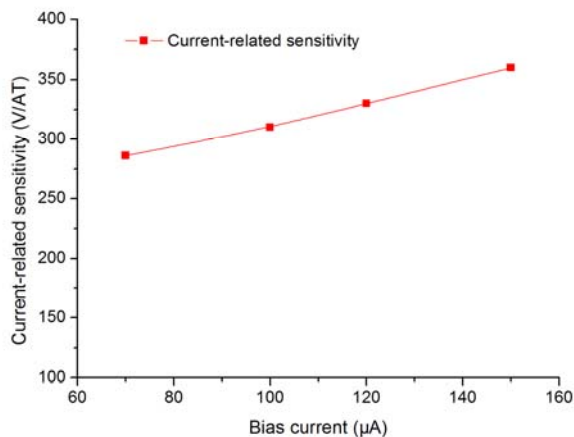
**Figure 9.** Measurement of the current-related sensitivity versus temperature.



The temperature first order coefficient of sensitivity is estimated to about 800 ppm/K. The variation of the current related sensitivity with the DC bias current is shown in Figure 10. Because of the junction effect increasing with the bias current, the effective thickness of the active area of the Hall plate is reduced. Thus, we observe that the sensitivity is increased with the bias current. The static Hall offset voltage between one pair of terminals was measured when the substrate is grounded and two other terminals are applied to 1.0 V and 0 V. A small Hall offset about 1 mV is obtained at temperature =  $27\text{ }^{\circ}\text{C}$ .

Next, the functions of the whole Hall sensor were measured. The digital output of the Hall sensor was observed by using an Agilent 3032A oscilloscope, as illustrated in Figure 11. It can be seen that the output level of the Hall sensor changes synchronously when the magnetic field changes from  $-2\text{ mT}$  to  $2\text{ mT}$ . A minimum detectable magnetic field of  $\pm 2\text{ mT}$  is obtained, showing a hysteric characteristic of  $4\text{ mT}$ . Note that the detectable sensitivity could be further improved by reducing the threshold voltage of the hysteresis comparator, whereas a too low threshold voltage will cause a poor anti-jamming ability of the hysteresis comparator. Therefore, the minimum detection sensitivity of  $\pm 2\text{ mT}$  is difficult to improve. In addition, the test results show that the Hall sensor can work well as the supply voltage changes from 2 V to 4 V while the temperature ranges from  $-40\text{ }^{\circ}\text{C}$  to  $120\text{ }^{\circ}\text{C}$ .

**Figure 10.** Measurement of the variation of the current-related sensitivity with the biasing current.



**Figure 11.** Digital output of the Hall sensor displayed on an Agilent 3032A oscilloscope.



Table 2 summarizes the measured important parameters of the digital Hall sensor die, which suggests that the CMOS integrated digital Hall sensor can provide high sensitivity and better temperature stability over a wide temperature range.

**Table 2.** Typical characteristics of Hall sensor.

Parameters	Value
Supply voltage	2–4 V
Hall plate sensitivity @100 $\mu\text{A}$	310 V/AT
Original Hall plate offset @1V	1 mV
Operating point $B_{OP}$ @27 $^{\circ}\text{C}$	2 mT
Release point $B_{OP}$ @27 $^{\circ}\text{C}$	–2 mT
Hysteresis @27 $^{\circ}\text{C}$	4 mT
Operating temperature range	–40–120 $^{\circ}\text{C}$

## 6. Conclusions

A highly sensitive digital Hall magnetic sensor using the X-FAB 0.18  $\mu\text{m}$  HV CMOS technology is introduced. The cross-shaped structure of Hall device is optimized to reduce Hall offset and improve sensitivity. In order to eliminate the relatively large offset, including Hall offset, amplifier's offset and  $1/f$  noise, the dynamic offset cancellation technique through Hall current spinning is applied. A novel signal conditioner with a simple structure is proposed for saving chip area and improving the performance of the sensor. The recovery of digital Hall output and offset cancellation are achieved with only two high-pass filters and a switch-controlled comparator. The whole signal conditioner only requires a pair of complementary clocks. Additionally, it is convenient to change the hysteresis characteristics by adjusting resistances, without needing an actual Schmitt trigger. The experimental results show that the sensor has a remarkable ability to measure a minimum  $\pm 2$  mT magnetic field and output a digital Hall signal over a wide temperature range from  $-40$  °C to  $120$  °C. Therefore, this Hall sensor is well suited for low magnetic field applications, such as integrated brushless DC motor drivers which require small chip size and high sensitivity.

## Acknowledgements

This work was supported by the Science and Technology Support Project, Jiangsu, China under Grant No. BE2009143.

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