A Power Amplifier with Large High-Efficiency Range for 5G Communication

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Abstract: This paper presents a new method to design a Doherty power amplifier (DPA) with a large, high-efficiency range for 5G communication. This is through analyzing the drain-to-source capacitance (C_{DS}) of DPAs, and adopting appropriate impedance of the peak device. A closed design process is proposed, to design the extended efficiency range DPA based on derived theories. For validation, a DPA with large efficiency range was designed and fabricated by using two equal devices. The measured results showed that the saturated output power was between 43.4 dBm and 43.7 dBm in the target band. Around 70% saturated drain efficiency is obtained with a gain of greater than 11 dB. Moreover, the obtained drain efficiency is larger than 50% at the 10 dB power back-off, when operating at 3.5 GHz. These superior performances illustrate that the implemented DPA can be applied well in 5G communication.

Keywords: Doherty power amplifier; drain-to-source capacitance; large efficiency range; 5G communication

1. Introduction

With the rapid development of communication technology, the amount of data transferred worldwide is increasing significantly [1]. Limited spectrum resources have become extremely precious. There are many methods to improve the efficiency of spectrum transmission. Modern wireless communication signals usually adopt complex modulation methods to improve the utilization efficiency of spectrum resources [2,3]. These signals are often large peak-to-average ratio signals, and traditional power amplifiers (PAs) are not suitable for amplifying these signals [4,5]. Therefore, higher performance is required from the power amplifiers.

Some power amplifiers for high peak-to-average ratio signals are proposed, such as Doherty [6], out-phasing [7], and envelope tracking [8]. Among them, Doherty PAs (DPAs) are widely used in practical base stations because of their simple structure and low cost. However, DPAs also have some inherent disadvantages, such as a narrow bandwidth and only 6 dB output power back-off (OBO) in traditional symmetrical DPAs [9,10]. It is apparent that a 6 dB OBO cannot meet current communication requirements. In order to extend the OBO range, many methods have been proposed [11–16]. In [11,12], a multiway is applied to extend OBO, which uses multiple peaking PA branches that turn on at various power levels to provide multiple efficiency peaks at and beyond 6 dB OBO. Asymmetrical topology is adapted to ensure the peak PA has a larger saturated current than that of the carrier PA, to increase OBO [13,14]. However, the multiway and asymmetrical architectures often increase design complexity and under-utilize the power capacity of active devices.

Recently, dual-input DPAs have been proposed to extend the OBO range by realizing wider load modulation, which relies on dynamically adjusting the phase and amplitude of the input signal by

using digital techniques [15,16]. However, dual-input DPAs with digital controlling techniques suffer from increased circuit complexity, and/or higher manufacturing costs.

Many efficiency range extension methods are also presented in symmetrical architecture [17–22]. In [17], a symmetrical DPA with complex impedance at the DPA combiner is demonstrated to achieve larger load modulation compared to a conventional symmetrical DPA. High efficiency over large dynamic ranges is achieved using symmetrical devices, while still maintaining full voltage and current utilization of both transistor cells. This is achieved by modifying the combiner [18]. In [19], an explicit circuit model of generalized symmetrical DPA is proposed to design DPAs with an extended high-efficiency range. A methodology is proposed for extending the high-efficiency power range of symmetrical DPAs by taking advantage of the output impedance of peaking stage [20]. Recently, a symmetrical DPA with an extended efficiency range has been presented, where the phase relationship between the carrier and peaking currents at the DPA's combiner is used to extend the dynamic load modulation range [21]. In [22], the transistor's nonlinear phase distortion architecture is used to enhance the average drain efficiency of the DPA with the proper choice of carrier and peaking PA load trajectories. In the fore-mentioned papers, current, impedance and even phase distortion are analyzed and used to enhance efficiency of DPAs by improving the design. In practical design, some methods are introduced to eliminate the influence of drain-to-source capacitance, C_{DS}. As described in [23,24], the quasi-lumped transmission line is used to absorb C_{DS} when designing the matching output network. In [25], the quarter-wave impedance inverter is approximated by the internal and packaged elements of transistors, together with carrier matching network. However, DPAs' theories with C_{DS} are not analyzed and derived in detail. Unlike the above papers, in this work, we are not committed to eliminating the impact of C_{DS} on DPA performance, although we have developed a method to use C_{DS} to achieve a larger OBO range. In other words, the existence of C_{DS} can be positive for expanding the OBO range through proper design. In [26], the nonlinear output capacitor of the transistor has been used to generate harmonic components, thus, improving the saturated drain efficiency. Different from [26], this work is aimed at a large range of high efficiency, including two levels of saturation and power back-off, not just the saturation level.

This paper briefly analyzes DPAs with the drain-to-source (C_{DS}). Adopting suitable impedance of peak device is presented to extend the high-efficiency range, which depends on the existence of the C_{DS}. The design parameters are derived in detail for DPAs with C_{DS}. A closed design process is proposed to design extended efficiency range DPA based on the modified theories and two equal transistors. An extended efficiency range DPA is fabricated using two identical devices. The structure of this paper is as follows: the theories of DPAs with C_{DS} are analyzed in Section 2; the closed design process of the extended efficiency range DPA is described in detail in Section 3; simulated and measured results are analyzed in detail in Section 4; Section 5 summarizes the content of this paper.

2. Theory Analysis of The Proposed DPA

The traditional DPA includes a carrier PA branch and a peak PA branch. At the combiner, there is a load of $R_{OPT}/2$. A transistor can be equivalent to an ideal current source. The equivalent traditional DPA topology is shown in Figure 1. There is an impedance converter line in the carrier PA branch, as shown in Figure 1. In the analysis of conventional ideal DPAs, the drain-source capacitance C_{DS} is often ignored. In the practical design process, the drain-source capacitance C_{DS} is usually adopted into the output matching circuits to reduce its impact on the performance of the PA.

As shown in Figure 1, we consider the current source and drain-source capacitance C_{DS} as comprising a black box. Therefore, considering the voltage V_C and current I_{C1} outside the black box, the analysis method of traditional DPAs is still applicable. The only difference is that conventional DPAs have an ideal current source, and the current source in this paper is with a C_{DS}.
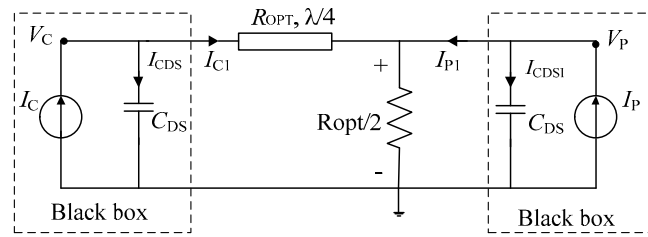
Figure 1. Conventional Doherty power amplifier (DPA) topology with drain-to-source capacitance (C_{DS}).

Based on Figure 1, a more general schematic diagram is shown in Figure 2. The output matching networks (OMN) and offset lines of carrier and peak PAs are represented by two ABCD transfer matrices. We will derive the design theories of DPAs with C_{DS} using the topology shown in Figure 2. While deriving the theories of DPAs, the C_{DS} is considered as shown in Figure 2.
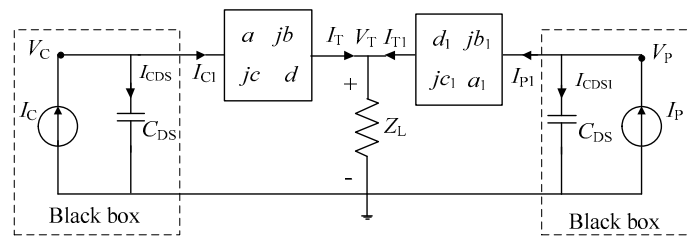

Figure 2. The proposed DPA topology.

Based on Figure 2, the following equations can be obtained based on two-port network theories.

$$\begin{bmatrix} V_C \\ I_C \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Z_{CDS}^{-1} & 1 \end{bmatrix} \begin{bmatrix} a & jb \\ jc & d \end{bmatrix} \begin{bmatrix} V_T \\ I_T \end{bmatrix}, \tag{1}$$

$$\begin{bmatrix} V_P \\ I_P \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Z_{CDS}^{-1} & 1 \end{bmatrix} \begin{bmatrix} d_1 & jb_1 \\ jc_1 & a_1 \end{bmatrix} \begin{bmatrix} V_T \\ I_{T1} \end{bmatrix} \tag{2}$$

Then, the voltage of the carrier device, V_C, and the voltage of the peak device, V_P, can be derived as

$$V_C = \frac{AQ_4 - A_1 Q_2}{Q_1 Q_4 - Q_2 Q_3} I_C + \frac{BQ_4 - B_1 Q_2}{Q_1 Q_4 - Q_2 Q_3} I_P \tag{3}$$

$$V_P = \frac{AQ_3 - A_1 Q_1}{Q_2 Q_3 - Q_1 Q_4} I_C + \frac{BQ_3 - B_1 Q_1}{Q_2 Q_3 - Q_1 Q_4} I_P \tag{4}$$

$$\begin{bmatrix} A & B \\ A_1 & B_1 \end{bmatrix} = \begin{bmatrix} \frac{aZ_L + jb}{jcZ_L + d} & \frac{Z_L/d_1}{jcZ_L + d} \\ \frac{Z_L}{d_1(jcZ_L + d)} & \frac{jb_1}{d_1} + \frac{a_1 dZ_L}{d_1(jcZ_L + d)} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} Q_1 & Q_2 \\ Q_3 & Q_4 \end{bmatrix} = \begin{bmatrix} 1 + \frac{A}{Z_{CDS}} & \frac{B}{Z_{CDS}} \\ \frac{A_1}{Z_{CDS}} & 1 + \frac{B_1}{Z_{CDS}} \end{bmatrix} \tag{6}$$

The carrier branch current I_T and the peak branch current I_{T1} at the combiner can be expressed as

$$I_T = \left[W - W Z_{CDS}^{-1} \frac{AQ_4 - A_1 Q_2}{Q_1 Q_4 - Q_2 Q_3} + Y Z_{CDS}^{-1} \frac{AQ_3 - A_1 Q_1}{Q_2 Q_3 - Q_1 Q_4} \right] I_C + \left[-Y + Y Z_{CDS}^{-1} \frac{BQ_3 - B_1 Q_1}{Q_2 Q_3 - Q_1 Q_4} \right] I_P \tag{7}$$

$$I_{T1} = \left[\frac{A_1 Q_1 - AQ_3}{Z_{CDS} d_1 (Q_2 Q_3 - Q_1 Q_4)} \right] I_C - \left[\frac{1}{d_1} - \frac{1}{Z_{CDS} d_1} \frac{BQ_3 - B_1 Q_1}{Q_2 Q_3 - Q_1 Q_4} \right] I_P, \tag{8}$$

where $W = \frac{d_1}{d_1(jcZ_L + d)}$, $Y = \frac{jcZ_L}{d_1(jcZ_L + d)}$.

The load impedance of the carrier transistor Z_C can be calculated as

$$Z_C = \frac{V_C}{I_C} \tag{9}$$

A coefficient of β can be defined as

$$\beta = \frac{Z_{C,BACK}}{Z_{C,SAT}}, \tag{10}$$

where $Z_{C,SAT}$ and $Z_{C,BACK}$ represent the load impedance of the carrier transistor at the saturation and the OBO level, respectively.

The OBO with C_{DS} effect included can be calculated as

$$\text{OBO} = 10\log\left[\frac{P_{OUT,SAT}}{P_{OUT,BACK}}\right] = 10\log\left[(2\beta)\left(\frac{I_{P,SAT}}{I_{C,SAT}}\right)\frac{(Z_{CDS} - V_{P,SAT}/I_{P,SAT})}{(Z_{CDS} - V_{C,SAT}/I_{C,SAT})}\right], \tag{11}$$

where $I_{C,SAT}$ and $I_{P,SAT}$ represent the saturated current of the carrier and the peak PA, respectively. From Equation (11), the $\frac{(Z_{CDS} - V_{P,SAT}/I_{P,SAT})}{(Z_{CDS} - V_{C,SAT}/I_{C,SAT})}$ is introduced due to the existence of C_{DS}, which makes the OBO range more flexible in design parameters compared to OBO expression of traditional DPAs. In fact, OBO is also related to output capacitance. Furthermore, we can use different Z_{CDS} to obtain a different OBO. Figure 3 shows the relationships between OBO, coefficient γ, frequency and capacitance. To keep the OBO larger than 6 dB, the capacitance is up to 1.4 pF. In this paper, the DPA with a large OBO range is designed at 3.5 GHz. Therefore, the appropriate capacitance value and coefficient γ can be obtained from Figure 3.

For an ideal symmetrical DPA, the saturated current of carrier transistor $I_{C,SAT}$ should be equal to the saturated current of peak transistor $I_{P,SAT}$. Therefore, Equation (11) can be simplified as

$$\text{OBO} = 10\log\left[(2\beta)\frac{(Z_{CDS} - V_{P,SAT}/I_{P,SAT})}{(Z_{CDS} - V_{C,SAT}/I_{C,SAT})}\right] \tag{12}$$

In the design of conventional DPA, the $V_{P,SAT}/I_{P,SAT}$ is equal to $V_{C,SAT}/I_{C,SAT}$ that is R_{OPT}. So, the OBO range expressed in Equation (12) is the same as that of traditional DPAs.

Here, the mentioned relationships should be defined as

$$V_{C,SAT}/I_{C,SAT} = R_{OPT} \tag{13}$$

$$V_{P,SAT}/I_{P,SAT} = \gamma R_{OPT}, \tag{14}$$

where γ is a coefficient. Therefore, Equation (12) can be modified as

$$\text{OBO} = 10\log\left[(2\beta)\frac{(Z_{CDS} - \gamma R_{OPT})}{(Z_{CDS} - R_{OPT})}\right] = 10\log\left[(2\beta)\left(1 + \frac{(R_{OPT} - \gamma R_{OPT})}{(Z_{CDS} - R_{OPT})}\right)\right] \tag{15}$$

From Equation (15), it is clear that the OBO would be larger than that of conventional DPAs when γ is between 0 and 1. A simple way to realize the γR_{OPT} is to use different size transistors for the carrier and peak PA. However, choosing different transistors means asymmetric topology, which has some drawbacks as described in the introduction section. So, in this paper, the same devices in the carrier and the peak PA are used.

For an ideal symmetrical DPA, β value being 2, the OBO is calculated and plotted in Figures 4 and 5. Figure 4 shows the voltage and current of the carrier PA and peak PA. From Figures 4 and 5, the OBO value is 6 dB when γ value is 1, which is the same as that of conventional DPAs. As γ decreases, the OBO range begins to extend. When γ decreases to 0.8, the OBO can ideally reach 12 dB. This back-off range is excellent. However, it is worth noting that the saturated output power of the

peak PA will decrease when load impedance deviates from the optimal impedance R_{OPT}. It can also be seen from Figure 5 that the drain efficiency at the saturated level is smaller than 78.5%, and the drain efficiency at the OBO level can reach 78.5%.
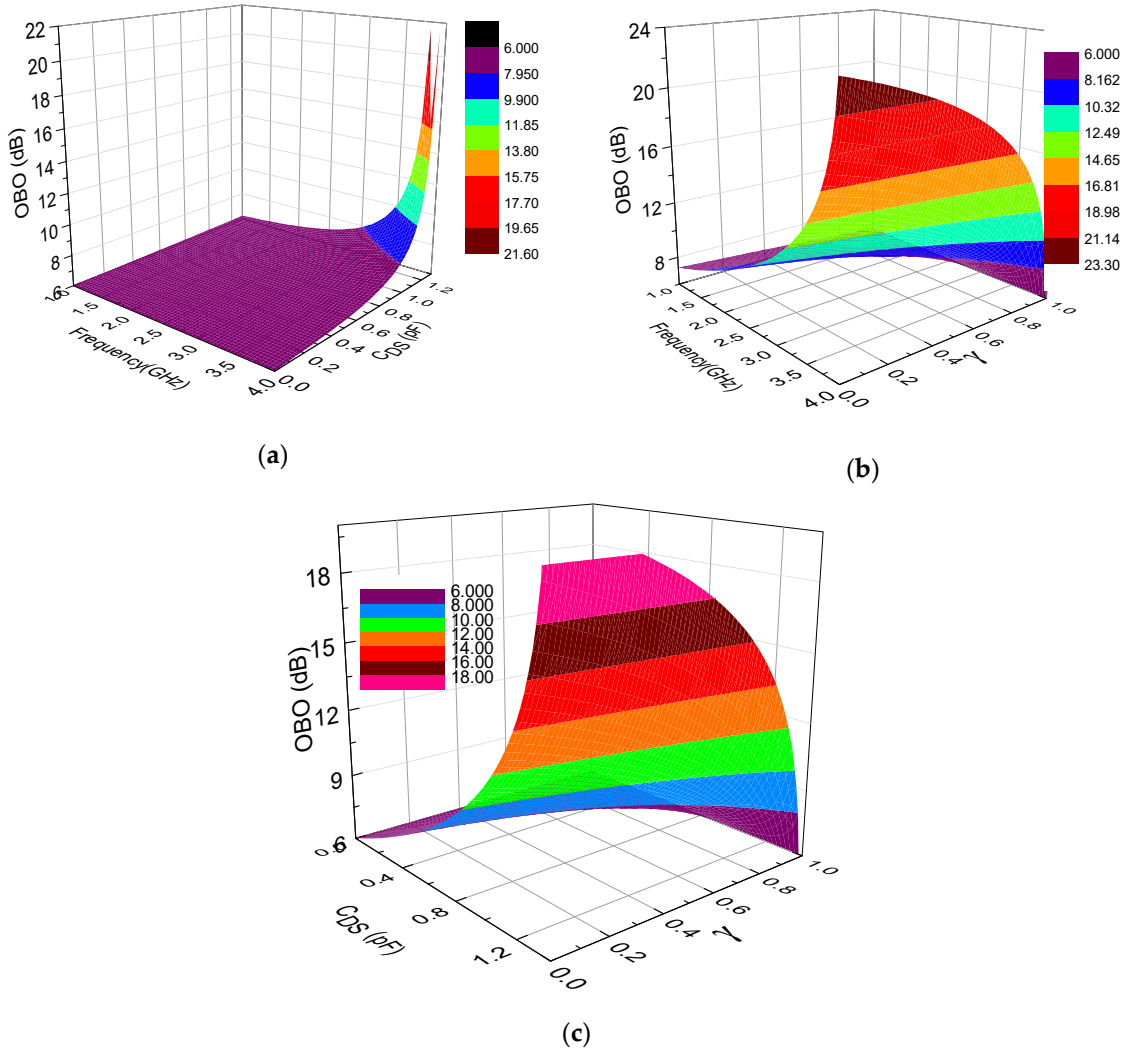

(a)

(b)

(c)

Figure 3. Relationships between output power back-off (OBO), coefficient γ, frequency and capacitance: (**a**) γ of 0.85, (**b**) capacitance of 1.22 pF, and (**c**) frequency of 3.5 GHz.
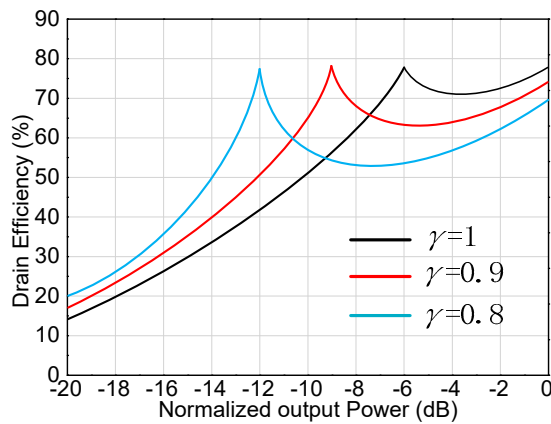

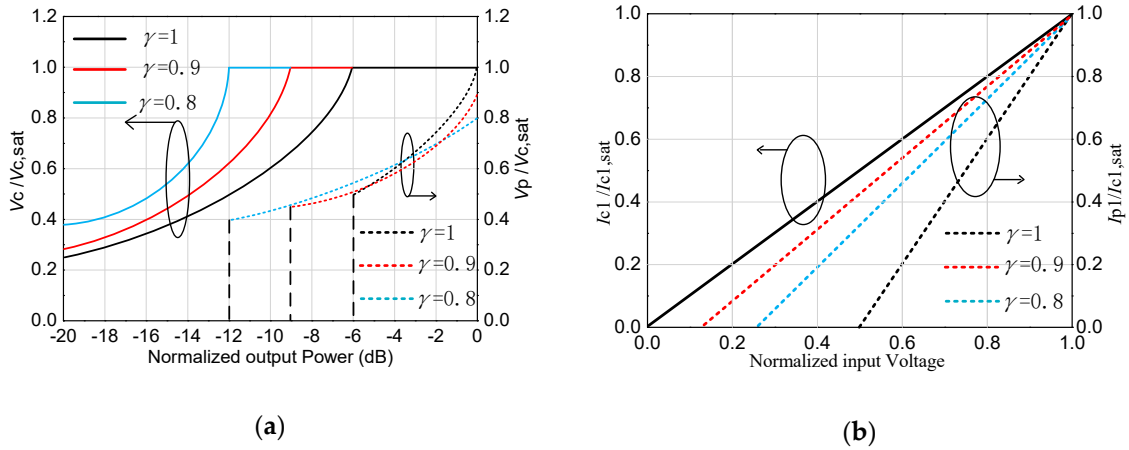**Figure 4.** Drain efficiency versus normalized output power.

Figure 5. Voltage and current of the carrier power amplifier (PA) and peak PA: (**a**) Voltage, and (**b**) Current.

The output power $P_{OUT,P}$ of peak PA can be calculated as

$$P_{OUT,P} = 0.5 \times \left(\frac{I_{max}}{2}\right)^2 \times \gamma R_{OPT} \tag{16}$$

It can be seen that the output power is a linear function of γ. Because γ is less than 1, the output power of the peak PA would decline. For example, γ of 0.91 should be taken for realizing the OBO of 9 dB. At the same time, the output power of peak PA will be 10% less. Different applications would mean a different tendency. So, in practical design, compromise should be made between saturated output power and OBO.

In traditional DPAs, if matching to a different γR_{OPT} resistance, the current of the peak PA and the carrier is usually different. Thus, the impedance modulation of combined nodes of DPA will be changed. Thereby, it becomes an asymmetrical DPA. In this paper the same transistor is used, however, the optimal load impedance of the peak PA is set to γR_{OPT}. In order to ensure that the saturated current of the peak PA and the carrier PA is consistent, the voltage of the peak PA should be set to γV_{max}. As seen from Figure 5, the current and voltage of the peak PA satisfy the desired value. It means that the saturated current of the peak PA is equal to that of the carrier PA. At the same time, the saturated voltage of the peak PA is equal to γV_{max}. Thus, the impedance modulation of combine node of DPA is the same as that of the symmetrical DPA. Therefore, this proposed DPA is still called a symmetrical DPA despite different output power of carrier PA and peak PA.

Figure 6 displays the impedance conversion of the DPA at the saturation and OBO level. In this paper, I_T is equal to I_{T1} and they are in phase. In saturation, impedance at the combiner seen from the carrier branch is $2Z_L$, and the load impedance Z_C of the carrier transistor is R_{OPT}. The $2Z_L$ is transformed to Z_C by using the $(OMN)_C$ and the C_{DS}. At the OBO level, the impedance at the combiner seen from the carrier branch is Z_L, and the load impedance Z_C of the carrier transistor is βR_{OPT}. The Z_L is also transformed to βR_{OPT} by using the $(OMN)_C$ and the C_{DS}. The impedance at the combiner seen from the peak branch is $2Z_L$, and the load impedance Z_P of the peak transistor is γR_{OPT} in saturation. The $2Z_L$ is transformed to R_{OPT} by using the $(OMN)_P$ and the C_{DS}. At the OBO level, the peak transistor is off, where the impedance Z_P is infinite. The impedance at the combiner seen from the peak branch is also ∞. This impedance conversion is also achieved by using the $(OMN)_P$ and the C_{DS}.

Figure 6. Impedance conversion of the DPA.

Combining the impedance conversion with Equations (1)–(10), the $(\text{OMN})_C$ and $(\text{OMN})_P$ parameters can be derived as

$$\text{a} = -\frac{R_{OPT}Z_{CDS}}{R_{OPT}+Z_{CDS}}(\beta-2)c, \tag{17}$$

$$\text{b} = \frac{R_{OPT}Z_{CDS}}{R_{OPT}+Z_{CDS}}Z_L(2\beta-2)c, \tag{18}$$

$$\text{c} = \sqrt{(2\beta-1)/[R_{OPT}Z_L(2\beta-2)(\beta+1)]}, \tag{19}$$

$$\text{d} = Z_Lc(2\beta-2)/(2\beta-1), \tag{20}$$

$$a_1 = \sqrt{\frac{\gamma R_{OPT}Z_{CDS}}{(0.9R_{OPT}+Z_{CDS})*2Z_L}}, \tag{21}$$

$$b_1 = -\sqrt{2Z_L\left(\frac{\gamma R_{OPT}Z_{CDS}}{\gamma R_{OPT}+Z_{CDS}}\right)}, \tag{22}$$

$$c_1 = 0, \tag{23}$$

$$d_1 = \sqrt{2Z_L/\left(\frac{\gamma R_{OPT}Z_{CDS}}{\gamma R_{OPT}+Z_{CDS}}\right)}. \tag{24}$$

3. Design of the Proposed DPA

In this section, a closed method is presented in detail to design the extended efficiency range symmetrical DPA based on the above-mentioned theories. In order to validate the proposed method, a DPA with extended efficiency range was designed using CGH40010F GaN HEMT, based on Rogers R4350B substrate. The drain voltage V_{ds} was set at 28 V. The gate voltage of the carrier PA V_{gs1} was −2.8 V and the gate voltage of the peak PA V_{gs2} was −5.7 V. The optimum load impedance R_{OPT} is determined as 32 Ω for CGH40010F considering V_{knee}. Load-pull simulation should be processed in the ADS software to obtain the optimized load impedance Z_{OPT} at the package plane, for deriving package parameters. Fortunately, the package parameters of CGH40010F can be found from [27], shown in Figure 7. As shown in Figure 7, the package parameters are included for consideration in the practical design process.

Figure 7. PA branch topology with device parameters.

3.1. Output Matching Network Design

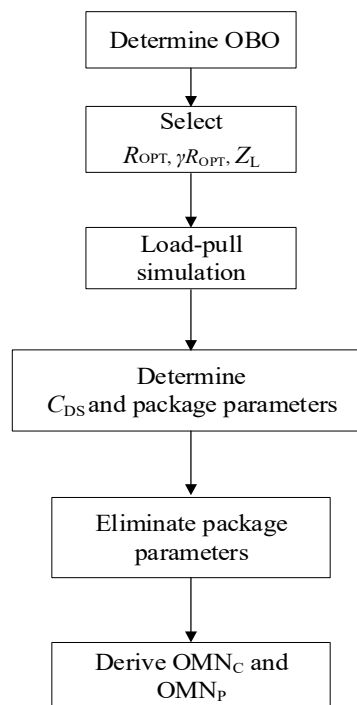The design process of output circuit network can be represented in Figure 8.

```
┌──────────────────────┐
│     Determine OBO     │
└──────────────────────┘
           │
           ▼
┌──────────────────────┐
│        Select         │
│  R_OPT, γR_OPT, Z_L   │
└──────────────────────┘
           │
           ▼
┌──────────────────────┐
│      Load-pull        │
│      simulation       │
└──────────────────────┘
           │
           ▼
┌──────────────────────┐
│       Determine       │
│ C_DS and package parameters │
└──────────────────────┘
           │
           ▼
┌──────────────────────┐
│  Eliminate package    │
│     parameters        │
└──────────────────────┘
           │
           ▼
┌──────────────────────┐
│  Derive OMN_C and     │
│       OMN_P           │
└──────────────────────┘
```

Figure 8. PA branch topology with device parameters.

Firstly, the OBO should be determined; in this work, a 10 dB OBO was chosen. Then, load impedance R_{OPT}, γR_{OPT} of carrier and peak device can be calculated using Equation (15), respectively. The value of γ was 0.85. The load impedance at the combine node Z_L should be set, and was determined as 15·(1 + 0.9) Ω. Thirdly, load-pull simulation should be used to derive the C_{DS} and the package parameters of transistor. In this work, a general transistor CGH40010F was taken, and its parameters have been reported in previous papers. So, this step can be omitted. Micro-strip line TL1 and TL2 should be added to eliminate the package influence on accuracy of OMN, owing to the fact that ABCD transfer matrices of OMN are derived including C_{DS}, and excluding package parameters. By selecting and optimizing the appropriate impedance and electrical length of the microstrip lines TL1 and TL2, the parasitic parameters can effectively be cancelled. Figure 9 shows the simulated value of impedances Z_{OPT1} and Z_{OPT2} that are labeled in Figure 7. It can be seen from Figure 9 that Z_{OPT1} and Z_{OPT2} have no large deviations. It confirms that the parasitic parameters are effectively eliminated by using microstrip lines TL1 and TL2. Then, the parameters value of (OMN)$_C$ and (OMN)$_P$ can be calculated based on Equations (17)–(24). The designed (OMN)$_C$ and (OMN)$_P$ based on the obtained values are shown in Figure 10.
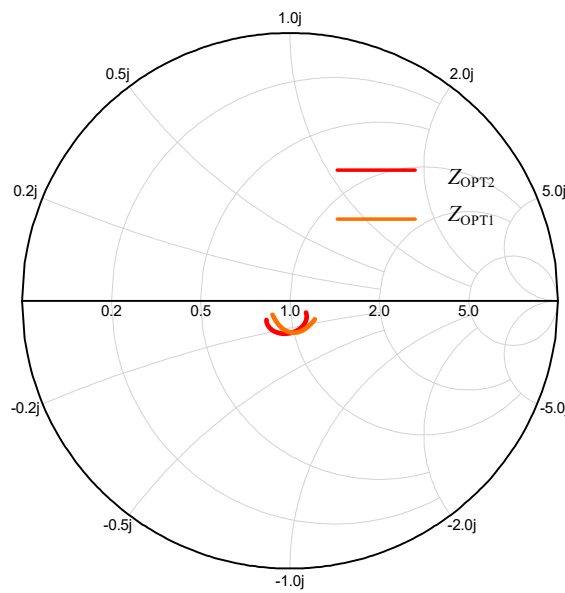
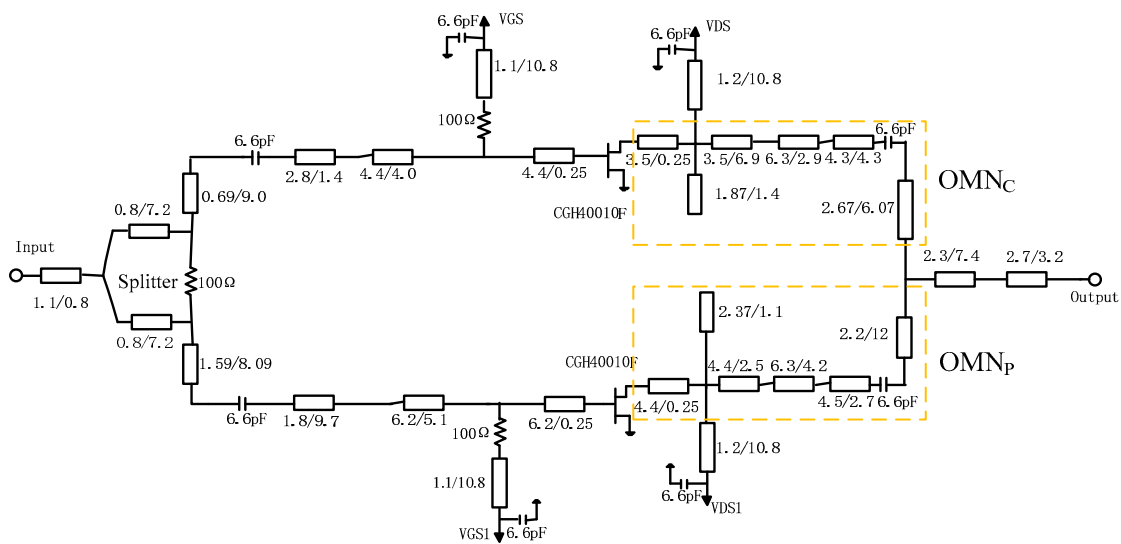**Figure 9.** Simulated impedance Z_{OPT1} and Z_{OPT2}.

Figure 10. Completed circuit schematic and parameters value.

3.2. Input Matching Network Design

Stepped impedance matching technique is used to synthesize suitable input matching networks and provide a targeted saturation gain of around 10 dB. A resistor *R* was added to the gate dc bias circuit to ensure the stability of both transistors. Before the input matching networks of PAs, a 3-dB Wilkinson divider was first employed to split the signal. Offset lines were also added in the input networks, to ensure that the signals of the carrier and peak branches were in phase at the combine node. Its circuit schematic is also shown in Figure 10.

3.3. Post Matching Network Design and DPA Overall Circuit Optimization

As mentioned before, the load impedance Z_L was set to be 15·(1 + 0.9) Ω. Post-matching circuits should be designed to enable the load impedance to be matched to the 50 Ω standard. After all networks were designed, these circuits were combined into a completed DPA. The circuit of distributed parameters was as shown in Figure 10. In this paper, optimization was done in the Advanced Design System (ADS) software to improve performance. Simulated results are plotted in Figures 11

and 12. Figure 11a,b display the drain efficiency versus output power for the proposed DPA and the conventional DPA at 3.4 GHz, 3.5 GHz, and 3.6 GHz, respectively.
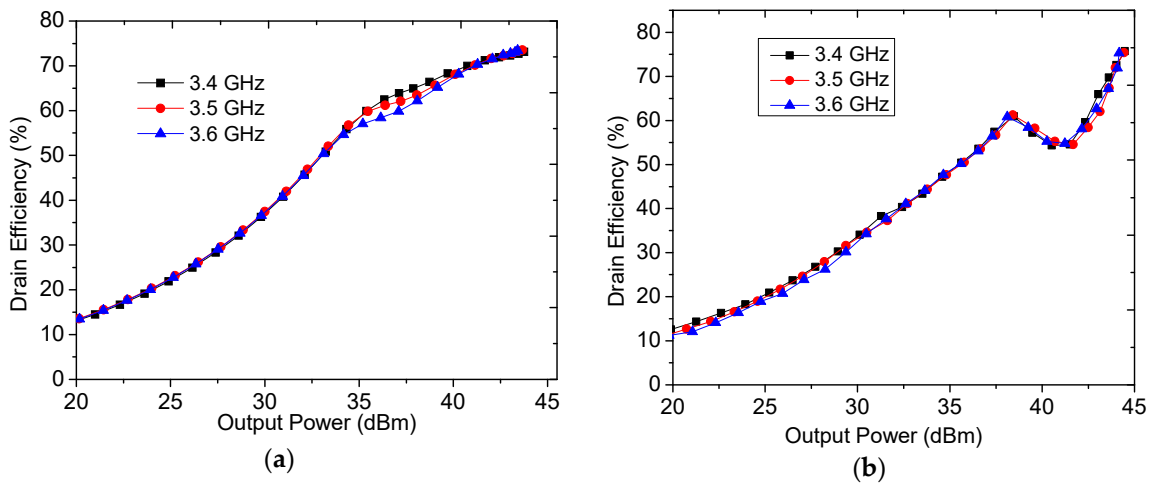
Figure 11. Simulated drain efficiency of DPA versus output power: (**a**) proposed DPA with 0.85 R_{OPT}, and (**b**) conventional DPA with R_{OPT}.
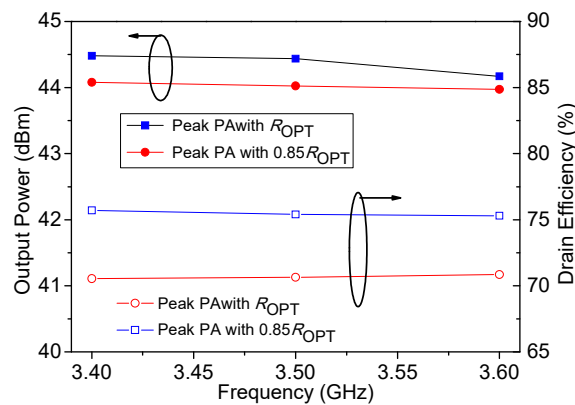

Figure 12. Simulated drain efficiency and output power of DPA in saturation.

Figure 11a,b show that the proposed DPA with load impedance 0.85 R_{OPT} of peak PA has a larger OBO compared to that of the conventional DPAs with load impedance R_{OPT} of the peak PA. This verifies the effectiveness of the proposed method. It also can be seen from Figure 11a that around 55% drain efficiency can be obtained at the 11 dB power back-off. Regarding saturated output power and drain efficiency, these are reduced by about 13% compared with that of conventional DPAs as shown in Figure 12. These simulated performances of the DPA validate the previously described theories. 0.85 R_{OPT} of peak PA is selected, to sacrifice a certain amount of output power and efficiency in the saturation state in exchange for larger OBO.

Figure 13 shows the simulated impedance traces that are consistent with the theories. As shown in Figure 13, in saturation, the load impedance of the peak PA is about 0.85 R_{OPT}, which is close to the theoretical value. The load modulation trajectories of the carrier PA also illustrate a larger OBO range compared to that of traditional DPAs. The load modulation trajectories of the proposed DPA are closer to the real axis, which means higher efficiency can be achieved, compared to that of the traditional DPA.
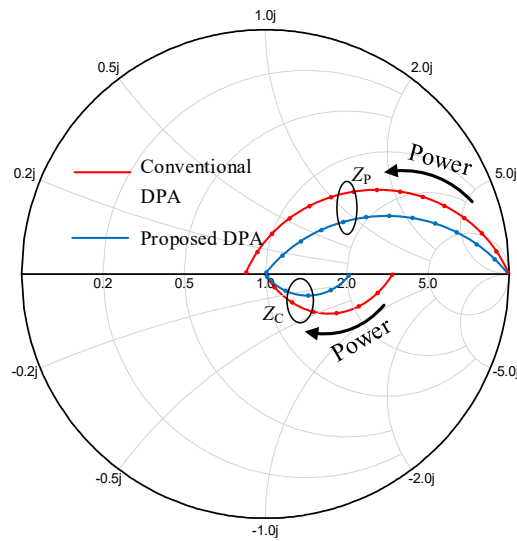
Figure 13. Simulated internal drain load impedance trajectories of the carrier and peak PA (normalized to R_{OPT}).

4. Experiment and Results Analysis

In order to demonstrate the actual performance of the designed DPA circuit, a DPA was fabricated based on the circuit schematic designed in the previous section. Figure 14 is a photograph of the fabricated DPA. The small signal characteristics S-parameter are firstly tested. The simulated and measured *S*-parameters are plotted in Figure 15.
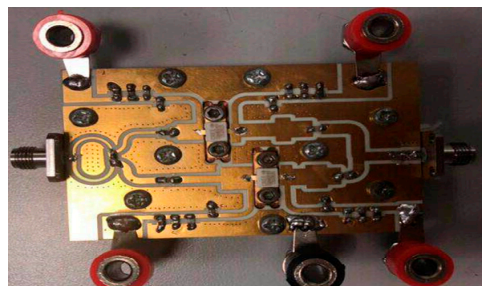

Figure 14. Photograph of the fabricated DPA.
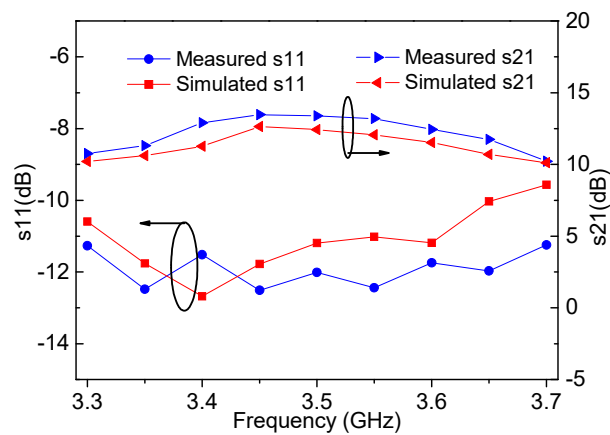
Figure 15. Simulated and measured small-signal frequency responses of the designed DPA.

4.1. Continuous Wave Testing

Performances of the designed DPA were tested using continuous wave signals. Measured output power, drain efficiency and gain are plotted in Figures 16 and 17. Seen from Figure 16, it can be observed that the saturated output power is 43.4–43.7 dBm, and the saturated drain efficiency is 70.5–70.8% in the frequency range of 3.4–3.6 GHz, while gain is between 10.7 dB and 10 dB. Figure 17 shows that drain efficiency at the 6 dB power back-off is 62.4–64.3%. At the 10 dB power back-off, drain efficiency can be larger than 50% (50.3–52.6%).
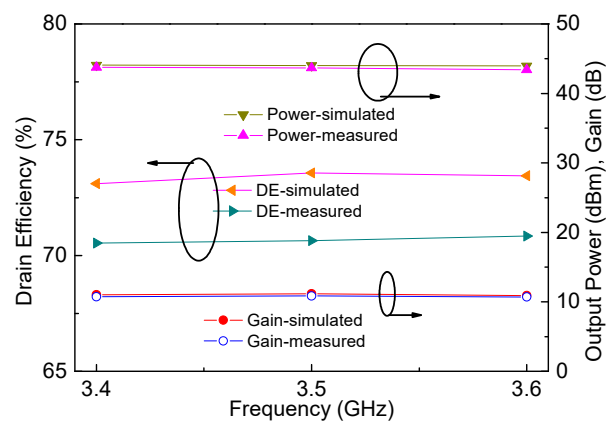
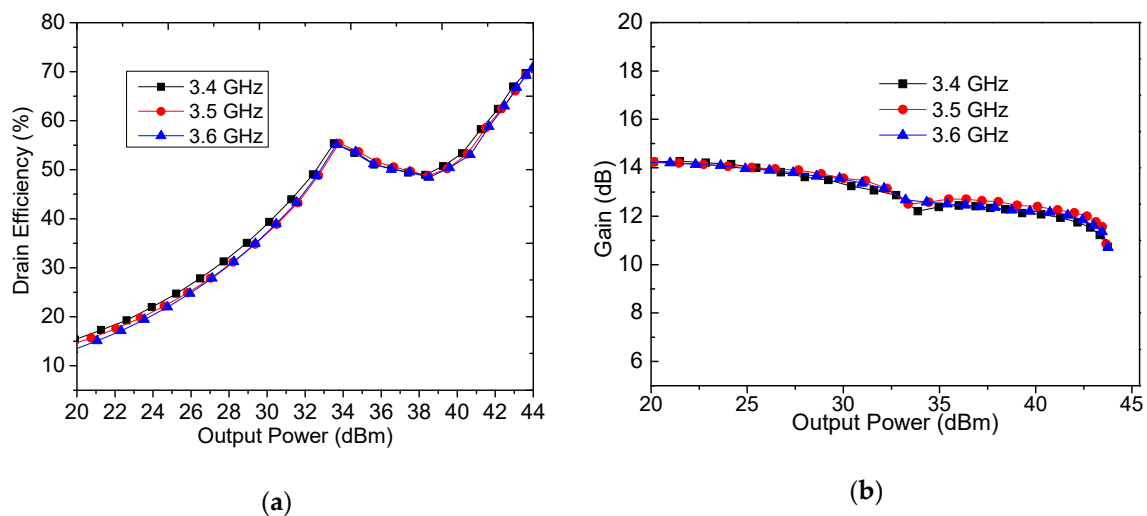**Figure 16.** Simulated and measured output power, drain efficiency, and gain in saturation.

(**a**)

(**b**)

Figure 17. Measured drain efficiency, gain, and power added efficiency (PAE) versus output power: (**a**) drain efficiency, and (**b**) gain.

In order to allow comparisons with previous reports on symmetrical extended efficiency range DPAs, Table 1 lists the performance reported in the relevant literature and the DPA designed in this paper. Except for reference [27,28], the OBO obtained by this work was larger than that of the listed papers. In fact, the drain efficiency at the OBO is a lot smaller than some listed papers, such as [17,19,21]. Compared with [27,28], the drain efficiency in this work is better than that of reference [27,28], with 10 dB OBO achieved. Moreover, it should be noted that the operating frequency is 3.5 GHz, which is higher than others reported in the literature. It is clear that the proposed DPA has higher operating frequency and OBO, making this DPA more suitable for 5G communication applications. The realized DPA has a high efficiency range of up to 10 dB, which is conducive to the wider development and application of DPAs in 5G communications.

Table 1. Performances Compared with Recent Symmetrical DPAs.

Ref.	Freq (GHz)	Pout@SAT (dBm)	DE@SAT (%)	OBO (dB)	DE@OBO (%)	PAE (%)	Gain (dB)	Tech	Bandwidth (MHz)
2014 [17]	2.0	42	67	8.7	57	N/A	10.4	GaN	100
2016 [18]	1.95	44	68	9	47	43	9.5	GaN	200
2017 [19]	2.1	42	72	9.5	58	N/A	10.2	GaN	250
2017 [20]	2.3	45	68	9	49	N/A	11	GaN	100
2019 [21]	2.2	43.6	71	9	54	50	9.7	GaN	200
2018 [22]	1.7	42	71	9	53	N/A	N/A	GaN	350
2019 [28]	2.2	44	69	10	45	N/A	10.5	GaN	200
2019 [29]	3.1	44	71	10	44	N/A	10	GaN	400
T. work	3.5	43.7	70.8	10	52.6	48.7	10.7	GaN	300

4.2. 20 MHz 9.5 dB LTE Testing

In order to characterize the linearity of the implemented DPA, the adjacent channel ratio (ACLR) was tested by using an LTE signal with a bandwidth of 20 MHz and peak-to average ratio of 9.5 dB. The measured ACLR with an average output power of 34.0 dBm is plotted in Figure 18. It can be observed that the ACLR is better than −29.4 dBc at 3.5 GHz. After adopting digital pre-distortion technology (DPD), the ACLR value is better than −53.6 dBc.
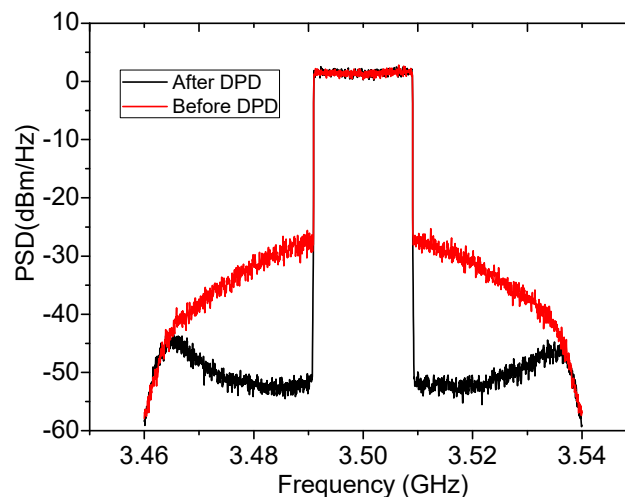
Figure 18. Measured adjacent channel ratio (ACLR) value.

5. Conclusions

This paper proposes a Doherty power amplifier with a large high-efficiency range. Theories of DPAs with C_{DS} included are derived, in which a new way was found for extending the efficiency range of DPAs, through selecting proper load impedance of the peak PA. An extended efficiency range DPA is successfully designed and fabricated by using two equal transistors based on the proposed theories. Measurement results show that the designed DPA can deliver over 43 dBm output power with drain efficiency of about 70% in saturation. Furthermore, at the 10 dB power back-off level, the drain efficiency is greater than 50%. More importantly, all these properties are obtained when the operating frequency is 3.5 GHz. These features indicate that the designed PA could be successfully applied in 5G communications in terms of operating frequency, high efficiency range, and linearity.

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