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# Design of Reconfigurable Time-to-Digital Converter Based on Cascaded Time Interpolators for Electrical Impedance Spectroscopy <sup>†</sup>

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<sup>†</sup> This paper is an extended version of “An efficient, wide range time-to-digital converter using cascaded time-interpolation stages for electrical impedance spectroscopy” published in Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) on Jeju, South Korea, 25–28 October 2016.

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Received: 17 February 2020; Accepted: 26 March 2020; Published: 29 March 2020



**Abstract:** This paper presents a reconfigurable time-to-digital converter (TDC) used to quantize the phase of the impedance in electrical impedance spectroscopy (EIS). The TDC in the EIS system must handle a wide input-time range for analysis in the low-frequency range and have a high resolution for analysis in the high-frequency range. The proposed TDC adopts a coarse counter to support a wide input-time range and cascaded time interpolators to improve the time resolution in the high-frequency analysis without increasing the counting clock speed. When the same large interpolation factor is adopted, the cascaded time interpolators have shorter measurement time and smaller chip area than a single-stage time interpolator. A reconfigurable time interpolation factor is adopted to maintain the phase resolution with reasonable measurement time. The fabricated TDC has a peak-to-peak phase error of less than  $0.72^\circ$  over the input frequency range from 1 kHz to 512 kHz and the phase error of less than  $2.70^\circ$  when the range is extended to 2.048 MHz, which demonstrates a competitive performance when compared with previously reported designs.

**Keywords:** electrical impedance spectroscopy (EIS); time-to-digital converter (TDC); time interpolator; phase; polar demodulator; quantization; reconfigurability

## 1. Introduction

Electrical impedance spectroscopy (EIS), which measures the impedance over a range of frequencies, has been widely used in today’s biomedical applications such as body composition analysis [1–3], cancer diagnosis [4–6], and detection of allergic contact reaction [7], and so on. The frequency range from 1 kHz to several MHz, which is associated with the polarization of macromolecules [8], is required for these applications. With growing demands on portable EIS systems, today’s research is focused on designing fully integrated EIS systems that support a wide frequency range.

The impedance spectrum can be obtained by measuring the impedance for a particular frequency and then repeating the measurement with sweeping the frequency, which is called the frequency response analyzing (FRA) method [9]. When a sinusoidal current signal is injected into the material under the experiment, the resulting sinusoidal voltage signal is generated with the magnitude and time delay that depend on the magnitude and phase of the material's impedance, respectively [10,11]. The EIS system is generally composed of two parts: a sinusoidal signal generator (SSG) and a demodulator. The SSG injects the sinusoidal current signal into the target material, and the demodulator measures the resulting voltage signal. Considering that the EIS system that supports sensor array includes several demodulators with one SSG [9,12,13], it is important to design a demodulator to be hardware-efficient and to have high precision.

Conventional quadrature demodulators extract real and imaginary parts of impedance using quadrature mixers and low-pass filters (LPFs) [12–14]. When the resulting signal depending on the target impedance is multiplied by a signal that is in phase with the injected signal and then low-pass filtered, the output value represents the real part of the impedance. When multiplied by a signal that is  $90^\circ$  out of phase with the injected signal and then low-pass filtered, the imaginary part of the impedance is provided. In such a process, incomplete synchronization among the aforementioned signals becomes a dominant source of error, and the need for phase-correction circuitry increases the implementation complexity [15]. To resolve this synchronization issue, polar demodulators, which asynchronously measure the magnitude variation and time delay of the resulting signal, have been proposed [10,11,15–17]. In particular, the polar demodulators in [10,11,17] mitigate the complexity of analog front-end significantly because the magnitude variation is measured without large-time-constant LPFs and the time delay is measured with one of simple logics such as XOR, XNOR, and latch. In quadrature demodulators, the large-time-constant LPFs limit measurement speed [17] and occupy large area. In polar demodulators, contrarily, the simple logic produces a pulse having the width that corresponds to the time delay, and then a time-to-digital converter (TDC) is used to quantize the pulse width. Note that the pulse width is proportional not only to the phase of impedance but also to the period of the injected signal. Therefore, the TDC should be able to handle wide input-time range to support the analysis at low frequencies, and also achieve a high resolution to support the analysis at high frequencies. It is, therefore, important to design the TDC to meet these requirements in a simple and efficient way for implementing a low-complexity polar demodulator.

Two types of TDCs have been proposed for the EIS system: TDCs based on a time-to-voltage converter (TVC) [15] and a counter [17–19]. The TVC converts the pulse width to the voltage by charging a capacitor with a current source, and the following analog-to-digital converter (ADC) quantizes the output of the TVC [15]. However, the phase error increases with the frequency of the injected signal because the full-scale output voltage of the TVC decreases as the frequency of the injected signal increases. Since counter-based TDCs have an input-time range that is theoretically unlimited [20], this type of TDCs appear to be attractive phase quantizers in the EIS system. However, the TDC in [17] requires high-speed counting clock for high-frequency analysis because the counting speed solely decides the time resolution. This TDC adopts a 3.3-GHz counting clock to support the maximum frequency of up to 10 MHz.

We have proposed two reconfigurable TDCs combining counters with time interpolators to improve resolution without increasing the counting clock speed and verified them by simulation [18,19]. Both TDCs employ a coarse counter to secure wide input-time range. The TDC in [18] uses cascaded time interpolators with a reconfigurable time interpolation factor. When the same large interpolation factor is used, the cascaded time interpolators have shorter measurement time and smaller chip area than a single-stage time interpolator. Since both the required input-time range and time resolution vary with the frequency of the injected signal, the reconfigurable time interpolation factor is employed to maintain phase error within an appropriate level while providing reasonable measurement time. Instead of the cascaded time interpolators, the TDC in [19] utilizes a time interpolator with a low

interpolation factor and a chain delay line to further reduce the phase error. Although the TDC in [19] shows improved precision, the TDC in [18] allows more efficient implementation in terms of chip size.

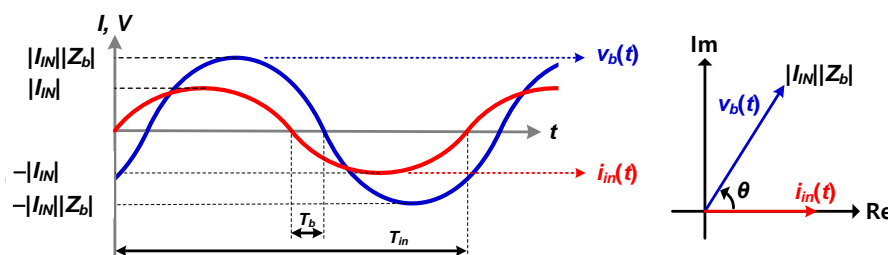
This paper presents the reconfigurable TDC based on cascaded time interpolators [18], which has been fabricated in 0.25- $\mu\text{m}$  CMOS process, with providing comprehensive explanation, detailed analysis, and measurement results. The fabricated TDC quantizes the pulse width corresponding to the phase of  $0^\circ$  to  $90^\circ$  with the peak-to-peak phase error of under  $0.72^\circ$  up to 512-kHz frequency and the phase error of under  $2.70^\circ$  up to 2.048-MHz frequency, demonstrating competitive performances compared to previously reported designs.

## 2. Background and Design Specifications

This section describes the impedance measurement principle and phase measurement scheme in EIS systems. From this background, design specifications are derived at the end of the section.

### 2.1. Impedance Measurement Principle

When a sinusoidal current signal  $i_{in}(t)$  is injected into the target material, a resulting sinusoidal voltage signal  $v_b(t)$  is generated, and its magnitude and time delay with respect to  $i_{in}(t)$  depend on the impedance of the material, as shown in Figure 1.  $Z_b$  is the impedance of the target material, and  $|Z_b|$  and  $\theta$  are the magnitude and phase of  $Z_b$ , respectively.



**Figure 1.** Magnitude and phase of the resulting voltage determined by the impedance under measurement.

Polar demodulators measure the magnitude and time delay of  $v_b(t)$  for a particular frequency.  $|Z_b|$  and  $\theta$  can be calculated as follows:

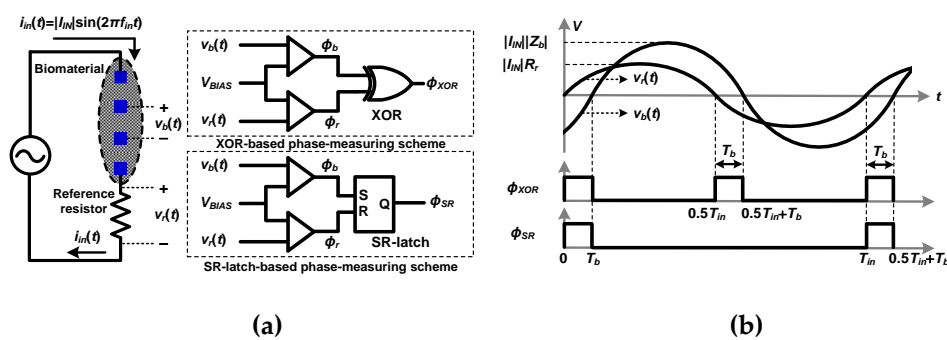
$$|Z_b| = \frac{|v_b(t)|}{|I_{IN}|}, \quad (1)$$

$$\theta = \frac{T_b}{T_{in}}, \quad (2)$$

where  $|v_b(t)|$  and  $T_b$  are the magnitude and time delay of  $v_b(t)$ , respectively.  $|I_{IN}|$  is the magnitude of  $i_{in}(t)$ , and  $T_{in}$  is the period of  $i_{in}(t)$  and  $v_b(t)$ . Impedance spectrum is obtained by using the FRA method, which analyzes one frequency at a time, repeatedly with sweeping the frequency [9].

### 2.2. Phase Measurement Scheme in Polar Demodulators

Figure 2 shows the phase measurement scheme adopted in polar demodulators [10,11,15–17]. When  $i_{in}(t)$  is injected into the target material and reference resistor,  $v_r(t)$  with the same phase as  $i_{in}(t)$  is generated from the resistor in addition to  $v_b(t)$ . Comparators convert  $v_r(t)$  and  $v_b(t)$  to clock signals,  $\phi_r$  and  $\phi_b$ , from which an XOR gate and an SR latch create clock signals,  $\phi_{XOR}$  and  $\phi_{SR}$ , respectively. These clock signals have the pulse width of  $T_b$ , which corresponds to  $\theta$ , as shown in Figure 2. From Equation (2), when the frequency of the injected current,  $f_{in} = 1/T_{in}$  is known,  $\theta$  can be determined by measuring  $T_b$ .



**Figure 2.** (a) Block diagram and (b) waveforms of the phase measurement scheme (reproduced from [19] with permission from the IEEE).

### 2.3. Design Specifications

Design specifications of TDC proposed in this paper are presented in Table 1.  $f_{in}$  is set from 1 kHz to 2.048 MHz because the proposed TDC is implemented in the form of a fully integrated chip for EIS systems in biomedical applications. Considering that the impedance measured in such applications [15] usually has capacitive reactance,  $\theta$  ranges from  $0^\circ$  to  $90^\circ$ , and the corresponding input-time range is 0 to 122 ns at the shortest when  $f_{in}$  is 2.048 MHz and 0 to 250  $\mu$ s at the widest when  $f_{in}$  is 1 kHz. Referring to performances of the previous works reported in [15,17], this TDC aims to have maximum phase error under  $1^\circ$  and phase resolution over 10 bits for the suggested range of  $f_{in}$ . This amount of phase error corresponds to 1.35 ns in the worst case when  $f_{in}$  is 2.048 MHz. Lastly, the frequency of the reference clock ( $f_{clk}$ ) is set to 32.768 MHz, which is only 16 times the maximum  $f_{in}$ . Compared to the TDC in [17], where  $f_{clk}$  is 330 times higher than the maximum  $f_{in}$ , the proposed TDC aims to achieve competitive phase error performance with much lower  $f_{clk}$ .

**Table 1.** Design specifications of the proposed time-to-digital converter (TDC).

Parameter	Target Level
Application	EIS for biomedical applications
Range of the injected signal frequency ( $f_{in}$ )	1 kHz to 2.048 MHz
Corresponding input-time range for $0^\circ$ to $90^\circ$	0–122 ns ( $f_{in} = 2.048$ MHz) to 0–250 $\mu$ s ( $f_{in} = 1$ kHz)
Phase resolution	>10 bit
Maximum phase error	$1^\circ$
Corresponding time error	<~1.35 ns ( $f_{in} = 2.048$ MHz), <~2.8 $\mu$ s ( $f_{in} = 1$ kHz)
Reference clock frequency ( $f_{clk}$ )	32.768 MHz

## 3. Architecture of the Proposed TDC

As shown in Table 1, the requirements of both the input-time range and time resolution vary with  $f_{in}$ . The proposed TDC operates across three different modes to meet the design specifications with maintaining reasonable measurement time. This section describes overall architecture and operation in each mode.

### 3.1. Overall Architecture and Operation

The block diagram of the proposed TDC is presented in Figure 3. The input pulse signal whose pulse width carries  $\theta$  is denoted as  $\phi_{in}$ .  $\phi_{clk}$  is the reference clock, and the outputs of the system are the digital bits,  $D_c$ ,  $D_{f1}$ , and  $D_{f2}$ . This TDC is composed of three stages, namely a coarse stage, the first fine stage, and the second fine stage. The coarse stage consists of a 12-bit coarse counter with digital logics. Each fine stage consists of a time splitter, a reconfigurable time interpolator, and a 4-bit counter. The coarse counter is used to implement a wide input-time range, and two fine stages are employed to

improve resolution without increasing  $f_{clk}$ . In each fine stage, the time splitter extracts quantization error of the preceding stage and the time interpolator stretches the quantization error. The resolution can be improved by quantizing the stretched quantization error through the fine counters and  $\phi_{clk}$ .

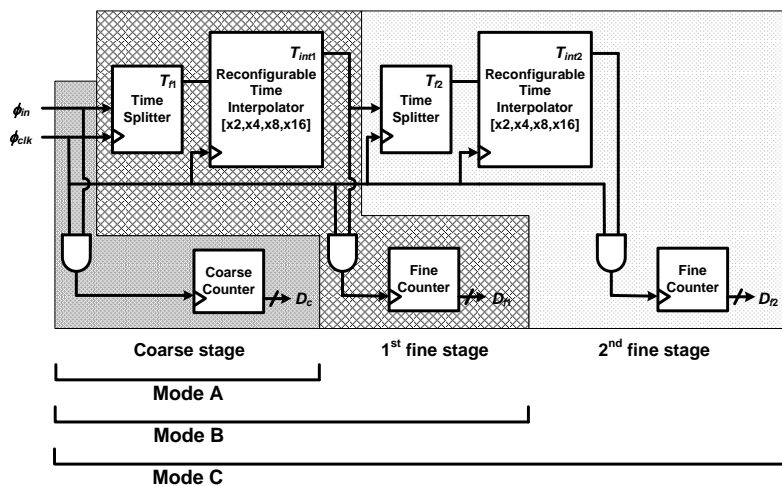


Figure 3. Block diagram of the proposed TDC (reproduced from [18] with permission from the IEEE).

The proposed TDC operates in one of the three modes to achieve the phase resolution over 10 bits. In mode A, only the coarse stage is used, and the time resolution is  $T_{clk}$ . For low  $f_{in}$  of 1 kHz and 2 kHz,  $f_{clk}$  is high enough to achieve target phase resolution. For 4-kHz  $f_{in}$  upwards, the fine stages are used with the coarse stage to further improve the time resolution without increasing  $f_{clk}$ . In mode B, the coarse stage and the first fine stage are used for  $f_{in}$  from 4 kHz to 32 kHz. The first fine stage further quantizes the quantization error of the coarse stage with a time interpolation factor of  $A_{T1}$ . The time resolution in mode B is  $T_{clk}/A_{T1}$ , which is  $A_{T1}$  times higher than the highest resolution in mode A while keeping  $f_{clk} = 32.768$  MHz. In mode C, for 32-kHz  $f_{in}$  upwards, the coarse stage and the first fine stage operate in the same manner. In addition, the second fine stage further quantizes the quantization error of the first fine stage. The time resolution in mode C is  $T_{clk}/(A_{T1}A_{T2})$ , which is  $A_{T1}A_{T2}$  times higher than the highest one in mode A, still keeping  $f_{clk} = 32.768$  MHz. When  $f_{in} = 2.048$  MHz, the coarse stage only achieves a 2-bit resolution for  $\theta$  range from  $0^\circ$  to  $90^\circ$  with  $f_{clk} = 32.768$  MHz. Therefore, the total interpolation factor ( $A_T$ ) of up to 256 is required to achieve a 10-bit resolution for the whole  $f_{in}$  range.  $A_{T1}$  and  $A_{T2}$  are set, as shown in Table 2, across three different modes, A, B, and C, for varying values of  $f_{in}$ .

Table 2. Assignment of the interpolation factor for different operation modes and values of  $f_{in}$ .

Mode	$f_{in}$ (Hz)	$0^\circ$ to $90^\circ$	$f_{clk}$ (Hz)	Coarse	$A_{T1}$	$A_{T2}$
C	2.048M	0~0.1221 $\mu$ s	32.768M	2 bit	16	16
	1.024M	0~0.2441 $\mu$ s	32.768M	3 bit	16	16
	512k	0~0.4883 $\mu$ s	32.768M	4 bit	16	16
	256k	0~0.9766 $\mu$ s	32.768M	5 bit	16	8
	128k	0~1.9531 $\mu$ s	32.768M	6 bit	16	4
	64k	0~3.9063 $\mu$ s	32.768M	7 bit	16	2
B	32k	0~7.8125 $\mu$ s	32.768M	8 bit	16	N/A
	16k	0~15.625 $\mu$ s	32.768M	9 bit	8	N/A
	8k	0~31.25 $\mu$ s	32.768M	10 bit	4	N/A
	4k	0~62.5 $\mu$ s	32.768M	11 bit	2	N/A
A	2k	0~125 $\mu$ s	32.768M	12 bit	N/A	N/A
	1k	0~250 $\mu$ s	16.384M	12 bit	N/A	N/A

When utilizing the time interpolator,  $A_T$  is determined by the ratio of discharging capacitance and discharging current [20]. If the current increases for implementing a large  $A_T$ , the power consumption of TDC increases accordingly. Moreover, since the pulse width of the interpolated signal increases, the conversion time increases significantly, which leads to the degraded conversion rate. Thus, the large  $A_T$  is realized in two steps by dividing  $A_T$  into  $A_{T1}$  and  $A_{T2}$  to offer much more relaxed design conditions.  $A_{T1}$  and  $A_{T2}$  can be adjusted between 2, 4, 8, and 16 to provide 1, 2, 3, and 4 additional bits, respectively. Reconfigurable  $A_{T1}$  and  $A_{T2}$  maintain the phase resolution over 10 bits with reasonably short measurement time.

### 3.2. Operation in Mode A

This mode offers only counter-based time quantization, and the timing diagram of its operation is depicted in Figure 4.

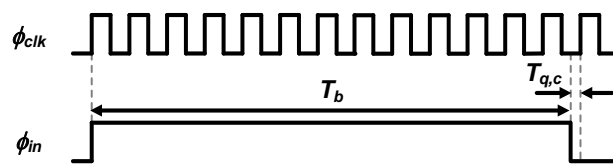


Figure 4. Timing diagram of the proposed TDC in mode A.

The proposed TDC in mode A outputs digital bits  $D_c$  with the relation as follows:

$$T_b = D_c \times T_{clk} - T_{q,c}, \tag{3}$$

where  $T_{q,c}$  is the quantization error of the coarse stage and smaller than  $T_{clk}$ . The time resolution in mode A becomes one period of the clock signal,  $T_{clk}$ . To achieve a 12-bit phase resolution for  $\theta$  range from  $0^\circ$  to  $90^\circ$  at low  $f_{in}$ , this mode is used for  $f_{in}$  of up to 2 kHz.

### 3.3. Operation in Mode B

Mode B uses the coarse stage and the first fine stage, each generating output digital bits,  $D_c$  and  $D_{f1}$ , respectively. The timing diagram of its operation is presented in Figure 5.

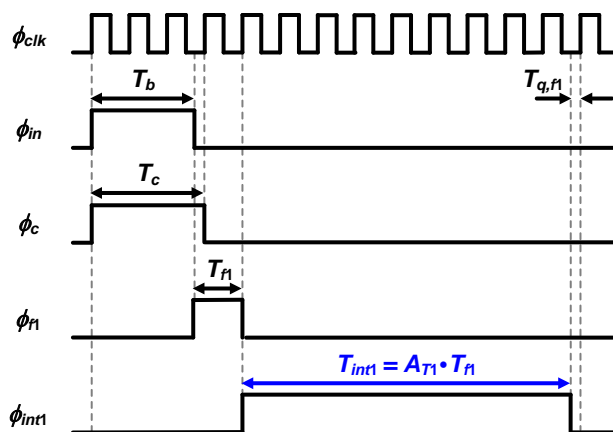


Figure 5. Timing diagram of the proposed TDC in Mode B.

The pulse width of  $T_{f1}$  is generated by the time splitter in the first fine stage and expressed as follows:

$$T_{f1} = T_{q,c} + T_{clk}. \tag{4}$$

The time interpolator in the first stage stretches  $T_{f1}$  to  $T_{int1}$ , which is described by:

$$T_{int1} = A_{T1} \cdot T_{f1}. \quad (5)$$

The fine counter quantizes  $T_{int1}$  with the reference clock, to output up to four fine digital bits,  $D_{f1}$ . The relation among  $T_b$ ,  $D_c$ , and  $D_{f1}$  is given by:

$$T_b = T_c - (T_{f1} - T_{clk}) = (D_c \times T_{clk}) - \left( \frac{T_{int1}}{A_{T1}} - T_{clk} \right) = (D_c \times T_{clk}) - \left( \frac{D_{f1} \times T_{clk} - T_{q,f1}}{A_{T1}} - T_{clk} \right), \quad (6)$$

where  $T_{q,f1}/A_{T1}$  is always smaller than  $T_{clk}$ . The time resolution in mode B is improved from  $T_{clk}$  to  $T_{clk}/A_{T1}$ , which is  $A_{T1}$  times higher than the highest resolution in mode A while keeping  $f_{clk} = 32.768$  MHz. To achieve a 12-bit phase resolution for  $\theta$  range from  $0^\circ$  to  $90^\circ$ ,  $f_{in}$  must satisfy the following condition:

$$\frac{1}{f_{in}} \cdot \frac{90}{360} \cdot \frac{1}{2^{12}} < \frac{T_{clk}}{A_{T1}}. \quad (7)$$

With the maximum  $A_{T1}$  of 16, this mode is used until  $f_{in}$  increases up to 32 kHz.

### 3.4. Operation in Mode C

The mode C uses the coarse stage, the first fine stage, and the second fine stage, each generating output digital bits,  $D_c$ ,  $D_{f1}$ , and  $D_{f2}$ , respectively. The timing diagram of its operation is presented in Figure 6.

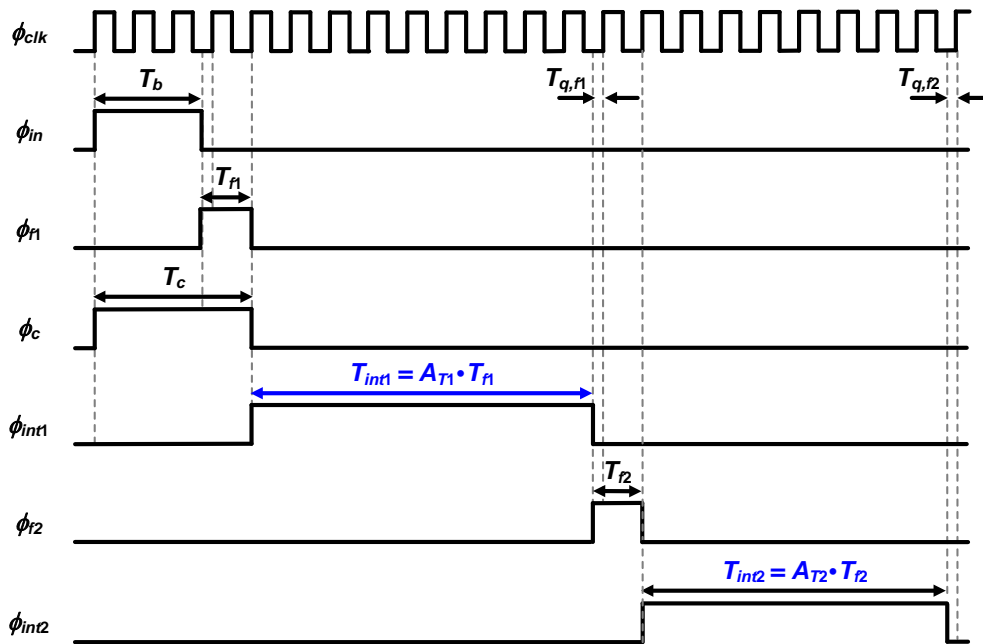


Figure 6. Timing diagram of the proposed TDC in mode C.

The coarse stage and the first fine stage operate in the same manner as in mode B. The time splitter in the second stage generates  $T_{f2}$ , which is expressed as:

$$T_{f2} = T_{q,f1} + T_{clk}. \quad (8)$$

The time interpolator in the second stage stretches  $T_{f2}$  to  $T_{int2}$ , which is described by:

$$T_{int2} = A_{T2} \cdot T_{f2}. \quad (9)$$

The fine counter in the second fine stage quantizes  $T_{int2}$  with the reference clock, to output up to four fine digital bits,  $D_2$ . The relation among  $T_b$ ,  $D_c$ ,  $D_{f1}$ , and  $D_{f2}$  is given by:

$$\begin{aligned} T_b &= (D_c \times T_{clk}) - \left( \frac{D_{f1} \times T_{clk} - T_{q,f1}}{A_{T1}} - T_{clk} \right) = (D_c \times T_{clk}) - \left\{ \frac{D_{f1} \times T_{clk} - (T_{f2} - T_{clk})}{A_{T1}} - T_{clk} \right\} \\ &= (D_c \times T_{clk}) - \left\{ \frac{D_{f1} \times T_{clk} - \left( \frac{D_{f2} \times T_{clk} - T_{q,f2}}{A_{T2}} - T_{clk} \right)}{A_{T1}} - T_{clk} \right\} \\ &= \{(D_c + 1) \times T_{clk}\} - \left\{ \frac{(D_{f1} - 1) \times T_{clk}}{A_{T1}} \right\} + \left( \frac{D_{f2} \times T_{clk} - T_{q,f2}}{A_{T1} A_{T2}} \right), \end{aligned} \quad (10)$$

where  $T_{q,f2}/(A_{T1}A_{T2})$  is always smaller than  $T_{clk}$ . The time resolution in mode C is improved from  $T_{clk}$  to  $T_{clk}/(A_{T1}A_{T2})$ , which is  $A_{T1}A_{T2}$  times higher than the highest resolution in mode A, even though  $f_{clk} = 32.768$  MHz is kept. To achieve a 10-bit phase resolution for  $\theta$  range from  $0^\circ$  to  $90^\circ$ ,  $f_{in}$  must satisfy the following condition:

$$\frac{1}{f_{in}} \cdot \frac{90}{360} \cdot \frac{1}{2^{10}} < \frac{T_{clk}}{A_{T1}A_{T2}}. \quad (11)$$

with the maximum  $A_{T1}$  and  $A_{T2}$  of 16, this mode is used for  $f_{in}$  of up to 2.048 MHz.

#### 4. Circuit Design

This section describes how the first fine stage is designed to realize time interpolation with reconfigurable  $A_{T1}$ . The second fine stage is designed to be identical to the first one.

##### 4.1. Time Splitter

Figure 7 shows the structure of the time splitter, which consists of three D flip-flops and one NOR gate. As shown in Figures 5 and 6, the time splitter extracts the quantization error of the coarse stage with an offset of  $T_{clk}$ . This offset is employed to avoid the metastability issue of the D flip-flops [20]. Therefore,  $T_{f1}$  takes the value from  $T_{clk}$  to  $2T_{clk}$ , corresponding to 30.52 ns to 61.04 ns. As shown in Equations (6) and (10), in mode B and C, the offset is compensated when  $T_b$  is calculated from the digital outputs.

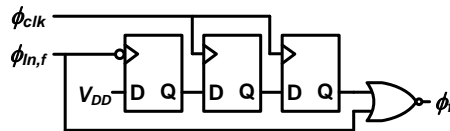


Figure 7. Structure of the time splitter (reproduced from [18] with permission from the IEEE).

##### 4.2. Reconfigurable Time Interpolator

Figure 8 shows the block diagram and timing diagram of the reconfigurable time interpolator. The reconfigurable time interpolator is similar to the time interpolator in [20]. A variable discharging capacitor, which has the capacitance of  $C_{INT}$ , is added to obtain reconfigurable  $A_{T1}$ .

While  $\phi_{f1}$ , which has the pulse width of  $T_{f1}$ , is high, a capacitor which has the capacitance of  $C_F$  is discharged by a constant current,  $I_F$ , such that  $v_1(t)$  drops by  $\Delta V$ .  $\Delta V$  is expressed as follows:

$$\Delta V = \frac{I_F \cdot T_{f1}}{C_F}. \quad (12)$$

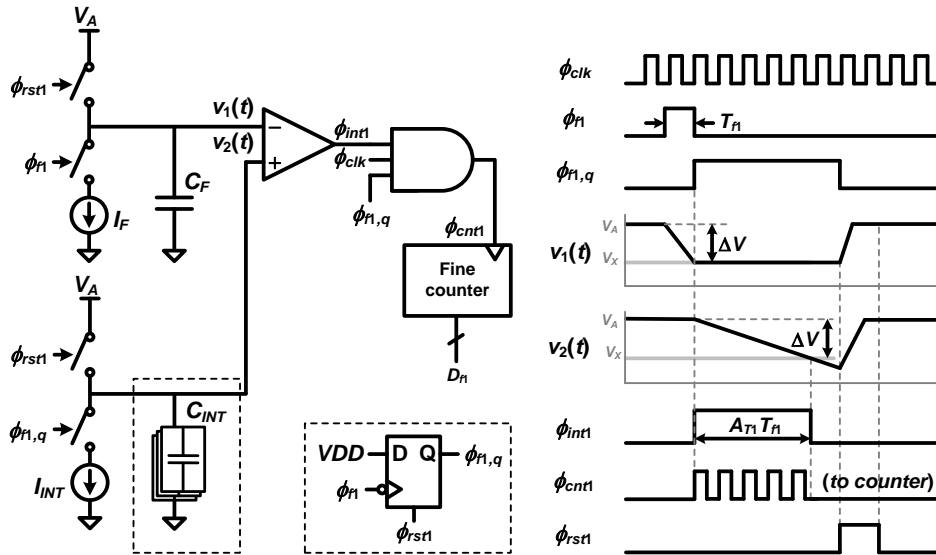
From the falling edge of  $\phi_{f1}$ , a capacitor of  $C_{INT}$  is discharged by a constant current,  $I_{INT}$ , during  $\phi_{f1,q}$  is high. In the same manner with Equation (12), the pulse width of  $\phi_{f1,q}$  is expressed as follows:

$$A_{T1} \cdot T_{f1} = \frac{C_{INT}}{I_{INT}} \cdot \Delta V = \frac{C_{INT}}{I_{INT}} \cdot \frac{I_F}{C_F} \cdot T_{f1} = \frac{C_{INT}}{C_F} \cdot \frac{I_F}{I_{INT}} \cdot T_{f1} = (M \cdot N) \cdot T_{f1}, \quad (13)$$



where  $M$  is the capacitance ratio,  $C_{INT}/C_F$ ,  $N$  is the current ratio,  $I_F/I_{INT}$ , and  $A_{T1}$  is  $M \cdot N$ .

In the proposed TDC,  $N$  is kept constant while  $M$  is controlled to change  $A_{T1}$  between 2, 4, 8, and 16. Adjustment of the capacitance value is selected over the current value because controlling the capacitance ratio is more accurate than controlling the current ratio in IC implementation. In each fine stage, since  $N$  is fixed to 2,  $C_F$  is kept constant as 3.6 pF, and  $C_{INT}$  is changed across 3.6 pF, 7.2 pF, 14.4 pF, and 28.8 pF.  $I_F$  and  $I_{INT}$  are 80  $\mu$ A and 40  $\mu$ A, respectively.



**Figure 8.** Block diagram and timing diagram of the reconfigurable time interpolator (reproduced from [18] with permission from the IEEE).

#### 4.3. Novel Features of the Proposed TDC

The proposed TDC employs time interpolation technique, which can improve time resolution without increasing  $f_{clk}$  in the counter-based TDC. However, two inherent issues are associated with large  $A_T$ . Although the resolution becomes much higher when the front-stage quantization error is interpolated with  $A_T$ , the chip size or power consumption increases by a substantial amount because  $A_T$  is determined by capacitance ratio or current ratio. Also, the conversion time increases significantly because the interpolated pulse width increases as  $A_T$  increases. A novel structure of cascading two separate fine stages resolves these two issues at the same time.

When  $A_T$  of 256 is obtained by using a single-stage time interpolator with  $C_F$  of 1 pF and  $C_{INT}$  of 256 pF, this results in excessively large chip size and poor area efficiency. In the proposed TDC, two interpolation stages are cascaded. As a result, the interpolation factor of only 16 is required in each stage instead of 256. In other words, this system requires two capacitors with the size of  $C_{INT}$ , which is equal to 16  $C_F$ . Compared to the single stage with  $A_T$  of 256, this approach reduces the area used for implementing the discharging capacitors by a factor of  $257/34 = \sim 7.6$  times considering that one time interpolator has two discharging capacitors with the sizes of  $C_{INT}$  and  $C_F$ . As the time interpolators in fine stages occupy a significant portion of the chip size, the area efficiency of the system is greatly improved. On the other hand, when  $A_T$  of 256 is set by the capacitance ratio, the current consumption of the cascaded time interpolation stages is two times higher than that of the single-stage time interpolator. For the single interpolator with  $A_T$  of 256, from the falling edge of  $\phi_c$ , the conversion time of  $A_T T_{f1}$  is required for fine conversion, and the maximum conversion time is  $2A_T T_{clk}$  considering the offset of the time splitter. For two cascaded interpolation stages with  $A_{T1}$  and  $A_{T2}$  of 16, the conversion time of each fine stage is  $A_{T1} T_{f1}$  or  $A_{T2} T_{f1}$ , and the maximum conversion time of each stage is  $2A_{T1} T_{clk}$  or  $2A_{T2} T_{clk}$ . Compared to the single interpolator with  $A_T$  of 256, when  $A_{T1} = A_{T2} = 16$ , the conversion time for fine conversion is reduced by approximately 8 times.

When  $N_f$  of time interpolation stages are cascaded and  $A_T$  is set by the capacitance ratio, the area efficiency ( $E_A$ ), power efficiency ( $E_P$ ), and conversion-time efficiency for fine stages ( $E_C$ ) can be defined and expressed as follows:

$$E_A = \frac{\text{Total capacitance in an interpolation stage when } N_f = 1}{\text{Total capacitance in interpolation stages when } N_f > 1} = \frac{(1 + A_T)C_F}{N_f(1 + \sqrt[N_f]{A_T})C_F} = \frac{1 + A_T}{N_f(1 + \sqrt[N_f]{A_T})}, \quad (14)$$

$$E_P = \frac{\text{The current consumption of an interpolation stage when } N_f = 1}{\text{The current consumption of interpolation stages when } N_f > 1} = \frac{I_{fine}}{N_f \cdot I_{fine}} = \frac{1}{N_f}, \quad (15)$$

$$E_C = \frac{\text{The max. conversion time through a fine stage when } N_f = 1}{\text{The max. conversion time through fine stages when } N_f > 1} \approx \frac{A_T \cdot 2T_{clk}}{N_f \cdot \sqrt[N_f]{A_T} \cdot 2T_{clk}} = \frac{A_T}{N_f \cdot \sqrt[N_f]{A_T}}, \quad (16)$$

where  $I_{fine}$  is the current consumption of a single time interpolation stage.

Table 3 summarizes  $E_A$ ,  $E_P$ , and  $E_C$  calculated using Equations (14)–(16). Although the maximum  $E_A \cdot E_P \cdot E_C$  value is obtained when  $N_f = 4$ , we chose  $N_f = 2$  to minimize the current consumption while taking advantages of the cascaded time interpolators in terms of area and conversion time. The largest capacitor with size of 28.8 pF is small enough to integrate on chip and  $2A_T T_{clk} = \sim 1 \mu\text{s}$  of conversion time for the fine stage is short enough.

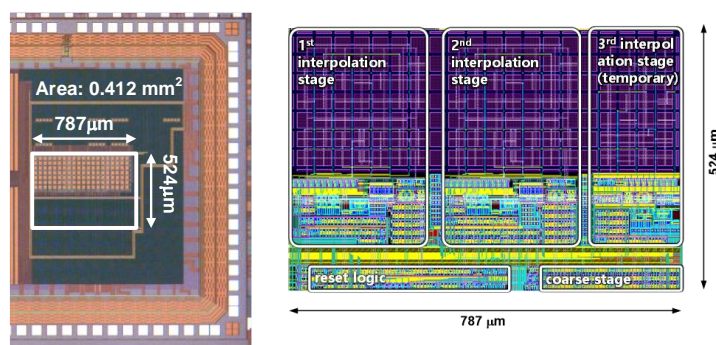
**Table 3.**  $E_A$ ,  $E_P$ , and  $E_C$  versus  $N_f$  when  $A_T$  is set by the capacitance ratio.

$A_T$	$N_f$	$E_A$	$E_P$	$E_C$	$E_A \cdot E_P \cdot E_C$
256	2	7.6	8	0.5	30.4
256	4	12.9	16	0.25	51.6
256	8	10.7	16	0.125	21.4

It is also possible to obtain  $A_T$  through the current ratio of  $I_F/I_{INT}$  in Figure 8. In this case, setting the current ratio to 256 directly affects the static power, severely degrading the power efficiency of the system. Total discharging current of cascaded time interpolation stages when  $N_f = 2$  could be 7.6-times smaller than that of a single time interpolation stage when  $N_f = 1$ , and the total capacitance of cascaded time interpolation stages when  $N_f = 2$  could be two times larger than that of a single time interpolation stage when  $N_f = 1$ . Compared to the single interpolator with  $A_T$  of 256 and  $N_f = 1$ , when  $N_f = 2$ , the time for fine conversion is reduced by approximately eight times. The optimization process when  $A_T$  is set by the current ratio would be similar to that when  $A_T$  is set by the capacitance ratio.

## 5. Measurement Results

The proposed TDC has been fabricated with a 0.25- $\mu\text{m}$  CMOS process. The size of the circuit is  $787 \mu\text{m} \times 524 \mu\text{m}$  ( $0.412 \text{ mm}^2$ ). The chip photograph and layout of the fabricated IC are presented in Figure 9.



**Figure 9.** Chip photograph and layout.

Figure 10 shows the measurement setup. Two Agilent 33250A function generators are used, one for generating  $\phi_{clk}$  and another for generating  $\phi_{in}$  whose pulse width varies from 0 to 0.25 of the period which corresponds to the phase of  $0^\circ$  to  $90^\circ$ . These two function generators are synchronized with each other. In the case of generating  $\phi_{in}$  in the form of pulse train, the period can be adjusted from 20.00 ns to 2000.0 s, and its pulse width can be controlled from 8.0 ns to 1999.9 s. Therefore, when  $f_{in} = 2.048$  MHz, the phase above  $5.9^\circ$  could be measured. Arduino DUE was selected for a microcontroller unit because it has 54 digital I/O pins which are enough for receiving digital output bits and transmitting assignment codes through SPI for the reconfiguration of TDC. Moreover, its clock speed of 84 MHz allows generating required signals to initialize the SPI communication and select between the read and write modes. Monitoring pads are placed on the main propagation path of signal to examine whether each block and each stage operate as expected. Keysight Technologies DSO7104A oscilloscope was used throughout the measurement. The oscilloscope has enough sample rate of 4 Gsps, bandwidth of 1 GHz, and four scope channels.

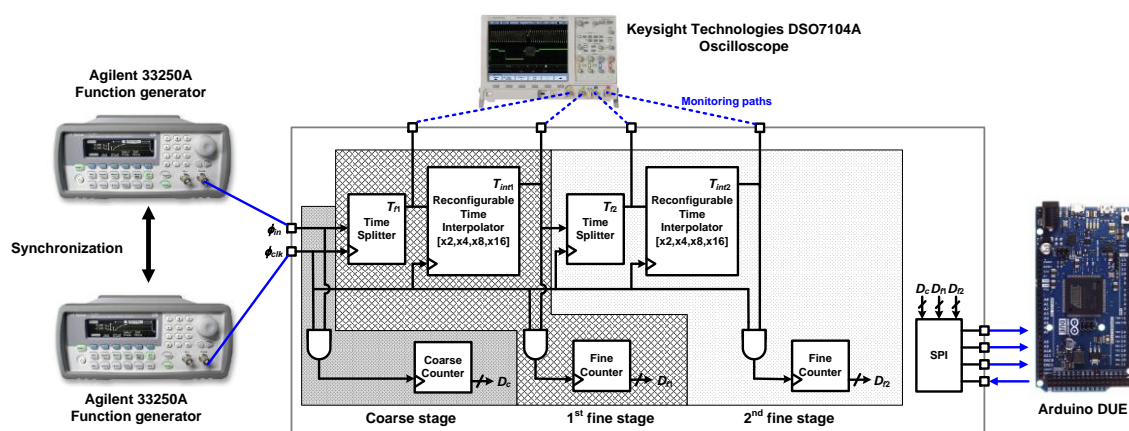


Figure 10. Measurement setup.

In this section, measurement results for one frequency in mode A, one in mode B, and one in mode C are shown. The input-output characteristics of the fabricated TDC are described in Figures 11a, 12a and 13a. Figures 11b, 12b and 13b present the phase errors in each frequency.

### 5.1. Mode A

Measurement results for  $f_{in} = 1$  kHz are shown in Figure 11. Only the coarse stage is used, and the TDC operates as a counter-based TDC with  $f_{clk} = 16.384$  MHz, halved from the 32.768-MHz clock signal provided by the function generator. The input-output characteristic of the TDC is shown in Figure 11a, where the horizontal axis indicates the pulse width of the input signal in seconds, and the vertical axis shows the TDC output code in units of LSB. The solid line represents theoretical output values for given pulse widths of the input. Figure 11b presents the phase error calculated from the digital output code as a function of the actual phase injected at the input. The input phase is varied with a step size of  $0.0005^\circ$ , which corresponds to about 1.4 ns. The difference between the maximum and minimum phase errors is about  $0.022^\circ$ , implying that the error of the measured output lies within 12-bit-resolution quantization error for  $\theta$  range from  $0^\circ$  to  $90^\circ$  and that the TDC operates as expected.

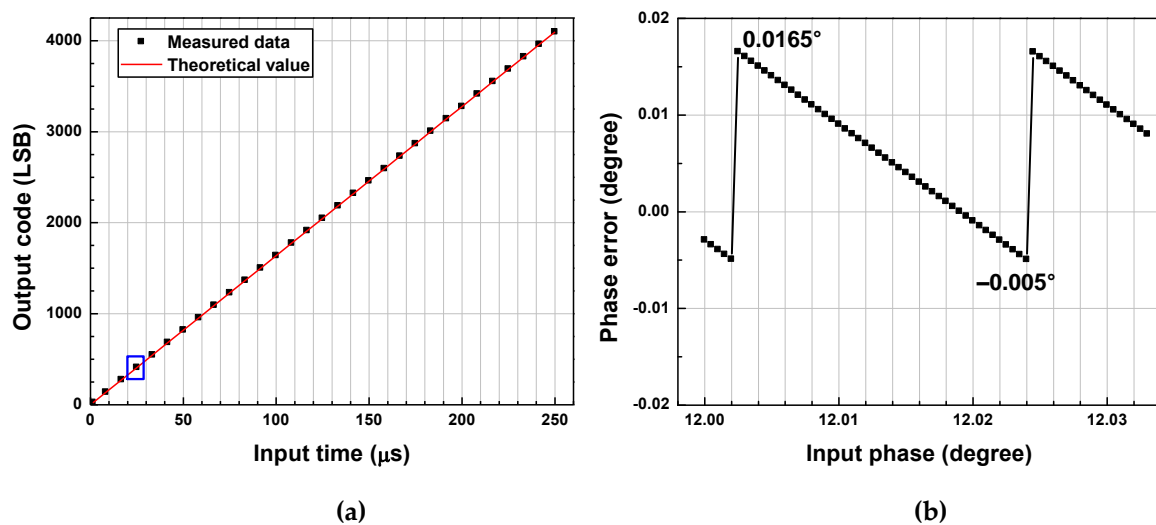


Figure 11. (a) Measured input-output characteristic of TDC, and (b) phase errors for  $f_{in} = 1$  kHz.

### 5.2. Mode B

Measurement results for  $f_{in} = 8$  kHz are shown in Figure 12. The coarse stage and the first fine stage are used with  $f_{clk} = 32.768$  MHz and  $A_{T1} = 4$ . However,  $A_{T1}$  of 4.05 is obtained from the measured  $T_{int1}$  and  $T_{f1}$ , and this value is substituted to Equation (6) to derive  $T_b$  using output code. The input-output characteristic of the TDC is shown in Figure 12a, where the horizontal axis, vertical axis, and solid line are as described in Figure 11a. Figure 12b presents the phase error calculated from the digital output code as a function of the actual phase injected at the input. The input phase is varied with a step size of  $0.0003^\circ$ , which corresponds to 0.1 ns. The peak-to-peak phase error is about  $0.022^\circ$ , implying that the error of the measured output lies within 12-bit-resolution quantization error for  $\theta$  range from  $0^\circ$  to  $90^\circ$ . This result shows a good agreement with the theoretical prediction.

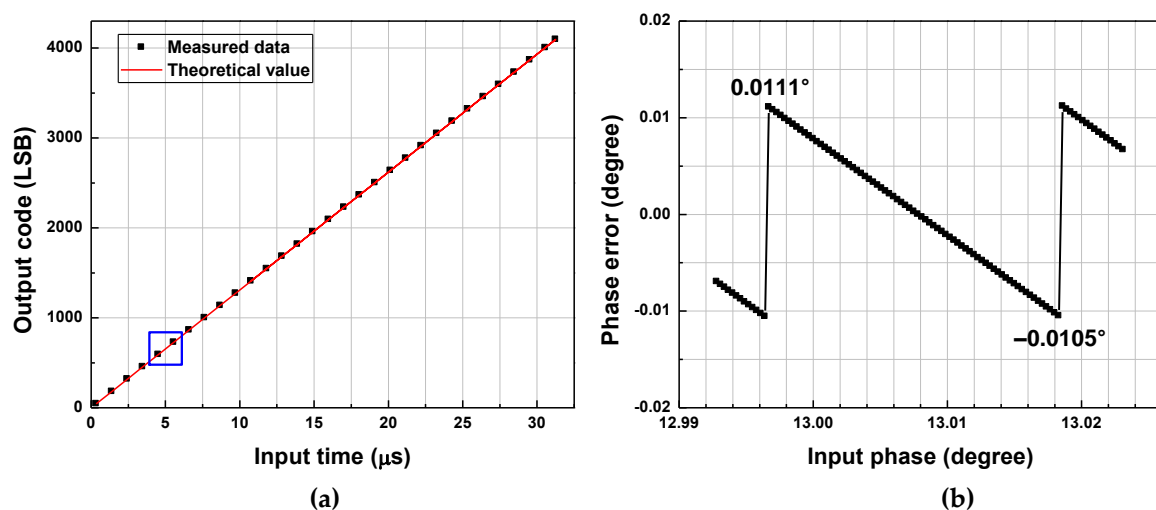
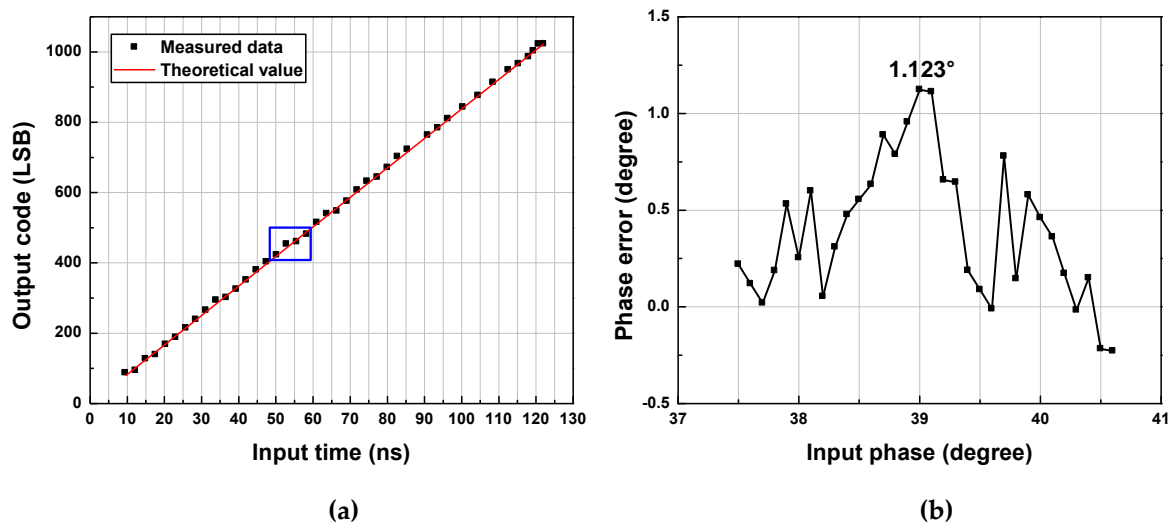


Figure 12. (a) Measured input-output characteristic of TDC, and (b) phase errors for  $f_{in} = 8$  kHz.

### 5.3. Mode C

Measurement results for  $f_{in} = 2.048$  MHz are shown in Figure 13. For  $f_{in} = 2.048$  MHz,  $A_{T1}$  and  $A_{T2}$  are both set to 16 to achieve the largest  $A_T$  of 256. However,  $A_{T1}$  of 15.9 and  $A_{T2}$  of 15.9 are obtained, and these values are substituted to Equation (10) to derive  $T_b$  using output code. The input-output characteristic of the TDC is shown in Figure 13a, where the horizontal axis, vertical axis, and the solid line are as described in Figure 11a. Figure 13b presents the phase error calculated from the digital

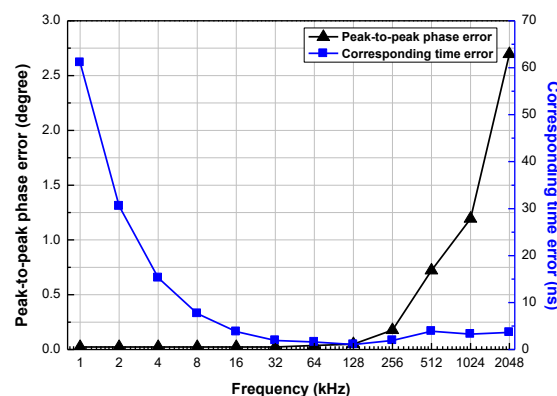
output code as a function of the actual phase injected at the input. The input phase is varied with a step size of  $0.07^\circ$ , which corresponds to 0.1 ns. The peak positive phase error is  $1.123^\circ$ , and the peak negative phase error is  $-1.846^\circ$ , resulting in the peak-to-peak phase error of  $2.969^\circ$ . This phase error is beyond the target quantization error of  $0.088^\circ$  and target phase error of  $1^\circ$ . The error analysis for the mode-C operation is presented in the next sub-section with a summary of the measurement results.



**Figure 13.** (a) Measured input-output characteristic of TDC, and (b) the maximum positive phase error for  $f_{in} = 2.048$  MHz.

#### 5.4. Error Analysis

The peak-to-peak phase error and corresponding time error for  $f_{in}$  from 1 kHz to 2.048 MHz are described in Figure 14. The peak-to-peak phase error is proportional to  $f_{in}$  and exceeds  $1^\circ$  for only when  $f_{in} = 1.024$  MHz and  $f_{in} = 2.048$  MHz.



**Figure 14.** Peak-to-peak phase error and corresponding time error for  $f_{in}$  from 1 kHz to 2.048 MHz.

Table 4 summarizes the exact values of the peak-to-peak phase error and corresponding time error as a function of  $f_{in}$ . It also shows the values of  $A_{T1}$  and  $A_{T2}$  set for the measurement. Although  $A_{T2}$  increases, the corresponding time error does not decrease below 1.06 ns.

Table 4. Peak-to-peak phase error and corresponding time error in mode C.

$f_{in}$ (Hz)	$A_{T1}$	$A_{T2}$	Target Phase Error (°)	Peak-to-Peak Phase Error (°)	Corresponding Time Error (ns)
64k	16	2	0.022	0.037	1.61
128k	16	4	0.022	0.049	1.06
256k	16	8	0.022	0.178	1.93
512k	16	16	0.022	0.721	3.91
1.024M	16	16	0.088	1.194	3.29
2.048M	16	16	0.088	2.696	3.66

These extra errors would come from the uncertainty of comparator operation in time interpolators. The schematic of comparators and the uncertainty caused by the comparator operation during time interpolation are shown in Figure 15a,b, respectively. The comparators are designed by cascading two self-biased inverters as in [21,22].

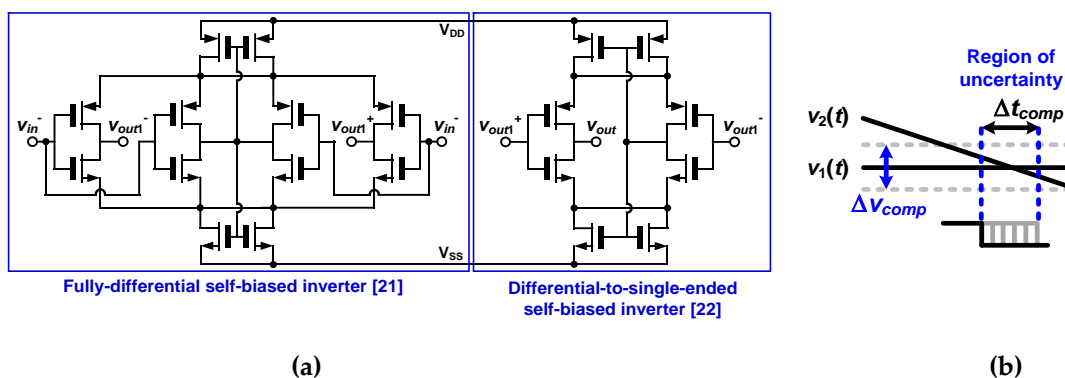


Figure 15. (a) Schematic of comparators and (b) the uncertainty caused by comparators during time interpolation.

As shown in Figure 15b, if there is a voltage-domain uncertainty of  $\Delta v_{comp}$  when  $v_1(t)$  and  $v_2(t)$  cross each other,  $\Delta v_{comp}$  causes a time-domain uncertainty of  $\Delta t_{comp}$ , which is given by:

$$\Delta t_{comp} = \Delta v_{comp} \frac{C_{INT}}{I_{INT}}. \tag{17}$$

Therefore,  $\Delta v_{comp}$  should be minimized in order to reduce  $\Delta t_{comp}$  and hence extra time errors. The finite resolution and noise of the comparator would cause the uncertainty in the voltage domain, which, in turn, is translated into the uncertainty in the time domain.

The resolution of the comparator ( $\Delta v_{min,comp}$ ), which means the minimum input difference that saturates the output, is expressed as follows [23]:

$$\Delta v_{min,comp} = \frac{V_{OH} - V_{OL}}{A_{v0}}, \tag{18}$$

where  $A_{v0}$  is the open-loop gain of the comparator,  $V_{OH}$  is the output voltage when the output is high, and  $V_{OL}$  is the output voltage when the output is low.  $V_{OH}$  and  $V_{OL}$  should be large and small enough, respectively, so that the following digital logic can distinguish binary states. That is, when the transient behavior of  $v_1(t)$  and  $v_2(t)$  is not fast enough or  $A_{v0}$  is not sufficiently large, the comparator suffers from a substantial uncertainty in time domain ( $\Delta t_{comp}$ ) because it will take relatively longer time for the following digital logic to determine binary states.

Considering that  $T_{f1}$  and  $T_{f2}$  vary within the range from  $T_{clk}$  to  $2T_{clk}$ , the crossing point of  $v_1(t)$  and  $v_2(t)$  in Figure 15b falls within the voltage range from 0.9 V to 1.4 V. In this voltage range,  $A_{v0}$  varies between 41.8 dB and 58.0 dB depending on the voltage level where  $v_1(t)$  and  $v_2(t)$  intersect.

From  $A_{v0} = 41.8$  dB and supply voltage of 2.5 V,  $\Delta v_{min,comp}$  is about 20.3 mV. For  $f_{in} = 128$  kHz with  $A_{T1} = 15.9$  and  $A_{T2} = 4.05$ ,  $\Delta t_{comp}$  in the first stage caused by  $\Delta v_{min,comp}$  is calculated as about 14.6 ns by substituting  $C_{INT} = 28.8$  pF and  $I_{INT} = 40$   $\mu$ A into Equation (17). This  $\Delta t_{comp}$  in the first fine stage is divided by  $A_{T1}$  after being quantized by the fine counter. Therefore, the fabricated TDC could not achieve the time error below 0.92 ns.

The noise of comparator would become another source of uncertainty. The input-referred noise voltage of the differential-to-single-ended self-biased inverter in Figure 15a is expressed as follows [24]:

$$\overline{V_{n,inv}^2(f)} = \left[ \frac{1}{W_P L_P} + \frac{1}{W_N L_N} \right] \cdot \frac{2K}{f \cdot C_{OX}} + \frac{8kT\gamma}{g_{m,N} + g_{m,P}}, \quad (19)$$

where  $W_P$  and  $L_P$  are the width and length of the input PMOS transistor, respectively, while  $W_N$  and  $L_N$  are the width and length of the input NMOS transistor, respectively.  $K$  is the process-dependent flicker noise constant.  $g_{m,N}$  and  $g_{m,P}$  are the transconductances of the NMOS and PMOS input transistors, respectively. The input-referred noise of the fully differential self-biased inverter is also given by Equation (19).

Since the noise of the first stage is dominant compared to that of the second stage and the 1/f noise can be ignored because of the wide bandwidth of the comparator, the input-referred noise voltage of the comparator can be approximated as follows:

$$\overline{V_{n,comp}^2(f)} \approx \frac{8kT\gamma}{g_{m,N} + g_{m,P}}. \quad (20)$$

When  $T = 300$  K,  $\gamma = 1$ , and noise bandwidth = 100 MHz, the input-referred noise of the comparator is about 1.8 mV<sub>rms</sub>, 180  $\mu$ V<sub>rms</sub>, and 18  $\mu$ V<sub>rms</sub> for  $g_{m,N} + g_{m,P} = 1$   $\mu$ S,  $g_{m,N} + g_{m,P} = 10$   $\mu$ S,  $g_{m,N} + g_{m,P} = 100$   $\mu$ S, respectively. Since our TDC consumes enough current, the uncertainty due to the comparator noise is not significant in our design. However, if the bandwidth of the comparator is very large and  $g_{m,N} + g_{m,P}$  is small, considerable uncertainties may occur. For  $f_{in} = 128$  kHz with  $A_{T1} = 15.9$  and  $A_{T2} = 4.05$ , the voltage-domain uncertainty of 1.8 mV<sub>rms</sub> causes  $\Delta t_{comp} = 1.3$  ns<sub>rms</sub>, which corresponds to the time error of 0.08 ns<sub>rms</sub>. In particular, it is important to ensure that the value of  $g_{m,N} + g_{m,P}$  is sufficiently large when the bandwidth of the comparator is wide.

Since the extra time errors are mainly due to the resolution of comparators, the errors would be mitigated if the comparators based on multi-stage amplifiers are used as in [15]. In such comparators, the optimum number of amplifier stages,  $N_{OPT}$ , is expressed as follows [15]:

$$N_{OPT} \approx 1.1 \times \ln \left( \frac{V_{OH}}{\Delta v_{min,comp}} \right) + 0.79. \quad (21)$$

By replacing the two-stage high-gain amplifiers with multiple stages of low-gain amplifiers, the improved  $\Delta t_{comp}$  can be obtained as  $\Delta v_{min,comp}$  is reduced.

Moreover, when  $A_{T2}$  increases from 8 to 16, the time error increases rather than decreases. Therefore, another way of improving the extra time error is measuring the quantization error of the first stage without performing time interpolation of the second fine stage. In [19], we employed a chain delay line in the second fine stage instead of the time interpolator, and the results were verified by simulation. Since the mismatches between unit delay cells would occur, the proposed architecture needs to be verified by measurement.

### 5.5. Performance Summary and Comparison

Table 5 summarizes performances of the presented TDC, together with those of two polar demodulators and two TDCs, reported previously. In comparison with the TDC in [20] that consists of a coarse counter and a single-stage time interpolator with large  $A_T$  of 250, our TDC offers lower complexity and shorter conversion time for achieving the same phase resolution, as analyzed in

Section 4.3. Compared to the TDC presented in this manuscript, another kind of our TDC in [19] seems to achieve smaller phase error. However, the TDC in [19] has not yet been verified by measurement. Through our future work, the TDC in [19] will be fabricated and measured. The phase error performance of our TDC presented in this paper is competitive when compared with previously reported designs in [15,17].

**Table 5.** Performance summary and comparison.

	This Work	<i>IEEE Sensors J.</i> ' 2013 [15]	<b>IEEE MWSCAS'</b> 2013 [17]	<i>IEEE TNS.</i> ' 2006 [20]	<b>IEEE MWSCAS'</b> 2017 [19]
Tech.	0.25 $\mu\text{m}$	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	0.18 $\mu\text{m}$
Application	EIS	EIS	EIS	N/A	EIS
Implementation scope	TDC	Polar demodulator	Polar demodulator	TDC	TDC
Architecture	Counter + Cascaded time interpolator	TVC with ADC	Counter	Counter + time stretchers	Counter+ time stretcher + chain-delay-line
$f_{in}$	1 kHz–2.048 MHz	0.1 kHz–100 kHz	0.1 kHz–10 MHz	N/A	1 kHz–2.048 MHz
$f_{clk}$	32.768 MHz	No use	3.33 GHz	80 MHz	32.768 MHz
Power	7.5 mW	21 mW	*28 mW	0.75 mW	<b>2.4 mW</b>
Supply	2.5 V	2.5 V	1.8 V	3 V–4 V	1.8 V
Area	0.41 $\text{mm}^2$	*0.40 $\text{mm}^2$	*0.40 $\text{mm}^2$	0.23 $\text{mm}^2$	0.35 $\text{mm}^2$
Time resolution	N/A	N/A	300 ps	50 ps	103 ps–244 ns
Phase error	<0.72° (@512 kHz) <2.70° (@2.048 MHz)	<3.95°	<2.2°	N/A	<0.088°
Remarks	Meas.	Meas.	Meas.	Meas.	Sim.

\* Total power consumption or size of entire polar demodulator for EIS system.

## 6. Conclusions

A reconfigurable time-to-digital converter (TDC) used to quantize the phase of impedance in electrical impedance spectroscopy (EIS) is introduced in this manuscript and verified through the fabricated IC. This TDC adopts a coarse counter to have a wide input-time range and cascaded time interpolators to improve resolution in the high-frequency analysis without increasing counting clock speed. When the same large interpolation factor is assumed, the cascaded time interpolators have shorter measurement time and smaller chip area than a single-stage time interpolator. The reconfigurable time interpolation factor maintains phase resolution within an appropriate level while providing reasonable measurement time. The fabricated TDC achieves the peak-to-peak phase error of under 0.72° for the input frequency range from 1 kHz to 512 kHz and the peak-to-peak phase error of 2.70° when it covers up to 2.048 MHz, demonstrating competitive performances in comparison with previously reported designs. Two precision improvement methods are also proposed: revision of the comparator, and revision of the second fine stage. As future work, we plan to fabricate the TDC that uses chain delay lines in the second fine stage and compare it with the TDC based on cascaded time interpolators.



**Author Contributions:** S.S., S.-J.K., and J.-H.P. implemented and measured the IC. S.S. and Y.J. analyzed the measurement results and wrote the draft of the manuscript through E.L. and J.K.'s editing and discussion. H.-J.Y. and M.J. helped in setting the target specification. S.-J.K. is the corresponding author, reviewed and edited this manuscript through discussion with H.-J.Y. and M.J. All authors discussed the results and commented on the manuscript. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was supported in part by Basic Science Research Program under grant number NRF-2018R1A6A3A01013018 and BK21 plus program through the National Research Foundation (NRF) of Korea funded by the Ministry of Education. In addition, this research was supported in part by the Convergence Technology Development Program for Bionic Arm (2017M3C1B2085296) through NRF of Korea funded by the Ministry of Science & ICT.

**Acknowledgments:** The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

**Conflicts of Interest:** The authors declare no conflict of interest.

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