sensors

MDPI

Article

DC Voltage Sensorless Predictive Control of a High-Efficiency PFC Single-Phase Rectifier Based on the Versatile Buck-Boost Converter

Catalina González-Castaño [1], Carlos Restrepo [2,*], Fredy Sanz [1], Andrii Chub [3] and Roberto Giral [4]

[1] Facultad de Ingeniería, Ingeniería Mecatrónica de la Universidad Manuela Beltrán, Bogotá 110231, Colombia; catalina.castano@docentes.umb.edu.co (C.G.-C.); fredy.sanz@umb.edu.co (F.S.)
[2] Department of Electromechanics and Energy Conversion, Universidad de Talca, Curicó 3340000, Chile
[3] Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, 19086 Tallinn, Estonia; andrii.chub@taltech.ee
[4] Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Escola Tècnica Superior d'Enginyeria, Universitat Rovira i Virgili, 43007 Tarragona, Spain; roberto.giral@urv.cat
* Correspondence: crestrepo@utalca.cl; Tel.: +56-75-2-201-815

Abstract: Many electronic power distribution systems have strong needs for highly efficient AC-DC conversion that can be satisfied by using a buck-boost converter at the core of the power factor correction (PFC) stage. These converters can regulate the input voltage in a wide range with reduced efforts compared to other solutions. As a result, buck-boost converters could potentially improve the efficiency in applications requiring DC voltages lower than the peak grid voltage. This paper compares SEPIC, noninverting, and versatile buck-boost converters as PFC single-phase rectifiers. The converters are designed for an output voltage of 200 V and an rms input voltage of 220 V at 3.2 kW. The PFC uses an inner discrete-time predictive current control loop with an output voltage regulator based on a sensorless strategy. A PLECS thermal simulation is performed to obtain the power conversion efficiency results for the buck-boost converters considered. Thermal simulations show that the versatile buck-boost (VBB) converter, currently unexplored for this application, can provide higher power conversion efficiency than SEPIC and non-inverting buck-boost converters. Finally, a hardware-in-the-loop (HIL) real-time simulation for the VBB converter is performed using a PLECS RT Box 1 device. At the same time, the proposed controller is built and then flashed to a low-cost digital signal controller (DSC), which corresponds to the Texas Instruments LAUNCHXL-F28069M evaluation board. The HIL real-time results verify the correctness of the theoretical analysis and the effectiveness of the proposed architecture to operate with high power conversion efficiency and to regulate the DC output voltage without sensing it while the sinusoidal input current is perfectly in-phase with the grid voltage.

Keywords: AC-DC conversion; sensorless; predictive control; buck-boost converter; high efficiency conversion; SEPIC; versatile buck-boost

Citation: González-Castaño, C.; Restrepo, C.; Sanz, F.; Chub, A.; Giral, R. DC Voltage Sensorless Predictive Control of a High-Efficiency PFC Single-Phase Rectifier Based on the Versatile Buck-Boost Converter. *Sensors* **2021**, *21*, 5107. https://doi.org/10.3390/s21155107

Academic Editors: J. C. Hernandez, Carlos R. Baier and Pat Wheeler

Received: 29 June 2021
Accepted: 20 July 2021
Published: 28 July 2021

1. Introduction

Sensorless control methods are widely used in different fields, among which the regulation of electrical machines stands out [1–3]. An AC motor control requires determining the speed and flux position of the motor; however, the mechanical sensor has the disadvantages of high cost, large volume, and poor anti-interference ability caused by temperature and electromagnetic noise. Sensorless control provides a low-cost option, and motors' sensorless speed control has positioned itself as a relevant alternative from a research and industry perspective [4]. The control of different kinds of motors can be done either with or without sensors. Sensorless control techniques are increasingly used to reduce the overall cost and size of actuating devices in many applications despite requiring more complex control algorithms. The literature presents numerous examples of the sensorless

control of electrical machines applied along with estimation of different operating variables (current, voltage, speed, position). In [5], a field-oriented control of a permanent magnet machine drive with an estimation of the currents and voltages of the LC-filter connected in series is presented. In [6], a speed estimation of a linear ultrasonic motor is used to avoid speed/position sensors. In [7], a motion control of a linear resonant actuator with two degrees of freedom is implemented without a position sensor. Another sensorless strategy for speed control of a permanent magnet synchronous motor is explained in [8]. Speed and rotor resistance estimations for an induction motor drive can be found in [9]. Similarly, speed sensorless vector control of an induction motor drive system is implemented in [10]. Finally, a complete review of position and speed sensorless methods for controlling brushless direct current motor drives is included in [11].

Sensorless control methods have also been used in power electronics applications, especially in controlling power factor correction (PFC) single-phase rectifiers [12–15]. The conventional PFC converter employs a switching power converter between the diode bridge rectifier providing rectified sinusoidal voltage and a DC regulated voltage at its output [13]. In general, the control of a single-phase PFC rectifier requires at least three sensors [15]:

- An AC voltage sensor: is employed to detect the phase angle of the source voltage, which is then used to generate the unitary sine current reference for the power factor control;
- A DC voltage sensor: is used to regulate the converter output voltage and provide load overvoltage protection;
- A DC current sensor: is utilized to achieve closed-loop power factor control, DC voltage regulation, and overcurrent protection to the load.

There are numerous issues associated with the use of many sensors in the control of PFC single-phase rectifiers, among which the following stand out:

- Increase of the complexity and cost of the control circuit that is a problem for applications with very stringent cost and space requirements.
- Reduction of the power converter reliability.
- Increase in noise coupling and grounding issues of mixed-signal printed circuit board (PCB) from the connection between the power converter and the controller.

Based on the above mentioned considerations, a reduction in the required number of sensors is highly desired in this application. In addition, sensing all the variables in either the input or the output side of the converter stage eliminates the need for galvanically isolated sensors in the control system and reduces the noise coupling between the power converter and the controller. From the three standard sensors of a conventional PFC rectifier, eliminating the DC voltage sensor is the most useful from the viewpoints of cost and reliability [13]. High reliability is desired in commercial single-phase PFC rectifiers, along with High power density and High efficiency (H3) [15]. On the one hand, a high power density is achieved with a high switching frequency that depends on the advance of power electronic components and materials (such as SiC or GaN), packaging techniques, thermal management techniques, and others [16]. On the other hand, the power conversion efficiency depends on the specific converter topology and the operating conditions. According to the literature studies, the primary breakdown of total losses in a power converter is the switching and conduction losses of the transistors and the inductor losses. Other kinds of power losses such as capacitance losses, gate drive losses, printed circuit board layout losses, EMI filter losses, and auxiliary power and controller energy consumption are negligible concerning those mentioned above [17–22].

In this paper, a new single-phase PFC rectifier based on the versatile buck-boost converter is proposed. This converter has comparative advantages such as high efficiency, wide bandwidth, smooth transition between buck and boost modes, and the possibility of controlling either input or output voltages or currents that have been addressed in previous works [23–26]. These relevant advantages tested in DC-DC applications, and

especially the high-efficiency property, can be extended to AC-DC applications, which is the primary goal of this article. Furthermore, this paper proposes a fair comparison with two other well-known classical buck-boost converters: the SEPIC [27–30] and the noninverting buck-boost converter, refs. [31,32] to demonstrate that the proposed versatile converter has a superior efficiency performance in the PFC applications.

Therefore, the main contributions of this paper can be summarized as follows:

- A novel PFC single-phase rectifier based on the VBB converter is presented. Its many advantages tested in DC-DC applications are now meant to be proved in an AC-DC PFC application.
- A high-reliability is obtained by reducing the number of sensors, as critical components in reliability of the converter [33]. This reliability improvement does not compromise the control performance [34]. The ideal voltage conversion ratio of the proposed rectifier converter is used to estimate the DC output voltage. In this way, the controller senses only input variables (DC current and AC voltage), which reduce the noise coupling between the converter input and output terminals.
- A high-efficiency converter topology operating as PFC single-phase rectifier is achieved. Its power conversion efficiency is compared with other classical PFC rectifiers as the SEPIC and the noninverting buck-boost converter.
- A converter topology with a wide bandwidth and, consequently, with fast control loops, is proposed. The design of two nested control loops corresponds to a predictive-based current controller (inner loop for the DC input current) and a proportional-integral (PI) voltage controller (outer loop for the DC output voltage). These controllers operate along with output voltage estimation and grid-synchronising phase-locked loop (PLL) running in a low-cost microcontroller. Each of the proposed controllers ensure fast-tracking of the control set-points, and low steady-state error under demanding tests that include changes in the output voltage reference and the resistive load.
- The theoretical predictions are validated with temporal and thermal simulations as well as with hardware-in-the-loop (HIL) real-time simulation, which has proven to be a handy tool in many applications [35–42].

The structure of this paper is as follows: in Section 2, the dynamic models of three buck-boost converters and the current control approach are presented. The methods used to calculate the losses are described in Section 3. The basic principles of the voltage sensorless control are explained in Section 4. Temporal and thermal simulation and HIL real-time simulation results are included in Section 5. Finally, the conclusions of this work are presented in Section 6.

2. Modeling of DC-DC Buck-Boost Converters

Buck-boost converters can be used in PFC single-phase rectifier applications if the output voltage to regulate is lower than the peak AC input voltage. In the following subsections, the dynamic models for the SEPIC, noninverting, and versatile buck-boost DC-DC converters are described to obtain the inductor current slopes. These slope equations are required for the current control design. In addition, information about the selected components and the main parameters of each converter is defined.

2.1. SEPIC Converter

Figure 1 shows the circuit topology of the SEPIC converter. The topology consists of two inductors, a capacitor, and two MOSFET switches. The averaged model of the SEPIC converter is as follows [43]:

$$\frac{di_g(t)}{dt} = \frac{-u_2(v_c + v_o) + V_g}{L_1} \tag{1}$$

$$\frac{di_L(t)}{dt} = \frac{u_1\, v_c - u_2\, v_o}{L_2} \tag{2}$$

$$\frac{dv_c(t)}{dt} = \frac{u_2\, i_g - u_1\, i_L}{C} \tag{3}$$

$$\frac{dv_{co}(t)}{dt} = \frac{u_2(i_g + i_L)}{C_o} - \frac{1}{R_o\, C_o} v_o \tag{4}$$

The complementary switches signals are u_1 and u_2, and it duty cycle is calculated as follows:

$$D = \frac{v_o}{v_g + v_o} \tag{5}$$

The inductors L_1 and L_2 are selected to obtain a ripple current of 2 A for $v_g = 200$ V and $v_o = 300$ V in boost mode (D > 0.5) according to the following expression and $L_s = L_1 = L_2$:

$$\Delta i_L = \frac{DV_g}{L_s f_s}. \tag{6}$$

Therefore, the selected value for both inductors L_1 and L_2 is 600 µH for a switching frequency of 100 kHz. The capacitor value is selected for a voltage ripple $\Delta v_c = 6$ V at the voltage operation point (v_g = 200 V and v_o = 300 V), with an output current load of 8 A, and following the design expression (7). Therefore, the value for the capacitor selected corresponds to C = 8 µF.

$$C = \frac{i_o D}{\Delta v_c f_s}. \tag{7}$$

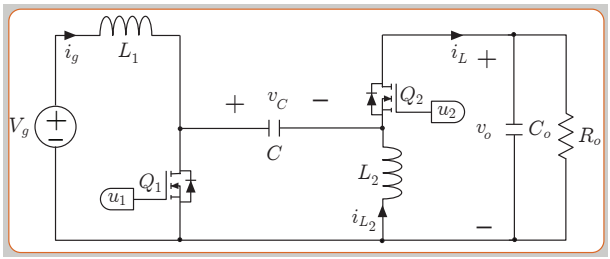


Figure 1. Topology of the SEPIC converter.

2.2. Noninverting Buck-Boost Converter (BB)

The noninverting buck-boost converter topology is shown in Figure 2, this power stage is composed of four switches and a single inductor L, and can operate in three modes [44]. For buck mode, switches Q_1 and Q_2 are turned in complementary manner, while Q_4 is turned off and Q_3 is turned on. For boost mode, switches Q_3 and Q_4 are turned on alternatively, while Q_1 is turned on and Q_2 is turned off. For buck-boost mode, the four switchers are operated as two high frequency interleaved half bridges. The mathematical model of the noninverting buck-boost converter is:

$$\frac{di_g(t)}{dt} = \frac{V_g\, u_{1H} - (1 - u_{2L})v_o}{L} \tag{8}$$

$$\frac{dv_o(t)}{dt} = \frac{i_g(1 - u_{2L})}{C_o} - \frac{v_o}{R_o C_o} \tag{9}$$

Table 1 presents the expressions for the peak-to-peak ripple signals of the noninverting buck-boost converter. T is the switching period, and D_1 and D_2 are the steady-state duty cycles in boost mode and buck mode, respectively. The maximum inductor current of the noninverting buck-boost is:

$$i_{gmax} = \begin{cases} \frac{P}{V_g} + \frac{V_g(V_o - Vg)}{V_o}\frac{T}{2L} & \text{for boost mode} \\ \frac{P}{V_o} + \frac{V_o(V_g - Vo)}{V_g}\frac{T}{2L} & \text{for buck mode.} \end{cases} \quad (10)$$

where P is the rated power of the converter. The single inductor is selected with a power rating of 3.2 kW, and a ripple current of 2 A at an input voltage $v_g = 200$ V and an output voltage $v_o = 300$ V, taking into account Equation (10) and the current ripple of Table 1. With an input voltage range V_g from 0 V to 400 V, and an output voltage range V_o from 0 V to 400 V. The selected value for the inductor is L = 330.75 µH with a switching frequency of 100 kHz.

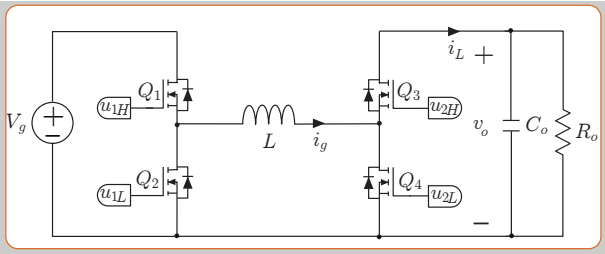


Figure 2. Topology of the noninverting buck–boost converter.

Table 1. Peak-to-peak ripple amplitudes for BB and VBB.

BB Converter	**Buck Mode**	**Boost Mode**
Δi_g	$\frac{(V_g - V_o)V_o T}{V_g L}$	$\frac{V_g(V_o - V_g)T}{V_o L}$
VBB Converter	**Buck Mode**	**Boost Mode**
Δi_L	$\frac{V_o T(V_g - V_o)L}{V_g(L^2 - M^2)}$	$\frac{V_g T(V_o - V_g)M}{V_o(L^2 - M^2)}$
Δi_g	$\frac{V_o T(V_g - V_o)M}{V_g(L^2 - M^2)}$	$\frac{V_g T(V_o - V_g)L}{V_o(L^2 - M^2)}$
Δv_c	$\frac{D_2 I_L}{C} T(D_2 - 1)$	$\frac{D_1 I_L}{C} T$

2.3. Versatile Buck-Boost Converter (VBB)

The buck-boost converter of Figure 3 has two half bridge MOSFETs and an $R_d C_d$ damping network connected in parallel with the intermediate capacitor C. The pair of coupled inductors has an unitary ideal turns ratio N_2/N_1, a coupling coefficient $k = 0.5$, a mutual inductance M =135 µH, and equal values for the primary (L_1) and secondary (L_2) self-inductances, being $L = L_1 = L_2 = 270$ µH. In this analysis, the use of the state-space averaging (SSA) method to model the converter leads to the following set of differential equations [45]:

$$\frac{di_g(t)}{dt} = \frac{L(V_g - v_c(1 - u_{1L})) - M(v_o - v_c\, u_{2H})}{L^2 - M^2} \quad (11)$$

$$\frac{di_L(t)}{dt} = \frac{M(V_g - v_c(1 - u_{1L})) - L(v_o - v_c\, u_{2H})}{L^2 - M^2} \quad (12)$$

$$\frac{dv_c(t)}{dt} = \frac{1}{C}\left(-i_L\, u_{2H} + i_g(-u_{1L} + 1) - \frac{1}{R_d}(v_c - v_{cd})\right) \quad (13)$$

$$\frac{dv_{cd}(t)}{dt} = \frac{v_c - v_{cd}}{C_d\, R_d} \quad (14)$$

$$\frac{dv_o(t)}{dt} = \frac{i_L}{C_o} - \frac{v_o}{R_o\, C_o} \quad (15)$$

The converter introduced in [46] for high-voltage applications has an input voltage V_g range of 200–400 V, and an output voltage range V_o from 0 V to 400 V. Experimental efficiencies reported in [46] demonstrate high values over 95% in all the operation range, with a maximum value of 98% when the input and output voltages of the converter are near. Table 1 presents the current and voltage ripple for the VBB converter. The selected parameters are listed in Table 2. The values of the mutual inductor and the self-inductance were selected based on Table 1 to obtain a current ripple $\Delta i_g = 2$ A at a switching frequency of 100 kHz for boost mode ($V_g = 200$ V and $V_o = 300$ V), which represents the most critical mode. The method to select the value for the components C_d, C and R_d is presented in [46]. The selection is a tradeoff between the capacitor size and ensures adequate and robust damping of the internal dynamics; the expression corresponds to:

$$R_d \approx 0.65\sqrt{\frac{M}{C}},\ C_d \geq 8C. \tag{16}$$

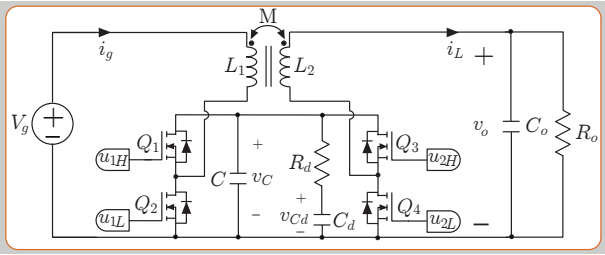


Figure 3. Topology of the buck–boost versatile converter, VBB.

Table 2. Selected components and parameters of the versatile buck-boost converter.

Parameter	Value or Type
Input voltage V_g	0–400 V
Output voltage V_o	100–400 V
Rated Power	3.2 kW
Switching frequency f_s	100 kHz
Output capacitor C_o	28 µF
Damping capacitor C_d	20 µF
Intermediate capacitor C	1.32 µF
Coupled inductor	$M = 135$ µH and $L = 270$ µH
Damping resistance R_d	5 Ω

3. Power Losses Methods

3.1. Electro-Thermal Model

The electro-thermal model is realized in PLECS, using the heat sink components for the power device SCT2450KEC employed for the switches of the buck-boost converters. This device is characterized by the maximum drain–source voltage equal to 1200 V and a permissible drain current equal to 10 A. The conduction, turn-on and turn-off switching losses are obtained from its datasheet, these were defined as simulation parameters, as shown in Figure 4. These relations are also linearly interpolated by the software. The software also enables implementing the dependence of switching energy losses. Separately, the energy values of the ON and OFF losses are entered, both for the MOSFET with diode model [47]. In addition, the thermal tool supports the quick entry of the MOSFET transient thermal impedance from the datasheet characteristics. The parameters of the MOSFET transient thermal impedance are selected from the datasheet for the power device SCT2450KEC.

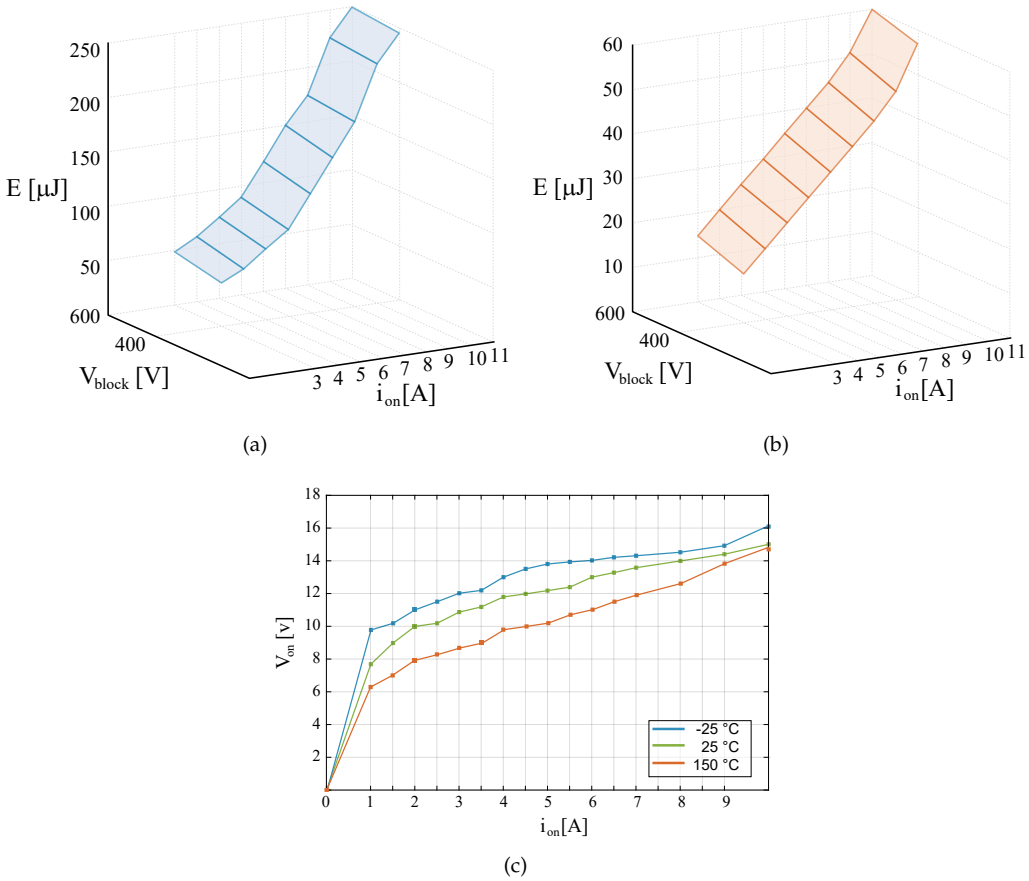


Figure 4. Switching and conduction losses of SCT2450KEC parameters of PLECS: (**a**) Turn on losses, (**b**) Turn off losses (**c**) Conduction losses.

3.2. Power Inductor Losses Calculation

The inductor power loss information is often provided by the core manufacturer. The power loss of the inductor estimation is calculated from the inductor core (P_{core}) and winding loss (P_{dcr}), using the expression:

$$P_{Lossinductor} = P_{core} + P_{dcr}. \tag{17}$$

P_{core} is generated by the changing magnetic flux field within a material. A general form of the core loss formula for core loss density (PL) is [48]:

$$PL = aB_{pk}^{b} f_s^{c}. \tag{18}$$

where a, b, c are constants determined from curve fitting, and B_{pk} is defined as half of the AC flux swing:

$$B_{pk} = \frac{B_{ACmx} - B_{ACmin}}{2}. \tag{19}$$

The units are: mW/cm^3 for PL; Tesla (T) for B_{pk}^{b} and kHz for f_s. B_{pk} can be obtained from the DC magnetization curve as follows:

$$B(H) = \left| \frac{a + bH + cH^2}{1 + dH + eH} \right|^{x}. \tag{20}$$

where a, b, c, d, e, and x are the constant parameters to fit the measured B-H curve data. H is the magnetic field intensity and is given by

$$H_{ACmax} = \frac{Ni_{Lmax}}{l_e} \tag{21}$$

$$H_{ACmin} = \frac{Ni_{Lmin}}{l_e} \tag{22}$$

where i_{Lmax} and i_{Lmin} are the maximum and minimum current points, respectively. N is the winding number of turns and l_e is the magnetic path length. The DC resistance of a conductor is given by [49]:

$$R_{wDC} = \rho_w \frac{l_w}{A_w} \tag{23}$$

where l_w is the length of the conductor, its uniform cross-sectional area is A_w, and its resistivity ρ_w. Therefore, the wire loss caused by DC resistance is:

$$P_{dcr} = I_{rms}^2 R_{wDC} \tag{24}$$

I_{rms} being the rms value of the ripple current applied to the inductor.

4. Voltage-Sensorless Predictive Controller for a Single Phase AC-DC Converter

The control in the AC-DC stage guarantees a high power factor, synchronizing the input current waveform with the electrical grid voltage. The signals needed to control the AC-DC stage include the line voltage V_{ac}, the input voltage v_g, the input current i_g and the output voltage v_o. The control scheme in Figure 5 is proposed, where the voltage-control loop is implemented to regulate the output voltage v_o and the current-control loop to regulate the input current i_g amplitude and phase. A phase locked loop (PLL) is used to synchronize with the grid, and a normalized rectified sinusoidal reference obtained from the PLL is multiplied by the desired peak current value (i_{peak}) given by the voltage controller, to obtain the input current loop reference ($i_{ref}[n]$). Figure 5 reveals the proposed DC voltage sensorless control, which is based on computing the input voltage V_g directly from the voltage line V_{ac} by means of an absolute value function, obtaining the signal $v_{gest}[n]$. Furthermore, an online output voltage v_o estimation is used to close the voltage loop using the computed duty cycles. The output voltage estimator of the SEPIC converter is calculated as follows:

$$v_{oest}[n] = \frac{d[n]v_g[n]}{1 - d[n]}. \tag{25}$$

The following voltage output estimator is implemented for the BB and VBB converter:

$$v_{oest}[n] = \frac{d_2[n]v_g[n]}{1 - d_1[n]}. \tag{26}$$

Then, a proportional-integral digital control ($G_{vpi}(z)$) is used to obtain the reference peak current ($i_{peak}[n]$).

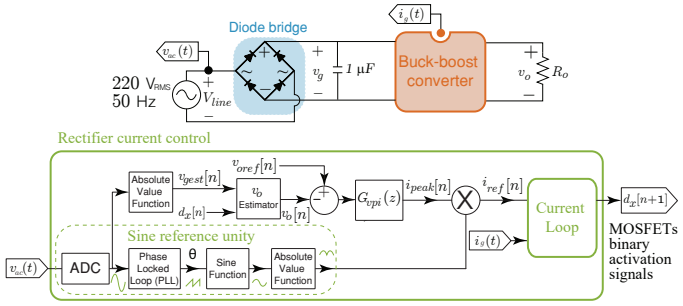


Figure 5. Block diagram of the buck-boost converter in an AC-DC application where its output voltage is regulated.

4.1. Proportional-Integral Voltage Controller

The proportional-integral controller regulates the output voltage of the DC bus to the reference value V_{oref}. The controller output is given by:

$$i_{peak}[n] = i_{Lp}[n] + i_{Li}[n]. \tag{27}$$

where i_{Lp} and i_{Li} are the proportional and integral components, respectively. Their values are related in the following way:

$$\begin{aligned} i_{Lp}[n] &= K_{pv}\ \ e_v[n], \\ i_{Li}[n] &= K_{iv}\ T_{samp}\ e_v[n] + i_{Li}[n-1]. \end{aligned} \tag{28}$$

where $K_{pv} = 2\pi\, f_c C_o$, $K_{iv} = K_{pv}/T_i$, $e_v[n]$ is the voltage error and T_{samp} is the sampling period ($1/f_{samp}$). Hence, the bandwidth of the voltage loop depends on the proportional coefficient (K_{pv}). The value of the crossover frequency (CF) for the voltage loop (f_c) should be lower than the CF for the current loop. The location of the PI zero should be lower than f_c ($1/(2\pi T_i) < f_c$) [50]. The zero corner frequency for the current loop should be much smaller than f_s being 10 times below f_s [51,52]. Therefore, the CF corresponds to 10 kHz for the current loop and 2500 Hz for the voltage loop. Finally, the location for the PI zero of the voltage loop is 250 Hz.

4.2. Predictive Digital Current Programmed Control

The predictive digital current programmed control (PDCC) has been presented in [53,54]. The aim of this strategy is to compute the duty cycle d_x in the $n+1$ time-sampling interval. The analysis for the buck-boost converters presented for the small model allows to find the converter's current output slope $\frac{di_g}{dt}$ for the SEPIC (see Figure 1), the noninverting buck-boost (see Figure 2) and versatile buck-boost (see Figure 3) converters. Current i_g has a periodic triangular ripple waveform with a rising slope m_1 and a falling slope $-m_2$. Table 3 presents the converter current i_g ripple waveform slopes based on the equation for $\frac{di_g}{dt}$ from (1), (8) and (12) for the boost and buck modes.

Table 3. Slopes of i_g current waveform.

SEPIC	$\boldsymbol{m_1}$	$\boldsymbol{-m_2}$
converter	$\frac{V_g}{L_1}$	$\frac{-v_c - v_o + V_g}{L_1}$
BB converter	$\boldsymbol{m_1}$	$\boldsymbol{-m_2}$
Buck	$\frac{V_g - v_o}{L}$	$-\frac{v_o}{L}$
Boost	$\frac{V_g}{L}$	$\frac{V_g - v_o}{L}$
VBB converter	$\boldsymbol{m_1}$	$\boldsymbol{-m_2}$
Buck	$\frac{L(V_g - v_c) - M(v_o - v_c)}{L^2 - M^2}$	$\frac{L(V_g - v_c) - Mv_o}{L^2 - M^2}$
Boost	$\frac{LV_g - M(v_o - v_c)}{L^2 - M^2}$	$\frac{L(V_g - v_c) - M(v_o - v_c)}{L^2 - M^2}$

The Euler approximation leads to the following discrete-time output current expression, assuming the converter's current output slope $\frac{di_g}{dt} \approx \frac{i_g[n+1] - i_g[n]}{T}$ from the averaged model.

$$i_g[n+1] = i_g[n] + T(m_1 + m_2)d_x[n] - m_2 T. \tag{29}$$

Hence, the resulting expression of the duty cycle is:

$$d_x[n+1] = -d_x[n] + \frac{1}{(m_1+m_2)T} e_i[n] + 2\frac{m_2}{m_1+m_2}, \tag{30}$$

where x corresponds to the operating mode of the bidirectional BB and VBB converters (x = 1 for boost mode, x = 2 for buck mode). In the case of the SEPIC converter $d_x[n] = d[n]$. Using the expressions of the output current slopes, m_1 and $-m_2$, in Table 3 at (30), the expression of $m_1 + m_2$ for the SEPIC converter is

$$m_1 + m_2 = \frac{v_c + v_o}{L_1}. \tag{31}$$

The corresponding sum of slopes for the BB converter can be expressed as:

$$m_1 + m_2 = \begin{cases} \frac{v_o}{L} & \text{for boost mode} \\ \frac{V_g}{L} & \text{for buck mode.} \end{cases} \tag{32}$$

Furthermore, for the VBB, it can be seen that

$$m_1 + m_2 = \begin{cases} \frac{L\, v_c}{L^2 - M^2} & \text{for boost mode} \\ \frac{M\, v_c}{L^2 - M^2} & \text{for buck mode.} \end{cases} \tag{33}$$

The expression $m_2/(m_1 + m_2)$ for the SEPIC converter is:

$$\frac{m_2}{m_1+m_2} = \frac{v_c + v_o - V_g}{v_c + v_o}. \tag{34}$$

For the VBB it is given by:

$$\frac{m_2}{m_1+m_2} = \begin{cases} \frac{-L(V_g - v_c) + M(v_o - v_c)}{L\, v_c} & \text{for boost mode} \\ \frac{-L(V_g - v_c) + Mv_o}{M\, v_c} & \text{for buck mode.} \end{cases} \tag{35}$$

Furthermore, for the BB converter can be expressed as:

$$\frac{m_2}{m_1+m_2} = \begin{cases} \frac{V_g + v_o}{V_g} & \text{for boost mode} \\ \frac{v_o}{V_g} & \text{for buck mode.} \end{cases} \tag{36}$$

The Equations (33) and (35) for the BBV converter can be simplified by substituting the voltage of the intermediate capacitor v_c by V_g in buck mode operation and by V_o in boost mode operation. Furthermore, for the SEPIC converter by substituting v_c by V_g in (31) and (34).

5. Simulation and Real-Time HIL Results

In this section, power conversion efficiency results of the VBB, BB and SEPIC converters are compared. Once the high efficiency of the VBB converter is verified, the experimental, simulation and HIL (Hardware in the loop) tests are presented to validate the proposed DC voltage sensorless control using the VBB converter.

5.1. Efficiency Results

In this section, efficiency results of the buck-boost converter topologies for AC-DC application are presented. The design of the buck-boost converters are realized under the same characteristic of switching frequency and peak to peak current ripple presented in Section 2. The thermal model to obtain the conduction and switches losses for the MOSFET was implemented in PLECS, this simulation is carried out using the heat sink components for the power device SCT2450KEC employed for the DC-DC converters. The power inductor losses estimation for the inductors takes into account the inductor design presented in [46], where the core used is the 77908 from Magnetics, which has a Kool Mμ material with a core relative permeability coefficient of 26, and the windings wire size is 18 AWG. The generalized block diagram of the buck-boost converters in AC–DC applications for current regulation is shown in Figure 6. In this case, to achieve a high power factor, a normalized rectified sinusoidal reference is synchronized to the line input voltage (V_{line}) and multiplied by the desired peak current value (i_{peak}) to obtain the current loop reference ($i_{ref}[n]$). The PDCC loop control described in Section 2 is used to track the rectified sinusoidal current reference. Figure 7a shows that the converter output voltage (V_o) is fixed to 200 V, which is lower than the peak value of the input voltage (v_g) that corresponds to the rectified voltage V_{line}, ensuring operation in both boost and buck modes at each semi–period of the grid. Figure 7b shows the results for the current control where the waveforms are i_g and its RMS current value, this last is about 4 A. The controlled current ripple has a peak-to-peak amplitude of about 2 A for an input voltage of 300 V and an output voltage of 200 V. The corresponding peak current reference is $i_{peak} = 6$ A. The simulated results show a good current reference tracking under changes of the operation mode (boost or buck) and peak current reference (i_{peak}), validating in this way the good control performance. The efficiencies of the converters are calculated taking into account the switches losses, the inductors core losses, and the damping resistor losses R_d for the versatile buck-boost converter, as follows:

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \tag{37}$$

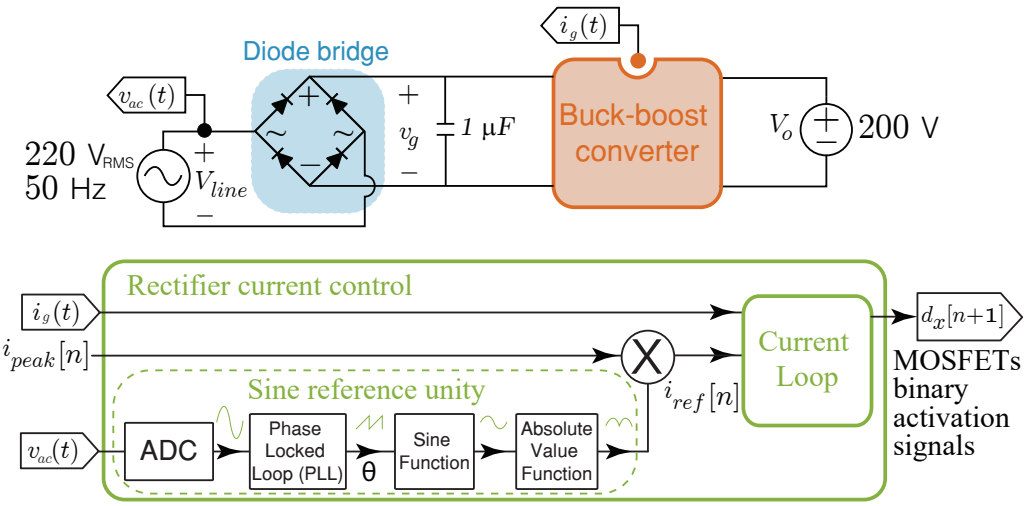


Figure 6. Block diagram of the buck-boost converter in an AC-DC application where its input current is regulated.

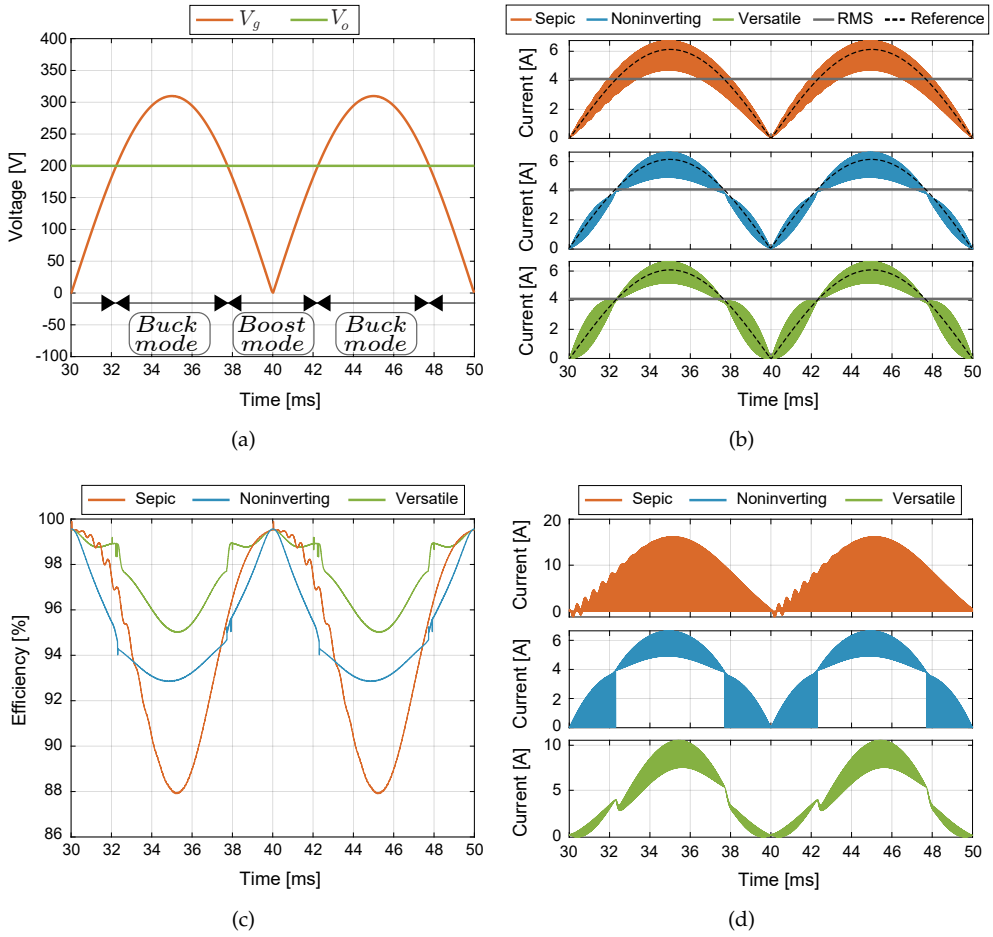


Figure 7. PLECS thermal simulation: (**a**) input and output voltage waveforms, (**b**) current control waveforms, (**c**) AC-DC conversion efficiency results over one period of the grid signal (20 ms), (**d**) output current converter.

Being P_{loss} the power losses for the inductor, switches and resistor elements of the converters. P_{in} is the input power, whose rms value is 900 W. Figure 7c shows the efficiency results in the time domain over one period of the grid signal (20 ms), where the efficiency changes for different operating points, while the operation modes can be determined by the input and output voltages seen in Figure 7a. For all converters, the highest efficiency is reached when the input current and voltage pass through the zero crossings, that is, when the converters do not process power. The SEPIC and versatile buck-boost converters show a similar efficiency behaviour when the output voltage is much higher than the input voltage for boost mode. The VBB converter has a better power conversion efficiency, higher than 95% for all the operation range while the SEPIC converter has a minimum efficiency near to 88% and the noninverting BB above 93%. In addition, the output currents i_o of all buck-boost converters are shown in Figure 7d. These results show that the versatile buck-boost converter has the lowest output current ripple. This advantage is very relevant since it reduces the output filter requirements in the converter output for many applications.

5.2. Experimental Results

The HIL test has been implemented into two subsystems: the plant and the controller. The plant subsystem corresponding to the AC-DC stages is deployed on the PLECS RT Box 1 for Hardware-in-the-loop (HIL) testing. The controller subsystem has been flashed to a low-cost digital signal controller (DSC), which corresponds to the Texas Instruments LAUNCHXL-F28069M as can be seen in Figure 8. The controller implements a double loop

control algorithm to regulate the AC-DC converter's output voltage. The sampling time of the plant is 2 µs.

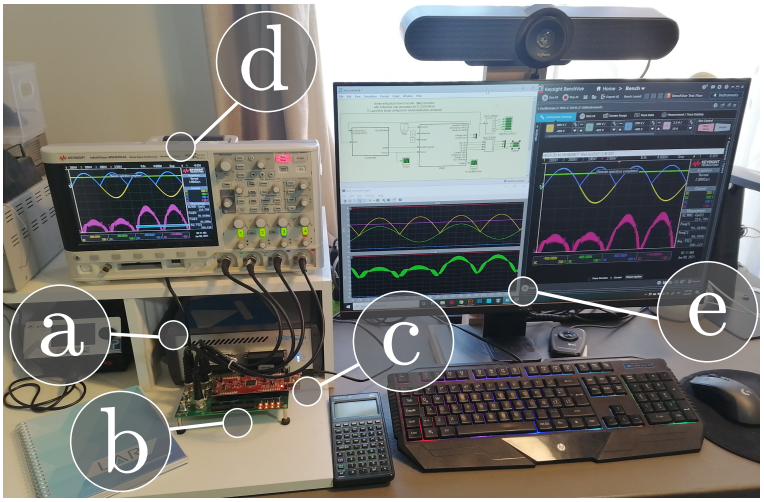


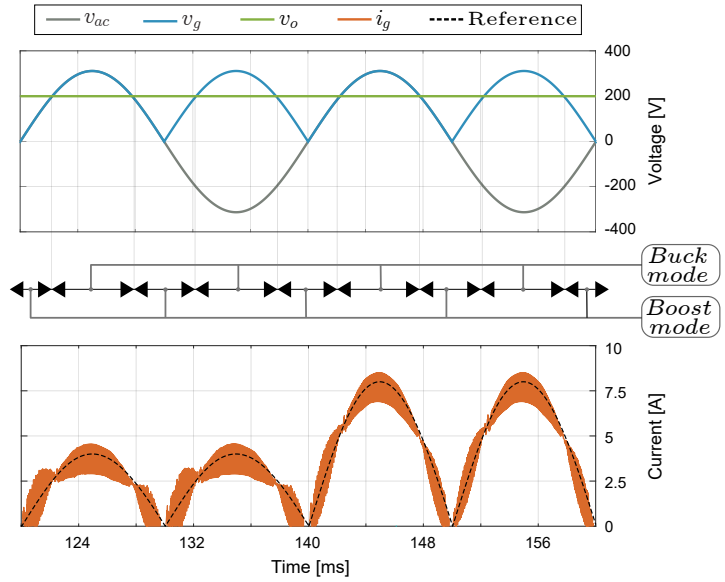
Figure 8. Hardware in-the-loop experimental setup: (**a**) PLECS RT-box , (**b**) RT Box LaunchPad Interface, (**c**) Texas Instruments LAUNCHXL-F28069M, (**d**) oscilloscope, (**e**) computer to program the RT Box and the microcontroller, perform the simulations, and communicate the data with the oscilloscope.

5.3. Inner Loop Current Control Results

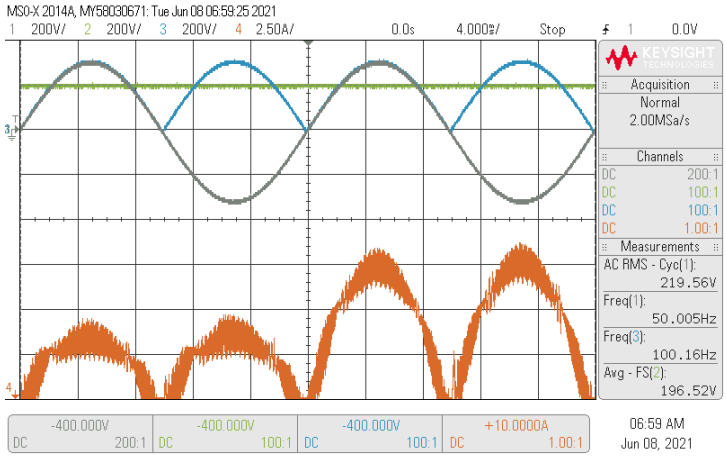
A dynamic response test of the current control has been performed to evaluate the inner loop based on a predictive digital strategy. Figure 9 shows the experimental results for an input rms voltage of 220 V and an input line voltage frequency (f_i) of 50 Hz. The signals sampled for the control are v_g, v_o, v_{ac} and i_L. The sampling time is 40 µs. The control scheme for the inner loop is shown in Figure 6. Experimental results in Figure 9 show that the input current (i_g) of the VBB converter is in phase with the input voltage (v_g) while the desired peak current (i_{peak}) changes from 4 A to 8 A. The converter output voltage (v_o) is fixed to 200 V, which is lower than the peak value of the input voltage (v_g) that corresponds to the rectified voltage v_{ac}, ensuring operation in both boost and buck modes in each grid half-period. The experimental results show good current reference tracking under changes of the operation mode (boost or buck) and peak current reference (i_{peak}). The inner loop control depends on the inductor parameter of the model, this coupled inductor value depends on the temperature, DC current and switching frequency [55,56]. Therefore, a sensitivity analysis for the current control of each converter parameter operating in boost mode ($V_g = 200$ V and $V_o = 400$ V) and buck mode ($V_g = 400$ V and $V_o = 200$ V) both with a i_{gref} =6 A, is shown in Figure 10. To reproduce the parameter mismatch, parameters in the model (L, M, C, C_d and R_d) are varied for ±20%, in order to investigate the individual effect of each parameter in the performance of the $MAPE(i_g)$, which is defined as

$$\text{MAPE}\ (i_{ref}) = \frac{100\%}{n} \cdot \sum_{t=1}^{n} \left| \frac{i_{ref} - i_g}{i_{ref}} \right|, \tag{38}$$

where n is the number of steps of the simulation. This measure corresponds to the mean absolute percentage error between the input current i_g and its respective reference i_{ref}. Therefore, from the obtained results of Figure 10, it can be stated that L and M have a higher sensibility in the input current tracking error for boost mode when the mutual and self inductance tolerance have values around ±20%. However, even in the worst case the $MAPE(i_g)$ has a small variation of 1.8% in boost mode. On the other hand, it is evident that the detuning of the other variables of the converter (C, C_d and R_d) do not have a relevant effect on the $MAPE(i_g)$.



(a)



(b)

Figure 9. Simulated (**a**) and experimental (**b**) dynamic behavior of the predictive digital current input control when the reference i_{ref} changes from 4 A to 8 A with a fixed output voltage $V_o = 200$ V. CH1: v_{ac} (200 V/div), CH2: v_o (200 V/div), CH3: v_g (200 V/div), CH4: i_g (2.5 A/div) and a time base of 4 ms.

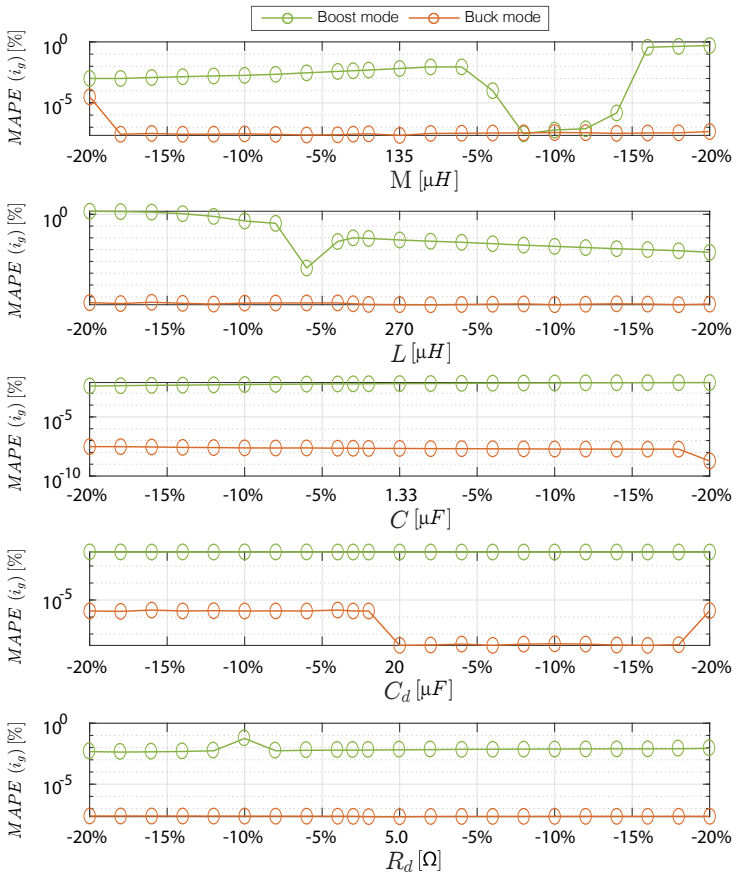
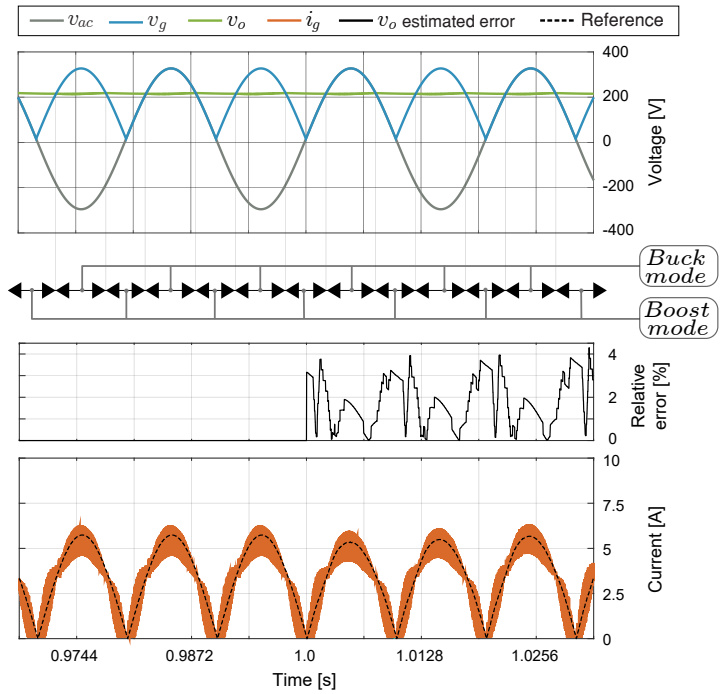


Figure 10. Sensitivity analysis of the predictive inner current loop under converter parameters variations (*M*,*L*,*C*, C_d and R_d) operating in boost mode ($V_g = 200$ V and $V_o = 400$ V) and buck mode ($V_g = 400$ V and $V_o = 200$ V) both with a $i_{ref} = 6$ A.

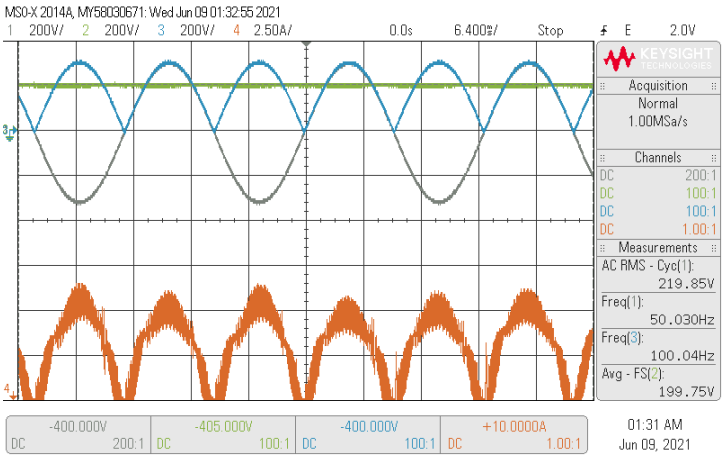
5.4. DC Voltage Sensorless Control Results

For the results shown in Figures 11, a 50 Ω load resistor has been used as is shown in Figure 5, the output capacitor is $C_o = 3$ mF and the crossover frequency of the voltage loop is 1.5 kHz. In Figure 11, the experimental results are presented for double loop control operating with sensor and sensorless modes. Until the first second the control strategy is in sensor mode, meaning that all the control variables are sensed. After the first second, the control strategy switches from sensor to sensorless mode, meaning that both v_g and v_o are estimated. The control strategy has a good output voltage estimation during the operation into the sensorless mode with a small relative error, as shown in Figure 11a. In sensorless mode, the only sensed variables are grid voltage V_{ac} and current i_g. Therefore, the proposed sensorless strategy allows reducing a critical sensor as the output voltage case reduces the converter costs, increases the power density, and increases the converter reliability without increasing the computational cost in the control strategy. Figure 11 shows a good performance of the control strategy in both sensor and sensorless mode, which validates the excellent estimation performed by the control algorithm. As can be observed at Figure 11, the output voltage is well regulated at 200 V for the DC voltage sensorless control, with a current input peak of 6 A. Figure 12 show experimental and simulated results for variations of the output voltage reference from 220 V to 200 V with a 100 Ω resistor load. The input current decreases following the changes of the output voltage, demonstrating the good performance of the DC voltage sensorless control for large variations of the voltage reference. A step variation in the load is shown in Figure 13, where the load current changes from 2 A to 4 A, and then from 4 A to 2 A. The voltage controller regulates v_o at the desired value $v_{oref} = 200$ V when the resisistive load changes between 100 Ω and 50 Ω.

The figures also demonstrate a good agreement between the experimental and simulation results, which validates the adequate operation of the proposed control method.

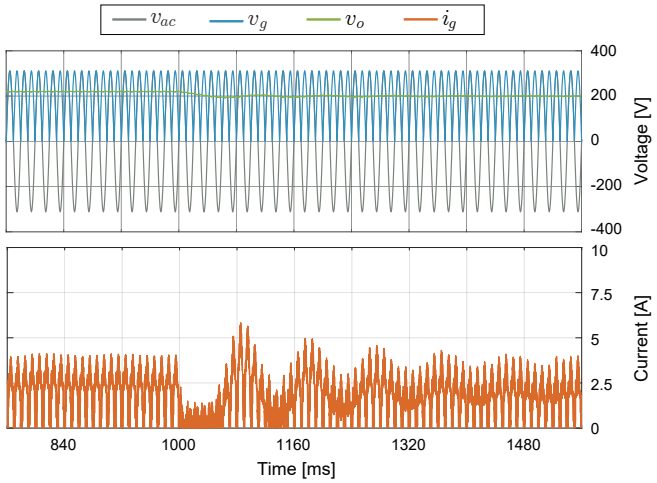


(a)

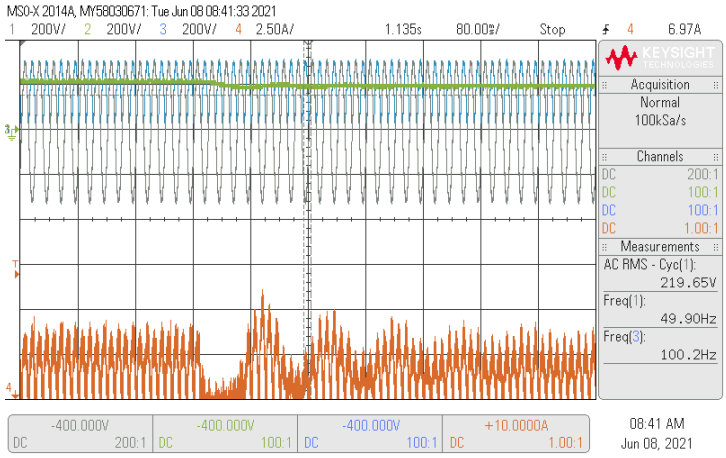


(b)

Figure 11. Simulated (**a**) and experimental (**b**) response of the double loop when the voltage sensorless control is switched on at 1 s with $v_{oref} = 200$ V. CH1: v_{ac} (200 V/div), CH2: v_o (200 V/div), CH3: v_g (200 V/div), CH4: i_g (2.5 A/div) and a time base of 6.4 ms.

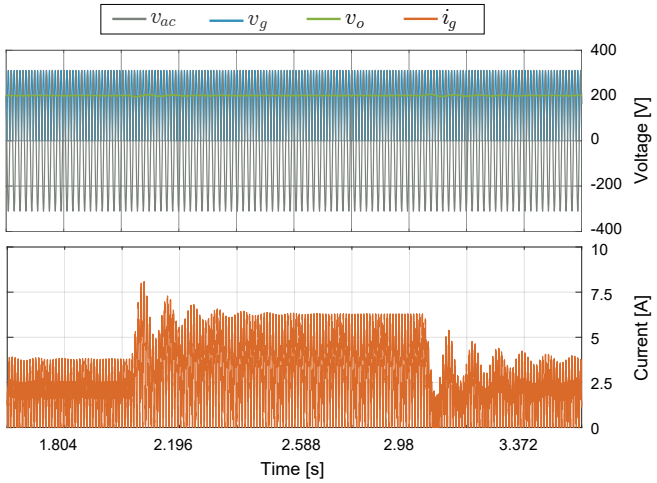


(a)



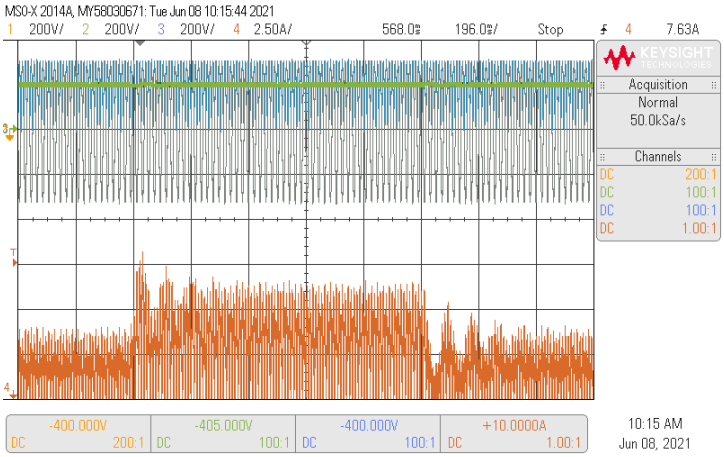
(b)

Figure 12. Simulated (**a**) and experimental (**b**) dynamic behavior of the double loop when the reference v_{oref} changes with steps of 20 V from 220 V to 200 V. CH1: v_{ac} (200 V/div), CH2: v_o (200 V/div), CH3: v_g (200 V/div), CH4: i_g (2.5 A/div) and a time base of 80 ms.



(a)

Figure 13. *Cont.*



(b)

Figure 13. Simulated (**a**) and experimental (**b**) dynamic behavior of the double loop for a 50% step change in the load. CH1: v_{ac} (200 V/div), CH2: v_o (200 V/div), CH3: v_g (200 V/div), CH4: i_g (2.5 A/div) and a time base of 196 ms.

6. Conclusions

This paper presents a DC voltage sensorless predictive control for the versatile buck-boost converter operating as PFC single-phase rectifier. The SEPIC, BB and VBB converters were compared with respect to power conversion efficiency. For a fair comparison, common power stage design parameters were considered for all buck-boost converters and the same discrete predictive current control was applied to them. A power inductor losses method was used to calculate the efficiency, and a PLECS thermal simulation has been developed to estimate the the MOSFET and inductor losses. Simulated results confirm the advantages of the proposed versatile buck-boost converter operating as PFC single-phase rectifier among which stands out high power conversion efficiency over a wide operation range. In addition, real-time HIL tests for the VBB converter have been performed using a PLEC RT BOX1 device. A double loop sensorless control to regulate the output voltage was implemented in a DSC Texas Instruments LAUNCHXL-F28069M. Temporal and thermal simulations and real-time HIL results verify the correctness of the proposed control for the versatile buck-boost converter operating in an AC-DC application.

Author Contributions: Conceptualization, R.G., C.R., F.S., A.C., and C.G.-C.; methodology, R.G., C.R., F.S., A.C., and C.G.-C.; software, C.R. and C.G.-C.; validation, C.R and C.G.-C.; formal analysis, R.G., F.S. and A.C; investigation, R.G., C.R., F.S., A.C., and C.G.-C.; resources, R.G., C.R., F.S., A.C., and C.G.-C.; data curation, R.G., C.R. and C.G.-C.; writing–original draft preparation, R.G., C.R. and C.G.-C.; writing–review and editing, R.G., C.R., F.S., A.C., and C.G.C.; visualization, R.G., C.R. and C.G.-C.; supervision, R.G., C.R. and F.S; project administration, A.C., R.G and C.R; funding acquisition, A.C., C.R. and F.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Chilean Government under Project CONICYT/FONDECYT 1191680, in part by the SERC Chile Project under Grant CONICYT/FONDAP 15110019, in part by the Spanish Agencia Estatal de Investigación and the Fondo Europeo de Desarrollo Regional (AEI/FEDER, UE) under Project DPI2016-80491-Rand DPI2017-84572-C2-1-R, in part by the Estonian Research Council under Grant PSG206, and in part by the Estonian Centre of Excellence in Zero Energy and Resource Efficient Smart Buildings and Districts, European Regional Development Fund, under Grant 2014-2020.4.01.15-0016 and MINCIENCIAS postdoc scholarship state 848-2019.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Xu, D.; Wang, B.; Zhang, G.; Wang, G.; Yu, Y. A review of sensorless control methods for AC motor drives. *CES Trans. Electr. Mach. Syst.* **2018**, *2*, 104–115. [CrossRef]
2. Yin, Z.; Gao, F.; Zhang, Y.; Du, C.; Li, G.; Sun, X. A review of nonlinear Kalman filter appling to sensorless control for AC motor drives. *CES Trans. Electr. Mach. Syst.* **2019**, *3*, 351–362. [CrossRef]
3. Wang, G.; Valla, M.; Solsona, J. Position Sensorless Permanent Magnet Synchronous Machine Drives—A Review. *IEEE Trans. Ind. Electron.* **2020**, *67*, 5830–5842. [CrossRef]
4. Li, Y.; Wu, H.; Xu, X.; Sun, X.; Zhao, J. Rotor position estimation approaches for sensorless control of permanent magnet traction motor in electric vehicles: A review. *World Electr. Veh. J.* **2021**, *12*, 9. [CrossRef]
5. Liang, C.M.; Lin, Y.J.; Chen, J.Y.; Chen, G.R.; Yang, S.C. Sensorless LC Filter Implementation for Permanent Magnet Machine Drive Using Observer-Based Voltage and Current Estimation. *Sensors* **2021**, *21*, 3596. [CrossRef]
6. Yan, Y.; Yang, M.; Yang, T.; Ye, S.; Jiang, W. Speed Sensorless Control of Linear Ultrasonic Motors Based on Stator Vibration Amplitude Compensation. *Sensors* **2020**, *20*, 6705. [CrossRef]
7. Kim, G.; Hirata, K. Motion Control of a Two-Degree-of-Freedom Linear Resonant Actuator without a Mechanical Spring. *Sensors* **2020**, *20*, 1954. [CrossRef] [PubMed]
8. Urbanski, K.; Janiszewski, D. Sensorless Control of the Permanent Magnet Synchronous Motor. *Sensors* **2019**, *19*, 3546. [CrossRef]
9. Gutierrez-Villalobos, J.M.; Rodriguez-Resendiz, J.; Rivas-Araiza, E.A.; Martínez-Hernández, M.A. Sensorless FOC Performance Improved with On-Line Speed and Rotor Resistance Estimator Based on an Artificial Neural Network for an Induction Motor Drive. *Sensors* **2015**, *15*, 15311–15325. [CrossRef] [PubMed]
10. Wang, S.Y.; Tseng, C.L.; Lin, S.C.; Chiu, C.J.; Chou, J.H. An Adaptive Supervisory Sliding Fuzzy Cerebellar Model Articulation Controller for Sensorless Vector-Controlled Induction Motor Drive Systems. *Sensors* **2015**, *15*, 7323–7348. [CrossRef] [PubMed]
11. Gamazo-Real, J.C.; Vázquez-Sánchez, E.; Gómez-Gil, J. Position and Speed Control of Brushless DC Motors Using Sensorless Techniques and Application Trends. *Sensors* **2010**, *10*, 6901–6947. [CrossRef]
12. López, F.; López-Martín, V.M.; Azcondo, F.J.; Corradini, L.; Pigazo, A. Current-Sensorless Power Factor Correction With Predictive Controllers. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 891–900. [CrossRef]
13. Ohnishi, T.; Hojo, M. DC voltage sensorless single-phase PFC converter. *IEEE Trans. Power Electron.* **2004**, *19*, 404–410. [CrossRef]
14. Yip, S.; Qiu, D.; Chung, H.S.H.; Hui, S. A novel voltage sensorless control technique for a bidirectional AC/DC converter. *IEEE Trans. Power Electron.* **2003**, *18*, 1346–1355. [CrossRef]
15. Qi, W.; Li, S.; Tan, S.C.; Hui, S.Y. Design Considerations for Voltage Sensorless Control of a PFC Single-Phase Rectifier Without Electrolytic Capacitors. *IEEE Trans. Ind. Electron.* **2020**, *67*, 1878–1889. [CrossRef]
16. Wang, Y.; de Haan, S.W.H.; Ferreira, J.A. Potential of Improving PWM Converter Power Density with Advanced Components. In Proceedings of the 2009 13th European Conference on Power Electronics and Applications, Barcelona, Spain, 8–10 September 2009; pp. 1–10.
17. Rodríguez, M.; Rodríguez, A.; Miaja, P.F.; Lamar, D.G.; Zúniga, J.S. An Insight into the Switching Process of Power MOSFETs: An Improved Analytical Losses Model. *IEEE Trans. Power Electron.* **2010**, *25*, 1626–1640. [CrossRef]
18. Hartmann, M.; Ertl, H.; Kolar, J.W. On the Tradeoff Between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers. *IEEE Trans. Power Electron.* **2012**, *27*, 3137–3149. [CrossRef]
19. Stupar, A.; Friedli, T.; Minibock, J.; Kolar, J.W. Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400-V DC Distribution Systems. *IEEE Trans. Power Electron.* **2012**, *27*, 1732–1744. [CrossRef]
20. Qi, W.; Li, S.; Yuan, H.; Tan, S.C.; Hui, S.Y. High-Power-Density Single-Phase Three-Level Flying-Capacitor Buck PFC Rectifier. *IEEE Trans. Power Electron.* **2019**, *34*, 10833–10844. [CrossRef]
21. Abdel-Rahman, S.; Stückler, F.; Siu, K. *PFC Boost Converter Design Guide*; Infineon Application Note; Infineon Technologies AG: Munich, Germany, 2016; Volume 2.
22. Baek, J.; Park, M.H.; Kim, T.; Youn, H.S. Modified Power Factor Correction (PFC) Control and Printed Circuit Board (PCB) Design for High-Efficiency and High-Power Density On-Board Charger. *Energies* **2021**, *14*, 605. [CrossRef]
23. Restrepo, C.; Calvente, J.; Cid-Pastor, A.; Aroudi, A.E.; Giral, R. A Noninverting Buck–Boost DC–DC Switching Converter with High Efficiency and Wide Bandwidth. *IEEE Trans. Power Electron.* **2011**, *26*, 2490–2503. [CrossRef]
24. Restrepo, C.; Calvente, J.; Romero, A.; Vidal-Idiarte, E.; Giral, R. Current-Mode Control of a Coupled-Inductor Buck–Boost DC–DC Switching Converter. *IEEE Trans. Power Electron.* **2012**, *27*, 2536–2549. [CrossRef]
25. Restrepo, C.; Konjedic, T.; Calvente, J.; Milanovic, M.; Giral, R. Fast Transitions Between Current Control Loops of the Coupled-Inductor Buck–Boost DC–DC Switching Converter. *IEEE Trans. Power Electron.* **2013**, *28*, 3648–3652. [CrossRef]
26. Restrepo, C.; Konjedic, T.; Member, S.; Calvente, J.; Giral, R.; Member, S. Hysteretic transition method for avoiding the dead-zone effect and subharmonics in a non-inverting buck-boost converter. *IEEE Trans. Power Electron.* **2014**, *30*, 3418–3430. [CrossRef]
27. Ordono, A.; Unamuno, E.; Barrena, J.A.; Paniagua, J. Interlinking converters and their contribution to primary regulation: A review. *Int. J. Electr. Power Energy Syst.* **2019**, *111*, 44–57. [CrossRef]

28. Meenadevi, R.; Premalatha, L. A novel bridgeless SEPIC converter for power factor correction. *Energy Procedia* **2017**, *117*, 991–998. [CrossRef]
29. Jassim, B.M. SEPIC AC-DC Converter for Aircraft Application. In Proceedings of the MELECON 2014–2014 17th IEEE Mediterranean Electrotechnical Conference, Beirut, Lebanon, 13–16 April 2014; pp. 12–16
30. Rosa, A.H.; De Souza, T.M.; Morais, L.M.; Seleme, S.I. Adaptive and nonlinear control techniques applied to sepic converter in dc-dc, pfc, ccm and dcm modes using hil simulation. *Energies* **2018**, *11*, 602. [CrossRef]
31. Yu, S.Y.; Chen, H.C. A comparison study of boost and Buck-boost power factor corrector for ultra-wide input voltage range applications. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014; pp. 2719–2726.
32. Chandran, C.; Chandran, L.R. Two switch buck boost converter for power factor correction. In Proceedings of the 2015 International Conference on Technological Advancements in Power and Energy (TAP Energy), Kollam, India, 24–26 June 2015; pp. 454–459.
33. Bae, S.; Kim, M. Effect of Sensors on the Reliability and Control Performance of Power Circuits in the Web of Things (WoT). *Sensors* **2016**, *16*, 1430. [CrossRef] [PubMed]
34. Adinolfi, G.; Graditi, G. Reliability Prediction of Smart Maximum Power Point Converter for PV Applications. In *System Reliability*; InTech: London, UK, 2017; doi:10.5772/intechopen.72130 [CrossRef]
35. Song, Q.; Wang, L.; Chen, J. A Decentralized Energy Management Strategy for a Fuel Cell–Battery Hybrid Electric Vehicle Based on Composite Control. *IEEE Trans. Ind. Electron.* **2021**, *68*, 5486–5496. [CrossRef]
36. Mishra, P.; Pradhan, A.K.; Bajpai, P. Adaptive Distance Relaying for Distribution Lines Connecting Inverter-Interfaced Solar PV Plant. *IEEE Trans. Ind. Electron.* **2021**, *68*, 2300–2309. [CrossRef]
37. Khalghani, M.R.; Solanki, J.; Solanki, S.K.; Khooban, M.H.; Sargolzaei, A. Resilient Frequency Control Design for Microgrids Under False Data Injection. *IEEE Trans. Ind. Electron.* **2021**, *68*, 2151–2162. [CrossRef]
38. Xu, Y.; Nian, H.; Chen, L. Small-Signal Modeling and Analysis of DC-Link Dynamics in Type-IV Wind Turbine System. *IEEE Trans. Ind. Electron.* **2021**, *68*, 1423–1433. [CrossRef]
39. He, H.; Quan, S.; Sun, F.; Wang, Y. Model Predictive Control With Lifetime Constraints Based Energy Management Strategy for Proton Exchange Membrane Fuel Cell Hybrid Power Systems. *IEEE Trans. Ind. Electron.* **2020**, *67*, 9012–9023. [CrossRef]
40. Li, J.; Zhou, Q.; Williams, H.; Xu, H. Back-to-Back Competitive Learning Mechanism for Fuzzy Logic Based Supervisory Control System of Hybrid Electric Vehicles. *IEEE Trans. Ind. Electron.* **2020**, *67*, 8900–8909. [CrossRef]
41. Liu, C.; Bai, H.; Zhuo, S.; Zhang, X.; Ma, R.; Gao, F. Real-Time Simulation of Power Electronic Systems Based on Predictive Behavior. *IEEE Trans. Ind. Electron.* **2020**, *67*, 8044–8053. [CrossRef]
42. Ling, Y.; Li, Y.; Xiang, J. Load Support by Droop-controlled Distributed Generations. *IEEE Trans. Ind. Electron.* **2021**, *68*, 8345–8355. [CrossRef]
43. Hren, A.; Slibar, P. Full order dynamic model of SEPIC converter. In Proceedings of the IEEE International Symposium on Industrial Electronics, ISIE 2005, Dubrovnik, Croatia, 20–23 June 2005; Volume 2, pp. 553–558.
44. Chang, C.W.; Wei, C.L. Single-inductor four-switch non-inverting buck-boost dc-dc converter. In Proceedings of the 2011 International Symposium on VLSI Design, Automation and Test, Hsinchu, Taiwan, 25–28 April 2011; pp. 1–4.
45. Mendez-Diaz, F.; Pico, B.; Vidal-Idiarte, E.; Calvente, J.; Giral, R. HM/PWM Seamless Control of a Bidirectional Buck–Boost Converter for a Photovoltaic Application. *IEEE Trans. Power Electron.* **2019**, *34*, 2887–2899. [CrossRef]
46. González-Castaño, C.; Restrepo, C.; Giral, R.; García-Amoros, J.; Vidal-Idiarte, E.; Calvente, J. Coupled inductors design of the bidirectional non-inverting buck–boost converter for high-voltage applications. *IET Power Electron.* **2020**, *13*, 3188–3198. [CrossRef]
47. Górecki, P.; Wojciechowski, D. Accurate Computation of IGBT Junction Temperature in PLECS. *IEEE Trans. Electron. Dev.* **2020**, *67*, 2865–2871. [CrossRef]
48. Imaoka, J.; Okamoto, K.; Shoyama, M.; Ishikura, Y.; Noah, M.; Yamamoto, M. Modeling, magnetic design, simulation methods, and experimental evaluation of various powder cores used in power converters considering their DC superimposition characteristics. *IEEE Trans. Power Electron.* **2018**, *34*, 9033–9051. [CrossRef]
49. Kazimierczuk, M.K. *High-Frequency Magnetic Components*; John Wiley & Sons: Hoboken, NJ, USA, 2009.
50. Teodorescu, R.; Liserre, M.; Rodriguez, P. *Grid Converters for Photovoltaic and Wind Power Systems*; John Wiley & Sons: Hoboken, NJ, USA, 2011; Volume 29.
51. Corradini, L.; Maksimovic, D.; Mattavelli, P.; Zane, R. *Digital Control of High-Frequency Switched-Mode Power Converters*; John Wiley & Sons: Hoboken, NJ, USA, 2015.
52. Calvente, J.; Ramirez-Murillo, H.; Vidal-Idiarte, E.; Giral, R.; Restrepo, C. Multisampled average current control of switching power converters. In Proceedings of the 2015 IEEE International Conference on Industrial Technology (ICIT), Seville, Spain, 17–19 March 2015; pp. 2120–2124.
53. Chen, J.; Prodic, A.; Erickson, R.W.; Maksimovic, D. Predictive digital current programmed control. *IEEE Trans. Power Electron.* **2003**, *18*, 411–419. [CrossRef]
54. Restrepo, C.; Konjedic, T.; Flores-Bahamonde, F.; Vidal-Idiarte, E.; Calvente, J.; Giral, R. Multisampled digital average current controls of the versatile buck–boost converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *7*, 879–890. [CrossRef]

55. Patiño, C.R. Pem Fuel Cell Modeling and Converters Design for a 48 vs. dc Power Bus. Ph.D. Thesis, Universitat Rovira i Virgili, Tarragona, Spain, 2012.
56. Jackiewicz, D.; Kachniarz, M.; Bieńkowski, A. Temperature Influence on the Functional Properties of Inductive Components with Mn–Zn Ferrite Cores. In Proceedings of the International Conference on Oxide Materials for Electronic Engineering, Lviv, Ukraine, 29 May–2 June 2017; Volume 59.