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Decision Levels and Resolution for Low-Power Winner-Take-All Circuit †

Ruxandra L. Costea

Electrical Engineering Department, Electrical Engineering Faculty, Polytechnic University of Bucharest, 060042 Bucharest, Romania; ruxandra.costea@upb.ro

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Abstract: Sensors in many applications must select the largest element in a sequence of currents. This can be performed in an analog way by the Winner-Take-All (WTA) circuit. This paper considers the classic version of the WTA Lazzaro circuit, working with MOS devices in a subthreshold regime. Since the separation of the gainer by analytically computable "decision levels" has recently been introduced, this paper aims to numerically verify and discuss these levels and their dependence on circuit and device parameters. For V_T, the threshold voltage of MOS devices, which is primarily responsible for differences between components (mismatch), its relationship with the output voltages is theoretically demonstrated and numerically checked.

Keywords: Winner-Take-All; subthreshold; decision levels; resolution; mismatch

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1. Introduction

Winner-Take-All (WTA) circuits are one of the most important building blocks in analog parallel signal processing, such as spatial acquisition and tracking, sound localization, image processing and neuromorphic systems [1–7]. The main function of a WTA is to select the highest input signal among multiple inputs, so two-input WTAs can also be used as half-wave and full-wave rectifiers [8–10]. Many WTA proposals can be found in the literature, such as voltage-mode configurations based on differential pair structures [11,12] or on inhibitory and local excitatory feedback loop circuits [13–16]. The first approach suffers from complexity and a high power comsumption, whereas the second approach has potential stability issues due to positive feedback.

In recent years, the processing of nanoamps has become increasingly important. These currents can come from sensors inside the human body—[17], from chemical reaction sensors, from motion tracking or from computer memory—[18]—to name just a few examples. In fact, the analog processing of very small signals was used in "neuromorphic" circuits initiated by Carver Mead at Caltech in the early 1990s [19,20]. In that context, the first W (inner) T(ake) A(ll) circuit appeared, known today as the "Lazzaro Circuit"—[21]. Its simplicity that leads to space savings on integrated chips has distinguished it technologically. Many improvements to the Lazzaro circuit have been proposed in the meantime [22,23], but the basic principle and configuration have not changed.

In [24], Sekerkiran et al. proposed a modified version of Lazzaro's WTA, which improved the resolution without requiring positive feedback, thus avoiding major stability issues. Their approach consisted of using an aditional transistor per cell to increase the open loop gain and, therefore, improve resolution. However, both Lazzaro's and Sekerkiran's WTAs need a high voltage swing at the input nodes to turn on the winning cell, which results in a slow response to abrupt input current changes.

The parameters of MOS and their interconnections must be as identical as possible. Integrated circuit technology, engaged in a race to reduce the size of chips and circuits, can-

not ensure the strict identity of the parameters on the same chip or on different chips. Thus appears the so-called "mismatch"—[22–25], whose size is a criterion for the performance of the chips. It is all the more important as the circuit works with lower currents. In this way, the study of the variation in the performances of the circuits with MOS transistors working in the subthreshold (or weak inversion) when the model parameters slide around the design value is decisive.

This paper considers the original Lazzaro circuit, working in the subthreshold as a selector of the maximum current rank. For the list of output voltages, a parallel paper co-authored by the present author—[26,27]—introduced a "higher decision level". Above it, only the highest rank (winner) in the output list must be placed. Similarly, a "lower decision level" must be above the second-largest rank and under the higher level. Both levels were rigorously defined and used to introduce the resolution performance of the selector.

In fact, we need two notions of resolution. One for the input lists—the input resolution—and one for the selection result—the output resolution. To be sensitive and efficient, a WTA fed with "crowded" lists must select the output through a "wide" separation. Below, after introducing the circuit static model in Section 2, we present the theoretical questions about decision levels and about the resolution in Sections 3 and 4. In Section 5, the monotonic dependence of the winner size on the threshold voltage V_T of MOS devices is proven. Section 6 contains numerically computed examples. Analytically computed decision levels and resolutions are extensively checked and analyzed.

2. The Circuit Model

For the subthreshold regime—i.e., when $V_{GS} \leq V_T$ and $V_{DS} \geq 0$—we use the usual MOS model [28] with the usual notations:

$$I_{DS} = I_0 \left[\exp\left(-\frac{V_S}{V_t}\right) - \exp\left(-\frac{V_D}{V_t}\right) \right] \exp\left(k\frac{V_G}{V_t}\right) \tag{1}$$

Then, the steady state of the Lazzaro WTA circuit in Figure 1 (with all devices in the subthreshold) can be obtained by $I_j = I_{T_j}$ and $I_C = \sum_{j=1}^{N} I_{T_j^\star}$ where I_{T_j} and $I_{T_j^\star}$ are the I_{DS} currents for T_j and $T_j^\star$, respectively. Thus, we will move on to the following:

$$U_j = V_t \ln\left[1 - \frac{I_j}{I_0}\exp\left(-k\frac{V}{V_t}\right)\right]^{-1}, \quad j \in \overline{1,N} \tag{2}$$

$$I_C = G(V, I) \tag{3}$$

where

$$G(V,I) = I_0\left[\exp\left(-\frac{V}{V_t}\right) - \exp\left(-\frac{V_{DD}}{V_t}\right)\right] \times \sum_{j=1}^{N}\left[1 - \frac{I_j}{I_0}\exp\left(-k\frac{V}{V_t}\right)\right]^{-k} \tag{4}$$

In the above equations, the MOS parameters are I_0, k and V_T while I_j, I_C and V_{DD} are outside constant sources. For an input list of currents $I = (I_1, I_2, \ldots, I_N)$, Equation (3) provides the common potential V with which Equation (2) gives the output voltages $U = (U_1, U_2, \ldots, U_N)$.

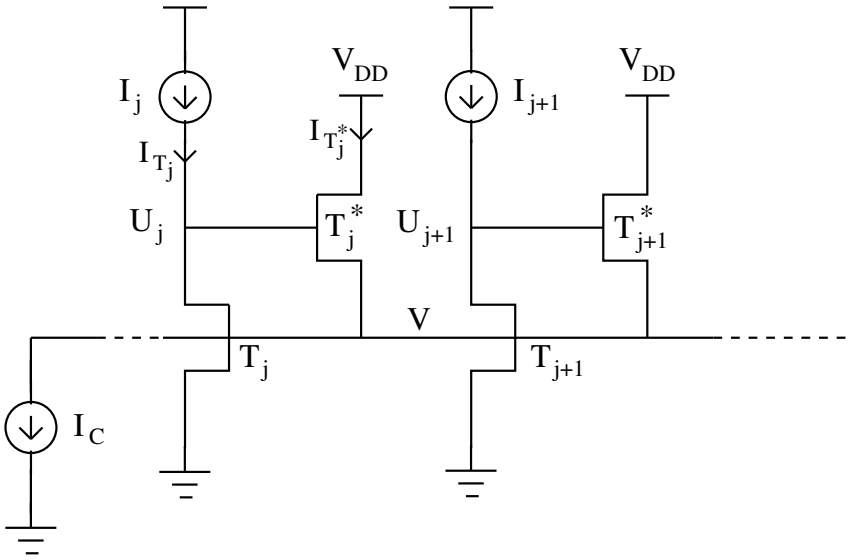

Figure 1. Two cells of Lazzaro WTA. $I_1, I_2, \ldots, I_N$ are input currents; $U_1, U_2, \ldots, U_N$ are output voltages; I_C is the bias current.

Obviously, we have to make sure that all transistors T_j and $T_j^\star$ work in the subthreshold, which means [26,29] V and U_j must be restricted to

$$0 \leq V \leq \min\{V_{DD}, V_T\} \tag{5}$$

$$0 \leq U_j \leq V_T + V, \quad j \in \overline{1, N} \tag{6}$$

As we prove in [26], the following restrictions are sufficient:

$$V_T < V_{DD} \tag{7}$$

$$I_0 \leq I_M \leq I_0 \exp\left(\frac{kV_T}{V_t}\right) \tag{8}$$

$$\frac{I_0}{N-1} \leq \Delta \leq \frac{I_M}{N-1} \tag{9}$$

$$I_C \geq G\left(V_T, \hat{\hat{C}}\right) \tag{10}$$

where I_M is the absolute maximum of currents allowed for processing. For Δ and $\hat{\hat{C}}$, see below. Let us note that the right side in (9) is not a restriction.

Finally, let us mention that, in [29], for the dynamic model of our circuit, the invariance of the solution in a weak inversion region as well as its asymptotic stability have been studied.

3. Decision Levels

To explain the issue of decision levels, let us start with a simple example.

Let us consider our WTA in the particular case of $N = 3$, fed with the infinite number of lists in $\mathcal{L}(3, I_M, \Delta)$, that is, lists with three currents, no bigger that I_M and separated from each other by the minimum distance Δ. The first list $I = (I_1, I_2, I_3)$ with the (decreasing) order $\sigma = (3, 1, 2)$ arrives at the WTA input—see Figure 2. The goal is to signal the "winning" rank $\sigma 1 = 3$ of the largest current I_3, even in the extreme case when "the loser"—which is the second-largest current I_1—is at the minimum distance Δ, $I_3 - I_1 = \Delta$ and Δ is so small that the two are not distinguishable on the $[0, I_M]$ scale.

The WTA circuit translates the reading of the winner rank to the output list of voltages $U = (U_1, U_2, U_3)$, which has the same order $\sigma = (3, 1, 2)$. However, the winner U_3 is now split from the loser U_1 by a gap $\overline{D} - \underline{D}$, which is sufficiently large on the $[0, U_M]$ scale.

In fact, we have to have $U_3 \geq \overline{D} > \underline{D} \geq U_1 > U_2$. $\overline{D}$ is called "the upper decision level" and has the property that it is surpassed only by the winner. Thus, the outputs (U_1, U_2, U_3) are compared with $\overline{D}$—see Figure 2—and rank 3 will be the unique winner.

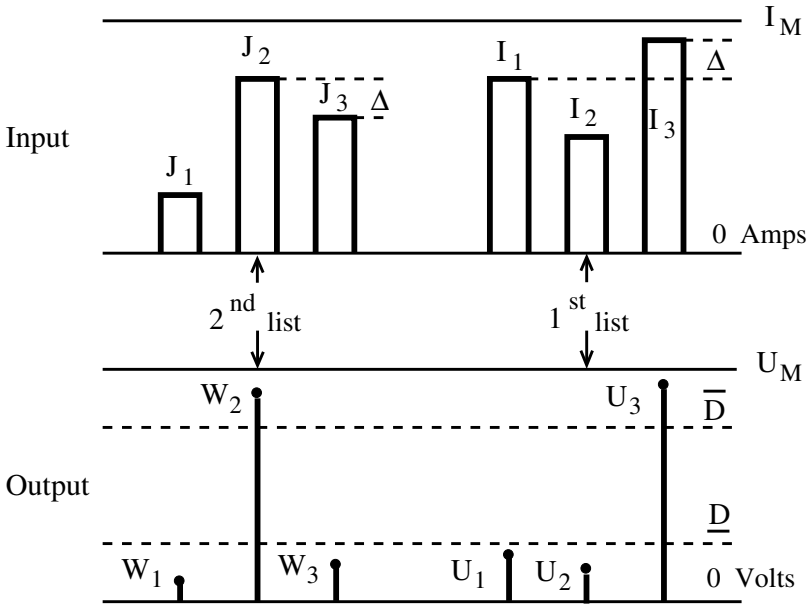

Figure 2. The input list (I_1, I_2, I_3) yields the output list (U_1, U_2, U_3); the input list (J_1, J_2, J_3) yields the output list (W_1, W_2, W_3). The winning ranks are "3" in the first case and "2" in the second, since U_3 and W_2 surpass $\overline{D}$.

Furthermore, $\underline{D}$ is called "the lower decision level", and all the "losers" (U_1 and U_2 here) are under it. The distance $\overline{D} - \underline{D}$ is significant on the scale $[0, U_M]$, where U_M is the maximum voltage. Returning to Figure 2, let us consider a second list (J_1, J_2, J_3) from $\mathcal{L}(3, I_M, \Delta)$ applied at the input. Suppose that $J_2 > J_3 > J_1$ and the winner rank "2" has to be signaled. This is performed by obtaining the output voltages (W_1, W_2, W_3) arranged as $W_2 \geq \overline{D} > \underline{D} \geq W_3 \geq W_1$, where the only rank surpassing the upper decision level $\overline{D}$ is "2", the winner. The losers are below the lower decision level $\underline{D}$. The processing should be similar for any list from $\mathcal{L}(3, I_M, \Delta)$ when using the same decision levels $\overline{D}$ and $\underline{D}$ and the same circuit parameters.

For the input list $I = (I_1, I_2, \ldots, I_N)$ written in the terminal order, let us denote $\sigma = (\sigma 1, \sigma 2, \ldots, \sigma N)$ a permutation of the indices such that the currents in $I^\sigma = (I_{\sigma 1}, I_{\sigma 2}, \ldots, I_{\sigma N})$ are in decreasing order:

$$I_M \geq I_{\sigma 1} > I_{\sigma 2} > \ldots > I_{\sigma N} \geq 0 \tag{11}$$

Then, from (2), it is clear that the output voltages $U = (U_1, U_2, \ldots, U_N)$ are in the same decreasing order, i.e.,

$$U_M \geq U_{\sigma 1} > U_{\sigma 2} > \ldots > U_{\sigma N} \geq 0 \tag{12}$$

Both $I_{\sigma 1}$ and $U_{\sigma 1}$ are called "winner" while both $I_{\sigma 2}$ and $U_{\sigma 2}$ are called "loser". To $U_{\sigma 3}, U_{\sigma 4}, \ldots, U_{\sigma N}$ and to $I_{\sigma 3}, I_{\sigma 4}, \ldots, I_{\sigma N}$ as well, we use the same name, "losers".

We will assume that the input currents $I \in \Re^N$ belong to the class $\mathcal{L}(N, I_M, \Delta)$, i.e., their components are inside the $[0, I_M]$ interval and are mutually separated by distance Δ at least. To abbreviate the writing, from here on, we will denote this class simply by $\mathcal{L}$. Thus,

$$I_{\sigma j} - I_{\sigma (j+1)} \geq \Delta, \;\; j \in \overline{1, N-1} \tag{13}$$

This leads to the existence of $[C_{jm}, C_{jM}]$ intervals in which each $I_{\sigma j}$ current is forced to belong:

$$I_{\sigma j} \in [C_{jm}, C_{jM}] \tag{14}$$

Here, for each $j \in \overline{1, N}$,

$$C_{jm} = (N - j)\Delta \tag{15}$$

and

$$C_{jM} = I_M - (j - 1)\Delta \tag{16}$$

We put

$$\hat{\overline{C}} = (C_{1M}, C_{2M}, C_{3M}, \ldots, C_{NM}) \tag{17}$$

the list of maximum currents of each rank from (10). Note that the intervals in (14) do not overlap. All possible lists at the input (i.e., satisfying (7)–(10)) have in common the number of elements N, the maximum current I_M and a measure of the agglomeration of the currents Δ. Let us denote by $\mathcal{L}$ this (infinite) family of input lists.

The raison d'*ê*tre of the WTA circuit is to identify the rank $\sigma 1$ of the highest current $I_{\sigma 1}$ in list I and to achieve this for any input list in $\mathcal{L}$ without changing the parameters or configuration.

A recent co-work by the author of this paper—[26]—has introduced two "decision levels", $\overline{D}$ and $\underline{D}$, which split the output list as follows:

$$U_M \geq U_{\sigma 1} \geq \overline{D} > \underline{D} \geq U_{\sigma 2} > U_{\sigma 3} > \ldots > U_{\sigma N} \tag{18}$$

Here, $\overline{D}$ is defined as the smallest winner of the output lists when all inputs in $\mathcal{L}$ are applied. Similarly, $\underline{D}$ is the highest loser for all inputs in $\mathcal{L}$. The main attraction of these particular levels consists of the fact that they can be obtained "semi-analytically".

Thus, it is proven that

$$\overline{D} = U_1(\overline{C}) \tag{19}$$

where

$$\overline{C} = (C_{1m}, C_{2m}, C_{3m}, \ldots, C_{Nm}) \tag{20}$$

is the $\mathcal{L}$-list with currents in (15). This means that the upper decision level $\overline{D}$ is exactly the winner of the output list $U = U(\overline{C}) = (U_1(\overline{C}), U_2(\overline{C}), \ldots, U_N(\overline{C}))$ when the currents in $\overline{C}$ are the input. It is shown that they are the smallest possible currents of each rank, computable as in (15).

Also, we have

$$\underline{D} = U_2(\underline{C}) \tag{21}$$

where

$$\underline{C} = (C_{1M}, C_{2M}, C_{3m}, \ldots, C_{Nm}) \tag{22}$$

—see (15) and (16). In other words, the lower decision level $\underline{D}$ is identified as the loser of the output list $U = U(\underline{C}) = (U_1(\underline{C}), U_2(\underline{C}), \ldots, U_N(\underline{C}))$ when the currents in $\underline{C}$ are the input. In addition, (22) shows that the first two currents in $\underline{C}$ are the highest in their class $\mathcal{L}$, while all others currents are the lowest possible in their respective rank. After $\overline{C}$ and $\underline{C}$ are evaluated, they are used as inputs I_j in (2)+(3) to compute (numerically) the outputs

$U(\overline{C})$ and $U(\underline{C})$. From them, the decision levels $\overline{D}$ and $\underline{D}$ are extracted as in (19) and (21), respectively.

Finally, we need the largest U_M voltage when applying $\mathcal{L}$. It can be shown that the maximum output voltage U_M is obtained if we apply—see [26]–at the input

$$\widehat{C} = (C_{1M}, C_{2m}, C_{3m}, \ldots, C_{Nm}) \tag{23}$$

and take the maximum voltage in the output

$$U_M = U_{\sigma 1}\left(\widehat{C}\right) \tag{24}$$

4. Resolutions

In order to appreciate the WTA performances, apart from the threshold $\overline{D}$ and $\underline{D}$, we need a measure of the finesse of selecting the winner. First, we need a measure of the "crowding" of the currents at the input.

The family $\mathcal{L}$ contains lists of currents on the $[0, I_M]$ scale, whose cramming is measured by Δ. The difference between the largest and the second-largest current of any list is at least Δ. The coefficient ω defined by

$$\omega = \frac{\Delta}{I_M} \tag{25}$$

This will be called "THE INPUT RESOLUTION". When ω is very small, perceiving I_w (the winner) and I_l (the loser) as distinct from each other is difficult and prone to error. On the output side, the voltages are similarly arranged on the $[0, U_M]$ scale. However, the positions of the w (i.e., winner) and l (i.e., loser) ranks are now controlled by the decision levels $\overline{D}$ and $\underline{D}$:

$$U_M \geq U_w \geq \overline{D} > \underline{D} \geq U_l > 0 \tag{26}$$

$\overline{D}$ and $\underline{D}$ do not change when a new list from $\mathcal{L}$ arrives. Under constraints in (7)–(10), $\overline{D}$ and $\underline{D}$ are fixed by (19) and (21). Each winner of each list surpasses $\overline{D}$. Each loser of each list in $\mathcal{L}$ falls under $\underline{D}$. The gap $\overline{D} - \underline{D}$ compared with the entire U_M will be denoted by Ω and called "THE OUTPUT RESOLUTION":

$$\Omega = \frac{\overline{D} - \underline{D}}{U_M} \tag{27}$$

The similarity between ω at input and Ω at output is complete. Both of them indicate how much of the "reading scale" is taken up by the smallest possible size difference between the w and l ranks. The circuit is effective if "it amplifies" the resolution of the input list. The large values for Ω/ω mean that the winning rank is highly distinct. To understand the WTA input–output mechanism, we study the function $\Omega(\omega)$ when I_M and I_C are unchanged. For clarity, we will translate the results obtained so far in terms of ω, where $\omega = \Delta / I_M$.

In [26], it is shown that

$$\Omega(\omega) > \omega \tag{28}$$

at least for a part of ω's "spectre". However, examples show that the ratio $\frac{\Omega}{\omega}$ is in the order of hundreds at least.

$$\frac{d\overline{D}(\omega)}{d\omega} > 0 \tag{29}$$

$$\frac{d\underline{D}(\omega)}{d\omega} < 0 \tag{30}$$

$$\frac{dU_M(\omega)}{d\omega} < 0 \tag{31}$$

From (27), it follows immediately that

$$\frac{d\Omega(\omega)}{d\omega} > 0 \tag{32}$$

which means that the $\Omega(\omega)$ function is monotonously increasing. This corresponds to "the intuition" that more disjointed current lists are processed more efficiently (i.e., the gap $\overline{D} - \underline{D}$ is bigger).

5. Exploring the Mismatch

The threshold voltage V_T is the value of the voltage V_{GS} that controls the transition between the distinct operating regions of the MOS. The value of V_T is influenced by the thickness of the oxide layer, as well as by body doping. Also, V_T depends a lot on the parasitic charge trapped between oxide and silicon. In contrast to this "accidental" charge, some charge can be introduced intentionally through the process called "ion implantation".

Moreover, it is well known that subthreshold design has dramatically increased the sensitivity to process variation. This fact is taken into account by introducing the variation in the zero current with threshold voltage. Indeed,

$$I_0 = I_0^{\star} \exp\left(-k\frac{V_T}{V_t}\right) \tag{33}$$

where $I_0^{\star}$ does not depend on V_T—see [28]. Subsequently, we use (33) in models (2) and (3) and try to evaluate the influence of V_T on the output U_j. Fortunately, we can analytically deduce a qualitative behaviour. Namely, we can show that U_j decreases with V_T:

$$\frac{\partial U_j}{\partial V_T} < 0 \tag{34}$$

For this, let us denote $F_j(V, I_0) = 1 - \frac{I_j}{I_0}\exp\left(-k\frac{V}{V_t}\right)$ and $d = \exp\left(-\frac{V_{DD}}{V_t}\right)$ such that the function in (4) becomes

$$G(V, I_0) = I_0\left[\exp\left(-\frac{V}{V_t}\right) - d\right]\sum_{j=1}^{N} F_j^{-k}(V, I_0) \tag{35}$$

Equation (3) with a fixed I_C gives

$$0 = \left.\frac{\partial G(V(I_0), I_0)}{\partial V}\right|_{I_0=cst} \times \frac{\partial V(I_0)}{\partial I_0} + \left.\frac{\partial G(V(I_0), I_0)}{\partial I_0}\right|_{V=cst} \tag{36}$$

We easily obtain

$$\left.\frac{\partial G}{\partial V}(V(I_0), I_0)\right|_{I_0=cst} < 0 \text{ and } \left.\frac{\partial G}{\partial I_0}(V(I_0), I_0)\right|_{V=cst} > 0$$

Then, (36) gives

$$\frac{\partial V(I_0)}{\partial I_0} > 0 \tag{37}$$

However, from (2),

$$U_j(V(I_0), I_0) = V_t \ln F_j(V(I_0), I_0)$$

and

$$\frac{\partial U_j}{\partial I_0} = \frac{\partial U_j}{\partial V}\bigg|_{I_0=cst} \times \frac{\partial V(I_0)}{\partial I_0} + \frac{\partial U_j}{\partial I_0}\bigg|_{V=cst} = V_t F_j \frac{\partial F_j}{\partial V}\bigg|_{I_0=cst} \times \frac{\partial V(I_0)}{\partial I_0} + V_t I_j \frac{\partial F_j}{\partial I_0}\bigg|_{V=cst}$$

Here, the two derivatives of F_j are positive and by also using (37) we derive $\frac{\partial U_j}{\partial I_0} > 0$. From (33), we obtain $\frac{\partial U_j}{\partial V_t} < 0$, which is (34).

6. Numerical Checks – Discussion

6.1. Decision Levels

In this paragraph, we deal with the decision levels $\overline{D}$ and $\underline{D}$ on the $[0, U_M]$ scale. The known quantities are k, V_T, I_0 and V_t (i.e., the MOS device parameters) then N, I_C and V_{DD} (circuit parameters) and I_M and Δ (i.e., $\mathcal{L}$ class characteristics). All these quantities must satisfy the restrictions (7)–(10). Their numerical values are $k = 0.9$, $V_T = 1$ V, $I_0 = 10^{-18}$ Amp, $V_t = 0.026$ V, $N = 100$, $I_C = 10^{-17}$ Amp, $V_{DD} = 1.5$ V, $I_M = 10$ nA and $\Delta = 0.01$ nA. We will call this case "Example 1". Now follows the analytical part of decision levels calculation. Our result is obtained in formula (20), (22) and (23), which give three particular input lists of currents $\overline{C}$, $\underline{C}$ and $\widehat{C}$. For their calculation, we use (15) and (16), which lead to $C_{jm} = (100 - j)0.01$ and $C_{jM} = 10 - (j - 1)0.01$, both in nAmps and for $j \in \overline{1,100}$. Thus, lists $\overline{C}$, $\underline{C}$ and $\widehat{C}$ from (20), (22) and (23) are now known. At this point, the numerical part of the calculation begins. We solve the 101 equations in (2) and (3) three times corresponding to the inputs $\overline{C}$, $\underline{C}$ and $\widehat{C}$. We obtain three output sequence $U(\overline{C})$, $U(\underline{C})$ and $U\left(\widehat{C}\right)$, respectively, each of 100 voltages. From each of them, we select one component according to (19), (21) and (24). Namely, the largest voltage in $U(\overline{C})$ is the upper decision level $U_1(\overline{C}) = \overline{D}$. The second-largest voltage in $U(\underline{C})$ is the lower decision level $U_2(\underline{C}) = \underline{D}$. Finally, the largest component in $U\left(\widehat{C}\right)$ is the maximum possible voltage when any of the $\mathcal{L}$ lists is processed: $U_1\left(\widehat{C}\right) = U_M$. For our circuit and device parameters, we obtain $\overline{D} = 726$ mV, $\underline{D} = 179$ mV and $U_M = 803$ mV, as shown in Figure 3a. So, out of the scale of 803 mV, any winner will be caught in the interval $\left[\overline{D}, U_M\right] = [726, 803]$, i.e., in the upper part of 9.6%. The loser will always be in the interval $[0, \underline{D}] = [0, 179]$, i.e., in the lower part of 22.3%—see Figure 3a. The rest of the scale, i.e., the interval $\left[\underline{D}, \overline{D}\right] = [179, 726]$, which represents 68.1% of the total, is the separation "gap" between the unique winner and the rest of the 99 losers.

The ratio $\omega\% = \Delta / I_M\% = \frac{0.01}{10}100 = 0.1\%$ is the "INPUT RESOLUTION" introduced in Section 4. It shows how crowded the lists we intend to process can be. At the output, we brought the "OUTPUT RESOLUTION" $\Omega\% = \left(\overline{D} - \underline{D}\right)/U_M\% = (726 - 179)/803 = 68.1\%$—see Figure 3a.

This means that the input resolution yields an input one of 681 times higher. The ratio Ω/ω is a performance index for WTA.

Now, we change V_T from 1 V to 1.1 V. For the same parameters, k, I_0, V_t, N, V_{DD}, I_M and Δ, we obtain the lists $\overline{C}$, $\underline{C}$ and $\widehat{C}$. Solving again the 101 equations from (2) and (3) (this time with $V_T = 1.1$ V), we obtain $U_1(\overline{C}) = \overline{D} = 515$ mV, $U_2(\underline{C}) = \underline{D} = 179$ mV and $U_1\left(\widehat{C}\right) = U_M = 589$ mV. Then, $\Omega\% = 57\%$—see Figure 3b and the comments in Section 6.2.

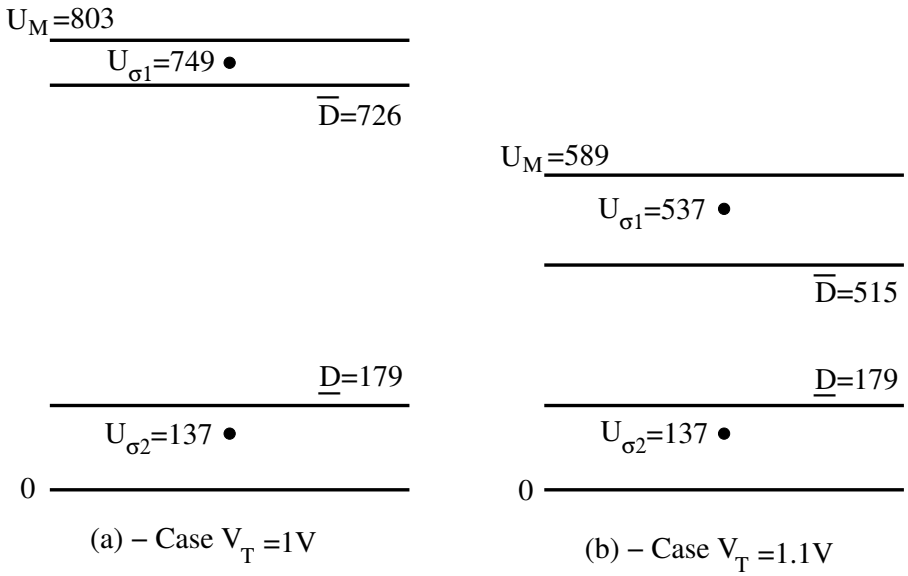

Figure 3. Example 1: $N = 100$, $I_M = 10\ mAmp$ and $\Delta = 0.01$ nAmp. Two cases for $V_T = 1$ V and $V_T = 1.1$ V. The winner $U_{\sigma 1}$, the loser $U_{\sigma 2}$, the maximum voltage U_M and the decision levels $\overline{D}$ and $\underline{D}$.

6.2. Mismatch

We take the device parameters in Example 1 except for I_0, which is replaced by (33) with $I_0^\star = 10^{-33}$ Amp. Also, we successively use in (33) V_T as 1 V, 1.02 V, 1.04 V, . . ., 1.1 V. For the class $\mathcal{L}$ with $I_M = 10$ nA and $\Delta = 0.01$ nA, $N = 100$, we follow the procedure in Section 6.1 and determine U_M, $\overline{D}$ and $\underline{D}$ for each of these six cases. The results are presented in Table 1.

Table 1. Example 2 Section 6.2. V_T, U_M, $\overline{D}$ and $\underline{D}$ in mV. Output resolution Ω in percent.

V_T	1000	1020	1040	1060	1080	1100
U_M	803	759	719	674	632	589
$\overline{D}$	726	684	642	600	557	515
$\underline{D}$	179	179	179	179	179	179
$\frac{\overline{D}-\underline{D}}{U_M}$ %	68%	66%	64%	62%	59%	57%

We notice that major effects occur when the threshold voltage V_T increases by 10%—See Figure 3a,b. The maximum voltage U_M decreases drastically by 27%, while the higher decision level $\overline{D}$ decreases by 29%. Remarkably, the lower decision level $\underline{D}$ is hardly influenced by the deviation of V_T. Even more remarkable is that the decrease in the output resolution by 10 percent does not sufficiently reflect the major worsening of the accuracy in the appreciation of the maximum $U_{\sigma 1}$. It turns out that the maximum output voltage U_M must accompany the output resolution parameter Ω in the WTA circuit specifications.

6.3. List Processing

Example 3

With the WTA data from the previous example, let us take a list of 100 currents given by

$$I_{2j} = (2j+1)\Delta, \quad j \in \overline{1,24} \tag{38}$$

$$I_{50+2j} = (197-4j)\Delta, \quad j \in \overline{0,25} \tag{39}$$

$$I_{2j+1} = 4j\Delta, \quad j \in \overline{0,49} \tag{40}$$

Among these 100 currents two groups are shown in Table 2 Column 1. The largest current in our list $I = (I_1, I_2, \ldots, I_{100})$ is found at terminal 50. If $\sigma = (\sigma_1, \sigma_2, \ldots, \sigma_{100})$ is the permutation that gives the descending order, then $\sigma_1 = 50$, i.e., $I_{\sigma_1} = I_{50} = 1.97$ nA, as in Table 2 Column 1. Also, the second-largest current is at terminal 99. Thus, $\sigma_2 = 99$, i.e., $I_{\sigma_2} = I_{99} = 1.96$ nA, as in Table 2. Now, we solve the Equations (2) and (3) with the above currents and $V_T = 1$ V. Out of the output $U = (U_1, U_2, \ldots, U_{100})$, Table 2 Column 2 shows the voltages U_{49} to U_{54} and U_{95} to U_{100}. It is verified that the order in U is given by the same permutation σ as currents, such that the winner is $U_{\sigma 1} = U_{50} = 749$ mV and the loser is $U_{\sigma 2} = U_{99} = 137$ mV—see Table 2 Figure 3. The winner is caught in the interval $\left[\overline{D}, U_M\right]$, while the loser $U_{\sigma 2}$ together with all other voltages $U_{\sigma 3}, \ldots, U_{\sigma 100}$ fall in the interval $[0, \underline{D}]$. The output resolution is $\Omega\% = 68\%$, way better than $\omega\% = 0.1\%$ at the input.

Next, we change the threshold voltage V_T (Table 2 Column 3) to 1.1 V and obtain an output similarly ordered, i.e., the winner is U_{50} and the loser is U_{99}. Their placement above $\overline{D} = 515$ mV and under $\underline{D} = 179$ mV, respectively, (see Table 1) shows the correctitude of detaching the largest element of the input list.

Table 2. Examples 3 and 4. $I_{49} - I_{54}$ and $I_{95} - I_{100}$, two groups of currents given in (38)–(40) are listed in Column 1. Column 2 shows output voltages for $V_T = 1$ V. Column 3 shows output voltages for $V_T = 1.1$ V. Column 4 shows the indices σj—the j-th current (and voltage) in descending order.

I_j **nA**	**Example 3** U_j **in mV** $V_T = 1$ **V**	**Example 4** U_j **in mV** $V_T = 1.1$ **V**	σ_j
$I_{49} = 0.96$	$U_{49} = 17.5$	$U_{49} = 17.3$	$\sigma_{24} = 49$
$I_{50} = 1.97$	$U_{50} = 749$	$U_{50} = 537$	$\sigma_1 = 50$
$I_{51} = 1$	$U_{51} = 18$	$U_{51} = 18$	$\sigma_{50} = 51$
$I_{52} = 1.93$	$U_{52} = 101$	$U_{52} = 101$	$\sigma_3 = 52$
$I_{53} = 1.04$	$U_{53} = 19$	$U_{53} = 19.5$	$\sigma_{48} = 53$
$I_{54} = 1.89$	$U_{54} = 83$	$U_{54} = 83$	$\sigma_5 = 54$
$I_{95} = 1.88$	$U_{95} = 80$	$U_{95} = 80$	$\sigma_6 = 95$
$I_{96} = 1.05$	$U_{96} = 19.5$	$U_{96} = 19$	$\sigma_{47} = 96$
$I_{97} = 1.92$	$U_{97} = 95$	$U_{97} = 95.5$	$\sigma_4 = 97$
$I_{98} = 1.01$	$U_{98} = 18.5$	$U_{98} = 18$	$\sigma_{49} = 98$
$I_{99} = 1.96$	$U_{99} = 137$	$U_{99} = 137$	$\sigma_2 = 99$
$I_{100} = 0.97$	$U_{100} = 17$	$U_{100} = 17$	$\sigma_{51} = 100$

7. Conclusions

Finding the maximum in continuous signal strings is a fundamental operation in signal processing. When processing speed is essential, the analog version is preferable. In this framework, the WTA circuit has imposed itself through technological simplicity. Of course, in this case we have to solve the problem of precision in separating the maximum rank ("winner") from the next rank ("loser"). This paper, in close connection with [26], verifies numerically that "the decision levels" work correctly. For this, the theoretical notions of decision levels, resolution and mismatch are specified first. Then, a class of strings of 100 currents is considered for which the decision levels and input and output resolution are analytically calculated. Numerical processing follows that simulates the operation of the WTA circuit. An ordered string of voltages is obtained at the output. It is verified that the largest element of this string exceeds the upper decision level while the rest of the elements are crowded much further, namely, below the lower decision level. The output resolution

compared to the input resolution indicates how much "the winner" is separated, i.e., the effectiveness of the WTA. It is theoretically shown that any of the output voltages decreases monotonically with increases in V_T. It is then verified by numerical calculation that the small increase in the threshold voltage of the MOS transistors leads to a drastic decrease in both the decision levels and the output resolution. Since the manufacturing technology cannot ensure a really constant V_T for series production, this is a major problem in the design of MOS circuits, especially those that work in the subthreshold.

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