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Investigation of Device- and Circuit-Level Reliability of Inverse-Mode Silicon-Germanium Heterojunction Bipolar Transistors

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Abstract: The reliability of inverse-mode silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) under dc stress and its potential impact on the performance of basic analog amplifiers are investigated. In order to properly reflect the stress effects in various circuit applications, the degradations under three different configurations (active bias, diode connection, and off state) were experimentally characterized with the stress voltages applied up to 3000 s for each case. Based on the changes in the Gummel response, the degradations in device parameters such as current gain (β), transconductance (g_m), and base-to-emitter resistance (r_π) were extracted and compared with the forward-mode counterpart. In addition, with the use of a small-signal equivalent model of a SiGe HBT, simple single-stage analog amplifiers were simulated as representative examples and their circuit-level performance metrics including gain and bandwidth were studied to estimate degradation characteristics with accumulated stress. It was found that transimpedance gain decreases and operation bandwidth increases to different levels due to device degradation, whereas a voltage amplifier exhibited much less changes.

Keywords: avalanche; breakdown; circuit-level reliability; electrical stress; forward mode (FM); Gummel; hot carrier; heterojunction bipolar transistor (HBT); inverse mode (IM); silicon germanium (SiGe); small-signal model

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1. Introduction

Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have provided unique advantages over conventional CMOS technologies in terms of high-frequency operation, noise characteristics, and large-signal performance, supporting seamless integration with CMOS technology [1–3]. In addition, a SiGe HBT is known to be robust against the total ionizing dose (TID) up to multi-Mrad irradiation by virtue of the intrinsic structure of the device that is less dependent on the oxide quality [4,5]. Regarding single-event effects (SEEs), which happen when a high-energy particle hits an active device and generates many excess charge carriers, however, SiGe technology has been known to be susceptible due to its junction-based operation [6–11]. Therefore, the use of a SiGe HBT under an SEE-intense environment (e.g., deep space) may impose a serious issue in signal integrity. Among various remedies and solutions, the use of an inverse-mode (IM) operation, which utilizes potential barriers and a low electric field, has been proposed as a viable radiation-hardening-by-design technique [12].

In most analog applications, forward mode (FM) SiGe HBTs are used to maximize circuit performance metrics. Unlike FM SiGe HBTs, the IM operation, where the physical emitter has higher voltage potential than the collector, is effective in mitigating the impact of single-event transients (SETs) and associated signal distortions for extreme-environment applications. This is due to the reduced transient peaks and/or durations compared with FM operation [12–15]. Since the IM configuration does not alter device intrinsic structure, there is no need to modify mask layers or include other peripheral circuitry [14,15]. On the other hand, one of the major concerns of using IM SiGe HBTs includes degraded performance due to unfavorable device dimensions and the doping profile [15–17]. Fortunately, with the help of technology scaling, dc and ac performance parameters have been improved for IM SiGe HBTs (e.g., current gain > 100, and unity-gain frequency > 50 GHz) as well as FM counterparts [18,19].

When it comes to device-level reliability under electrical stress, however, there have been few studies about degradations associated with IM operation [20,21]. Since most papers have focused on FM SiGe HBTs in the literature [2–15,20–24], proper design guidelines or performance estimation associated with IM SiGe HBTs is more or less limited. Whereas some characteristics of IM SiGe HBTs might be inferred from reliability results of FM cases, in order to fully exploit the benefits and compensate for the risks of IM SiGe HBTs, it is critical to analyze their degradation characteristics under electrical stress over time and evaluate robustness or weaknesses. In addition, the degradation results of a device are more beneficial if they are related to circuit-level stress conditions. As most SiGe HBTs are employed in analog circuit applications, parameter changes in a device affect circuit performance significantly. Hence, a relevant correlation between an IM SiGe HBT and a circuit in comparison with FM operation needs to be investigated.

In this paper, we study the different trends of degradations under three electrical stress conditions for a SiGe HBT in an amplifier. Three distinct stress conditions are active-bias, diode-connection, and off-state configurations, all of which are widely used in many analog circuits. The findings of this work can be used for the design and analysis of robust reliable circuits and systems and the prediction of performance. The organization of the paper is as follows. In Section 2, the stress conditions are described in detail and in Section 3, degradation results will be presented and analyzed. Section 4 will discuss expected circuit-level performance degradations based on the device characteristics and Section 5 summarizes the findings of this work.

2. Hardware Preparation and Test Setup

The devices under test (DUTs) used in this work were all NPN SiGe HBTs. They were fabricated in GlobalFoundries' 130 nm SiGe BiCMOS technology platform (8HP), which provides the unity-gain frequency (f_T) of 200 GHz and the maximum oscillation frequency (f_{MAX}) of 265 GHz [25]. Among available transistor options in the process, the high-performance version of SiGe HBTs was chosen. The (physical) emitter area was 2.5 μm (length) × 0.12 μm (width). In addition, the terminal organization of DUTs was configured as the C-B-E-B-C layout (C: collector, B: base, E: emitter), in which the collector current is distributed into two separate paths from the center (emitter) to both ends (collector).

As a versatile electronic component, a SiGe HBT is utilized in a different configurations in a variety of analog circuits. It can be employed as a voltage/current gain element, a biasing component, and a controlling device. Based on its key usage in circuit applications, it is exposed to the following stress conditions: (1) active bias, (2) diode connection, and (3) off state. Under each condition, the characteristics of a SiGe HBT were measured and compared for both the forward mode (FM) and inverse mode (IM). All devices were measured in an on-wafer test setup using a probe station and Keysight 4155C. The focus of this work is on single HBTs that are biased to operate in FM and IM each, under three distinct stress conditions.

In Figure 1, stress conditions including terminal connection and DC voltages are shown. The left column (Figure 1a–c) represents FM stress cases, whereas the right column

(Figure 1d–f) is for IM cases. After each electrical stress, device Gummel was measured under V_{CB} = 0 V. In IM configurations, the electrical connections of the physical collector and the emitter were swapped electrically. Under the active-bias stress conditions (see Figure 1a,d), the collector and the emitter terminals were reverse-biased and the base current was applied such that at the collector, the current was about 1 mA, setting the base-to-emitter voltage (V_{BE}) accordingly. Next, in the diode-connection cases (Figure 1b,e), the base and the electrical collector terminals are tied together and a high V_{CE} voltage was applied to stress a DUT. Lastly, Figure 1c,f illustrate the off-state stress condition, where the base is connected to a ground node. For each setup, the stress time was set to 3000 s, at which degradations were noticeable for all combinations of the operation mode and stress configurations. The stress voltages were set by finding the maximum voltage under which devices survived for both FM and IM. For the active-bias and off-state conditions, V_{CE} was swept with a 0.1 V step, whereas in the diode-connection condition, V_{CE} (=V_{BE}) was swept with a 0.04 V step. From the measured Gummel, degradation characteristics of devices were compared and major device parameters such as current gain and transconductance were extracted for a performance analysis.

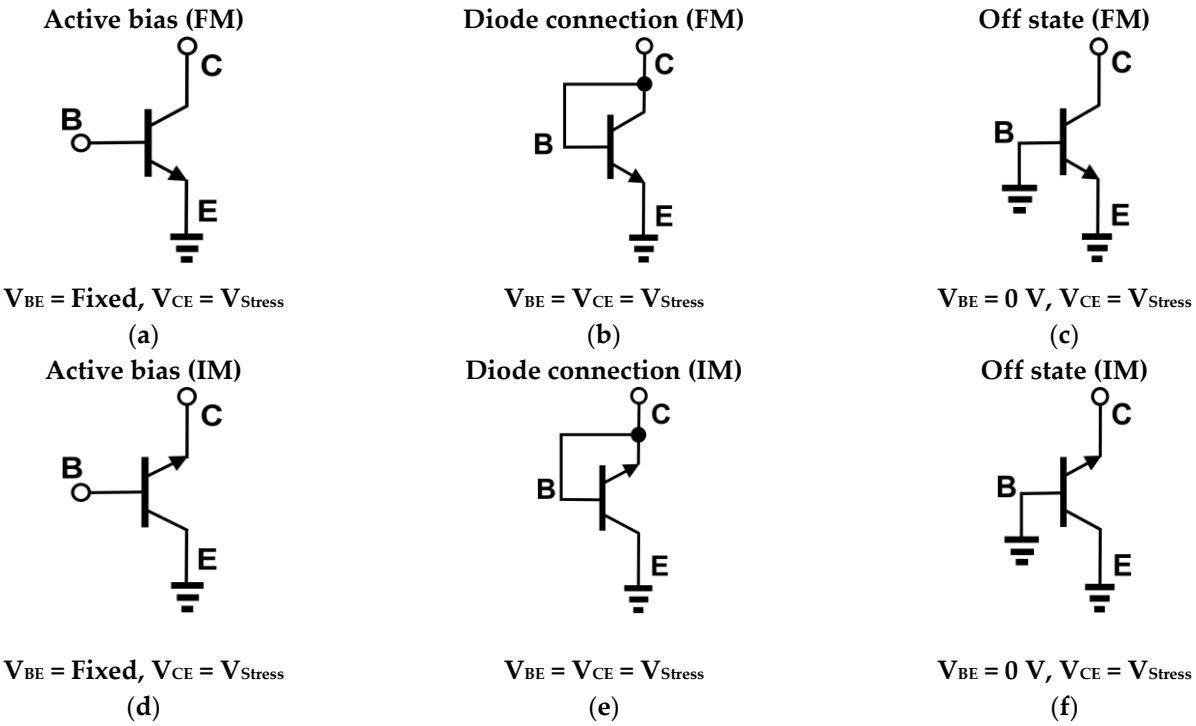
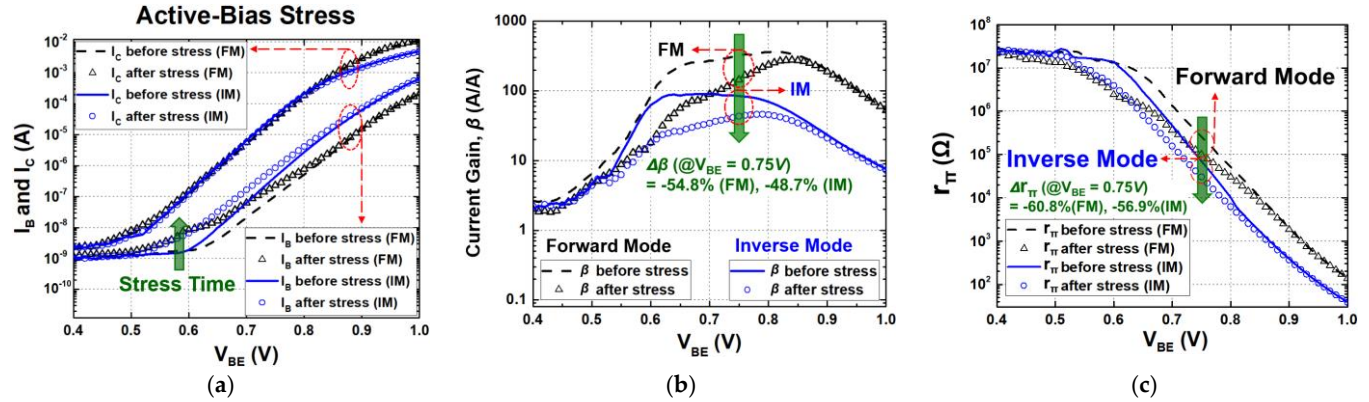


Figure 1. Stress conditions of a SiGe HBT in forward mode (**a**–**c**), and inverse mode (IM) (**d**–**f**). For an IM SiGe HBT, terminal names of C and E denote an electrical collector and an electrical emitter, respectively.

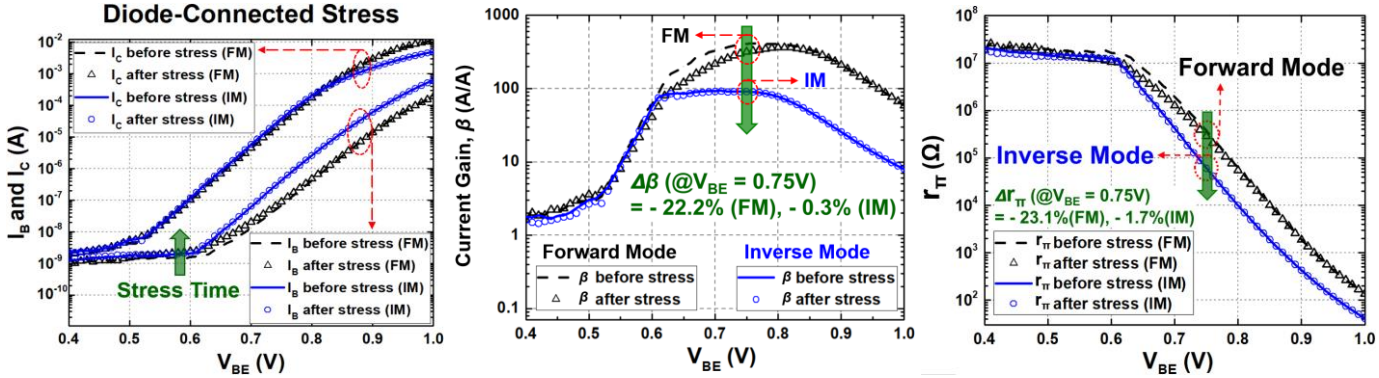
3. Experimental Results

The overall transistor characteristics under each stress condition (active bias, diode connection, and off state) are shown in Figures 2–4, respectively. The degradations in the electrical collector current (I_C) and the base current (I_B) of a SiGe HBT were measured for both FM and IM before and after 3000 s of stress time. As shown in Figures 2a, 3a and 4a, the changes in I_C were much less than those of I_B in general. Because of an increase in I_B, current gain (β) reduces over stress and the degradations are severe when V_{BE} is below approximately 0.8 V, whereas moderate or negligible deviations were observed with high V_{BE} [3,26,27].



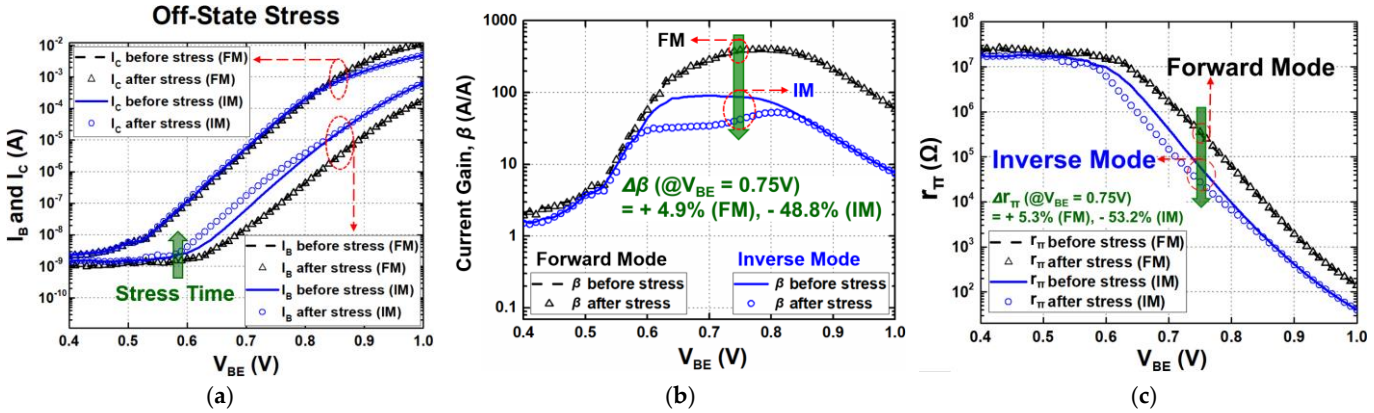
(**a**) (**b**) (**c**)

Figure 2. (**a**) Gummel plot (I_C and I_B versus V_{BE}); (**b**) degradation of current gain (β); (**c**) base-to-emitter resistance (r_π) degradation under active-bias stress condition.



(**a**) (**b**) (**c**)

Figure 3. (**a**) Gummel plot (I_C and I_B versus V_{BE}); (**b**) degradation of current gain (β); (**c**) base-to-emitter resistance (r_π) degradation under diode-connection stress condition.



(**a**) (**b**) (**c**)

Figure 4. (**a**) Gummel plot (I_C and I_B versus V_{BE}); (**b**) degradation of current gain (β); (**c**) base-to-emitter resistance (r_π) degradation under off-state stress condition.

To understand the degradation mechanism of SiGe HBTs by electrical stress, it is necessary to investigate hot carriers and the avalanche effect. The formation of hot carriers in the CB depletion of SiGe HBTs is triggered by the high reverse bias CB voltage (V_{CB}), which generates a high electric field and results in the generation of high-energy hot carriers within the emitter–base (EB) spacer [26–29]. These minority carriers at the base shift toward the collector–base (CB) depletion region due to the high CB voltage (and electric field). When a hot carrier with sufficient energy reaches the oxide, it can form a trap at the emitter–base (EB) spacer and shallow trench isolation (STI) oxide interface

through impact ionization and cause the avalanche effect [26–30]. In the literature, device breakdown is characterized with the collector–emitter breakdown voltage with an open base (BV_{CEO}) and the base–collector breakdown voltage with an open emitter (BV_{CBO}), which are commonly used to determine the operating limits of SiGe HBTs [26,30–33]. For example, BV_{CEO} can be obtained by measuring the I_C when I_B is zero and is the point at which base current reversal (BCR) begins during the forward-active operation. Therefore, if V_{CE} is greater than BV_{CEO}, device breakdown is triggered by multiple carriers, which leads to a significant increase in current via positive feedback [34].

An increase in the base current of a SiGe HBT by sufficient V_{CE} can be modeled with the avalanche effect and it can be expressed as follows [35].

$$I_B = \frac{I_{C,0}}{\beta_0} \times e^{\frac{V_{be}}{V_T}} - (M-1)I_{C,0} \times e^{\frac{V_{be}}{V_T}} \quad (1)$$

In (1), $I_{C,0}$ is the collector current before stress, V_T is the thermal voltage, β_0 is the DC current gain, and M is the avalanche-current multiplication factor. With a fitting parameter n, M is written below.

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n} \quad (2)$$

BV_{CBO} is typically a few times larger than BV_{CEO} and BV_{CEO} can be written as follows [35].

$$BV_{CEO} = V_{BE} + \frac{BV_{CBO}}{\sqrt[n]{\beta_0 + 1}} \quad (3)$$

Based on the above equations, degradations in the base current due to the avalanche effects can be further analyzed along with physics-based device simulations.

The non-ideal base current increases with the stress voltage. Consequently, the current gain is reduced by the leakage current at the base, which eventually degrades the circuit/system performance [36–38]. Whereas the key mechanism of degradation is related to hot carriers in a SiGe HBT, however, the electrical configuration of a device in a circuit leads to different performance changes. In a variety of analog applications, a SiGe HBT is under and among an active bias, diode connection, and off state, which will not present the same degradation characteristics between FM and IM. Therefore, for circuits with IM SiGe HBTs, it is pivotal to understand device characteristics under each stress condition for predicting long-term reliability issues in the design phase and dealing with potential performance loss.

In the active-bias configuration, the stress voltage was applied by keeping the electrical EB junction forward-biased and the electrical CB junction reverse-biased (Figure 1a,d). Here, the applied stress (V_{CE}) was 2.7 V, and the total stress time was 3000 s. As shown in Figure 2a, I_B increased due to trap generation as the stress was accumulated, whereas the changes in I_C were much less. Similar degradation trends were observed in both FM and IM operation, but FM was more susceptible to the stress. This is because unlike FM, the STI oxide in IM has fewer mid-gap states, so the increase in the base current is lower [15–17]. Moreover, the STI oxide interface is located further away from the EB depletion region at the neutral base [15,16]. In addition, the STI oxide in IM is already highly defective, which helps to limit the increase in the base current. The peak I_B increase was 121% and 95.1% with an electrical V_{BE} of 0.75 V in FM and IM, respectively.

Regarding the device performance of a SiGe HBT, current gain (β) versus V_{BE} before and after the active-bias stress is presented in Figure 2b. As implied from Figure 2b, β started to degrade when V_{BE} is below about 0.9 V. The largest reductions were observed when V_{BE} was at about 0.6–0.7 V and comparable degradations occurred in both FM and IM. These characteristics show that SiGe HBTs may suffer from potential performance loss under the active-bias stress if they operate in low-power applications. In these applications, typical V_{BE} ranges will be at around 0.75 V or less to provide moderate gain and low bias currents [19,31,39]. Specifically, under this bias voltage, the current gain was degraded by

54.8% and 48.7% in FM and IM operations, respectively, limiting the lifetime of the devices. In the aspect of device modeling, the base-to-emitter resistance (r_π) versus V_{BE} is shown in Figure 2c. Like current gain in Figure 2b, r_π exhibits more degradation in the lower-V_{BE} region ($V_{BE} < 0.7$). After 3000 s of stress, r_π was reduced by 60.8% and 56.9% for FM and IM, respectively. These degraded resistances along with transconductance (g_m) will be used in the small-signal model to predict circuit performance over stress in the next section. In summary, the degradations in device characteristics are severe in both FM and IM, but the degree of changes is less in IM than those in FM. With negligible degradations in I_C, the increase in I_B is lower by 25.9% in IM than in FM, and consequently, β and r_π degrade by 6.1% and 3.9% less in IM, respectively.

In the case of diode-connection stress, the base and the collector terminals were tied together as a diode-connected device, and then, the same stress voltage was applied (Figure 1b,e). The base and the collector currents were measured for the stress time up to 3000 s and the applied stress voltages of V_{BE} (=V_{CE}) were set to 1.22 V. In Figure 3a, similar to the active-bias condition, I_B increases as the stress accumulates, indicating that the stress voltage causes interface traps to form at the EB spacer oxide and STI edges [13–15,26–29]. Whereas the overall degradation was reduced in comparison with the active-bias stress, it is shown that there are relatively large variations in FM and little variations in IM. The former and the latter exhibit an increase in I_B by 30.13% and 1.73% in FM and IM, respectively, under the bias point with V_{BE} of 0.75 V. Since in diode-connection configuration, electrical base and collector terminals have the same voltage, the number of generated hot carriers is reduced due to the low avalanche effect, causing a small number of traps in the oxide layer. On the other hand, in IM, the STI region is less affected than the spacer in FM, leading to the better response in IM. After applying the stress voltage for 3000 s, the degradation of β is shown in Figure 3b. β decreases by 22.2% and 0.3% in FM and IM, respectively. And r_π shows a degradation of 23.1% and 1.7% in FM and IM, respectively (Figure 3c). Whereas the overall degradation for FM was less than the active-bias case, however, the reduction in β exceeds 10%, which may limit the lifetime of a given device. For IM, however, the decrease was 0.3% and 1.7%, respectively, which implies that an IM SiGe HBT can remain within a usable range of the lifetime in terms of long-term reliability [30].

In the off-state stress configuration, the base terminal was grounded, while the stress voltage is applied only to the electrical collector (Figure 1c,f). Stress time was the same as in the previous cases and the applied stress voltages were set to turn off the device; V_{BE} and V_{CE} were 0 V and 3.6 V, respectively. In contrast to the other stress conditions, it shows a little degradation in I_B in FM, but a significant increase in IM (Figure 4a). An increase of −4.9% and 113.2% was observed in FM and IM with a V_{BE} of 0.75 V, respectively. The small degradation in FM implies that the EB spacer is not introduced to additional traps. On the other hand, in IM, a high electric field applied across the EB junction leads to damages, and consequently, a leakage current due to breakdown effects. Figure 4b shows β versus V_{BE} before and after stress. It reads a 4.9% increase in FM and a 51.2% decrease in IM, which can be implied from the Gummel response. As shown in Figure 4c, r_π increases by 5.3% in FM, but decreases by 53.2% in IM after 3000 s of voltage stress. Since there were little changes in I_B under FM, the resulting decrease in r_π and β was negligibly small. It showed that a variation in current gain was 4.9% under the bias of V_{BE} = 750 mV after 3000 s of stress, which is within the boundary of 10% reduction in terms of device lifetime. In contrast to the previous active-bias and diode-connection conditions, the off state showed a worse degradation in IM. This shows that the off state is significantly affected by electrical stress in IM.

Figure 5 shows g_m vs. V_{BE} of SiGe HBTs in FM and IM. For all stress conditions, degradations in I_C between the fresh and the stressed cases were much less than those of I_B. Since g_m is, by definition, a partial derivative of I_C with respect to V_{BE}, it will present as almost similar g_m as long as I_C does not change much. From the stress experiment, all three stress cases of FM and the diode-connection and off-state conditions of IM exhibited little deviations in g_m (less than about 7%) from the fresh states, whereas the active-bias

condition of IM showed a slight increase by about 15%, depending on the bias voltage. For simplicity, a full-scale and a zoomed-in response of g_m under the active-bias condition only is plotted in Figure 5. Despite the fact that these deviations seem small, they can directly affect circuit performance numbers especially in a voltage-driven amplifier. More details will be discussed in Section 4.

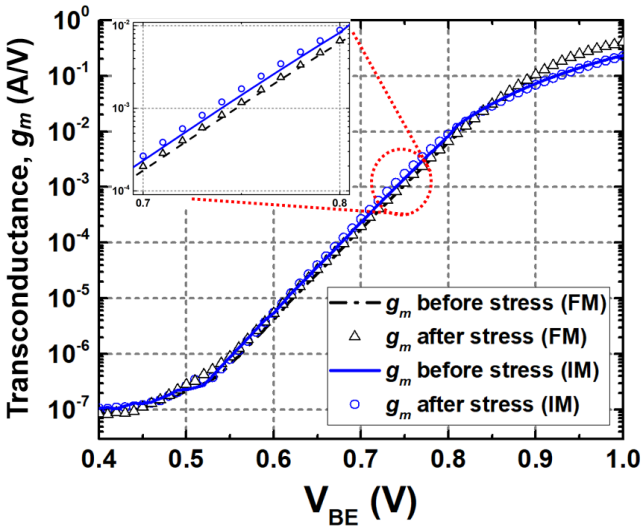


Figure 5. Transconductance (g_m) before and after stress under active-bias condition in FM and IM.

Based on the degradation experiments, it is concluded that electrical stress leads to an increase in I_B of a SiGe HBT in general, thereby affecting device parameters such as β and r_π. Depending on the stress configurations (active bias, diode connection, and off state) and operation mode (FM or IM), the degradation characteristics are different. From the device structure, the EB spacer and STI oxide are the main components that receive damages such as the generation of traps and mid-gap states. Increased reverse bias at the electrical CB junction causes impact ionization, which leads to the formation of energy carriers that can migrate to the EB spacer and STI oxide interface. As a result, these high-energy carriers create traps that lead to base current degradation, damaging the interface and shortening the device lifetime. The generation rates of hot electrons and hot holes at the STI interface are typically much higher than at the EB spacer interface. This results in higher trap density along the STI, indicating that more severe degradation is caused for FM than IM under stress, as shown in the Gummel characteristics before and after stress in Figure 6 [13–19]. The highly doped emitter (electric collector) in IM modulates the neutral base width more than FM, so there is less of an avalanche effect to form hot carriers. Therefore, there is a reduced number of hot carriers generated at the electrical CB junction in IM. With a lesser number of traps, the leakage current from the base is reduced, as shown in the Gummel characteristics of FM and IM under active-bias and diode-connection stress conditions in Figure 6 [15,40–42]. In contrast to active-bias and diode-connection stress conditions, off-state stress conditions show greater degradation in IM. This can be expected due to the higher doping concentration of the electrical collector in the presence of high collector–base voltage, which leads to a breakdown effect that does not occur in FM, resulting in the appearance of a leakage current at the base.

The overall device characteristics under three stress conditions in FM are summarized in Table 1. Three important parameters of a SiGe HBT including current gain, transconductance, and base-to-emitter resistance show different degradation results. Under the active-bias case, reductions were the most severe, showing a degradation in β more than 50%. It implies that normal operation as an amplifier would be significantly affected in terms of performance. On the other hand, the off-state configuration resulted in the least degradation. Thus, it is a good approach to ground the base terminal of a SiGe-HBT amplifier to minimize or avoid stress while it is not in operation. Table 2 shows the device

characteristics under the three stress conditions in IM. The degradation characteristics are better in IM than FM in the active-bias and diode-connection configurations. Unlike these two states, in the off state, we can see that the degradation is greater in the IM than in the FM under electrical stress conditions, especially in the case of β, where the degradation characteristic is 51.2% in IM compared to 4.9% in FM, which is outside the degradation limit of 10% in IM. Therefore, it may be a good alternative to avoid the off-state configuration when using SiGe-HBT amplifiers as IM. Lastly, it is worth presenting the device degradations versus the collector current because bipolar transistors and circuits are fundamentally biased via I_C. Figure 7 shows β versus I_C for the three stress states; Figures 7a, 7b and 7c illustrate the degradation characteristics of β under active-bias stress, diode-connected stress, and off-state stress conditions, respectively.

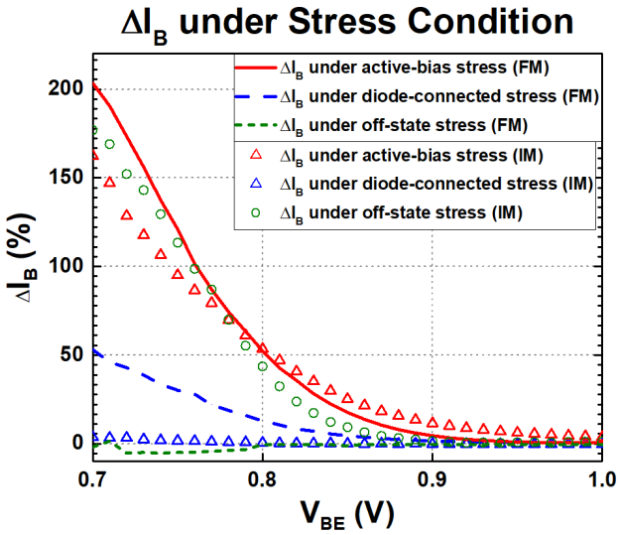


Figure 6. Changes in I_B under three stress conditions of FM and IM SiGe HBTs before and after stress.

Table 1. Degradation of FM SiGe HBTs under each stress (3000 s).

Degradations in Parameter	Active Bias	Diode Connection	Off State
Average $\Delta\beta$ (%) [0.6 V $\leq V_{BE} \leq$ 0.9 V]	−47.89	−21.15	+0.96
Average Δg_m (%) [0.6 V $\leq V_{BE} \leq$ 0.9 V]	+11.97	+1.38	+0.46
Average Δr_π (%) [0.6 V $\leq V_{BE} \leq$ 0.9 V]	−53.46	−22.16	+1.48
$\Delta\beta$ (%) [V_{BE} = 0.75 V]	−54.75	−22.23	+4.88
Δg_m (%) [V_{BE} = 0.75 V]	+6.8	+1.14	+0.47
Δr_π (%) [V_{BE} = 0.75 V]	−60.82	−23.14	+5.25

Table 2. Degradation of IM SiGe HBTs under each stress (3000 s).

Degradations in Parameter	Active Bias	Diode Connection	Off State
Average $\Delta\beta$ (%) [0.6 V $\leq V_{BE} \leq$ 0.9 V]	−45.94	−1.11	−37.16
Average Δg_m (%) [0.6 V $\leq V_{BE} \leq$ 0.9 V]	+5.17	+1.21	−8.52
Average Δr_π (%) [0.6 V $\leq V_{BE} \leq$ 0.9 V]	−46.93	−2.27	−39.75
$\Delta\beta$ (%) [V_{BE} = 0.75 V]	−48.73	−0.30	−51.20
Δg_m (%) [V_{BE} = 0.75 V]	+15.70	+1.25	+3.52
Δr_π (%) [V_{BE} = 0.75 V]	−56.89	−1.70	−53.21

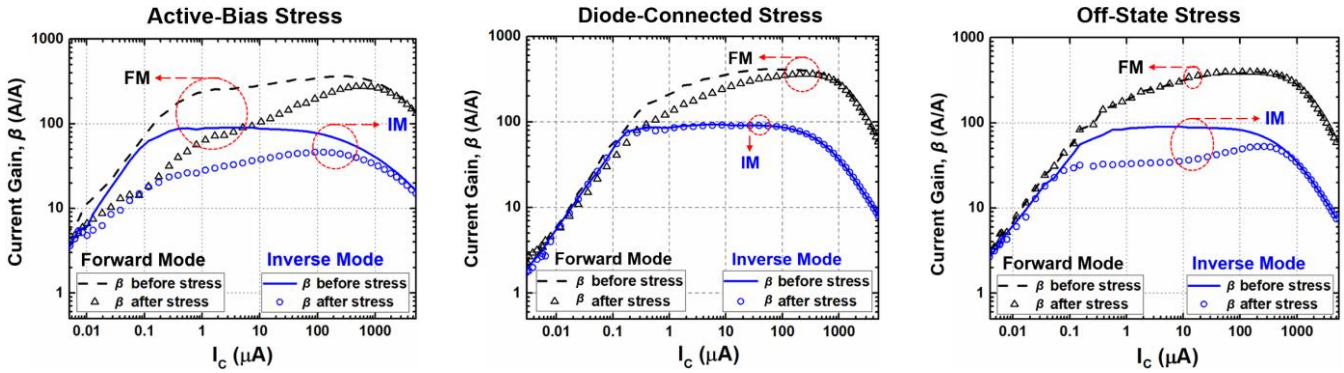


Figure 7. Degradations in current gain (β) versus I_C under (**a**) active-bias, (**b**) diode-connected, and (**c**) off-state stress conditions.

4. Simulation of Circuit-Level Degradation

In order to study the aging effect of SiGe HBTs in a circuit, a SiGe-HBT-based transimpedance amplifier (TIA), which accepts a current input and generates a voltage output, and a SiGe-HBT voltage amplifier, which accepts a voltage input and generates a voltage output, were designed. The performances of amplifiers were evaluated with the small-signal models and process-design-kit models. On the left side of Figure 8, the upper and lower red boxes denote TIA and voltage amplifier configurations, respectively, whereas on the right side, the blue boxes show potential stress conditions. For normal operation, it is biased in the safe operation area (SOA) with a power supply (V_{CC}) of 1.8 V and a load resistance of 20 kΩ. On the other hand, when under stress situations, V_{CC} is assumed to be raised up to 3.6 V.

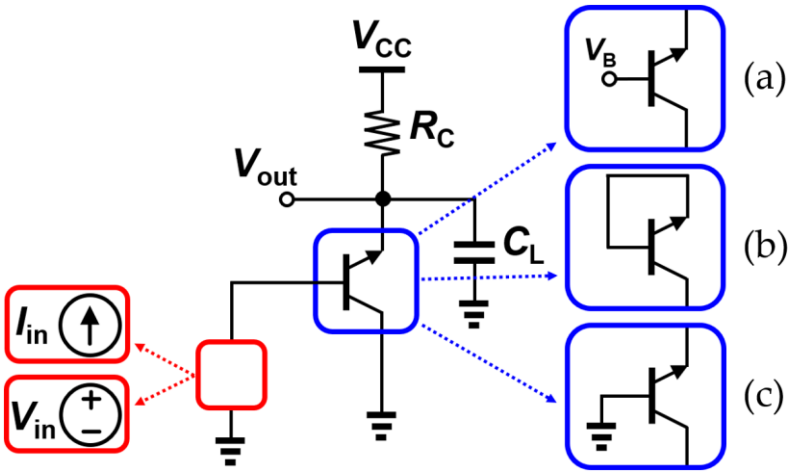


Figure 8. Basic schematic of TIA or voltage amplifier under (**a**) active-bias; (**b**) diode-connection; and (**c**) off-state conditions. Red boxes show types of signal sources and blue boxes show possible types of stress.

In this situation, the transistors are under the same stress conditions as in the previous section. Figure 8a represents a typical common emitter (CE) amplifier that undergoes large V_{CB} stress, whereas Figure 8b shows that diode-connection stress is biased in a way such that V_{BE} and V_{CE} are matched under a 3.6 V power supply. Lastly, in the off-state stress condition, the based terminal is grounded, resulting in no I_C and having V_{CE} the same as the stress voltage, as shown in Figure 8c. Using the degraded small-signal parameters from different stress conditions, as investigated in Section 3, the small-signal performance under normal operation was re-simulated and compared with the initial performance. The

device parameters used in the circuit are given in Tables 3 and 4. They show the initial and degraded values of g_m, r_π, and the early voltage (V_A) with stress, which was used to investigate the effect of stress on the circuit performance. The early effect (or the base-width modulation) of each device was included in the performance analysis. In addition, a load capacitance of 100 fF attached in parallel at the output node to represent a potential input impedance of a subsequent stage. For simple AC modeling, the base-to-emitter, base-to-collector (C_{BC}), and collector-to-emitter (C_{CE}) capacitances are extracted from the design kit model. Since it has been reported in the literature that the variations in device capacitance due to DC stress are almost negligible (less than 5%) [31,43], constant values were assumed in the following simulations.

Table 3. Parameter values of FM SiGe HBTs used in the amplifier.

Device Stress Conditions		g_m (mS)	r_π (kΩ)	V_A (V)
Active bias	Before stress	220	1.10	36.65
	After stress	99.9	1.16	34.09
Diode connection	Before stress	220	1.10	36.65
	After stress	169	1.11	36.21
Off state	Before stress	220	1.10	36.65
	After stress	232	1.09	36.52

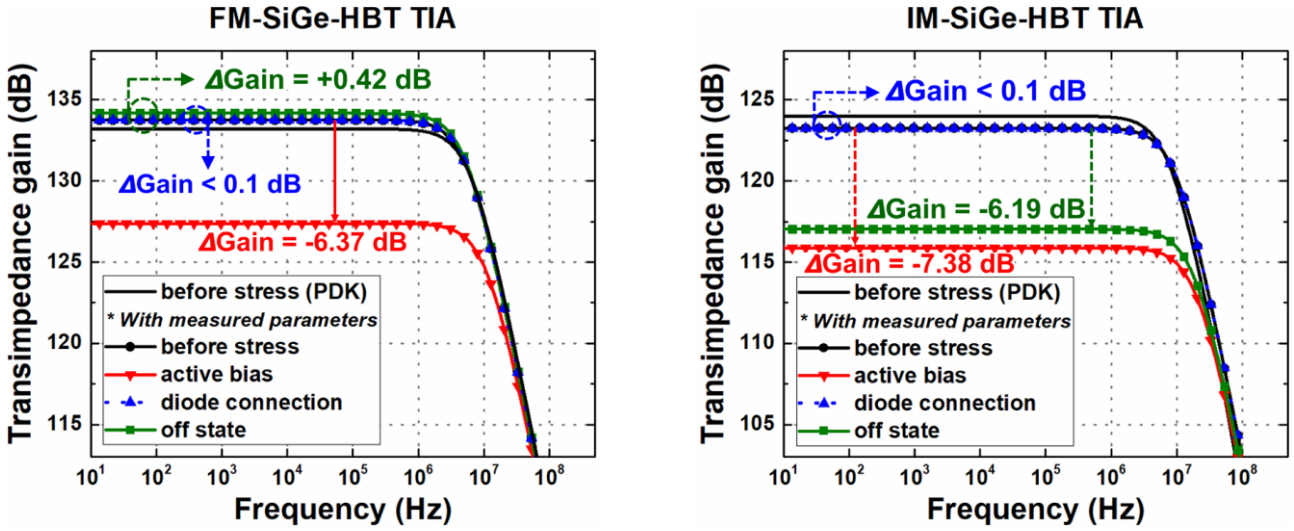
Table 4. Parameter values of IM SiGe HBTs used in the amplifier.

Device Stress Conditions		g_m (mS)	r_π (kΩ)	V_A (V)
Active bias	Before stress	60	1.50	1.72
	After stress	28.9	1.33	1.72
Diode connection	Before stress	60	1.50	1.72
	After stress	59.7	1.50	1.68
Off state	Before stress	60	1.50	1.72
	After stress	28.3	1.55	1.64

The Bode plot of each stress condition in FM is shown in Figure 9a along with the pre-stress response. For a verification purpose, the results from the PDK models were simulated with Cadence Virtuoso [44] for a pre-stress condition and the overall differences were within only 1~2 dB. As discussed in Section 3, the stress-induced variations in base-to-emitter resistance (r_π) and transconductance (g_m) have different degradation characteristics for each state. In the active-bias stress, there were little variations in g_m but a large degradation in r_π, which implies that the gain will vary because the voltage applied between the base and the emitter (or simply, across r_π) will be reduced. The overall degradation in TIA gain was the worst among three cases, exhibiting a reduction of about 6.4 dB. With regard to amplifier bandwidth, it is shown that the location of the dominant pole (at the output) is shifted toward a higher frequency, slightly increasing the bandwidth. This is due to the presence of the internal feedback capacitor C_{BC}.

In contrast, the other two stress cases did not show significant changes in TIA gain and bandwidth. Regarding the diode-connection stress case, one thing to note is that when the V_{CC} is raised to 3.6 V, the effective bias applied at the base and collector node is about 0.8 V, which indicates that the device is still in the safe operation area (SOA). From the device test, it was verified that there was no noticeable degradation under this bias condition. Therefore, in the amplifier configuration, the performance variations are negligible. Lastly, in the off-state stress, the degradations in r_π and g_m result in a gain increase of 0.4 dB, which is attributed to a small increase in r_π (see Figure 9a). In Figure 9b, before- and after-stress results in the IM TIA are shown. Similarly to the FM TIA case, it exhibits large degradation in the active-bias stress conditions and negligible changes in the diode connection in terms of gain and bandwidth. For the off-state stress, however, performance degradations were

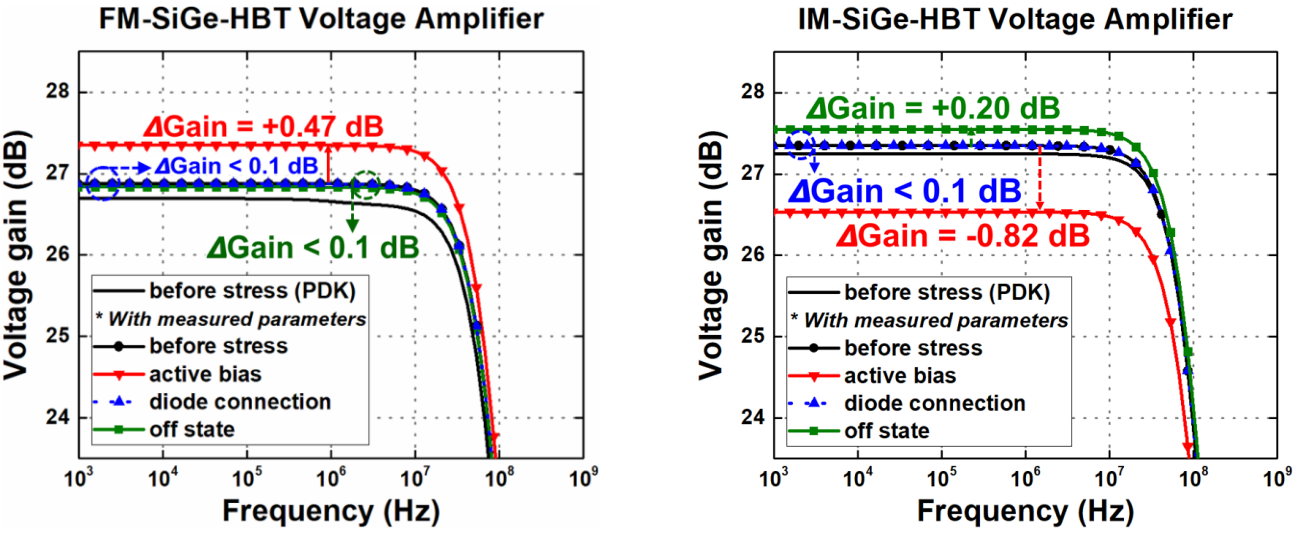
severe and close to those of the active-bias case, meaning that the IM operation may present long-term reliability risk, as implied from Table 2.



(**a**) (**b**)

Figure 9. Bode plot of TIA gain under three stress conditions of (**a**) FM; and (**b**) IM (after 3000 s of stress).

In Figure 10, the Bode plots of the FM and IM SiGe-HBT voltage amplifiers are shown. In this amplifier configuration, the gain of the circuit is now directly dependent on g_m and is not affected by the variations in r_π, presenting similar trends to the characteristics of g_m under the three stress conditions extracted in Section 3. The FM voltage amplifier showed an increase of 0.47 dB and 0.04 dB in the active-bias and off-state conditions, respectively. In the IM case, it showed a decrease of 0.82 dB and an increase of 0.2 dB in the active-bias and off-state conditions, respectively. Lastly, both the FM and IM voltage amplifiers exhibited no degradation in the diode-connection stress. It is interesting to observe that the voltage amplifier shows a relatively minor change in performance for the given stress time, compared with the TIA. This implies that the SiGe HBTs will present more robust operation if they are driven by input voltages rather than input currents.



(**a**) (**b**)

Figure 10. Bode plot of voltage amplifier gain under three stress conditions of (**a**) FM; and (**b**) IM (after 3000 s of stress).

Tables 5 and 6 summarize the degradation characteristics of the circuits under investigation in terms of gain and bandwidth. From Table 5, the gain of the FM SiGe-HBT TIA under the active-bias stress was the most sensitive, whereas the diode-connection and the off-state stress cases do not lead to significant performance degradations. When it comes to the IM operation, SiGe-HBT TIA showed the least degradation under the diode connection, whereas the active bias and off state showed similar degradation to the FM counterparts. Investigations at the device and circuit levels provide insight into the degradation characteristics of SiGe HBTs in the three stress conditions and the impact of the degradation characteristics in circuit performance. Therefore, it can be expected that degradation at the system level can be predicted in advance, thereby reducing the stress-induced degradation of the circuit and analyzing for a potential lifetime improvement of the circuit. First, when the circuit is in a non-operational state, biasing it in active-bias conditions can lead to unwanted degradation. Second, if the device is not in use, it can be biased in the off state in FM. On the other hand, when IM is used, putting it in the off-state condition will degrade the device performance. Thus, it is safe for IM SiGe HBTs to be in the diode connection for better long-term reliability as long as power consumption is acceptable. As shown in Table 6, the degree of degradations is much less in a voltage amplifier configuration. Since this is partly due to the circuit configuration where the input signal does not see the variations in r_π, a more in-depth analysis is necessary for different input signal networks even if a voltage is used. In short, these results can be utilized in an early-phase reliability analysis of SiGe-based circuits and systems. In addition, by understanding the different characteristics of FM and IM, better design and optimization can be conducted.

Table 5. Predicted changes in gain and bandwidth of a TIA.

Device Stress Conditions		Forward Mode	Inverse Mode
Active bias	ΔGain (dB)	−6.37	−7.38
	ΔBW (%)	+95.49	+88.5
Diode connection	ΔGain (dB)	- *	- *
	ΔBW (%)	- *	- *
Off state	ΔGain (dB)	+0.42	−6.22
	ΔBW (%)	−4.41	+73.44

*: No degradation observed.

Table 6. Predicted changes in gain and bandwidth of a voltage amplifier.

Device Stress Conditions		Forward Mode	Inverse Mode
Active bias	ΔGain (dB)	+0.47	−1.06
	ΔBW (%)	−0.007	+0.023
Diode connection	ΔGain (dB)	- *	- *
	ΔBW (%)	- *	- *
Off state	ΔGain (dB)	+0.04	+0.30
	ΔBW (%)	-	−0.007

*: No degradation observed.

5. Summary

Investigations on SiGe-HBT reliability have been conducted on both device- and circuit-level operations. Degradation characteristics of a SiGe HBT were monitored in three different stress conditions: forward bias, diode connection, and off state. For each case, current gain, transconductance, and base-to-emitter resistance were extracted for forward- and inverse-mode operations. Based on the degradation results, performance changes in SiGe-HBT TIAs and voltage amplifiers have been investigated, using small-signal models and analyses. In terms of amplifier gain and bandwidth, the variations in amplifier performance have been compared and it shows a close relationship with device

degradation characteristics. The findings of this work will be useful for various SiGe-HBT circuit and system applications.

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