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Switching Device Dead Time Optimization of Resonant Double-Sided LCC Wireless Charging System for Electric Vehicles

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Abstract: Aiming at the reduction of the influence of the dead time setting on power level and efficiency of the inverter of double-sided LCC resonant wireless power transfer (WPT) system, a dead time soft switching optimization method for metal–oxide–semiconductor field-effect transistor (MOSFET) is proposed. At first, the mathematic description of double-sided LCC resonant wireless charging system is established, and the operating mode is analyzed as well, deducing the quantitative characteristic that the secondary side compensation capacitor C_2 can be adjusted to ensure that the circuit is inductive. A dead time optimization design method is proposed, contributing to achieving zero-voltage switching (ZVS) of the inverter, which is closely related to the performance of the WPT system. In the end, a prototype is built. The experimental results verify that dead time calculated by this optimized method can ensure the soft switching of the inverter MOSFET and promote the power and efficiency of the WPT.

Keywords: inverter; dead time; soft switching; resonant wireless charging; electric vehicles

1. Introduction

Electric vehicles (EVs) have gained popularity in recent years, for their inherent environmental benefits of reduced gas emissions [1,2]. Battery systems and charging techniques are the most critical technology supporting EV market penetration [3]. As a new wireless power transfer technology, the resonant wireless power transfer (WPT) technology, which is based on magnetic field coupling between the transmitting and receiving coils, has been seen development in recent years [4]. Compared with the traditional charging method (e.g., plug-in), the WPT technology eases drivers from the problem of cable-exposure, tripping hazards, and risks on the snowy or rainy days [5]. In addition, with the characteristics of flexible application, safety, and reliability, WPT technology has been applied to various applications, such as medical implantation equipment, underwater robots, and electric vehicle (EV) charging [6,7].

A typical EV WPT system consists of AC/DC (PFC and BUCK circuit), DC/AC (inverter circuit), resonant compensation network, transmitting coil and receiving coil, rectifier, and battery [8]. The inverter circuit is used to transfer DC power into high frequency square wave voltage, which is key for the compensation network to achieve resonance. This paper adopts a full-bridge inverter circuit to meet high power EV charging conditions. In the inverter, if the upper and lower leg of the MOSFET are switched on at the same time, it will lead to short circuit, once the input voltage is too

high, the MOSFET will be damaged. Therefore, it is required that a pair of the MOSFETs be switched on until another pair of MOSFETs are completely switched off, which means there should be dead-time between the drive signals.

Therefore, to improve the efficiency of the WPT system, it is necessary to adopt an optimal dead-time. Most previous work on the dead-time focused on the buck or boost circuit [9], all of which are required to sample the load current or voltage, increasing the complexity of control. Other work [10] has analyzed the relation between the optimal dead-time and turn-off related switching parameter, but it did not focus on the resonant compensation network. In [8], the double-sided LCC resonant compensation network and its tuning method was proposed, which realizes unity power factor at both the input and output. Moreover, tuning the secondary series capacitor C_2 provides the zero-voltage switching (ZVS) condition for the MOSFET of the inverter, however, the paper did not propose a specific dead-time design method. Therefore, in this paper, a dead-time design method is proposed, by tuning the secondary series capacitor C_2 to ensure the circuit is inductive. Considering the parasitic capacitor of the MOSFET, it is crucial to adopt the optimal dead-time to improve the power and efficiency of the WPT system. An inappropriate dead-time will lead to damage of MOSFETs.

In this paper, the dead-time optimization method of ZVS is studied in the double-sided LCC resonant compensation network. The mathematical equivalent model of the double-sided LCC resonant compensation network is established, and the relation between the equivalent impedance phase of the primary side and the incremental capacitance of the secondary side capacitor C_2 is obtained in Section 2. Section 3 analyzes the process of charge and discharge of the parasitic capacitor of the MOSFET in a switching period, then the influence of the dead-time on the soft-switching is discussed. In the case of fixed secondary series compensation capacitor C_2, the optimization method of the dead-time is proposed in Section 4. Experimental results verify the feasibility and correctness of the proposed method in Section 5. Finally, Section 6 concludes this paper.

2. Analysis of Double-Sided LCC Resonant Compensation Network Equivalent Characteristic

The configuration of the double-sided LCC resonant WPT system is shown in Figure 1. The inverter consists of four MOSFETs (S_1~S_4) and parasitic capacitors (C_{s1}~C_{s4}), parasitic antiparallel diodes (D_1~D_4). L_1 and L_2 are the self-inductances of the transmitting and receiving coils, respectively. L_p, C_p, and C_1 are the primary side compensation inductor and capacitors. Ls, Cs, and C_2 are the secondary side compensation components, the secondary side is symmetrical to the primary side. M is the coefficient inductance of the two main coils. The rectifier consists of fast recovery diodes (D_5~D_8), a filtering capacitor C_o, and a filtering inductor L_o.

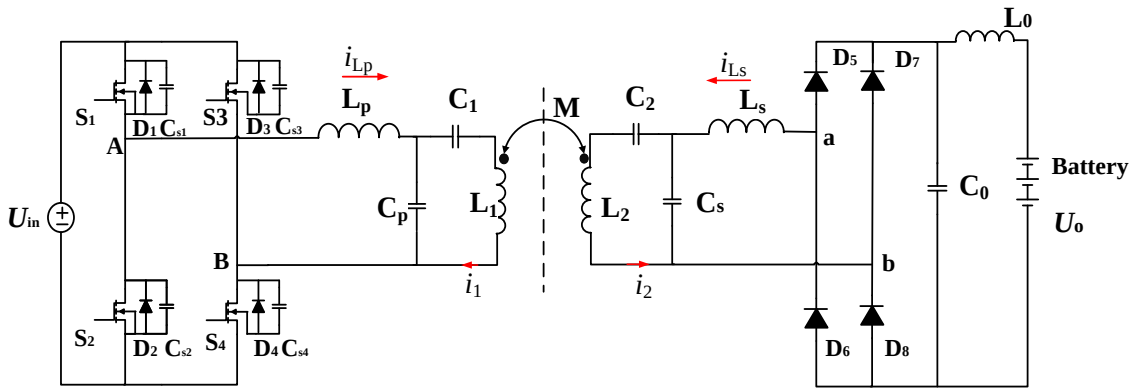

Figure 1. Schematic of double-sided LCC resonant compensation network.

For the convenience of analysis, the parasitic resistance of the capacitors, inductors, and coils are ignored. The primary and secondary resonant compensation equivalent network is shown in

Figure 2 [11]. Where $U_e = \frac{2\sqrt{2}}{\pi}U_o$. Where RL represents the equivalent impedance of the battery and rectifier. According to [8], the receiving terminal can realize the unity power factor, thus, the equivalent impedance can be represented as a pure resistance, defined as $R_L = \frac{\pi^2 {U_o}^2}{8P_{out}}$, P_{out} is the output power of the WPT system.

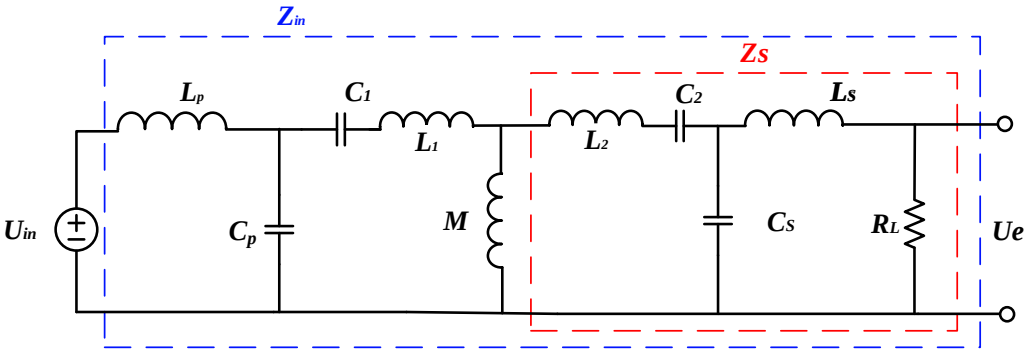

Figure 2. Equivalent schematic of double-sided LCC resonant compensation network.

The equivalent impedance of the secondary side circuit is

$$Z_s = \frac{(R_L + j\omega_0 L_s) \cdot \frac{1}{j\omega_0 C_s}}{R_L + j\omega_0 L_s + \frac{1}{j\omega_0 C_s}} + j\omega_0 L_2 + \frac{1}{j\omega_0 C_2} \tag{1}$$

where ω_0 is the resonant frequency.

The equivalent impedance of secondary side Z_r was reflected to the primary side by the mutual inductance M of the coils, Z_r is defined as

$$Z_r = \frac{{\omega_0}^2 M^2}{Z_s} \tag{2}$$

Therefore, the equivalent impedance of the primary side is defined as

$$\boldsymbol{Z_{in}} = \frac{(j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} + Z_r) \cdot \frac{1}{j\omega_0 C_p}}{j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} + Z_r + \frac{1}{j\omega_0 C_p}} + j\omega_0 L_p \tag{3}$$

According to [5], the parameters of double-sided LCC resonant compensation network are designed by the following equations

$$\begin{cases} L_p \cdot C_p = \frac{1}{\omega_0^2} \quad , \quad L_s \cdot C_s = \frac{1}{\omega_0^2} \ , \\ L_1 - L_p = \frac{1}{\omega_0^2 C_1} \ , \ L_2 - L_s = \frac{1}{\omega_0^2 C_2} \circ \end{cases} \tag{4}$$

Substitute (2) and (4) into (1) and (3), the equivalent impedance of the equivalent double-sided LCC compensation network is given by

$$\boldsymbol{Z_{in}} = \frac{{\omega_0}^2 L_p^2 L_s^2}{M^2 R_L} \tag{5}$$

It is a pure resistant load. In this case, the inverter output voltage is in phase with the output current, and unity power factor achieves, but it is not a suitable condition for MOSFETs to achieve ZVS. According to [8], by tuning the secondary series capacitor C_2, making the circuit be inductive and thus providing conditions for the MOSFET to achieve ZVS.

After tuning the C_2, the equivalent impedance of the primary side circuit is

$$Z'_{in} = R + jX \tag{6}$$

here ΔC_2 is the incremental value, $R = \frac{\omega_0{}^2 L_p^2 L_S^2}{M^2 R_L}$, $X = \frac{L_p^2}{\omega_0 M^2} \cdot \frac{\Delta C_2}{(C_2+\Delta C_2)C_2}$.

As is known, the ZVS condition mainly depends on the variation of load resistance and mutual inductance, in this paper, by using the equivalent resistance $\boldsymbol{Z_{in}}$, which relates to the load resistance R_L and mutual inductance M, as (5) and (6) shown above. It is a simple method to integrate various conditions into one variable.

3. Time Domain Analysis of the Double-Sided LCC Compensation Network

3.1. Time Domain Analysis of Switching Mode

To facilitate the analysis, the following assumptions are made [12]:

1. All the MOSFETs and diodes are ideal;
2. All the capacitors, inductors and coils are ideal;
3. $C_{s1} = C_{s2} = C_{s3} = C_{s4} = C_{oss}$, where C_{oss} is the output capacitor of the MOSFET;

Considering the dead-time, the main operating waveform is shown in Figure 3.

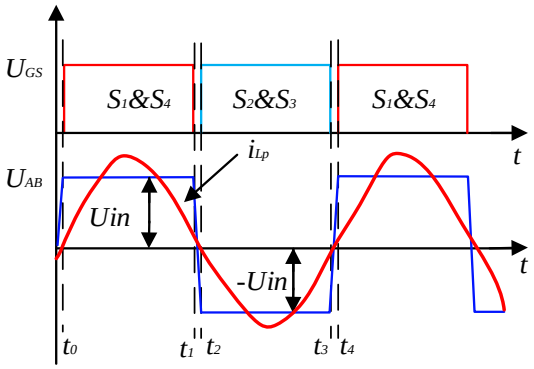

Figure 3. Operation waveform of the inverter.

A switching cycle can be divided into four stages. The first half switching cycle is analyzed.

Mode 1 (t_0, t_1): before the S_1 and S_4 are turned on, the inverter output current i_{Lp} is freewheeling through D_1 and D_4, C_{s1} and C_{s4} has been discharged to zero voltage. At the moment t_1, S_1, and S_4 achieve zero voltage turn-on. $U_{AB} = U_{in}$ at this time.

Mode 2 (t_1, t_2): at t_1, both the S_1 and S_4 are turned off, the inverter output current i_{Lp} (the instantaneous current when MOSFET turned off is called cut-off current) is charging the capacitor C_{s1} and C_{s4} to voltage U_{in}, while capacitors C_{s2} and C_{s3} are discharged to zero voltage.

The mode 3 and mode 4 are similar to mode 1 and mode 2, respectively. By tuning the capacitor C_2 and dead-time optimization, the turn-off current can be minimized and reduce the MOSFET turn-off loss.

3.2. The Influence of Dead-Time on Soft-Switching

From the above analysis, the inverter output current charges and discharges the parasitic capacitors of the MOSFET during the dead-time. If the dead-time is set inappropriately, it will lead to a lower transmitting power and efficiency. Therefore, the dead-time setting is crucial for MOSFET to achieve ZVS.

Take the left arm of the inverter as an example, if the dead-time is set too short, the S_1 will be turned on before the parasitic capacitor completely discharged, at the moment S_1 is turned on, the parasitic capacitor short-circuits and produces an impulse current on the MOSFET, if the impulse current is larger than the pulsed drain current of the MOSFET, the MOSFET will break down.

If the dead-time is set too long, when the parasitic capacitor C_1 has been discharged completely, while the S_1 do not be turned on, C_1 is involved in the circuit resonant, and to be charged again, making S_1 fail to achieve ZVS. It is found that there is a positive current on the S_1 before the S_1 is switched on, which will also produce an impulse current on the S_1.

4. Optimization Method of Dead-Time of Inverter MOSFET

According to the above analysis, to ensure MOSFETs achieve ZVS and reduce the switching loss, on the one hand, the dead-time should be large enough to charge or discharge both the MOSFET's and PCB's parasitic capacitor, on the other hand, it is required that the inverter current be close to zero at the switching point, which means the dead-time should smaller than the diode freewheeling time. Therefore, the dead-time is required to meet with the expression

$$t_c + t_{off} < t_{DT} < t_d$$

where t_c is the time of charging and discharging the parasitic capacitors, t_{off} is the turn-off time of MOSFET, and t_d is the diode freewheeling time.

4.1. Calculation of Parasitic Capacitor Charging Time

Since the time for charging and discharging the parasitic capacitor is relatively short compared to a switching period, the turn-off current I_{off} can be approximately regarded as constant. According to [13], the time of parasitic capacitor charging and discharging is defined as

$$t_c = (2C_{oss} + C_{stray})\frac{U_{in}}{I_{off}} \tag{7}$$

where C_{stray} is the parasitic capacitor of PCB.

Considering the high order harmonics of the square voltage [14], the inverter first order output current is defined as

$$I_{Lp\_1st} = \frac{\sqrt{2}U_{in}}{|Z'_{in}|}\sin(\omega t + \theta_{1st}) \tag{8}$$

where θ_{1st} is the phase angle of the first order input impedance. At the moment MOSFET is turned off, $t = \pi$, the first order turn-off current is

$$I_{off\_1st} = \sqrt{2}U_{in}\frac{X}{R^2 + X^2} \tag{9}$$

Similarly, the high order turn-off current is given by

$$I_{off\_(2k+1)th} \approx \frac{\sqrt{2}U_{in\_(2k+1)th}X_{(2k+1)th}}{R^2_{(2k+1)th} + X^2_{(2k+1)th}} \tag{10}$$

Therefore, the total turn-off current can be given by

$$\begin{aligned} I_{off} &= I_{off\_1st} + \sum_{k=1}^{\infty} I_{off\_(2k+1)th} \\ &= \frac{\sqrt{2}U_{in}X}{R^2+X^2} + \sum_{k=1}^{\infty}\frac{\sqrt{2}U_{in}}{2k+1}\frac{X_{(2k+1)th}}{R^2_{(2k+1)th}+X^2_{(2k+1)th}} \end{aligned} \tag{11}$$

4.2. Calculation of Diode Freewheeling Time

From the above analysis, at the end of the diode freewheeling, another pair MOSFETs should be turned on, which means when the equivalent inductor of the circuit was completely discharged, the inverter current should be zero [15]. In fact, by using MATLAB, according to (7), all the high order current lags behind the inverter output voltage U_{AB} by about 90°. Figure 4 shows the effect of the high order harmonic current on the inverter current.

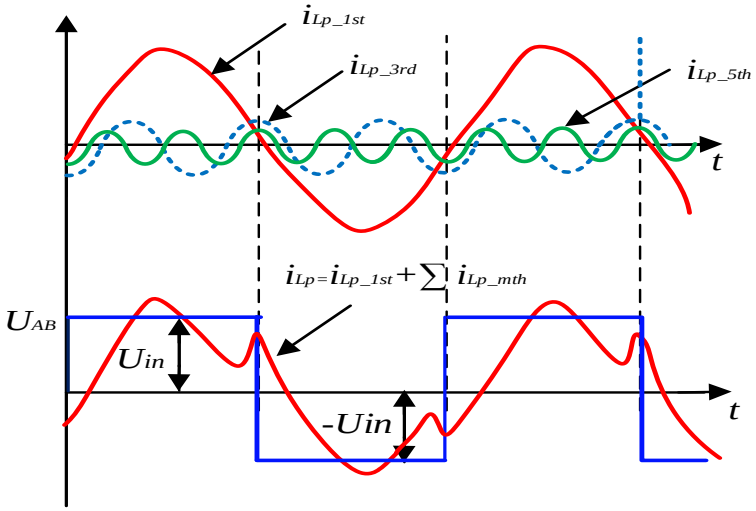

Figure 4. Effect of high order inverter current.

From Figure 4, it is found that the zero-crossing point of the inverter current is mainly decided by the third harmonic current. Thus, the dead-time roughly meets with the following expression

$$I_{Lp\_3rd} = \sqrt{2} I_{rms\_3rd} \sin(3\omega_0 t_d + \theta_{3rd}) \tag{12}$$

So the diode freewheeling time is given by

$$t_d = \frac{\theta_{3rd}}{360} \frac{1}{3f} \tag{13}$$

where f is the inverter switching frequency and θ_{3rd} is the phase angle of the third order input impedance.

5. Experiment Results

In order to validate the optimization method of dead time of switching devices in double-sided LCC resonant WPT system, a prototype is established, the experimental platform is shown in Figure 5.

The input voltage U_{in} = 100 V, output voltage U_o = 48 V, resonant frequency f = 95 kHz, the transfer gap h = 150 mm. The parameter of the double-sided LCC resonant WPT system are listed in Table 1.

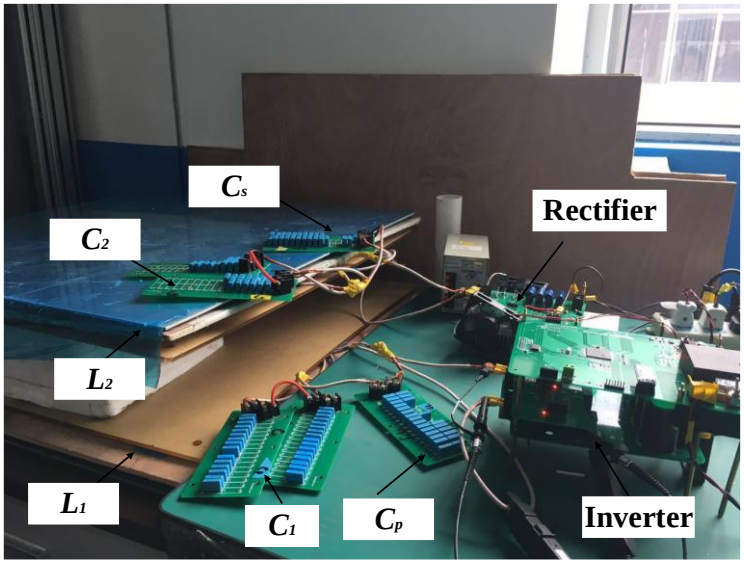

Figure 5. Experiment platform.

Table 1. Double-sided LCC resonant WPT system parameter.

Parameter	Value
Transmitting (receiving) coil $L_1(L_2)$/uH	260
Compensation inductor L_p, L_s/uH	66
Mutual inductor M/uH	67.6
Parallel capacitor C_p, C_s/nF	42.3
Primary series capacitor C_1/nF	14.4
Secondary series capacitor C_2/nF	15.4
Output equivalent resistance R_L/Ω	25.8

By increasing the capacity of C_2, the WPT system circuit is inductive, the specific capacity of C_2 can be set according to practical application, for convenience, in this paper we set ΔC_2 = 1 nF.

In this work, Infineon IPW60R070C6 CoolMOS MOSFET is chosen as the inverter switches, its turn-off time is 88 ns, output capacitor C_{oss} = 215 pF. From the above analysis and parameters, it can be calculated that the dead-time should meet with the expression:

$$325\,\text{ns} < t_{DT} < 875\,\text{ns} \tag{14}$$

Considering the increase of MOSFET temperature, which may lead to the increase of MOSFET turn-on and turn-off time, the optimal dead-time is set 500 ns.

Figure 6 shows the voltage and current of MOSFET when t_{DT} = 500 ns, t_{DT} = 1.2 us, respectively.

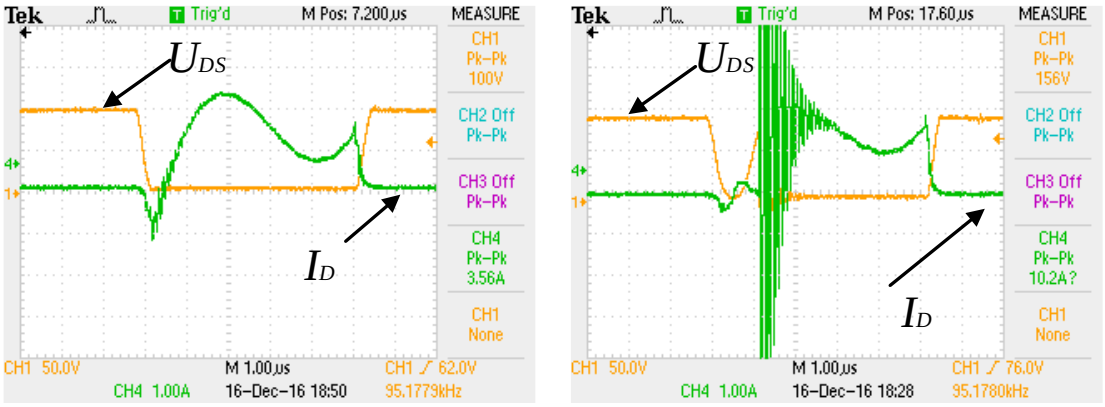

Figure 6. Voltage and current of MOSFET (**a**) t_{DT} = 500 ns; (**b**) t_{DT} = 1.2 us.

From Figure 6a, before MOSFET turned on, there is negative current on the MOSFET because of the diode freewheeling, when the drive voltage U_{GS} go rise to 90%, the MOSFET has forward current (I_D) and the MOSFET achieve zero voltage switch on. From Figure 6b, because of the long dead-time, before the MOSFET is turned on, there is positive current on the MOSFET, even after the MOSFET is turned off, the voltage of the switch drops sharply to zero.

Figure 7 shows the voltage and current of inverter when t_{DT} = 500 ns, t_{DT} = 1.2 us, respectively.

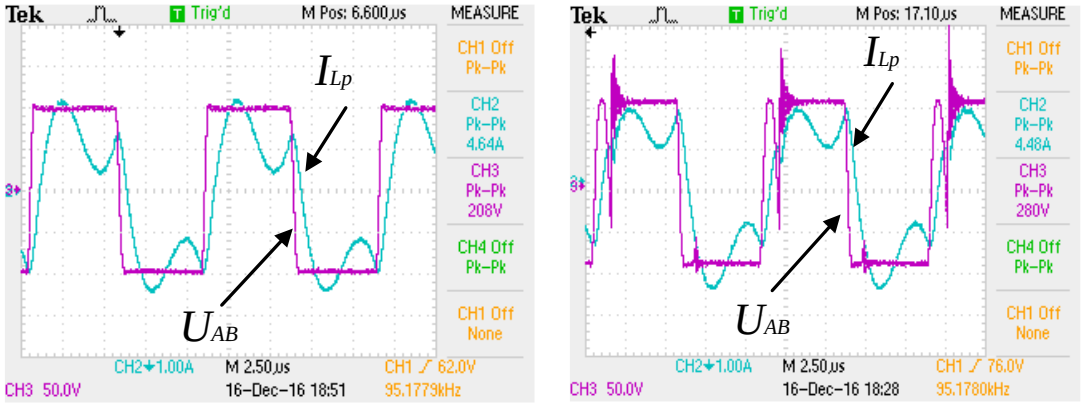

Figure 7. Voltage and current of inverter (**a**) t_{DT} = 500 ns; (**b**) t_{DT} = 1.2 us.

From Figure 7b, if the dead-time is too large, there is high frequency oscillation of the inverter. From the experimental results, a dead-time setting that is too short or too long will lead to distortion output voltage and current of the inverter, causing a lower efficiency and transmitting power of the WPT system.

It is known that the longer the dead time, the less effective value of the inverter voltage. When the input power is about 100 W, in Figure 8, the conduction loss of both the dead-time situations is about 0.02 W, much less than the switching loss. It also shows that the turning on/off loss is much smaller if the proper dead time is chosen. By selecting the optimal dead time, the MOSFETs can achieve ZVS and eliminate voltage and current distortion, promoting transmitting efficiency.

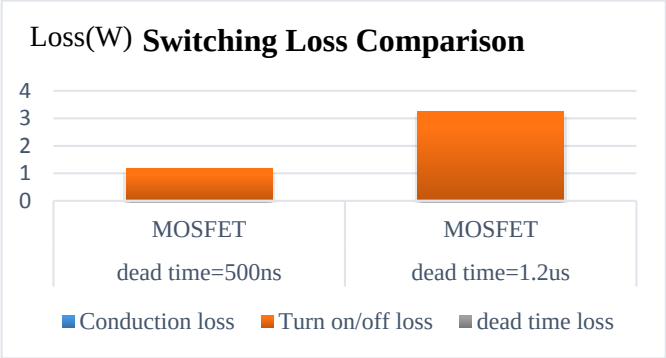

Figure 8. Switching loss comparison.

6. Conclusions

In this paper, the problem of soft-switching of the MOSFET in the double-sided LCC resonant WPT system is studied and analyzed. Based on the theoretical calculation of the equivalent impedance, the condition of MOSFET to achieve ZVS is verified. By analyzing the time-domain model of a switching period, the influence of dead-time on MOSFET is studied. Finally, an optimization of switching device dead-time of double-sided LCC WPT system is proposed. The feasibility of this method is verified by experiment results.

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Author Contributions: Xi Zhang proposed the original idea and built the mathematical model. Ziyang Lai developed all the hardware. Rui Xiong helped improve the parameter analysis. Zhe Li did some simulation work. Zhiming Zhang designed the primary and secondary coils. Liang Song completed the software. All authors carried out the data analysis, discussed the results and contributed to writing the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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