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Isolated DC-DC Converter for Bidirectional Power Flow Controlling with Soft-Switching Feature and High Step-Up/Down Voltage Conversion

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Abstract: In this paper, a novel isolated bidirectional DC-DC converter is proposed, which is able to accomplish high step-up/down voltage conversion. Therefore, it is suitable for hybrid electric vehicle, fuel cell vehicle, energy backup system, and grid-system applications. The proposed converter incorporates a coupled inductor to behave forward-and-flyback energy conversion for high voltage ratio and provide galvanic isolation. The energy stored in the leakage inductor of the coupled inductor can be recycled without the use of additional snubber mechanism or clamped circuit. No matter in step-up or step-down mode, all power switches can operate with soft switching. Moreover, there is a inherit feature that metal–oxide–semiconductor field-effect transistors (MOSFETs) with smaller on-state resistance can be adopted because of lower voltage endurance at primary side. Operation principle, voltage ratio derivation, and inductor design are thoroughly described in this paper. In addition, a 1-kW prototype is implemented to validate the feasibility and correctness of the converter. Experimental results indicate that the peak efficiencies in step-up and step-down modes can be up to 95.4% and 93.6%, respectively.

Keywords: bidirectional DC-DC converter; high voltage conversion ratio; galvanic isolation; soft-switching feature

1. Introduction

In order to reduce carbon emission and mitigate global warming, green energies, such as photovoltaic (PV) panel, fuel cells, and wind turbine, attract a great deal of interest and have a high rate of growth in installed capacity. A complete configuration of distributed generation system (DGS), as shown in Figure 1, not only includes green-energy sources but also combines an energy storage system for power conditioning to use electricity optimally. For grid connection, a DC-bus voltage up to around 400 V is required, which is much higher than a battery voltage. Therefore, a bidirectional DC-DC converter (BDC) with high voltage ratio to charge/discharge battery is mandatory in the DGS.

Conventional high step-up converters used in PV panel and fuel cells can boost a low voltage to a higher level to serve as an interface between the distributed generator and the DC bus [1–3]. Nevertheless, they only control power flow in unique direction. Bidirectional power flow control is necessary for battery system. A solution is to adopt two high-voltage-ratio converters. One is high-step-up converter for battery discharging and the other is high-step-down converter for charging, but this approach increases cost significantly. Therefore, BDC is the current design trend, which is

capable of governing energy in either power flow direction by a single converter. BDCs can be simply classified as non-isolated type [4–6] and isolated type [7,8].

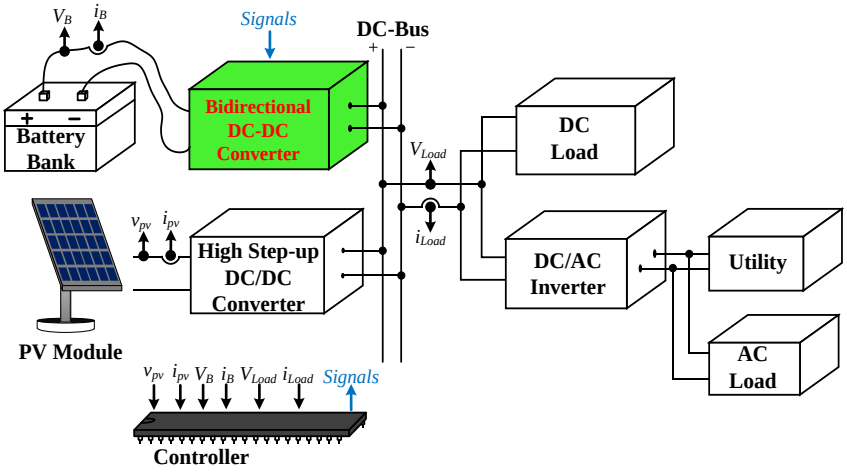

Figure 1. Configuration of distributed generation system.

Increasing switching frequency of a power converter can reduce the size of magnetic and capacitive elements and thus has the benefit of achieving high power density. However, the higher switch frequency is, the lower conversion efficiency will be. In order to eliminate switching loss, employing resonant unit with auxiliary switches for soft-switching achievement is a common approach [9–11]. In literature [12], the authors develop a dual-bridge converter to fulfill bidirectional power flow controlling along with zero voltage switching (ZVS) at main switch, in which even resonant tank is utilized but the use of additional auxiliary switch can be avoided. Nevertheless, a great many switches are needed and its voltage ratio is incapable of high step-up/down applications.

The open H-bridge converter can function as a non-isolated BDC [13]. Even though this converter can achieve ZVS feature and possesses simple structure, its voltage gain is less than 2 at the duty ratio of 0.5. For higher voltage ratio, heavy switch duty cycle is the only solution to this problem, but this approach will degrade converter efficiency. To avoid excessive duty cycle operation, switched capacitor technology will be an alternative for high voltage-gain conversion [14]. However, current spike that occurs at the switching transients confines its applications and accompanies electromagnetic interference (EMI) problem, especially in high power rating. Incorporating switched capacitor along with coupled inductor into a power converter is a key to suppressing inrush current and obtaining enough voltage conversion ratio [15–18]. Since the coupled inductor can also feature electrical isolation, a BDC including coupled inductor is the major development. However, the energy dissipation caused from leakage inductor will degrade converter efficiency [19,20]. That is, clamped circuit or snubber mechanism for leakage energy harvesting is imperative. Isolated BDCs based on H-bridge topology have been proposed in the literature [21,22], which can achieve ZVS feature inherently, avoiding additional device usage. Nevertheless, low voltage ratio and more power switches required become their disadvantages. In [23], another isolated BDC which accomplishes leakage-energy recycling and can obtain high voltage-ratio conversion is presented. Nevertheless, some limitations still exist, such as ZVS only occurs at high-voltage side and duty ratio has to be greater than 0.5.

In this paper, a novel BDC is proposed, which has the advantages of galvanic isolation, high voltage conversion ratio, soft-switching feature at all power switches, high efficiency, being suitable for high power applications, and low component count. Figure 2 shows its configuration of the power stage. The symbols in the circuit are summarized in the followings. V_L and V_H denote the terminal voltages at low-voltage side and high-voltage side, respectively; L_1 is a choke inductor; S_1, S_2, S_3, S_4, S_5, and S_6 are active switches, while D_{S1}–D_{S6} and C_{S1}–C_{S6} express their related anti-parallel body diodes and parasitic capacitors; the magnetically-coupled device has winding N_1, magnetizing inductor L_{m1},

and leakage inductor L_{k1} at low-voltage side, meanwhile N_2, L_{m2}, and L_{k2}, respectively, at high-voltage side; C_{b1} and C_{b2} are low-voltage capacitors; and C_{o1} and C_{o2} are high-voltage capacitors. The conversion efficiency of proposed BDC can be improved because of the following reasons:

(1) No matter in buck or boost mode, the energy stored in leakage inductors, L_{k1} and L_{k2}, can be recycled without any snubber mechanism or clamped circuit.
(2) All active semiconductor components can be switched with ZVS or zero current switching (ZCS) to eliminate switching losses.
(3) Switches S_1–S_4 endure a low voltage stress so that semiconductor device with a smaller $R_{ds(on)}$ can be chosen to reduce conduction losses.

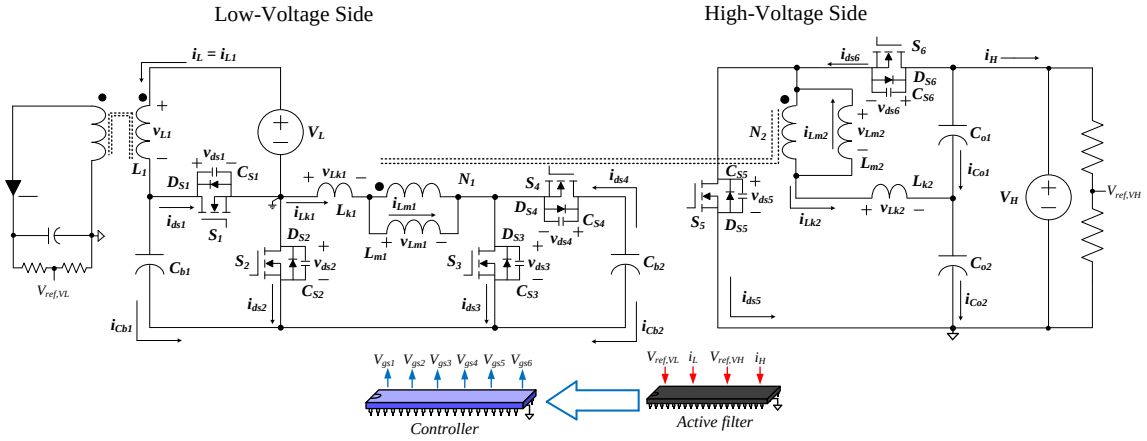

Figure 2. Schematic of the proposed bidirectional converter.

Following the introduction described in Section 1, this paper is organized as follows. The operation principle of the proposed converter is explained in Section 2. Section 3 presents the steady-state analysis. Experimental results measured from a 1-kW prototype are illustrated and discussed in Section 4, while conclusion is summarized in Section 5.

2. Operation Principle of the Proposed Converter

As shown in Figure 2, the direction of energy flow can be handled by controlling the active switches so that the converter can operate in either step-up mode or step-down mode. In step-up mode, main switches S_1, S_2, S_3, and S_4 are in switching pattern while S_5 and S_6 are in charge of rectifying. At this mode, S_1 and S_2 operate complementarily and so do both switches S_3 and S_4. The voltage gain of V_L to V_H is determined by the duty ratio of S_1. With respect to step-down mode, main switches S_2, S_4, S_5, and S_6 will be in switching pattern and the rest of main switches serve as rectifier. In addition, S_2, S_4, and S_5 are turned on and off simultaneously and complementary to S_6. The duty ratio of S_6 dominates the voltage gain of V_H to V_L in step-down mode. To describe the operation of the converter, some assumptions are made as follows:

(1) In Figure 2, capacitances of C_{b1}, C_{b2}, C_{o1}, and C_{o2} are large enough so that all the voltages across them can be regarded as constant in a switching cycle.
(2) Parasitic capacitor and body diode of each switch are considered, but the internal resistance is neglected.
(3) The leakage inductance of the coupled inductor is much less than magnetizing inductance.
(4) All the magnetic components are designed in continuous conduction mode (CCM).
(5) The turns ratio of secondary to primary of the coupled inductor, N_2/N_1, is defined as n.

2.1. Step-Up Mode

The converter operation in step-up mode is divided into nine main stages over one switching cycle, which are discussed stage by stage below. The equivalents of the nine stages are depicted in Figure 3, while Figure 4 illustrates the corresponding conceptual waveforms.

Stage 1 [t_0, t_1]: In this stage, referring to Figure 3a, all the switches are in off state. The energy stored in the parasitic capacitor C_{S3} is drawn out but capacitor C_{b1} is charged, as referred to the red dashed line in Figure 3a. Meanwhile, energy of L'_{m1} is forwarded to capacitor C_{o2} and the output V_H, where L'_{m1} stands for the total amount of magnetizing inductance seen looking into the primary (at low-voltage side) of the coupled inductor. After the voltage across C_{S3} drops to zero, the body diode D_{S3} conducts to continue the currents flowing through L_1 and L_{k1} thus to create ZVS turn-on condition for S_3.

Stage 2 [t_1, t_2]: This stage begins at the moment the switches S_1 and S_3 are turned on. The S_3 is turned on with ZVS. During this time interval, S_2, S_4, S_5, and S_6 are still in off-state. The voltage of the parasitic capacitor C_{S1} drops. After the voltage v_{ds1} is less than input voltage V_L, inductor L_1 will absorb energy from V_L and the current i_{L1} increases, as referred to the blue dashed line in Figure 3b. In stage 2, the energy of L_{k1} is continuously releasing to C_{b1}. The equivalent circuit of this stage is illustrated in Figure 3b. When the current i_{Lk1} falls to zero, this mode ends.

Stage 3 [t_2, t_3]: Figure 3c depicts the equivalent circuit of this stage, in which all the switch have the same statuses as in Stage 2. Inductor L_1 continuously absorbs the energy from V_L. Capacitor C_{b1} transmits energy to L_{k1}, L'_{m1} and the secondary (at high-voltage side) of the coupled inductor, of which current path is indicated by the red dashed line in Figure 3c. The currents i_{Lk1} and i_{Lm1} increase. In the high-voltage side, C_{o1} is charged via the loop of N_2-D_{S6}-C_{o1}-L_{k2} but C_{o2} discharges via the loop of L_{k2}-N_2-D_{S6}-V_H-C_{o2}. This mode ends when S_3 is turned off.

Stage 4 [t_3, t_4]: This stage begins at time $t = t_3$, and the equivalent circuit is illustrated in Figure 3d. During this time interval, all the switches are in off state except S_1. Input V_L and capacitor C_{b1} charge inductor L_1 and capacitor C_{b2}, respectively. In addition, C_{b1} forwards energy to high-voltage side via the coupled inductor to charge C_{o1}. The C_{S4} releases energy. That is, v_{ds4} decreases. The body diode of S_4 will be forward biased after v_{ds4} drops to zero, which provides ZVS condition for S_4. The associated current path is referred to the red dashed line in Figure 3d. The leakage energy in L_{k2} is recycling to C_{o1} over the interval of Stage 4.

Stage 5 [t_4, t_5]: When S_4 is turned on, the operation of the converter enters into Stage 5. As shown in Figure 3e, in this stage switches S_1 and S_4 are closed, whereas S_2, S_3, S_5, and S_6 are open. The voltage polarity of L_{k1} is reversed and the current i_{Lk1} begins decreasing. Capacitor C_{b2} is charged by L_{k1} and C_{b1} and the current flowing through S_4 is decreased, as referred to the red dashed line in Figure 3e. The energy in L_{k2} is kept on recycling to C_{o1}, which is the same as in Stage 4. At the moment that i_{Lk2} equals zero, this stage ends and D_{S6} is reversely biased.

Stage 6 [t_5, t_6]: During the time interval of Stage 6, the switches S_1 and S_4 are still in on state and S_2, S_3, S_5, and S_6 in off state. Figure 3f is the corresponding equivalent, in which C_{b1} charges L_{k1}, L'_{m1}, and C_{b2}, as referred to the red dashed line. The currents flowing through L_{k1} and L'_{m1} are identical and increase simultaneously. With respect to current i_{L1}, since the voltage across L_1 is V_L, the current i_{L1} continues linearly increasing. This stage continues until S_1 is turned off.

Stage 7 [t_6, t_7]: Figure 3g depicts the equivalent circuit of Stage 7, in which all switches are open except S_4. There are two loops, V_L-L_1-C_{b1}-C_{S2} and L_{k1}-L'_{m1}-S_4-C_{b2}-C_{S2}, to draw the energy stored in the parasitic capacitor of S_2. When the voltage across C_{S2} falls to zero, the body diode of S_2 conducts and S_2 can achieve ZVS, as referred to the both dashed lines in red and blue in Figure 3g. In the high-voltage side of the converter, the both in-series capacitors C_{o1} and C_{o2} supply power to output.

Stage 8 [t_7, t_8]: After the time $t = t_7$, switches S_2 and S_4 are in on state but S_1, S_3, S_5, and S_6 are in off state. The equivalent circuit is illustrated in Figure 3h. As referred to the both red and purple dashed line in Figure 3h, capacitor C_{b1} is charged by V_L and L_1, while the C_{b2} absorbs energy from L'_{m1} and L_{k1}. All the currents i_{L1}, i_{Lk1} and i_{Lm1} decrease. In addition, the energy stored in magnetizing inductor is forwarded to the secondary of the coupled inductor to charge C_{o2}. This stage ends as the current i_{Lk1} falls to zero.

Stage 9 [t_8, t_9]: During the time interval of Stage 9, the switches S_2 and S_4 are still in on state and S_1, S_3, S_5, and S_6 in off state. The equivalent circuit is illustrated in Figure 3i. Capacitor C_{b1} is still charged by V_L and L_1. Additionally, capacitor C_{b2} pumps energy to inductor L_{k1} via switches S_4, as referred to the red dashed line in Figure 3i. The energy stored in the magnetizing inductor is transferred to the secondary to charge C_{o2} and power the output. In this stage, inductor currents i_{L1} and i_{Lm1} decrease but i_{Lk1} and i_{Lk2} increase. When switches S_2 and S_4 are turned off at $t = t_9$, this stage ends. The operation in step-up mode over one switching cycle is completed.

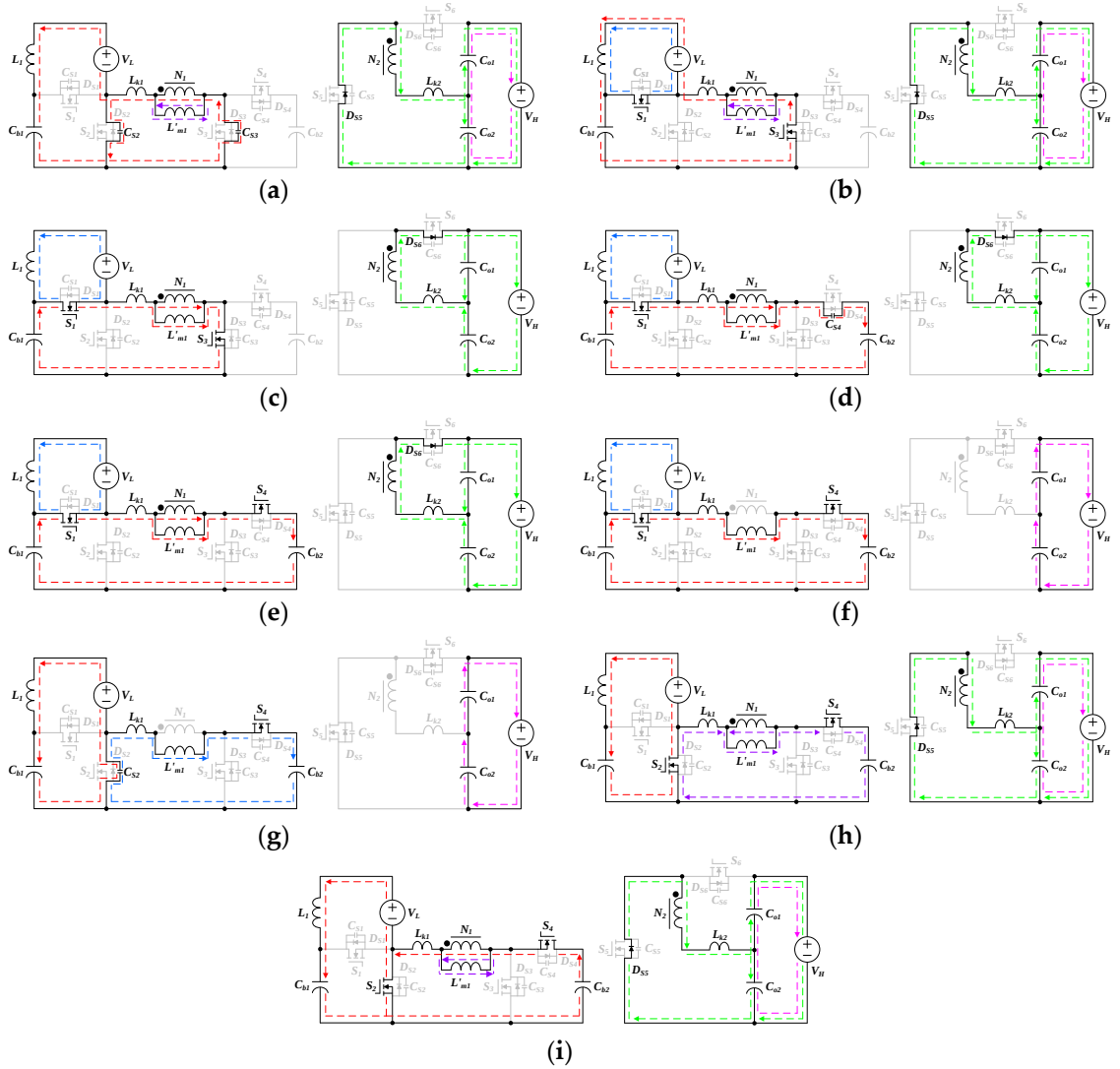

Figure 3. Equivalent circuit of proposed bidirectional converter in step-up mode: (**a**) Stage 1; (**b**) Stage 2; (**c**) Stage 3; (**d**) Stage 4; (**e**) Stage 5; (**f**) Stage 6; (**g**) Stage 7; (**h**) Stage 8; and (**i**) Stage 9.

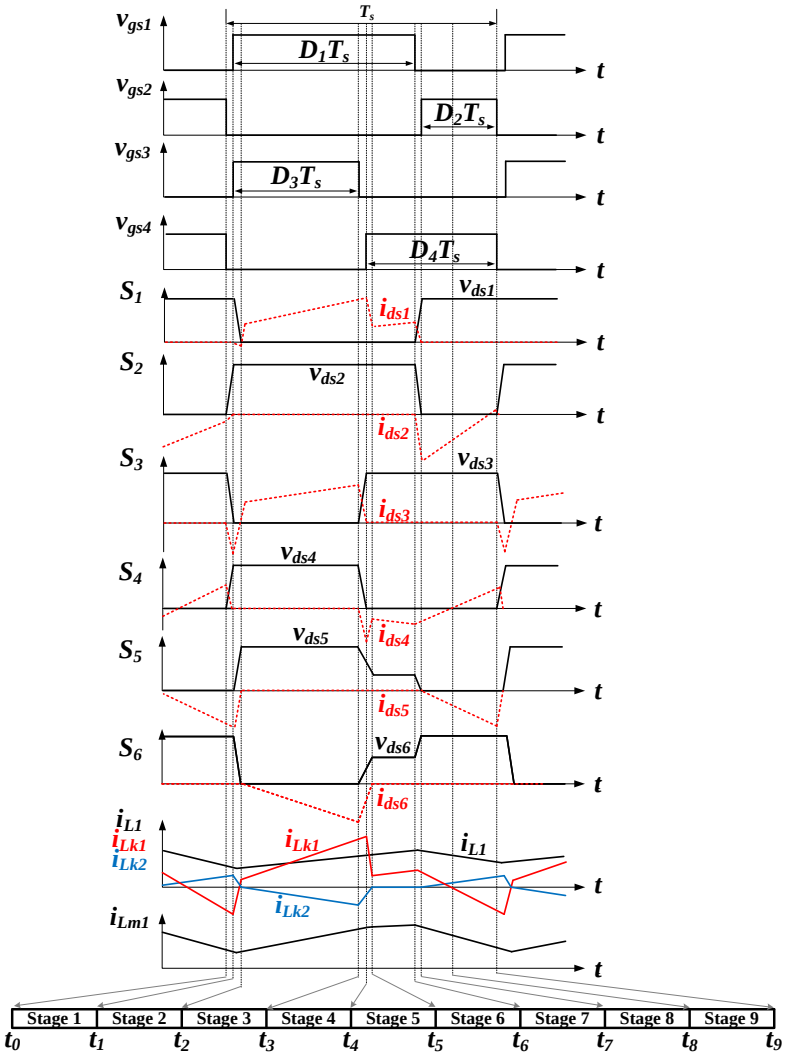

Figure 4. Key waveforms of the proposed converter in step-up mode.

2.2. Step-Down Mode

In step-down mode, S_2, S_4, and S_5 are controlled at high switching pattern and complementary to SW_6, while SW_1 and SW_3 serve as rectifiers. The converter operation over one switching cycle in step-down mode can be divided into 12 stages, which are described stage by stage in the following. The related equivalents and corresponding waveforms are depicted in Figures 5 and 6, respectively.

Stage 1 [t_0, t_1]: Referring to Figure 5a, all the switches are in off state. Since S_5 has been turned off, the voltage of C_{S5} increases. Accordingly, the voltage across L'_{m2} (the inductance seen looking into the high-voltage side of the coupled inductor) and L_{k2}, which is equal to $v_{Co2} - v_{ds5}$, decreases; meanwhile the energy stored in the parasitic capacitor of S_6 releases via the loop of C_{S6}-C_{o1}-L_{k2}-L'_{m2}. In low voltage side, the body diodes of S_2 and S_4 are forward biased because of the continuity of i_{Lk1}. The voltage across L_1 equals $v_{Cb1} - V_L$. Since v_{Cb1} is larger than V_L, the current i_{L1} increases negatively, as referred to the red dashed line in Figure 5a. During this stage, C_{o2} will energize C_{b2} via the coupled inductor and the loop L_{k1}-N_1-D_{S4}-C_{b2}-D_{S2}. This mode ends at the moment v_{ds5} reaches the magnitude of V_H. That is, S_5 is completely turned off and its blocking voltage is clamped to V_H.

Stage 2 [t_1, t_2]: During this time interval, all the switches still stay in off state. The equivalent circuit of this stage is illustrated in Figure 5b. The voltage polarity across L'_{m2} and L_{k2} reverses and the value of $v_{Lm2} + v_{Lk2}$ is equal to v_{Co1}. That is, magnetizing inductor L'_{m2} and leakage inductor L_{k2} release energy to C_{o1} and V_H via body diode D_{S6}, as indicated by the purple dashed line in Figure 5b. Since

voltage polarity of the coupled inductor has been changed, the body diode D_{S2} will be reversely biased and the parasitic capacitor C_{S1} releases energy to V_L. In stage 2, the current flowing L_{k1} almost equals that in L_1. Therefore, switch S_2 is turned off at ZCS. When S_6 is turned on with ZVS, the operation of the converter enters into next stage.

Stage 3 [t_2, t_3]: In this stage, switch S_6 is closed. L'_{m2} and L_{k2} proceed with energy releasing toward C_{o1} and V_H, and leakage energy in L_{k1} is dumped to C_{b2} at the same time. Accordingly, all the currents in them decrease. As referred to the blue dashed line in Figure 5c, the current of L_1 draws out the stored energy in C_{S1} and then force the parasitic diode D_{S1} in forward bias. The L_1 delivers energy to V_L and its current decreases linearly. In stage 3, the current flowing through L_{k2} is greater than that in L'_{m2} but its magnitude drops much steeper. This stage continues until i_{Lk1} drops to zero. Figure 5c shows the equivalent circuit of this stage.

Stage 4 [t_3, t_4]: This stage begins at time $t = t_3$, and the equivalent circuit is illustrated in Figure 5d. During this time interval, all switches are still in turn-off condition except S_6. Magnetizing inductor L'_{m2} forwards energy to C_{o1} and C_{b1} via switch S_6 and the ideal transformer, respectively. The current direction of L_{k1} changes, which results in energy releasing of C_{S3} and the charging of C_{S4}. Associated current path is shown as the red dashed line in Figure 5d. The leakage inductor L_{k1} will confine the charge current of C_{S4}, resulting in ZCS turn-off at S_4. When the voltage v_{ds4} rises to v_{Cb2}, Stage 5 begins.

Stage 5 [t_4, t_5]: The equivalent circuit of this stage is illustrated in Figure 5e, in which all the switches are turned off except S_6. Capacitor C_{o1} still absorbs energy from L'_{m2} and L_{k2}. In addition, L'_{m2} forwards energy to C_{b1} by the ideal transformer and via the loop of N_1-L_{k1}-D_{S1}-C_{b1}-D_{S3}. This current path is referred to the red dashed line in Figure 5e. The current flowing through L_{k2} keeps on decreasing. This stage ends at the time that i_{Lk2} is zero. That is, energy in L_{k2} is completely recycled.

Stage 6 [t_5, t_6]: Figure 5f depicts the equivalent circuit of this mode, in which all switches have the same statuses as in Stage 5. The current direction of i_{Lk2} changes at $t = t_5$, and L_{k2} absorbs energy from C_{o1}, as referred to the green dashed line in Figure 5f. The circuit operation in low voltage side is identical to that in Stage 5. Therefore, the inductor L_1 keeps on energy supplying toward V_L and its current decreases linearly. Stage 6 continues until switch S_6 is turned off at $t = t_6$.

Stage 7 [t_6, t_7]: During the interval that S_6 is open, the voltage v_{ds6} increases. Therefore, the voltage, $v_{Lm2} + v_{Lk2}$, drops and the parasitic capacitor C_{S5} dumps its stored energy, as referred to the green dashed line in Figure 5g. The circuit operation in low-voltage side behaves identically to Stage 6. When the energy in C_{S5} is drawn out completely and v_{ds6} rises to V_H, this stage stops. Figure 5g expresses the operation of the converter in Stage 7.

Stage 8 [t_7, t_8]: In Stage 8, the body diode D_{S5} is in forward bias, which provides a ZVS condition for S_5. The green dashed line in Figure 5h shows this current path. Leakage energy in inductors L_{k2} and L_{k1} is recycled to C_{o2} and C_{b1}. In addition, L_1 proceeds with energy releasing to V_L while L'_{m2} still forwards energy to low voltage side via the ideal transformer. When switches S_2, S_4, and S_5 are turned on simultaneously, this stage ends. The corresponding equivalent circuit is depicted in Figure 5h.

Stage 9 [t_8, t_9]: At $t = t_8$, the operation of the converter enters into Stage 9. Figure 5i is the equivalent. The voltage polarity of the ideal transformer reverses because S_2 and S_4 are closed. Over the time interval of Stage 9, L_{k2} and L_{k1} continuously dump their stored energy and thus the currents i_{Lk1} and i_{Lk2} reduce. Additionally, the voltage level of v_{Cb1} is higher than V_L, which results that the inductor L_1 absorbs energy from C_{b1} and its current increases negatively and linearly, as referred to the blue dashed line in Figure 5i. This stage lasts until i_{Lk2} drops to zero.

Stage 10 [t_9, t_{10}]: After the time $t = t_9$, the current direction of L_{k2} changes and i_{Lk2} increases. Switch statues in Stage 9 are identical to that in Stage 10. That is, S_2, S_4, and S_5 are in on state, whereas S_1, S_3, and S_6 stay in off state. The equivalent circuit is shown in Figure 5j, in which the L'_{m2} draws energy from C_{o2} and the voltage across L_1 is still kept at $V_{Cb1} - V_L$. As the red dashed line in Figure 5j indicates, leakage inductor L_{k1} continues releasing energy and i_{Lk1} decreases. When i_{Lk1} is zero at $t = t_{10}$, this stage ends.

Stage 11 [t_{10}, t_{11}]: Figure 5k shows the equivalent circuit of this stage, in which the statuses of all switches are kept as in Stage 10. During this time interval, C_{b1} continuously supplies energy to V_L and L_1 by the loop of C_{b1}-L_1-V_L-S_2, of which current path is referred to the blue dashed line in Figure 5k. The current directions of N_1 and N_2 reverse and the current i_{Lk1} rises positively. Meanwhile, capacitor C_{b2} charges and C_{o2} discharges.

Stage 12 [t_{11}, t_{12}]: From the equivalent circuit depicted in Figure 5l, switches S_2, S_4, and S_5 remain closed, while S_1, S_3, and S_6 are open. In Stage 12, inductors L_{k2} and L'_{m2} are magnetized by C_{o2} with the same circuit behavior in Stage 11. Since the magnitude of i_{Lk1} is greater than i_{L1}, the current flowing through S_2 becomes reverse, and then S_2 achieves ZCS at turn-off transition, as referred to the red dashed line in Figure 5l. The operation of the converter over one switching cycle is completed when the switches S_2, S_4, and S_5 are turned off simultaneously.

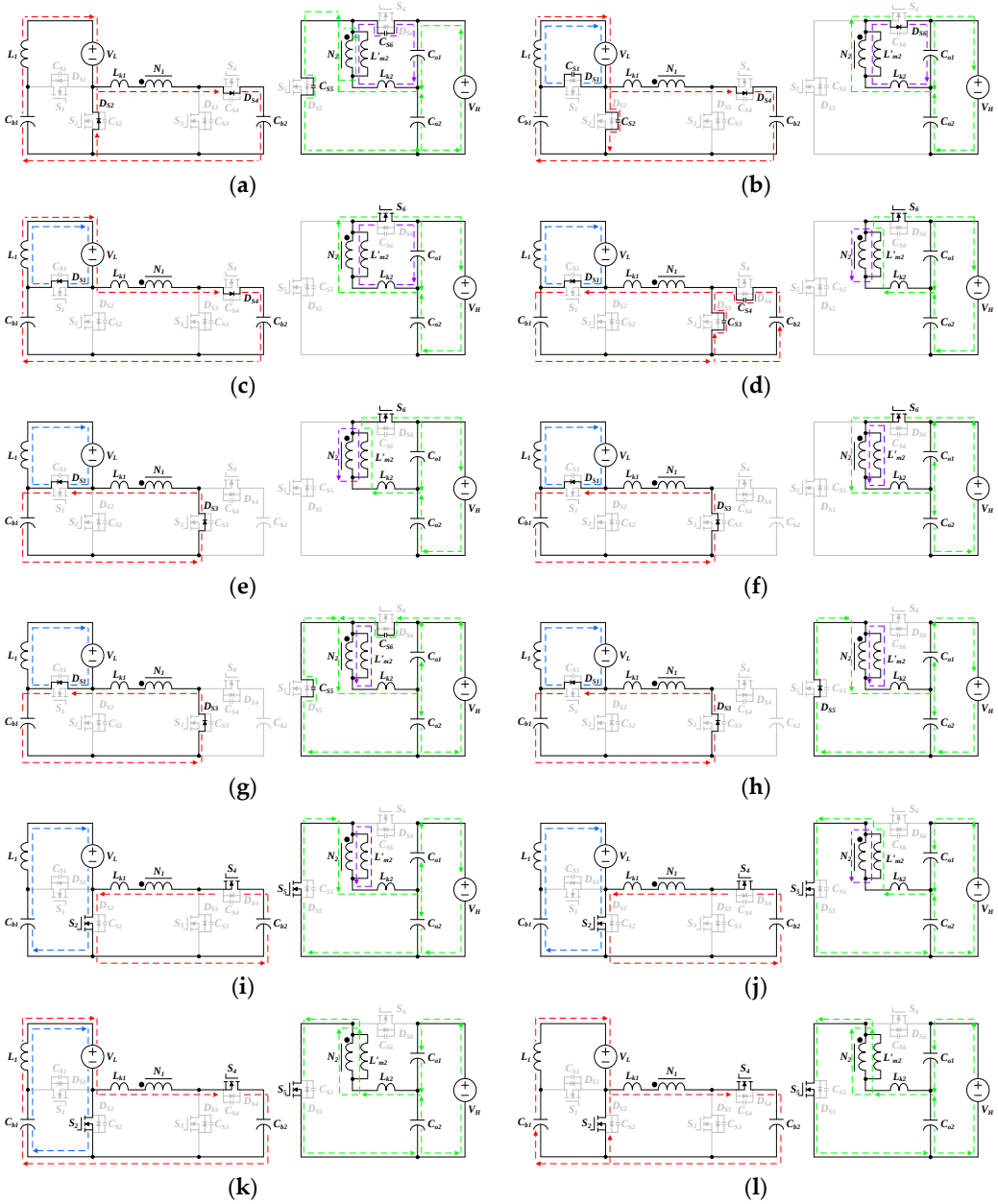

Figure 5. Equivalent circuit of proposed bidirectional converter in step-down mode. (**a**) Stage 1; (**b**) Stage 2; (**c**) Stage 3; (**d**) Stage 4; (**e**) Stage 5; (**f**) Stage 6; (**g**) Stage 7; (**h**) Stage 8; (**i**) Stage 9; (**j**) Stage 10; (**k**) Stage 11; and (**l**) Stage 12.

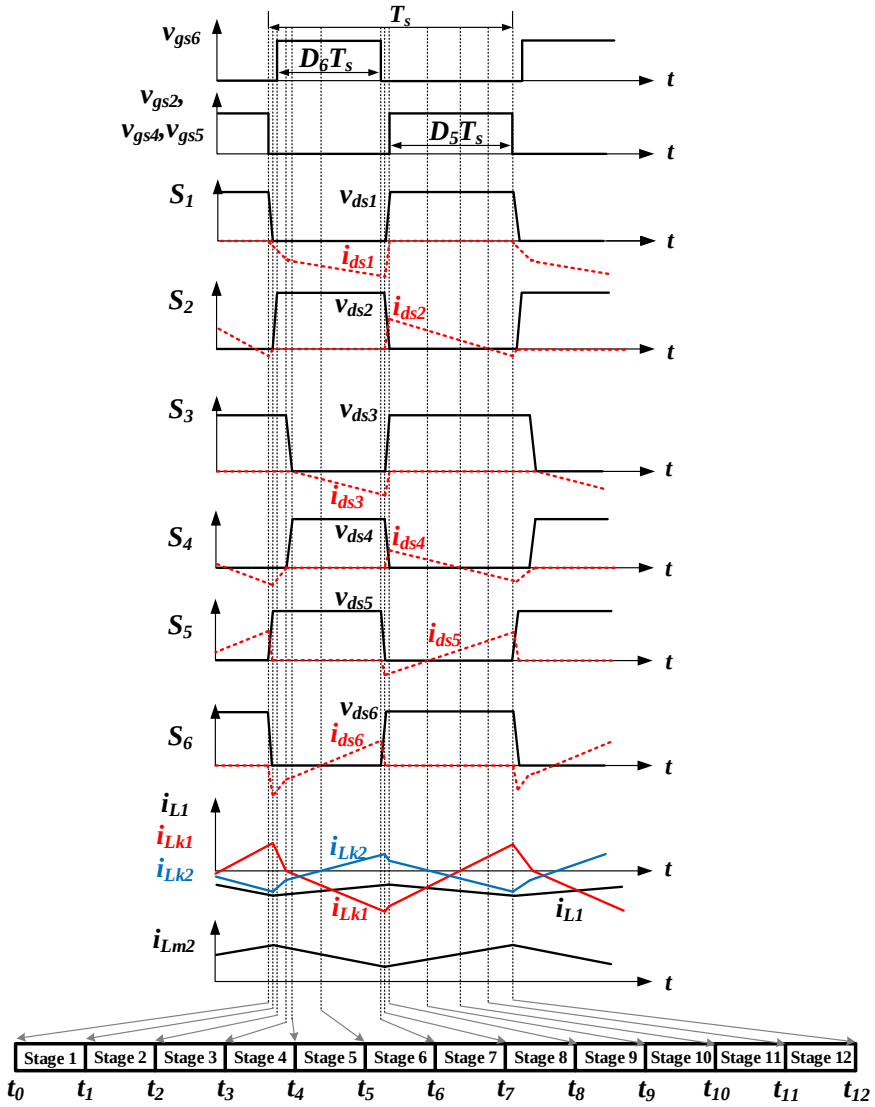

Figure 6. Key waveforms of the proposed converter in step-down mode.

According to the aforementioned operation principle, the switching characteristics of all power switches are summarized in Table 1.

Table 1. The switching characteristics of the proposed converter.

Mode	Main Circuit					
	Low-Voltage Side				High-Voltage Side	
	S_1	S_2	S_3	S_4	S_5	S_6
Step-up	ZVS	ZVS	ZVS	ZVS	none	none
Step-down	none	ZCS	none	ZCS	ZVS	ZVS

3. Steady-State Analysis

In this section, the steady-state analysis of the BDC includes voltage conversion ratio, voltage stress derivation, and magnetic element design. To simplify the analysis, the assumptions made in Section 2 are considered except the neglect of leakage inductors. In addition, the phenomenon that occurs at switching transient is also ignored.

3.1. Step-Up Mode

Voltage gain of the converter in step-up mode is first investigated. Because the output voltage V_H is the sum of V_{Co1} and V_{Co2}, the relationships of V_{Co1} to V_L and V_{Co2} to V_L have to be found in advance. The voltage V_{Co1} is n times the magnitude of V_{Cb1} and V_{Co2} is n times the V_{Cb2} under the condition that leakage inductor is neglected. Accordingly, V_{Cb1} and V_{Cb2} in terms of V_L should be determined before the finding for V_{Co1} and V_{Co2}. Since S_1 and S_2 are switched complementarily, the input voltage V_L can be boosted via inductor L_1. As a result, the voltage across C_{b1} is given by

$$V_{Cb1} = \frac{V_L}{1 - D_1}, \tag{1}$$

where D_1 is the duty ratio of S_1. Refer to Figure 4 at any time there are two switches in closed state simultaneously over one switching cycle. While S_1 and S_3 are on, the voltage across L'_{m1} is V_{Cb1} and thus the amount of current increase can be estimated by

$$\Delta i_{Lm1,S3on} = \frac{V_{Cb1}}{L'_{m1}} D_3 T_s \tag{2}$$

In Equation (2), the D_3 denotes the duty ratio of S_3. After S_3 is turned off, switch S_4 will be turned on. That is, the both switches S_1 and S_4 are in on state. The voltage across L'_{m1} becomes $V_{Cb1} - V_{Cb2}$. If V_{Cb1} is greater than V_{Cb2}, the L'_{m1} will proceed with current increasing. The increment can be expressed as

$$\Delta i_{Lm1,S3off} = \frac{(V_{Cb1} - V_{Cb2})}{L'_{m1}} (D_1 - D_3) T_s \tag{3}$$

The switch S_2 will be turned on when switch S_1 is turned off. That is, S_2 and S_4 are in on state simultaneously and the voltage across L'_{m1} is $-V_{Cb2}$. The current flowing through L'_{m1} decreases, which is given by

$$\Delta i_{Lm1,S1off} = \frac{V_{Cb2}}{L'_{m1}} (1 - D_1) T_s \tag{4}$$

In steady state, the net current change on L'_{m1} is equal to zero. From Equations (2)–(4), the following relationship can be derived

$$\frac{V_{Cb1}}{L'_{m1}} D_3 T_s + \frac{(V_{Cb1} - V_{Cb2})}{L'_{m1}} (D_1 - D_3) T_s - \frac{V_{Cb2}}{L'_{m1}} (1 - D_1) T_s = 0 \tag{5}$$

Substituting Equation (1) into Equation (5) becomes

$$V_{Cb2} = \frac{D_1}{(1 - D_1)(1 - D_3)} V_L \tag{6}$$

The output voltage $V_H = V_{Co1} + V_{Co2}$, which can be also obtained from

$$V_H = n(V_{Cb1} + V_{Cb2}) \tag{7}$$

Therefore, the conversion ratio of output voltage to input voltage in step-up mode, $M_{step\text{-}up}$, can be found by

$$M_{step\text{-}up} = \frac{V_H}{V_L} = \frac{n(1 + D_1 - D_3)}{(1 - D_1)(1 - D_3)} \tag{8}$$

As referring to the switching sequence in step-up mode, during the interval that S_2 and S_4 are open but S_1 and S_3 are closed, the S_2 and S_4 endure the voltages of V_{Cb1} and V_{Cb2}, respectively. After the above switch status, S_2 and S_3 will be open but S_1 and S_4 are closed. The blocking voltages at S_2 and S_3 are V_{Cb1} and V_{Cb2}, respectively. The switch status that S_1 and S_3 are off but S_2 and S_4 are on

proceeds the converter operation. The voltages across S_1 and S_3 in this time interval are also V_{Cb1} and V_{Cb2} in turn. In brief, the voltage stresses with respect to S_1, S_2, S_3 and S_4 can be determined as follows:

$$v_{S1\text{-}stress} = v_{S2\text{-}stress} = \frac{V_L}{1 - D_1} \tag{9}$$

$$v_{S3\text{-}stress} = v_{S4\text{-}stress} = \frac{D_1}{(1 - D_1)(1 - D_3)} V_L \tag{10}$$

At high-voltage side, the switch S_5 will withstand a voltage of at least V_H when the intrinsic diode of S_6 is forward biased. Similarly, S_6 also endures a reverse voltage up to V_H during the interval that the diode D_{S6} is on. That is,

$$v_{ds5} = v_{ds6} = \frac{n(1 + D_1 - D_3)}{(1 - D_1)(1 - D_3)} V_L \tag{11}$$

With respect to inductance design, the average current carried by magnetic component has to be calculated in advance. For L'_{m1}, the application of amp-second balance criterion (ASBC) at C_{b2} can give an assistance to the finding for the average of i_{Lm1}. The C_{b2} charges during the time interval $[t_5, t_6]$, in which S_1 and S_4 are in on state. On the contrary, C_{b2} discharges during $[t_8, t_9]$, while S_2 and S_4 are closed. The charging current of C_{b2} is equal to i_{Lm1} and discharging current will be $i_{Lm1} + ni_{ds5}$. Thus, the following relationship holds:

$$i_{Lm1}(D_1 - D_3)T_s + (i_{Lm1} - \frac{n}{1 - D_1} i_H)(1 - D_1)T_s = 0 \tag{12}$$

From Equation (12), the average current carried by L'_{m1} can be given as

$$I_{Lm1} = \frac{n}{1 - D_3} I_H \tag{13}$$

If the voltage across C_{b1} is close to V_{Cb2}, the current i_{Lm1} can be regard as constant in Stage 6. This phenomenon can be found in Figure 4. Assume that L'_{m1} is in BCM. The following relationship can be found:

$$\frac{[(D_1 - D_3)T_s + T_s]\frac{V_{Cb1}}{L'_{m1}} D_3 T_s}{2T_s} = \frac{n}{1 - D_3} I_H \tag{14}$$

Solving for L'_{m1} results:

$$L'_{m1,min} = \frac{D_3(1 - D_3)^2 R_H}{2n^2 f_s} \tag{15}$$

where $L'_{m1,min}$ is the minimum inductance of L'_{m1} for CCM operation, R_H stands for load resistance at high-voltage side, and f_s is switch frequency.

To determine the minimum inductance of L_1, $L_{1,min}$, for CCM operation, average current of i_{L1} has to be contacted. This average current can be found by applying ASBC to C_{b1}. Capacitor C_{b1} charges during the time interval $[t_7, t_9]$, in which both switches S_2 and S_4 are closed. There are two intervals to discharge the energy in C_{b1}. One is $[t_2, t_4]$, in which S_1 and S_3 are closed, and the other is and $[t_4, t_7]$, in which S_4 and S_1 are in on state. Based on ASBC, the following relationship holds:

$$(-\frac{n}{D_3} i_H - i_{Lm1}) D_3 T_s + i_{Lm1}(D_3 - D_1)T_s + i_{L1}(1 - D_1)T_s = 0 \tag{16}$$

Using Equation (13) and substituting for i_{Lm1}, the average current flowing through L_1 can be represented as

$$I_{L1} = \frac{n(1 + D_1 - D_3)}{(1 - D_1)(1 - D_3)} I_H \tag{17}$$

The current increment on L_1, Δi_{L1}, is estimated by

$$\Delta i_{L1} = \frac{V_L}{L_1} D_1 T_s \tag{18}$$

Hence, the minimum of i_{L1}, $I_{L1,min}$, is given by

$$I_{L1,min} = \frac{n(1 + D_1 - D_3)}{(1 - D_1)(1 - D_3)} I_H - \frac{V_L}{2L_1} D_1 T_s \tag{19}$$

At BCM, $I_{L1,min} = 0$. Solving for L_1 yields

$$L_{1,min} = \frac{D_1 (1 - D_1)^2 (1 - D_3)^2 R_H}{2n^2 (1 + D_1 - D_3)^2 f_s} \tag{20}$$

in which $L_{1,min}$ is the minimum inductance of L_1 for CCM. If $R_H = 640\ \Omega$, $f_s = 40$ kHz, $n = 3$, and $D_1 = D_3$. Figure 7a depicts the relationships between inductance L'_{m1} and duty ratio D_1 while Figure 7b is for inductance L_1 versus D_1.

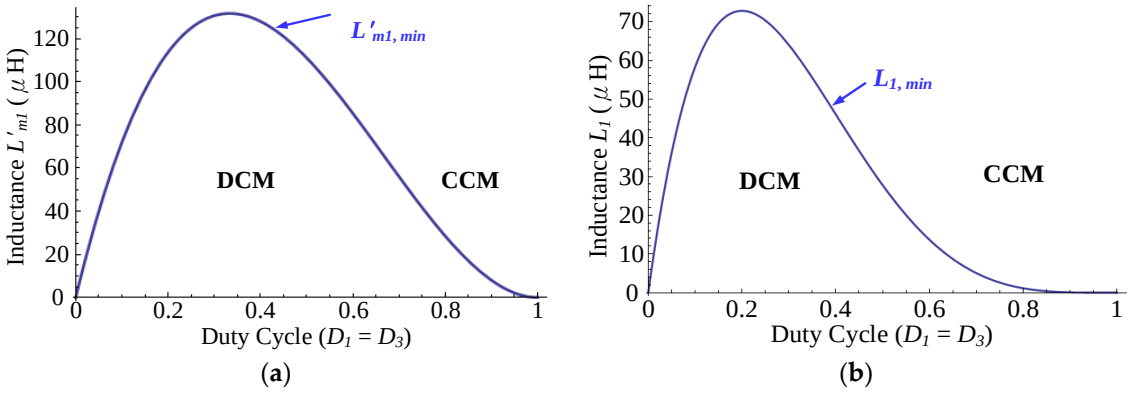

Figure 7. Magnetic component design for (**a**) L'_{m1} and (**b**) L_1 under the duty ratio $D_1 = D_3$.

3.2. Step-Down Mode

All the assumptions in the above subsection are also adopted for the steady-state analysis in step-down mode. The switches S_2, S_4, and S_5 are controlled simultaneously and complementary to S_6. During the interval that S_6 is in turned-on state and S_2, S_4, and S_5 are in turned-off state, the voltage V_{Co1} will directly impose on the high-voltage side of the transformer. Then, the body diodes D_{s1} and D_{s3} forward conduct and the voltage V_{Cb1} will be equal to V_{Co1}/n. The inductor L_1 supplies energy to V_L. This state will last for $D_6 T_s$. During the interval $(1 - D_6)T_s$, S_6 becomes off but S_2, S_4, and S_5 are on. The voltage polarity of the coupled inductor at high-voltage side reverses and its magnitude equals V_{Co2}. In addition, the voltage across inductor L_1 is $V_{Cb1} - V_L$ while V_{Cb2} equals V_{Co2}/n. Applying volt-second balance criterion (VSBC) to L_1 yields

$$V_L = (1 - D_6) V_{Cb1} \tag{21}$$

Equation (21) can also be expressed as

$$V_L = \frac{(1 - D_6) V_{Co1}}{n} \tag{22}$$

Similarly, applying VSBC to magnetizing inductor L'_{m2}, the following relationships can be found:

$$V_{Co1} = (1 - D_6) V_H \tag{23}$$

and

$$V_{Co2} = D_6 V_H \tag{24}$$

Substituting Equation (23) into Equation (22) has the result:

$$M_{step\text{-}down} = \frac{V_L}{V_H} = \frac{(1 - D_6)^2}{n} \tag{25}$$

in which $M_{step\text{-}down}$ stands for the ratio of output to input voltage as in step-down mode. Figure 8a shows the curves of $M_{step\text{-}up}$ versus duty ratio D_1, while $M_{step\text{-}down}$ versus duty ratio D_6 is illustrated in Figure 8b.

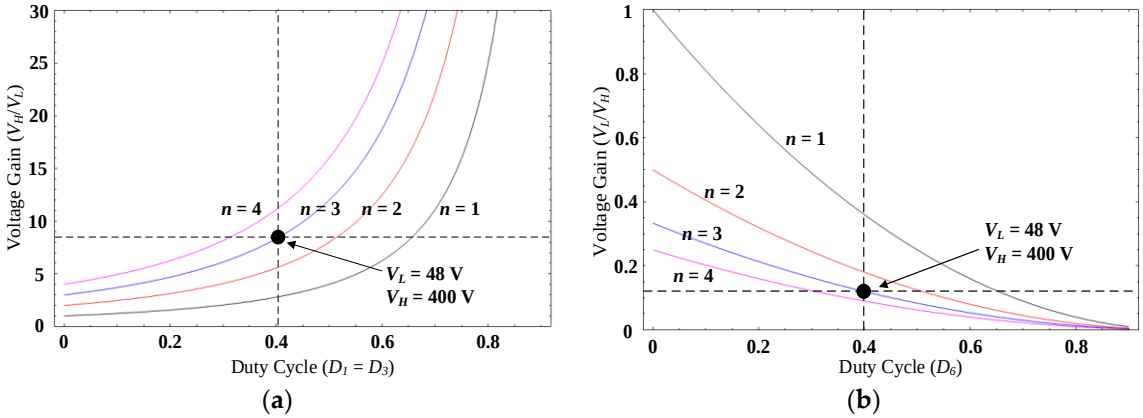

Figure 8. Voltage conversion ratio of the proposed bidirectional converter: (**a**) step-up mode; and (**b**) step-down mode.

The discussion relating to the voltage stresses of the semiconductor devices is followed up. Because the diode D_{S1} and switch S_2 conduct complementarily, from the mesh of C_{b1}-S_1-S_2, it can be found that voltage stress of S_1 is identical to that of S_2 and equals V_{Cb1}. Similarly, D_{S3} and S_4 are in complementary conduction, and the voltage stresses of S_3 and S_4 will be equal to V_{Cb2}. At high-voltage side, from the outermost loop, S_5-S_6-V_H, the input voltage V_H will impose on S_5 and S_6 alternately. That is, S_5 and S_6 have to stand a voltage of V_H.

The current gain of the converter is a reciprocal of the voltage ratio shown in Equation (25). Therefore, the input current I_H is given by

$$I_H = \frac{(1 - D_6)^2}{n} I_L = \frac{(1 - D_6)^2 V_L}{n R_L} \tag{26}$$

where R_L denotes the load resistance at low-voltage side. From Figure 5f, the average current of magnetizing inductance L'_{m2} is equals to $\frac{-i_{ds3}}{n} - i_{ds6}$, which can be further estimated by

$$I_{Lm2} = \frac{(1 - D_6) I_L}{n D_6} - \frac{I_H}{D_6} \tag{27}$$

In addition, the current decrement on L'_{m2} over one switching cycle, Δi_{Lm2}, can be expressed as

$$\Delta i_{Lm2} = \frac{D_6 T_s V_{Co1}}{L'_{m2}} \tag{28}$$

Using Equation (23) and Equation (25) to substitute for V_{Co1} yields

$$\Delta i_{Lm2} = \frac{D_6 T_s n V_L}{(1 - D_6) L'_{m2}} \tag{29}$$

The minimum value of i_{Lm2} can be calculated by $I_{Lm2} - \frac{\Delta i_{Lm2}}{2}$ and is computed as

$$I_{Lm2,min} = \frac{(1-D_6)V_L}{nR_L} - \frac{D_6 T_s n V_L}{2(1-D_6)L'_{m2}} \tag{30}$$

At boundary, $I_{Lm2,min} = 0$. Then, solving for L'_{m2} can obtain the following relation for determining the minimum inductance for CCM:

$$L'_{m2,min} = \frac{n^2 D_6 R_L}{2(1-D_6)^2 f_s} \tag{31}$$

In order to find the minimum value of L_1 for continuous current operation, $L_{1,min}$, the average current of L_1, I_{L1}, has to be found. The I_{L1} is equal to the output current I_L, which is given by

$$I_{L1} = \frac{V_L}{R_L} \tag{32}$$

The change on inductor current i_{L1} can be computed from

$$\Delta i_{L1} = \frac{D_6 T_s V_L}{L_1} \tag{33}$$

Accordingly, minimum of I_{L1} is

$$I_{L1,\min} = \frac{V_L}{R_L} - \frac{D_6 T_s V_L}{2L_1} \tag{34}$$

Let $I_{L1,min} = 0$ and solving for L_1 can obtains:

$$L_{1,min} = \frac{D_6 R_L}{2 f_s} \tag{35}$$

Assume that R_L is 9.216 Ω, f_s is 40 kHz, and $n = 3$. Figure 9a depicts the relationship between D_6 and L'_{m2}, while L_1 versus D_6 is illustrated in Figure 9b.

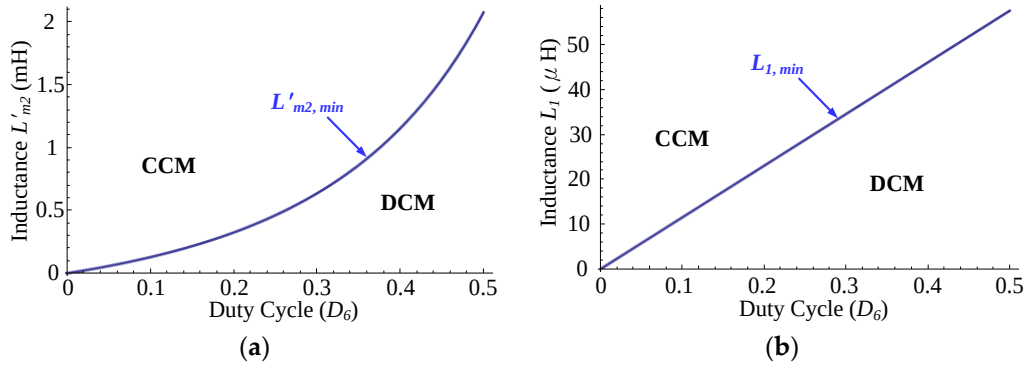

Figure 9. The relationship between the inductance and duty ratio D_6: (**a**) L'_{m2}; and (**b**) L_1.

Figure 10 is the equivalent circuit of proposed converter considering non-ideal parameters, in which r_{L1} represents the inductor resistance at the low voltage side and $r_{ds}1$, $r_{ds}2$, $r_{ds}3$, $r_{ds}4$, $r_{ds}5$, and $r_{ds}6$ are the on-state resistance of switches S_1, S_2, S_3, S_4, S_5, and S_6, respectively; and r_{lk1} and r_{lk2} are the primary winding resistances and the secondary one respectively. By using VSBC and ASBC, the non-ideal voltage conversion ratio $M'_{step\text{-}up}$ and conversion efficiency $\eta_{step\text{-}up}$ in step-up mode can be obtained as

$$M'_{Step\text{-}up} = \frac{-n(-2(1+D_1-D_3)f_s L_m+(-1+D_3)D_3(-2r_{ds4}+(-3+2D_3)r_{lk1}))}{2(-1+D_1)(-1+D_3)f_s L_m\left(1+\frac{n^2\left((-1+D_1)^2D_1r_{ds3}+D_3{}^3(r_{ds1}+D_1r_{L1})-2D_3{}^2\left((1+D_1)r_{ds1}+D_1\left(r_{ds2}-D_1r_{ds2}+r_{L1}+D_1r_{L1}+(-1+D_1)^2r_{lk1}\right)\right)+D_3\left((1+D_1)^2r_{ds1}+D_1\left(-3(-1+D_1)r_{ds2}+(1+D_1)^2r_{L1}+3(-1+D_1)^2r_{lk1}\right)\right)\right)}{(-1+D_1)^2D_1(-1+D_3)^2D_3R_H}+\frac{-\frac{r_{ds5}}{-1+D_1}+\frac{r_{ds6}}{D_3}+r_{lk2}}{R_H}\right)} \quad (36)$$

$$\eta_{Step\text{-}up} = M'_{Step\text{-}up}\left[\frac{(1-D_1)(1-D_3)}{n(1+D_1-D_3)}\right] \quad (37)$$

In addition, step-down voltage ratio $M'_{step\text{-}down}$ and efficiency $\eta_{step\text{-}down}$ are estimated by

$$M'_{Step\text{-}down} = \left[\frac{(-1+D_6)^2D_6nR_L}{(-1+D_6)^3(-r_{ds6}+D_6(r_{ds5}+r_{ds6}))+n^2(r_{ds1}+r_{ds3}+r_{lk1}+D_6(r_{ds2}-D_6r_{ds2}+(-2+D_6)r_{ds3}+R_L+r_{L1}+(-2+D_6)r_{lk1}))}\right] \quad (38)$$

$$\eta_{Step\text{-}down} = M'_{Step\text{-}down}\left[\frac{n}{(1-D_6)^2}\right] \quad (39)$$

Based on Equations (36) to (39), relationships of voltage gain versus duty ratios D_1 and D_3 in step-up mode are depicted in Figure 11a,b, respectively; meanwhile, so do Figure 11c,d for step-down operation. Figure 12 shows the non-ideal voltage gain in step-up mode under different choke resistances.

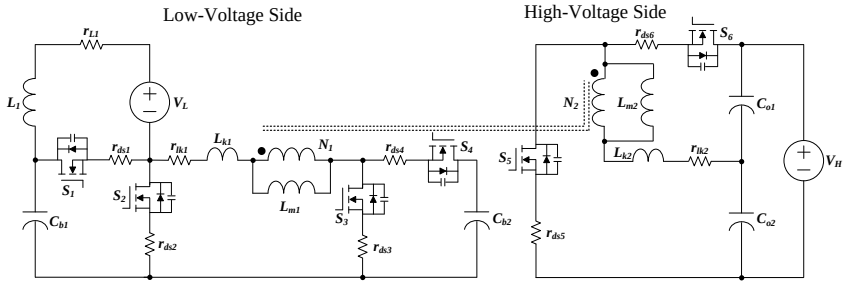

Figure 10. The non-ideal equivalent circuit of the converter.

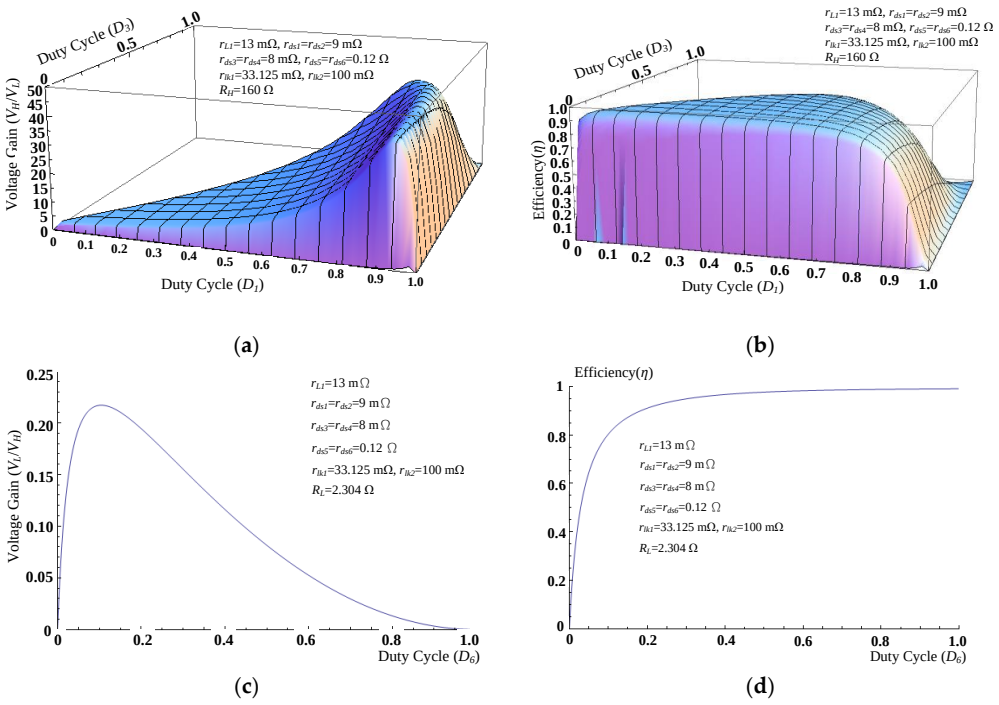

Figure 11. The relationships of voltage gain versus duty ratio and efficiency versus duty ratio while considering non-ideal effect: (**a**) $M'_{step\text{-}up}$; (**b**) $\eta_{step\text{-}up}$; (**c**) $M'_{step\text{-}down}$; and (**d**) $\eta_{step\text{-}down}$.

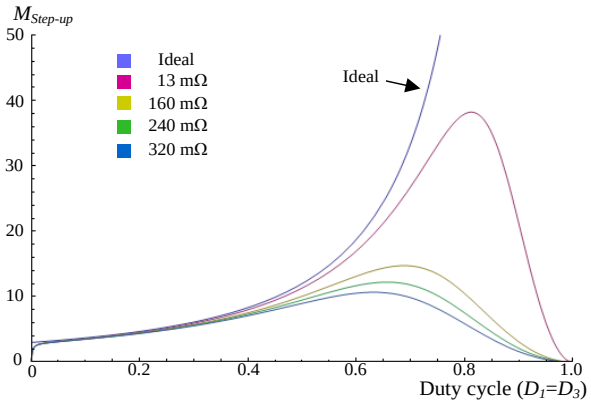

Figure 12. The step-up voltage gain under different choke resistances.

Among all power switches, the main switch S_1 will endure the maximum current stress no matter in step-up or step-down mode. Thereby, the current stress determination is focused on S_1. This current stress can be estimated by the sum of the valley current of inductor L_1 and the peak current of leakage inductance L_{k1}. That is,

$$I_{ds1,peak} = \frac{I_L(2-D_6)}{D_6} - \frac{V_L D_6}{2f_s L_1} \tag{40}$$

As for the current stresses of the other active switches in step-down mode, the ASBC should be applied to capacitors C_{o1}, C_{o2}, C_{b2}, and C_{b1}, which yields

$$I_{ds2,peak} = I_L \frac{2-D_6}{D_6} - \frac{V_L D_6}{2f_s L_1} \tag{41}$$

$$I_{ds3,peak} = I_{ds4,peak} = 2\frac{I_L(1-D_6)}{D_6} \tag{42}$$

$$I_{ds5,peak} = I_{ds6,peak} = \frac{I_L(1-D_6)(2+D_6)}{nD_6} - \frac{nD_6 V_L}{2(1-D_6)f_s L'_{m2}} \tag{43}$$

Similarly, in step-up mode, current stresses of switches can be expressed as

$$I_{ds1,peak} = \frac{nI_H\left[2(1-D_1+D_1D_3)-{D_3}^2\right]}{D_3(1-D_1)(1-D_3)} + \frac{V_L D_3}{2f_s L_1} \tag{44}$$

$$I_{ds2,peak} = nI_H \frac{2-D_3}{(1-D_1)(1-D_3)} + \frac{V_L D_1}{2f_s L_1} \tag{45}$$

$$I_{ds3,peak} = I_{ds4,peak} = nI_H \frac{2-D_3}{D_3(1-D_3)} + \frac{V_L D_3}{2f_s L'_{m1}(1-D_1)} \tag{46}$$

$$I_{ds5,peak} = \frac{2I_H}{(1-D_1)} \tag{47}$$

$$I_{ds6,peak} = \frac{2I_H}{D_3} \tag{48}$$

4. Experimental Results

To validate the proposed BDC, a 1-kW prototype is built with the specifications and components summarized in Table 2. If a converter operates in discontinuous conduction mode (DCM), it can easily avoid switching loss. However, during the interval of high power loading, serious conduction loss will result in unacceptable efficiency. The proposed converter intrinsically has the outstanding feature of

soft switching at all power switches even in CCM. Therefore, we design the converter operation from DCM into CCM at 250-W power loading for overall efficiency consideration. Accordingly, a Toroids 55195-A2 MPP core and an EE-55 core are adopted to form main inductor and coupled inductor, respectively. To make sure the CCM and DCM operate, as mentioned, the main inductance L_1 should be 46 μH and magnetizing inductance L'_{m1} is 130 μH with a turns ratio of n = 3.

Table 2. Specifications and components used in experimentations.

Symbols	Values & Types
V_L (Low voltage)	48 V
V_H (High voltage)	400 V
P_o (Output power)	1 kW
f_s (Switching frequency)	40 kHz
L_1 (Filter inductance)	46.2 μH
L'_{m1} (Magnetizing inductance)	130 μH
L_{k1} (Leakage inductance)	2.07 μH
L_{k2} (Leakage inductance)	18.82 μH
n (Transformer turns ratio)	3
C_{b1} and C_{b2} (Capacitances)	33 μF
C_{o1} and C_{o2} (Capacitances)	220 μF
S_1 and S_2 (Switches)	IXFH160N15T2
S_3 and S_4 (Switches)	IXTP160N075T
S_5 and S_6 (Switches)	IXFH52N50P2

According to the discussion in Section 3, voltage and current stresses of all active switches can be specified, which offers us a benefit to choose appropriate semiconductor devices for prototype constructing. Since a lower $R_{ds(on)}$ can achieve a higher conversion efficiency, active switches which meet the power rating and have conduction resistance as low as possible are considered. At low-voltage side, power MOSFETs IXFH160N15T2 with on-state resistance $R_{ds(on)}$ of 9 mΩ is chosen as S_1 and S_2, while IXTP160N075T with 6 mΩ $R_{ds(on)}$ as S_3 and S_4. With regard to the active switches S_5 and S_6 at high-voltage side, power MOSFET IXFH52N50P2 is considered, of which $R_{ds(on)}$ is 0.12 Ω. Microcontroller ATMEGA328P-PU is in charge of the converter controlling. Additionally, PV simulator Chroma 62050H-600S, high voltage power supply IDRC CDSP-500-010C, electronic load Chroma 63202 are adopted for terminal source or load. All waveforms are measured by oscilloscope KEYSIGHT DSOX4024A. Figure 12 shows the voltage and current waveforms measured from switches S_1–S_6, while D_1 = 0.44 and D_3 = 0.3. In Figure 13a, the first trace and second trace are the switch voltage and current of S_1, respectively, whereas the third and fourth traces depict the measurements of S_2. From Figure 13a, it can be found that S_1 endures a voltage of around 100 V. This value is consistent with the estimation in Equation (9). The measured i_{ds1} matches the conceptual waveform in Figure 4. In addition, the waveforms of v_{ds2} and i_{ds2} release that ZCS turn-off feature is achieved at S_2. Figure 13b presents the practical measurements of v_{ds3}, i_{ds3}, v_{ds4}, and i_{ds4}, which illustrates that both switches S_3 and S_4 can be turned on with ZVS. While operated in step-up mode, S_5 and S_6 of the converter are in the role of rectifier. Figure 13c presents the zoomed-in waveforms of S_1 and S_2, and Figure 13d is for S_3 and S_4. The blocking voltages of v_{ds5} and v_{ds6} are both equal to 400 V, as shown in Figure 13e, which conforms to the calculation of Equation (11). Figure 13f confirms a stable output and CCM operation in L_1; moreover, the measurements of i_{Lk1} and i_{Lk2} are consistent with the waveforms in Figure 4.

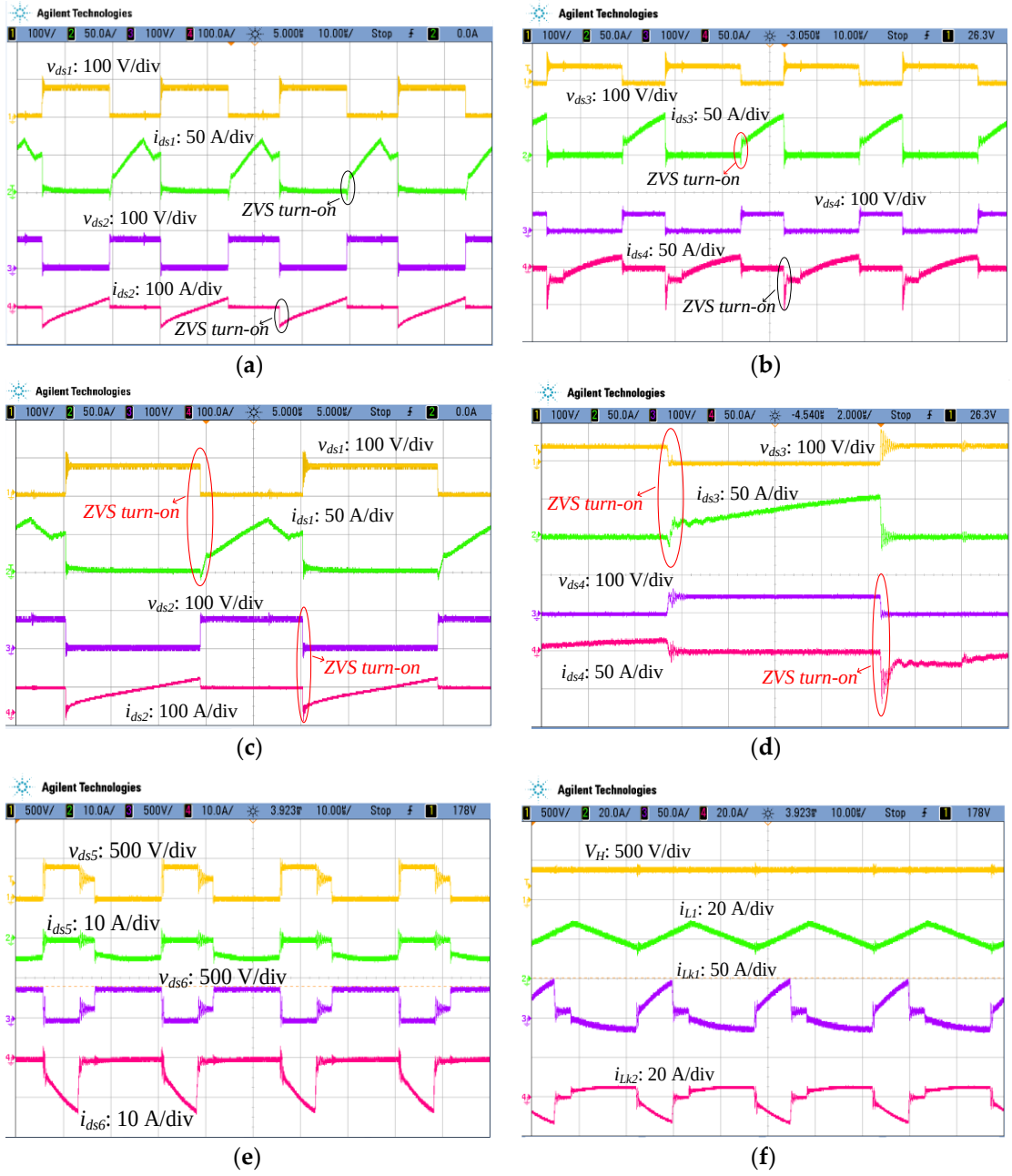

Figure 13. Experimental results in step-up mode operation at P_o = 1 kW: (**a**) measurements from S_1 and S_2; (**b**) measurements from S_3 and S_4; (**c**) zoomed-in waveforms measured from S_1 and S_2; (**d**) zoomed-in waveforms of S_3 and S_4; (**e**) measurements from S_5 and S_6; and (**f**) waveforms of V_H, i_{L1}, i_{Lk1}, and i_{Lk2}.

While operating in step-down mode with D_6 = 0.37, related practical waveforms are shown in Figure 14. From Figure 14a,b, it can be seen that both switches S_1 and S_3 are just in charge of rectifying whereas S_2 and S_4 can accomplish ZCS turn-off feature. Figure 14c reveals that S_5 and S_6 are turned on with ZVS and their voltage stresses are about 400 V. The output voltage at low-voltage side and the currents of L_1, L_{k1}, and L_{k2} are also given in Figure 14d, in which a constant 48 V output and CCM operation in L_1 are illustrated.

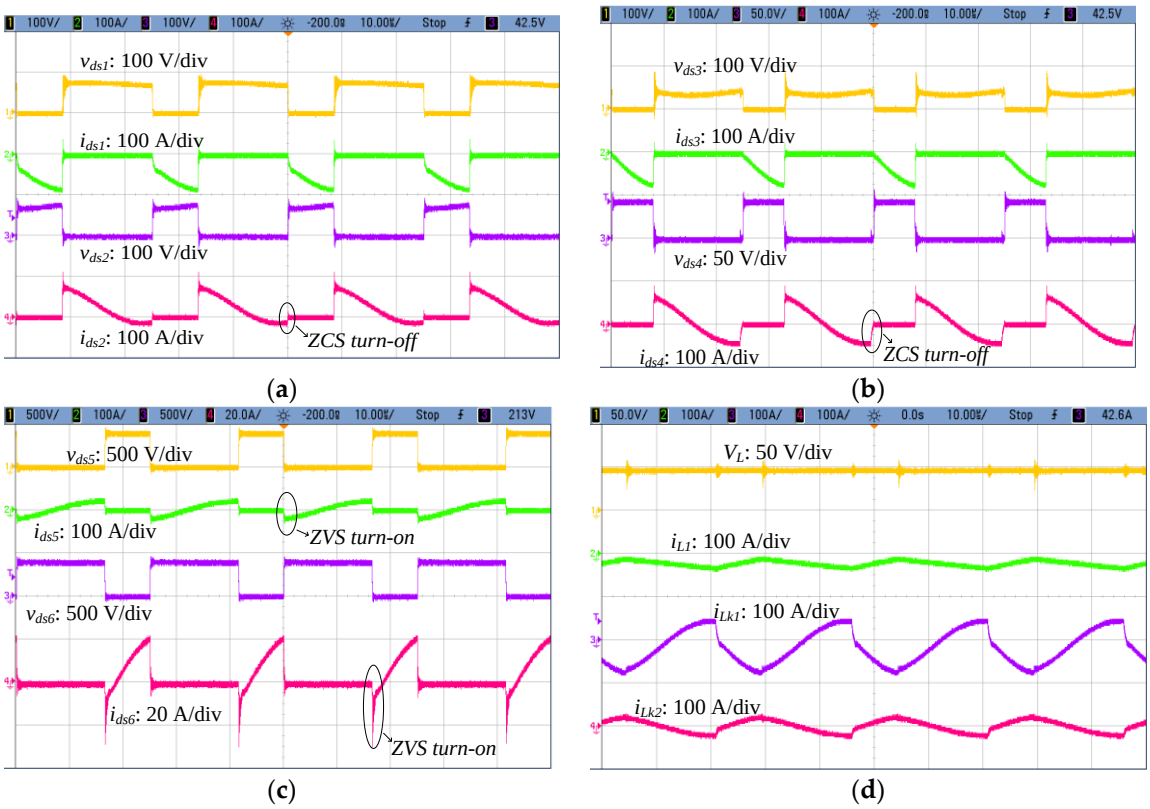

Figure 14. Experimental results in step-down mode operation at P_o = 1 kW: (**a**) measurements from S_1 and S_2; (**b**) S_3 and S_4; and (**c**) S_5 and S_6; and (**d**) the waveforms of V_L, i_{L1}, i_{Lk1}, and i_{Lk2}.

Figure 15 depicts measured efficiency of the prototype. The maximum values of the practical efficiency in step-up and step-down modes are up to 95.4% and 93.6%, respectively, while P_o is equal to 1 kW. The efficiency values are measured after 1hr burn-in test and the maximum temperature of all active components is around 56 °C. Figure 16 shows the photo of the prototype, where its length, width, and height are 17.2, 14.6, and 4.2 cm in turn. Therefore, its power density is 948.13 kW/m^3. In addition, the converter's weight is 0.985 kg. That is, specific power is 1.015 kW/kg.

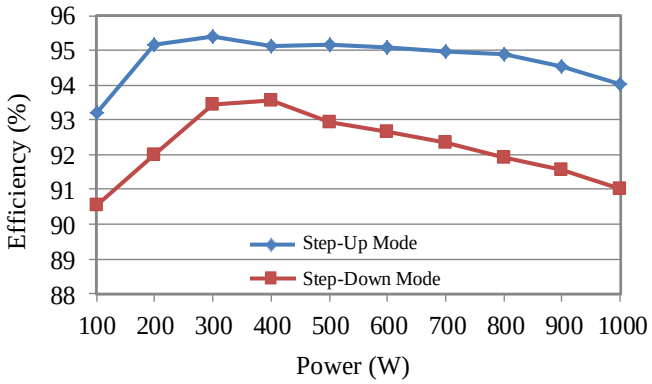

Figure 15. Measured efficiency of the proposed bidirectional DC-DC converter.

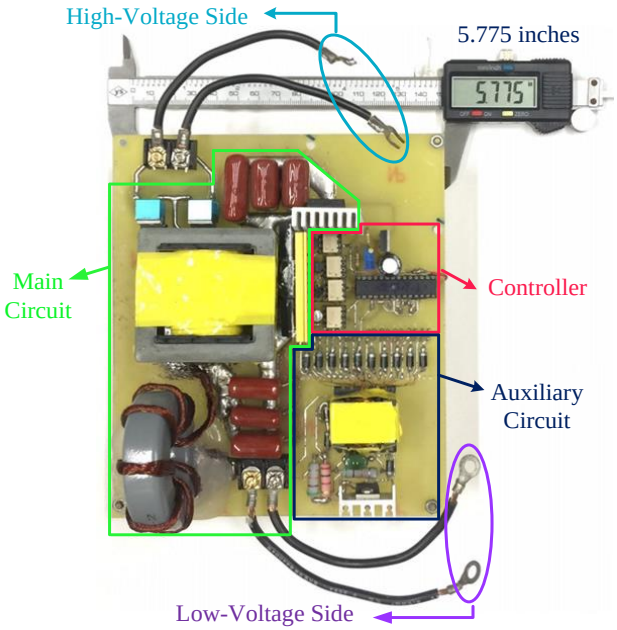

Figure 16. The photo of the experimental setup.

Table 3 summarizes the comparison of the proposed converter with other bidirectional converters in [24–27]. The proposed converter has the better features such as galvanic isolation, soft switching at all switches, no any diode required, and high voltage-ratio conversion. For example, in step-up mode and under the conditions that n = 3 and duty cycle is 0.5 (in addition, $D_1 = D_3$ in the proposed converter), the proposed one can achieve a much higher voltage gain up to 12 while those in [24–27] are 11, 3, 6, and 12, respectively. For clearer presentation, the plots to express the comparison result among the mentioned converters are shown in Figure 17. In high conversion ratio converters, current-sharing path structure along with interleaved control can suppress current ripples and then lowers current stress and conduction loss [27–30]. However, bi-directional power flow controlling or more power components needed are still their demerits.

Table 3. Performance comparisons of proposed BDC with other bidirectional DC-DC converters proposed in [25–27].

References	**[24]**	**[25]**	**[26]**	**[27]**	**Proposed**
Topology	**Non-Isolated**	**Isolated**	**Isolated**	**Isolated**	**Isolated**
Voltage conversion ratio in step-up mode (V_H/V_L)	$[(1+n)/(1-D)]+n$	n	$n/(1-D)$	$2n/(1-D)$	$[n(1+D_1-D_3)]/[(1-D_1)(1-D_3)]$
Voltage conversion ratio in step-down mode (V_L/V_H)	$D/(1+n+nD)$	$1/n$	$(1-D)/n$	$(1-D)/2n$	$(1-D_6)^2/n$
Output power	200 W	500 W	1 kW	1.5 kW	1 kW
Number of MOSFETs	5	8	4	8	6
Number of diodes	0	0	2	0	0
Number of inductors	0	1	1	0	1
Number of coupled inductors	1	1	1	2	1
Number of capacitors	3	1	4	5	4
Full-load efficiency (Step-up/step-down)	93%/90%	92.4%/91.7%	85%/89%	96.5%/95.8%	94.1%/91%

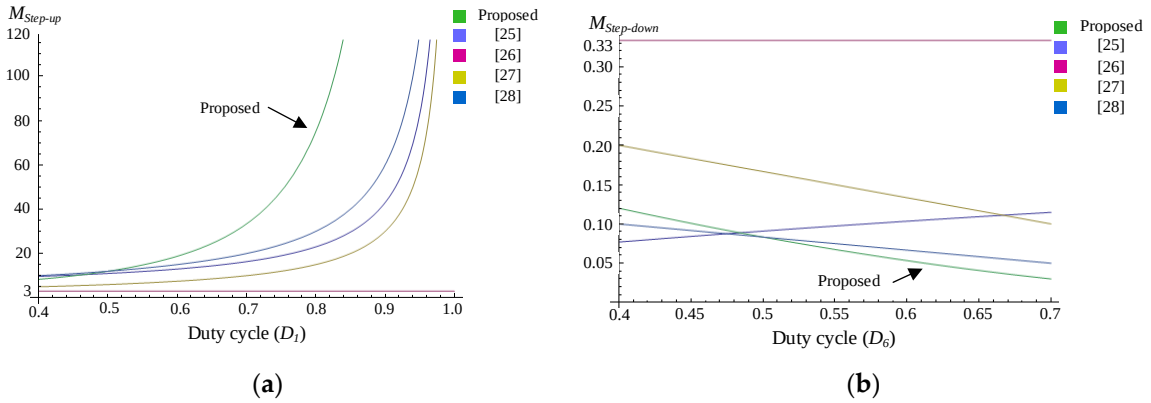

Figure 17. The comparison plots of conversion ratio: (**a**) step-up mode; and (**b**) step-down mode.

5. Conclusions

This paper has proposed a high efficiency and high voltage-ratio isolated bidirectional DC-DC converter. A coupled inductor is employed for achieving galvanic isolation, in which the energy stored in leakage inductor can be recycled without additional components. The main contribution of this paper is that voltage stress across semiconductor devices can be lowered by adjusting duty ratio, all power switches can complete soft switching feature in step-up and step-down modes, and higher voltage conversion can inherently be achieved. Because semiconductor device endures low voltage stress, MOSFETs with low $R_{ds,on}$ can be employed. Unlike conventional converters whose voltage gain is merely determined by a fixed duty ratio, the proposed converter has the ability of compromising the duty ratios of switches at primary side to meet a certain voltage gain and to find an available power component. Operation principle of the circuit and detailed derivation of voltage gain, voltage stress, and current stress are carried out. Finally, experimental results measured from a 1-kW prototype have verified the theoretical analysis and feasibility.

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