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A High-Frequency Isolated Online Uninterruptible Power Supply (UPS) System with Small Battery Bank for Low Power Applications

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Abstract: Uninterruptible power supplies (UPSs) are widely used to deliver reliable and high quality power to critical loads under all grid conditions. This paper proposes a high-frequency isolated online UPS system for low power applications. The proposed UPS consists of a single-stage AC-DC converter, boost DC-DC converter, and an inverter. The single-stage AC-DC converter provides galvanic isolation, input power factor correction, and continuous conduction of both input and output current. The low battery bank voltage is stepped up to high dc-link voltage by employing a high voltage gain boost converter, thus allows the reduction of battery bank to only 24 V parallel connected batteries. Operating batteries in parallel improves the battery performance and resolves the issues related to conventional battery banks that arrange the batteries in series combination. The inverter provides regulated output voltage to the load. A new cascaded slide mode (SM) and proportional-resonant (PR) control for the inverter has been proposed, which regulates the output voltage for both linear and non-linear loads. The controller shows excellent performance during load transients and step changes. Besides, the controller for boost converter and AC-DC converter is presented. Operating principle and experimental results of 1 kVA laboratory setup have been presented for the validation of proposed system.

Keywords: uninterruptible power supply (UPS); single-stage AC-DC converter; high-frequency isolation; boost converter; power factor correction

1. Introduction

Uninterruptible power supplies (UPSs) deliver clean, conditioned, and reliable power to critical loads such as communication systems, network servers, medical equipment, etc. [1]. Typically, the UPS provides unity power factor, high efficiency, high reliability, low cost, and continuous power supply, irrespective of the grid conditions [2–4].

UPS systems can be categorized as online, offline, and line interactive UPS systems [5]. Among them online UPS systems are the most popular and common configuration, as they provide isolation to the load from the grid and have negligible switching times. A conventional online UPS system consists of a rectifier for PFC, battery bank, and an inverter connected with the load. Grid frequency transformers are normally employed to reduce the battery bank voltage and provide isolation from

the transients and spikes generated inside the grid. Since the transformer is operating at the grid frequency, it increases the volumetric size and weight of the system significantly.

High-frequency transformer-based UPSs offer an effective solution to the problems mentioned above by reducing the size of the system as well as providing suitable galvanic isolation between the load and grid. Besides, these UPS systems have high power factor correction, zero voltage switching (ZVS) of the chopper and converter stage, and low-cost design [6,7]. However, due to high dc-link voltage, several batteries are connected in a series arrangement, which reduces the reliability of the system.

Table 1. Comparison of high-frequency transformer UPSs for different battery banks.

Reference	Rated Power	Input/Output Voltage	Battery Bank Voltage	Number of Batteries
[8]	300 VA	120	48	4
[9]	2 kVA	220	108	9
[10]	150 VA	120	48	4
[11]	2 kVA	110	180	15
[12]	3.3 kVA	220	120	10

Table 1 shows a comparison of the different high-frequency transformer-based UPS with series connected batteries. Series battery arrangement has major drawbacks and limitations in charging and discharging. A small imbalance in voltages occurs across the battery cells during charging and discharging because the voltages across each cell is not equal. Hence, their performance is different during charging and discharging operations. Severe overheating, low performance, and even destruction may be caused by battery overcharging [13]. Similarly, deep discharge will permanently damage the battery cells [14]. Due to this reason, a small battery bank with batteries operating in parallel improves the performance of the battery bank significantly. The batteries operating in parallel have the following advantages:

(1) The number of batteries is not restricted to the dc-link voltage. The volume, weight, and backup time of the battery bank should be designed according to the specific application.
(2) Cost reduction as no extra voltage balancing circuit is required.
(3) Damaged batteries can be isolated or replaced in the battery bank leaving the sensitive system operation uninterrupted. This is a prime function of UPS systems.
(4) Since the discharging currents of the batteries can be profiled individually, hence the stored energy in the batteries can be utilized more efficiently.

In this paper, a new high-frequency isolated online UPS system configuration is proposed. The proposed UPS consists of a single-stage AC-DC converter, DC-DC boost converter, and H-bridge inverter as shown in Figure 1. The single-stage AC-DC converter provides galvanic isolation, high input power factor, continuous flow of input and output current, with minimum semiconductor devices within the circuit. A high-gain DC-DC converter is introduced to step up the low battery bank voltage to high dc-link voltage in order to feed it to the inverter. This allows the use of a low voltage battery bank in the UPS system. Besides, the converter follows the condition of ZVS and synchronous rectification (SR), which increases the system efficiency. A new cascaded slide mode (SM) and proportional-resonant (PR) controller have been implemented in the inverter control which show good performance with low total harmonics distortion (THD) and high stability for both non-linear and impulsive loads. The volumetric size and cost of the proposed system are comparatively very small as no bulky grid frequency transformer has been used, with a small battery bank, and high efficiency. Hence, the proposed UPS system with its low cost and weight is an excellent choice for low power applications. A 1 kVA laboratory prototype has been constructed to verify the performance of the system. The proposed UPS system shows excellent steady state and dynamic performance.

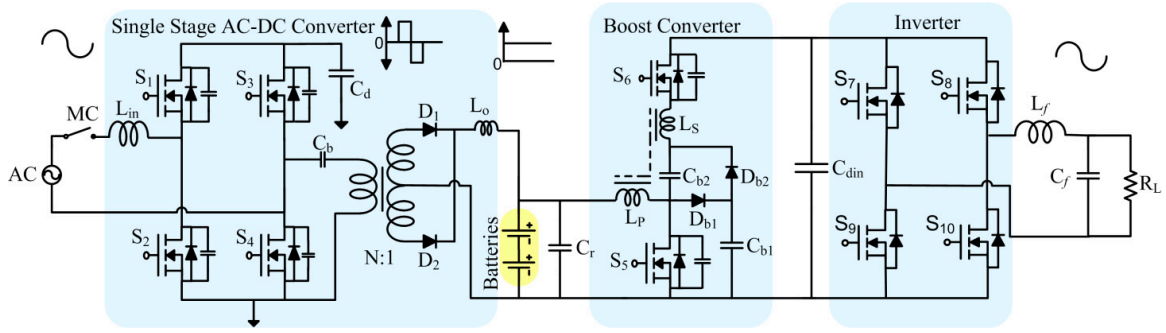


Figure 1. Circuit diagram of the proposed UPS system.

2. Circuit Description

The proposed system consists of a single-stage AC-DC converter at the front end, a H-bridge inverter at the back end, and a high-gain boost converter connected with the battery bank of the UPS system. The single-stage AC-DC converter provides rectification, with power factor correction (PFC) as well as high-frequency isolation between the load and grid. The boost converter with high-voltage gain steps up the low battery bank voltage to high dc-link voltage in order to feed it to the inverter. The H-bridge inverter with a new robust control scheme is proposed for operation under the non-linear loading condition and provides the fast transient response during change of modes.

2.1. Modes of Operation

The UPS operates in two modes, i.e., grid mode and battery mode, as shown in the Figure 2.

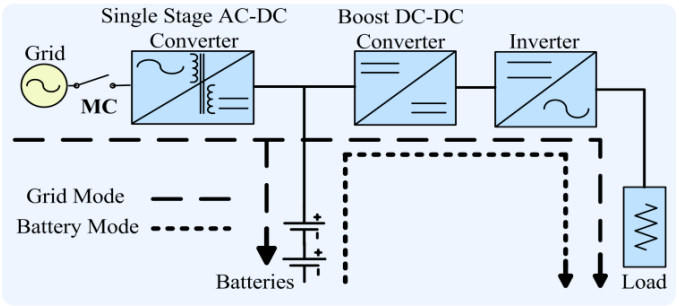


Figure 2. Modes of operation of proposed UPS system.

2.1.1. Grid Mode

When the grid voltage is stable and there is no power failure, the UPS system operates in grid mode. The single-stage AC-DC converter regulates the voltage across C_r. Meanwhile; the boost converter steps up battery bank voltage across C_r and provides it to the inverter. The inverter provides regulated output voltage to the connected load.

2.1.2. Battery Mode

In case of utility power disruption or any voltage sag, the magnetic contactor (MC) is opened, and the single-stage AC-DC converter stops operation. Now the battery supplies power to the load via the boost converter and inverter connected to it. The arrangement of the battery is such that it provides uninterruptible energy to the boost converter at the time of utility line failure. The value of the dc-link capacitor is kept high in order to provide sufficient energy to the inverter during the transition between the power modes.

A bypass switch has been added in the system to increase the reliability of the system. In case of internal faults in the system or overloading and overheating of the circuit, the bypass switch turns ON and provides a direct path for the power from the utility grid to the connected load [15].

2.2. AC-DC Converter

A number of single-stage AC/DC converters have been proposed in the literature [16–21]. Commonly a full bridge diode rectifier has been employed at the front-end of DC/DC converters [22–26], but four diodes operating at line frequency results in high conduction losses, thus dropping the efficiency of the converter. In order to eliminate the aforementioned problems, a bridgeless single-stage PFC AC/DC converter has been implemented in our design.

In [27], a bridgeless single-stage half bridge AC/DC converter has been proposed. It uses only two active switches and two diodes as passive switches to achieve the AC/DC conversion with reduced size and efficient operation. However, the circuit operates in DCM and is not suitable for high power applications. A totem-pole bridgeless PFC connected with high frequency linked DC/DC regulator has been analyzed in [28]. The dc-link capacitor is reduced, which helps in reducing the total cost and size of the system, but the circuit still operates under critical conduction mode of operation.

A single-stage AC/DC converter has been proposed in [29]. The converter operates in continuous condition mode (CCM) and is designed for high power applications, but extra diodes have been used in the circuit which reduces the overall efficiency of the circuit. Also, two separate controllers have been used, which increases the cost and complexity of the circuit.

A new AC-DC converter topology has been introduced, which combines an asymmetrical dc-dc converter with a half bridge PFC rectifier forming a single-stage AC-DC converter. No front end diode rectifier has been used in the circuit. Using the proposed converter, galvanic isolation as well as high efficiency are achieved with only four active switches that reduces the volumetric size of the circuit considerably. Other features of the single-stage converters include continuous conduction of the input and output current, ZVS condition, and excellent input power factor.

The operation of the AC-DC converter in both the positive and negative cycle is symmetrical. Therefore, only the positive cycle is considered in the discussion. Duty cycle D controls the switches S_2 and S_3, while duty cycle (1-D) controls switches S_1 and S_4. Figure 3 presents the waveforms and operating modes of the AC-DC converter.

2.2.1. Mode 1

In this mode, switches S_2 and S_3 turn ON under ZVS conditions. The boost inductor L_{in} is charged by input AC line voltage V_{in} through the switch S_2 and S_3. The inductor current is represented by the following equation:

$$\Delta i_{Lin} = \frac{1}{L_{in}}(V_{in} + V_d)DT_s \tag{1}$$

The blocking capacitor C_b is charged by the dc-link capacitor C_d through S_3 and the secondary side of the high-frequency transformer is fed by the energy stored in the magnetizing inductor L_m. The magnetizing inductor current i_{Lm} is represented under the initial condition $i_{Lm}(0)$ by Equation (2):

$$i_{Lm}(t) = i_{Lm}(0) + \frac{(V_d - V_b)DT_s}{L_m} \tag{2}$$

The secondary voltage is $V_{sec1} = -\frac{N_s}{N_p}V_p = -\frac{N_s}{N_p}(V_d - V_b)$, $V_{sec2} = \frac{N_s}{N_p}(V_d - V_b)$. The current through the diode D_1 is same as the output filter inductor current, and is given as:

$$i_{D1} = i_{Lo}(\max) = i_{Lo}(0) + \frac{1}{L_o}(N(V_d - V_b) - V_{out})DT_s \tag{3}$$

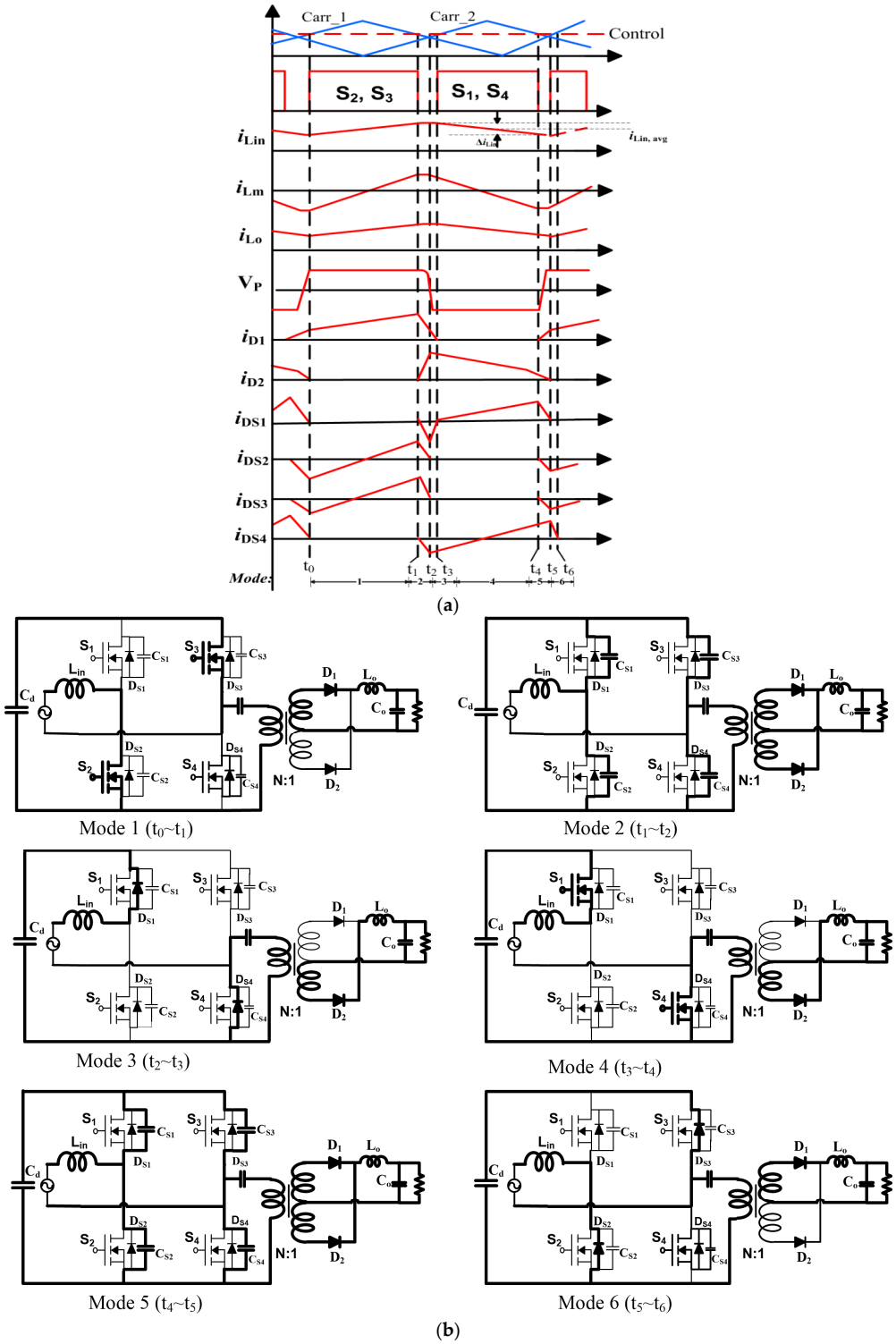


Figure 3. Single-stage AC-DC Converter: (**a**) Operation waveforms; (**b**) Modes of operation during one switching cycle T_S.

2.2.2. Mode 2

Both the switches S_2 and S_3 turn OFF during this mode. The parasitic capacitance C_{S2} is charged and C_{S1} is discharged using inductor current i_{Lin}. Similarly, the capacitance C_{S3} is charged and capacitance C_{S4} is discharged by the primary current i_P of the transformer.

The voltage across the switches S_1 and S_4 reduces to zero while the voltage across the switch S_2 and S_3 increases to V_d. At the secondary side, the output filter inductor current freewheels through the diodes D_1 and D_2.

2.2.3. Mode 3

In Mode 3, the dc-link film capacitor C_d starts charging by getting energy from the boost inductor and as a result i_{Lin} starts decreasing. As the voltage across S_1 reduces to 0, the body diode D_{S1} turns ON. Similarly, the blocking capacitor is fed by the magnetizing inductance L_m through the body diode D_{S4}. As a result, i_{Lm} will induce the flux in the high-frequency transformer secondary winding, and the power will be fed to the output capacitor C_r.

2.2.4. Mode 4

In the start of Mode 4, both the switches S_1 and S_4 turn ON following the ZVS condition. The DC-link capacitor C_d is charged by the stored energy released by the boost inductor L_{in}. The inductor current is given by:

$$\Delta i_{Lin} = \frac{1}{L_{in}}(V_{in} - V_d)(1 - D)T_s \tag{4}$$

The input current flows through L_{in}, S_1, C_d, and S_2. Similarly, the magnetising current i_{Lm} starts decreasing from maximum as represented by the following Equation (5):

$$i_{Lm}(t) = i_{Lm}(\max) - \frac{V_b}{L_m}(1 - D)T_s \tag{5}$$

The high-frequency transformer secondary winding feed energy to the output capacitor D_2. The output filter inductor current i_{LO} is represented by Equation (6):

$$i_{Lo} = i_{Lo}(t) = i_{Lo}(0) - \frac{1}{L_o}N(V_d - V_b)(1 - D)T_s \tag{6}$$

2.2.5. Mode 5

In Mode 5, the switches S_1 and S_4 turn OFF. The parasitic capacitor C_{S2} is discharged and C_{S1} is charged by both the current from the transformer primary windings and the input inductor L_{in} to and from V_d, respectively. Now the voltage across S_2 is zero, and the voltage across S_1 is V_d. Similarly, the capacitance C_{S4} is charged and C_{S3} is discharged by the primary current i_P of the transformer. Thus, the voltage across S_4 is V_d. At the secondary side, the output filter current freewheels through the diode D_1 and D_2.

2.2.6. Mode 6

In Mode 6, the body diode D_{S2} turns ON because of charging of the inductor. Similarly, the voltage across the switch S_3 is zero. This causes the body diode D_{S3} to be turned ON and the primary current starts flowing through it. In the end of Mode 6, both the S_2 and S_3 turn ON under the condition of ZVS.

2.2.7. Continuous condition mode (CCM) of operation of input inductor

The proposed AC-DC converter operates in CCM with continuous input current. The minimum inductor for CCM operation can be determined by (7):

$$L_{in} > \frac{V_d^2 T_s D(1 - D)^2}{2P_o} \tag{7}$$

The average current ripple is given by Equation (8):

$$\Delta i_{L_{in}} = \frac{|V_m \sin \omega t| DT_s}{2L_{in}} \tag{8}$$

The peak current is given by (9):

$$i_{L_{in}}\big|_{peak} = i_{L_{in}(avg)} + \Delta i_{L_{in}} = \frac{|V_m \sin \omega t|}{R_e} + \frac{|V_m \sin \omega t| DT_s}{2L_{in}} \tag{9}$$

where R_e is the emulative resistance of the converter. Equation (9) shows that the inductor peak current is not very high because large value of inductor is selected which maintains the continuous conduction.

2.2.8. Discontinuous conduction mode (DCM) of operation of the input inductor

If the proposed UPS system is designed for low power applications, the input inductor can be operated in discontinuous conduction mode [30]. The peak boost inductor current follows the line voltage with a fixed duty ratio to supply the output power for a constant output voltage. Suppose the converter is lossless and the duty ratio is fixed, the boost inductor L_b should be determined by (10):

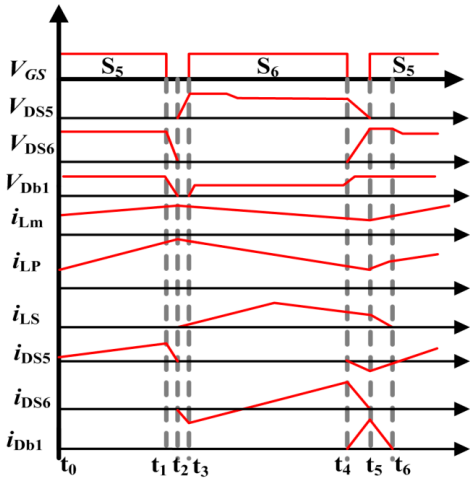
$$L_{in} < \frac{V_{in}^2 DT_s}{2P_o} \tag{10}$$

where P_o is the maximum output power. For positive line period, the peak boost inductor current during T_S is expressed as (11):

$$i_{Lb,\ peak} = \frac{V_{in} DT_s}{L_b} \tag{11}$$

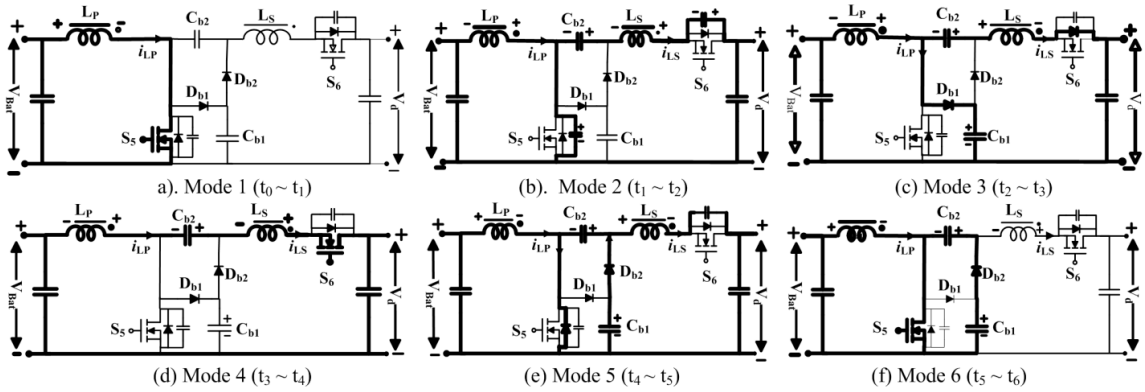
2.3. Boost Converter

A high-gain DC-DC converter has been introduced to obtain high dc-link voltage from the low voltage battery bank [31]. SR has been applied to decrease the conduction losses and force the circuit to operate under ZVS conduction. In order to get the high-voltage gain, coupled inductor is utilized with L_P and L_S as primary and secondary winding inductance respectively. The characteristic waveform and modes of operation of the DC-DC converter is shown in the Figure 4.



(**A**) Characteristic waveform of the boost converter

Figure 4. *Cont.*



(**B**) Topological stages: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; (**f**) Mode 6

Figure 4. DC-DC boost converter; (**A**) Characteristic waveform; (**B**) Topological stages.

2.3.1. Mode 1 (t_0~t_1)

During Mode 1, the switch S_5 is ON, while the switch S_6 is OFF. Low battery bank voltage is applied at the input of the DC-DC boost converter. Capacitor C_{b2} remains charged before Mode 1 and the magnetizing current i_{Lm} of the coupled inductor increases linearly, as shown in the Figure 5.

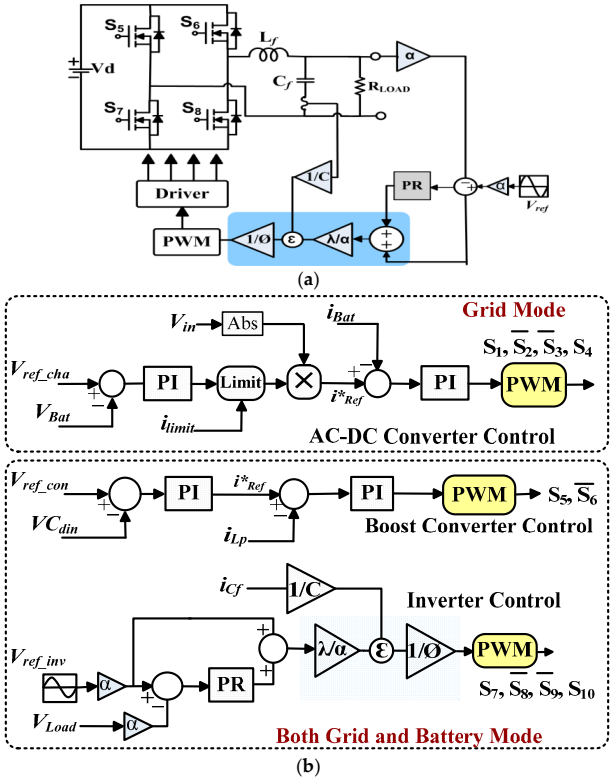


Figure 5. Proposed control scheme: (**a**) Inverter control; (**b**) Control circuit UPS system.

Applying KVL, we get:

$$V_L = V_{Lp} = V_{LS}/N \tag{12}$$

The voltage across the primary winding can be find using voltage second balance:

$$V_{LP}(1 - D) = V_L D \tag{13}$$

2.3.2. Mode 2 (t_1~t_2)

The switch S_5 turns OFF in Mode 2. The primary current i_{LP} charges the parasitic capacitance across the switch S_5 and the secondary current i_{LS} discharges the parasitic capacitance across switch S_6. When the voltage across switch S_5 equals to the capacitor voltage V_{Cb1}, this mode finishes.

2.3.3. Mode 3 (t_2~t_3)

Since the switch S_5 is OFF, the primary current i_{LP} decreases due to leakage inductance. However, the secondary current i_{LS} increases, which results in the turning ON of the body diode of switch S_6. As the voltage across the switch S_5 is higher than capacitor C_{b1}, it charges C_{b1} through diode D_{b1}. Hence, the voltage stress across the switch S_5 has been reduced. V_{Cb1} is the voltage across the capacitor C_{b1}, and is represented by Equation (14):

$$V_{Cb1} = V_L + V_{LP} \tag{14}$$

Using (13):

$$V_{Cb1} = V_L/(1-D) \tag{15}$$

2.3.4. Mode 4 (t_3~t_4)

In Mode 4, the switch S_6 turns ON under ZVS conditions. Both the windings of the coupled inductor and the capacitor C_{b2} series connected together transfer maximum energy to the output capacitor C_{din} of the converter. The i_{LS} starts increasing until it reaches the i_{LP}, then it follows the i_{LP} till the end of the Mode 4. Thus, the energy stored in both the windings of the coupled inductor discharges across the high voltage side of the circuit. D_{b1} and D_{b2} are reverse biased during this mode. Applying voltage second balance, we get Equation (16):

$$V_H = V_L + V_{LS} + V_{Cb2} + V_{Lp} \tag{16}$$

$$V_H = V_L + V_{Cb2} + (N+1)V_{LP} \tag{17}$$

2.3.5. Mode 5 (t_4~t_5)

During this mode, the switch S_6 turns OFF. The current i_{LS} charges the parasitic capacitance of the switch S_6. Capacitor C_{b2} is charged by the capacitor C_{b1} through the diode D_{b2}:

$$V_{Cb2} = V_{Cb1} = V_L/(1-D) \tag{18}$$

By substituting (13) and (18) into (17), presents the voltage gain of the converter:

$$V_H = V_L + V_L/(1-D) + (N+1)D/(1-D)V_L \tag{19}$$

$$G_{boost} = V_H/V_L = (2+ND)/(1-D) \tag{20}$$

The body diode of the switch S_5 turns ON because of the polarities of capacitor C_{b2} and inductor L_P.

2.3.6. Mode 6 (t_5~t_6)

During this mode, the switch S_5 turns to ON state under ZVS conditions. Since no current is derived by switch S_5 from the clamped circuit, thus the switching losses remains low due to ZVS, results in increasing the efficiency of the converter. Mode 6 finishes at the point when both the V_{Cb1} and V_{Cb2} become equal. The turn ratio N = 4 is selected to satisfy the G_{boost} gain in order to step up the battery bank voltage to required dc-link of inverter.

3. Control Strategy

The control schemes for regulating different parts of the proposed UPS, in different modes of operation are shown in Figure 5. The control scheme for inverter and boost converter keeps operating in both the normal and battery powered mode. On the other hand, for a single-stage converter the control scheme operates only in normal mode of operation for charging the battery as well as supplying power to the boost converter.

3.1. Inverter Control

A conventional full bridge voltage source inverter has been used to perform DC to AC conversion. SM control is famous for its excellent performance against non-linear loading conditions. SMC is also robust in operation and easy to implement for a full bridge inverter. In order to control the output voltage of the inverter, cascaded control algorithm of SMC and PR has been proposed for the control of inverter. The inner current loop is controlled by the SM control while the outer voltage loop is controlled by the PR control. Smoothed control law in narrow boundary layer has been used to eliminate the phenomena of chattering SMC. The smoothed control law is applied to the pulse width modulator that results in the fixed switching frequency of the inverter. Thus, the proposed controller adopted the characteristic of both SMC and PR control.

The circuit diagram of a single phase inverter with LC filter and proposed controller for non-linear load is shown in Figure 5a, where V_d is the applied DC-link voltage, V_{out} the filter capacitor C_f output voltage. i_{Lf} is the inductor L_f current and i_o the output current through the load R, given by $i_o = V_{out}/R_{Load}$. The state equations of the inverter are given as:

$$\frac{d}{dt}\begin{bmatrix} V_{out} \\ i_{Lf} \end{bmatrix} = \begin{bmatrix} 0 & 1/C_f \\ 1/L_f & 0 \end{bmatrix}\begin{bmatrix} V_{out} \\ i_{Lf} \end{bmatrix} + \begin{bmatrix} 0 \\ V_d/L_f \end{bmatrix} u + \begin{bmatrix} 0 \\ i_o/C_f \end{bmatrix} \tag{21}$$

where $u = Control\ input = \{-1,\ 0,\ +1\}$.

In order to implement the sliding mode control, the voltage error x_1, and its derivative $x_2 = \dot{x}_1$ need to be find:

$$x_1 = V_{out} - V_{ref} \tag{22}$$

$$x_2 = \dot{x}_1 = \dot{V}_{out} - \dot{V}_{ref} = {}^{i_{Cf}}/_{C_f} - \dot{V}_{ref} \tag{23}$$

where $V_{ref} = V_m \sin(\omega t)$. Consider the slide surface equation:

$$S = \lambda x_1 + x_2 \tag{24}$$

Now to apply the sliding control law to the inverter, putting the value of x_1 and x_2:

$$S = \lambda\left(V_{out} - V_{ref}\right) + \frac{i_{Cf}}{C_f} - \dot{V}_{ref} \tag{25}$$

$$S = \lambda\left(V_{out} - V_{ref}\right) + \frac{1}{C_f}\left(i_{Cf} - i_{ref}\right) \tag{26}$$

The sliding mode controller has the common inherent property of chattering. Chattering affects the control accuracy and reduces the efficiency of the circuit. In order to overcome the chattering, a smoothed SM control has been implemented. This can be achieved by smoothing out the control discontinuity in a thin boundary layer neighboring the sliding surface:

$$B(t) = \{x, |S(x;t)| \leq \varnothing\}\ \varnothing > 0 \tag{27}$$

where $\varnothing$ is the boundary layer thickness and $\varepsilon = \frac{\varnothing}{\lambda}$ is the boundary layer width. Hence, interpolating S inside $B(t)$, for instance, and replacing S by an expression $S/\varnothing$, Equation (26) will be:

$$\frac{S(x)}{\varnothing} = \frac{\lambda}{\varnothing}\left[V_{out} - V_{ref}\right] + \frac{1}{C_f \varnothing}\left[i_{Cf} - i_{ref}\right] \tag{28}$$

The smoothing control discontinuity assigns a low pass filter structure to the local dynamics thus eliminating chattering. The control law needs to be tuned very precisely in order to achieve a trade-off between the tracking precision and robustness to the uncontrolled dynamics. Hence, the final equation for the control of the inverter can be derived by combining the proportional resonant control and SM control for the current loop:

$$\frac{S(x)}{\varnothing} = \frac{1}{C\varnothing}\left[i_C - i_{ref}\right] + \frac{\lambda}{\varnothing}\left[K_p\left(V_{out} - V_{ref}\right) + k_i\left(\frac{2s}{s^2 + 2\omega_c s + \omega_o^2}\right)\left(V_{out} - V_{ref}\right)\right] \tag{29}$$

Thus Equation (29) shows the dynamic behavior in both SM and PR compensator control. The error in the voltage loop is compensated by the appropriate PR parameters, thus, the output voltage is compelled to follow the reference AC voltage leading to system stability while the SMC drives the system to the zero sliding surface with maximum stability. Since the capacitor error current contains the ripples from the inductor, the current peak may reach high values, so $\varnothing$ should be carefully assigned a value in order to compensate the slope from the high current ripple of the capacitor. Hence, the PR controller eliminates the steady-state error at resonant frequency or harmonic at that frequency. The response time of the system λ determines the dynamics and robustness of the system. It is clear from Equation (29), that a smaller value of λ leads to a slow response time, while higher λ values though increase the response time, but take a longer time to reach the sliding surface. Thus the optimal value for λ is equal to the switching frequency of the inverter.

According to [32], the slope of the carrier wave is $4V_m \times fs$, where V_m is the magnitude and fs is the frequency of carrier wave. The slope of the error signal to the modulator is given by $V_{DC}/4LC\varnothing$. According to the limitation of the pulse width modulator, slope of error signal < slope of the carrier signal:

$$4V_m \times fs < {}^{V_{DC}}/_{4LC\varnothing} \tag{30}$$

Thus, the minimum value of $\varnothing$ can be calculated using (30):

$$\varnothing \cong \frac{10V_{DC}}{16LCV_m f_S} \tag{31}$$

Table 2 shows the comparison of the proposed control scheme with the SM control and other common controllers. The proposed controller shows an improvement in terms of reducing the THD and transient response (T_S) with robust control of the inverter.

Table 2. Comparison of different control methods.

Parameters	Model Predictive Control [33]	SPWM Control [34]	Rotating SMC [35]	Fix-Freq SMC [36]	Proposed Work
V_{DC}	529	405	300	360	350
V_{RMS}	150	220	200	220	220
C_f (uF)	40	202	100	9.4	6.6
L_f (mH)	2.4	0.03	0.250	0.357	0.84
THD (L)	2.85%	1.11%	-	1.1%	0.45%
THD (NL)	3.8%	3.8%	2.66%	1.7%	1.25%
T_S (ms)	50	60	-	0.5	0.3

3.2. Battery Charger Control

The AC-DC converter of the UPS system acts as a battery charger as shown in Figure 5. In this control scheme, the faster inner current loop regulates the inductor current so that its average value during each period follows the rectified input voltage. The slower outer voltage loop maintains the battery voltage close to reference voltage and generates the control signal for the current loop. The steady state analysis of the AC-DC converter shows stable performance during grid mode. The state space equations of the rectifier are derived as:

$$\frac{di_L}{dt} = \frac{V_{in}}{L_{in}}D + \frac{(V_{in} - V_d)}{L_{in}}(1 - D) \tag{32}$$

$$\frac{dv_d}{dt} = -\frac{V_d}{RC_d}D + \left(\frac{i_L}{C_d} - \frac{V_d}{RC_d}\right)(1 - D) \tag{33}$$

Assuming the current loop has high bandwidth as compared to the voltage loop, and dc-link capacitor C_d is large enough to give approximately constant voltage i.e., $dv_d/dt = 0$. With $\hat{V}_{in} = 0$, the small signal control $\hat{d}$ to input current $\hat{i}_L$ transfer function $G_{i_L d}(s)$ of the inner current loop is give by:

$$G_{i_L d}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_d}{s(L_{in})} \tag{34}$$

The stability of the current loop depends on the current loop gain, hence a suitable proportional-integral (PI) controller $G_i(s) = k_{pi} + \frac{k_{ii}}{s}$, is used for compensating the current loop. The Bode plot of the current loop gain $T_i = G_{i_L d}(s) \cdot G_i(s)$ is obtained considering the circuit parameters shown in Table 4. The values of the proportional gain K_{pi} and integral gain K_{ii} are selected as 2.3 and 1200, respectively, for the stable operation of the current loop. Figure 6a presents the Bode plot of the current loop gain with phase margin of 89° and stable operation of the rectifier.

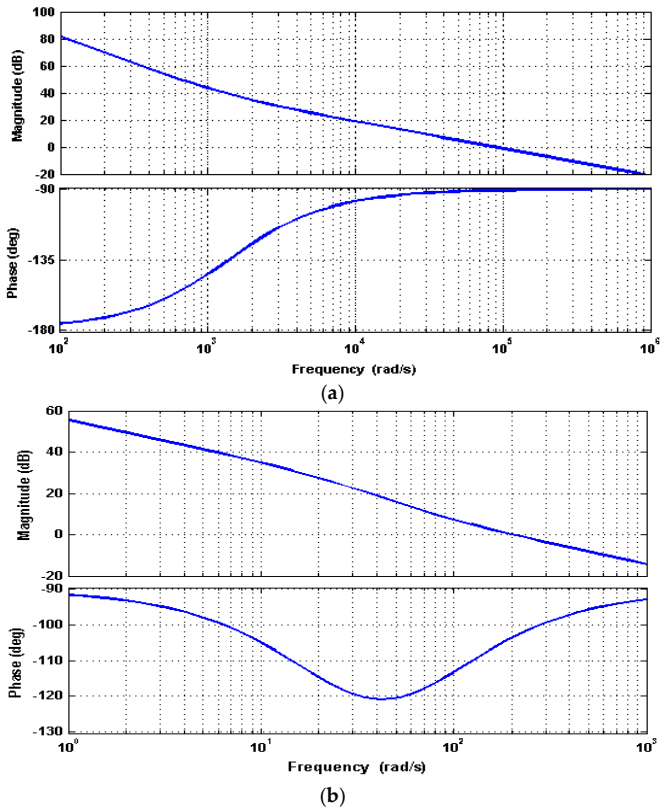


Figure 6. Bode response of rectifier; (**a**) Current loop gain; (**b**) Voltage loop gain.

The same approach is used to compensate the voltage loop of the average current control scheme. $\hat{v}_c$ is the reference current for the current loop. Assuming constant input voltage, the small signal control $\hat{v}_c$ to output transfer function $G_{V_dV_c}(s)$ of the voltage loop is derived as:

$$G_{V_dV_c}(s) = \frac{\hat{v}_d}{\hat{v}_c} = \frac{V_{in}R}{2V_d(sCR+2)} \tag{35}$$

In order to force the output voltage to follow the reference voltage V_{Ref}, a proportional-integral (PI) compensator has been employed. Combining the power stage with the PI controller $G_v(s) = k_{pv} + \frac{k_{iv}}{s}$ provides the overall loop gain.

$T_v = G_v.G_{V_dV_c}(s)$ of the voltage loop. The values of K_{pv} and K_{iv} in voltage loop are selected as 1.2 and 13, respectively. The stability of the voltage loop can be analyzed using the Bode plot obtained by considering the parameters from Table 4, as shown in Figure 6b. The system shows good stability with a positive phase margin.

In charging mode, the controller operates as constant current mode CC or constant voltage mode CV depending on the battery voltage as shown in the Figure 5b. In current loop, the battery input current i_{Bat} is forced to follow the reference current i_{Ref} using a PI compensator in (36):

$$i^* = K_p\Big(i_{Ref} - i_{Bat}\Big) + K_i\int\Big(i_{Ref} - i_{Bat}\Big)dt \tag{36}$$

Similarly, the battery voltage is regulated by the voltage loop using the PI compensator that forces the output battery voltage V_{Bat} to follow the reference voltage V_{ref}. The current limiter is introduced to limit the maximum charging current of the battery. If the i_{ref} is greater than i_{limit}, the battery is charged at constant current (CC Mode), in contrast if the i_{ref} is less than i_{limit}, the battery is charged at constant voltage (CV mode).

3.3. Boost Converter Control

The steady state analysis of the boost converter is performed using average state variable method [30]. The state space equation for the converter with coupled inductor is derived as:

$$\frac{di_P}{dt} = \frac{V_{Bat}}{dt}D + \frac{(V_{Bat} - V_d)}{L_m(N+1)}(1-D) \tag{37}$$

$$\frac{dV_o}{dt} = \frac{i_p}{C(N+1)}(1-D) - \frac{V_o}{RC} \tag{38}$$

Now we perturb the system and consider only the dynamic terms and eliminate the product of the AC terms because of very small value. The final equation after Laplace transform is:

$$s\hat{v}_o = \hat{i}_P\left(\frac{1-D}{C(N+1)}\right) - \frac{\hat{v}_d}{RC} - \frac{I_P}{C(N+1)}\hat{d} \tag{39}$$

$$s\hat{i}_P = \hat{v}_{Bat}\left(\frac{D}{L_m} + \frac{1-D}{L_m(N+1)}\right) - \hat{v}_d\left(\frac{1-D}{L_m(N+1)}\right) + \hat{d}\left(\frac{V_{Bat}}{L_m} - \frac{V_{Bat}+V_d}{L_m(N+1)}\right) \tag{40}$$

Solving (37) and (38) gives the transfer function of the converter:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{s\left(-\frac{I_P}{C(N+1)}\right) + \frac{(1-D)}{C(N+1)}\left(\frac{V_{Bat}}{L_m} + \frac{V_d - V_{Bat}}{L_m(N+1)}\right)}{s^2 + s\frac{1}{RC} + \frac{(1-D)^2}{(1+N)^2L_mC}} \tag{41}$$

Considering the gain due to clamp capacitor C_{b2}, the transfer equation is given by:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{s\left(-\frac{I_P}{C(N+1)}\right) + \frac{(1-D)}{C(N+1)}\left(\frac{V_{Bat}}{L_m} + \frac{V_d - V_{Bat}(D/1-D)}{L_m(N+1)}\right)}{s^2 + s\frac{1}{RC} + \frac{(1-D)^2}{(1+N)^2 L_m C}} \tag{42}$$

The stability of the converter can be analyzed using the Bode plot shown in Figure 7. The system shows good stability with a positive phase margin and it has no right half plane poles. It is easy to achieve high crossover frequencies by adjusting a suitable gain of the compensators as the phase never reaches −180. The voltage across DC-link capacitor C_{din} is regulated by using a suitable voltage compensator [37]. The PI compensator is used to track the DC-link voltage V_d to follow the reference voltage, as shown in Figure 7.

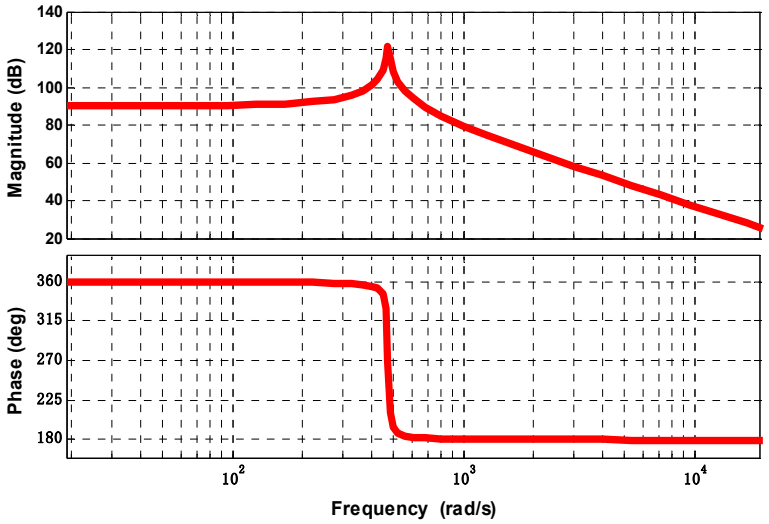


Figure 7. Bode plot of the boost converter.

4. Experimental Results

In order to validate the performance of our UPS system, a laboratory prototype has been implemented. The specifications of the UPS are shown in Table 3. The control scheme for the single-stage converter, boost converter, and H-bridge inverter has been implemented using DSP TMS320F28335. The design parameters of the single-stage converter and DC-DC converter are shown in Tables 4 and 5, respectively. The backup storage system consists of two batteries (each battery is 24 V/35 Ah), or parallel batteries, depending upon the backup time for the connected load.

Table 3. Specifications of the proposed UPS system.

Parameters	Symbol	Value
Input Voltage	V_{in}	220 V
Output Voltage	V_{out}	220 V
Grid Frequency	f_r	50 Hz
Output Frequency	f_o	50 Hz
Number of Batteries	V_b	2 Parallel connected (24 V/35 Ah)
Maximum Output Power	$P_{o,\max}$	1 kVA
DC-link Voltage	V_d	360 V

Table 4. Design parameters of the single-stage AC-DC converter.

Parameters	Symbol	Value
Input Inductor	L_{in}	1.2 mH
Switches	S_1~S_4	SPP11N60C3
Fast Diodes	D_1, D_2	C3D10060A
Switching frequency	f_s	50,000 Hz
H. F Transformer	T	L_m = 600 uH, TDK core PQ-40/40
DC-Link Capacitor	C_d	1900 uF

Table 5. Specifications of the boost DC-DC converter.

Parameters	Symbol	Value
DC-Link Voltage	V_{d_INV}	360 V
Battery Bank Voltage	V_b	24 V
Switching Frequency	f_s	30,000 Hz
Coupled Inductor	L_P, L_S	Turns ratio N = 4; Magnetizing Inductor L_m = 107 uH; PQ-5050 core
Capacitor	C_{b1}, C_{b2}	C_{b1}, C_{b2} = 2 × 2.2 uF (ceramic), C_d = 1900 uF
Switches	S_5 ,S_6	IPW60R045CP MOSFET (Infineon Technologies, Santa Clara, CA USA)
Diodes	D_{b1}, D_{b2}	Ultrafast Recovery diode UF5408

The utility input voltage and current waveform in normal mode of operation is shown in Figure 8a. The input is sinusoidal, with unity power factor and THD less than 5%. The output voltage and current waveform during linear loads and non-linear load are shown in Figure 8b,c. The waveform is sinusoidal for linear loads with THD less than 1%. For a non-linear load designed according to the standard of IEC62040-3, the THD is 1.25% [38].

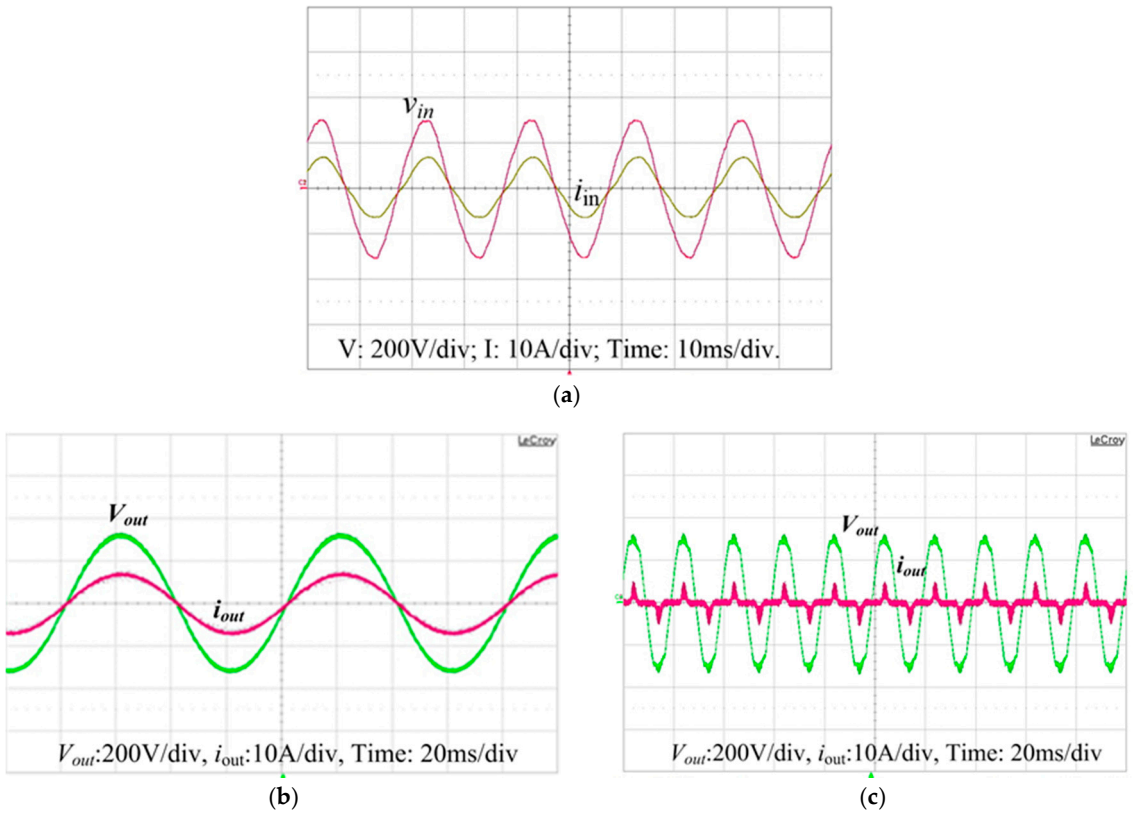


Figure 8. Experimental waveform of the input output voltage and current of the UPS system. (**a**) Input line voltage and current; (**b**) Inverter with linear Load; (**c**) Inverter with Non-linear load.

Figure 9a shows the drain to source voltage and current of the switches S_3 and S_4. Both the switches are operating under the condition of ZVS. Figure 9b shows the drain to source voltage of the switches S_5 and S_6 of the boost converter. Both switches are operating under the condition of ZVS. Also the voltage stress across the switches is also limited. When the grid power is interrupted, the system switches from grid mode to battery mode. The rectifier is no longer in operation and the boost converter provides regulated dc-link voltage.

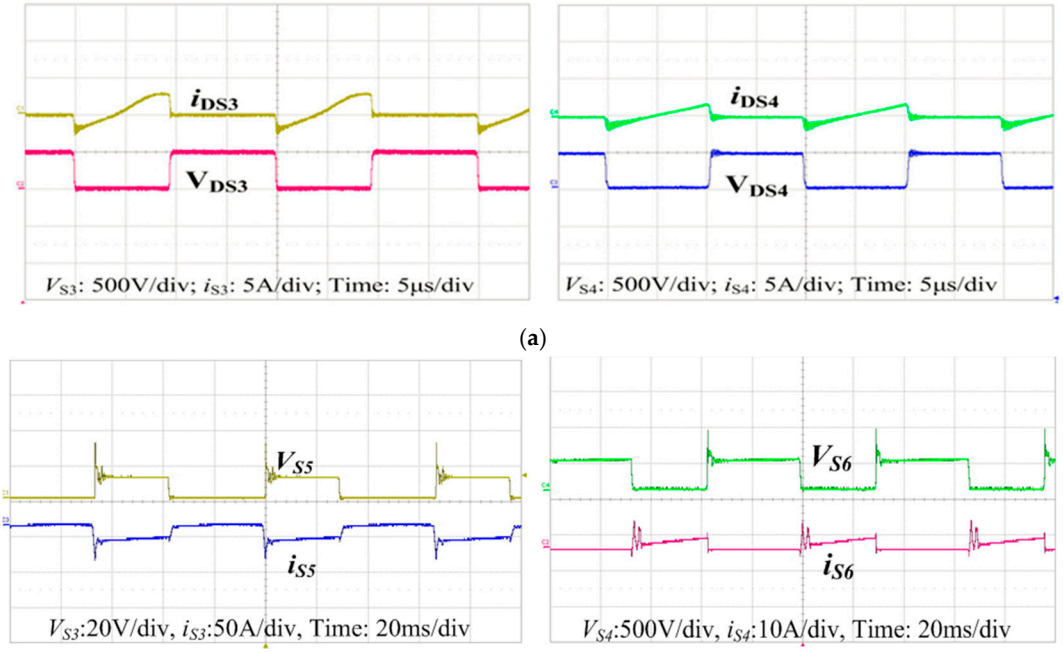


Figure 9. Drain to source voltage and current of the switches. (**a**) S_3 and S_4 of single-stage AC-DC Converter; (**b**) S_5 and S_6 of boost DC-DC converter.

The transient effect in the output voltage is very small and the UPS system provides uninterruptible power to the load as shown in Figure 10a. Similarly, the transition from battery mode back to grid mode upon the restoration of the grid power is shown in Figure 10b. There is a small transient at the turning ON point of the AC-DC converter. This transient is due to the inductor which remains charged due to previous grid mode of operation. However the small transient can be controlled by a suitable snubber circuit. Figure 10 also shows that the inverter keeps operating in both the grid and battery powered mode of operation and the load is getting power without any interruption. Figure 11 shows a photograph of our laboratory prototype. Figure 12 shows the efficiency graph with maximum efficiency of 95% during battery mode and 91% during grid mode of operation. Thus utilizing soft switching in boost converter reduces the switch losses and increases the efficiency of the system. The efficiency in battery mode is high as compared to grid mode because less number of power stages are operation during this mode. Table 6 shows a comparison of the different high-frequency transformer isolated UPS systems. The proposed UPS shows a distinct improvement in terms of increasing the efficiency, reducing the size of the battery bank, and decreasing the volumetric size and weight of the system.

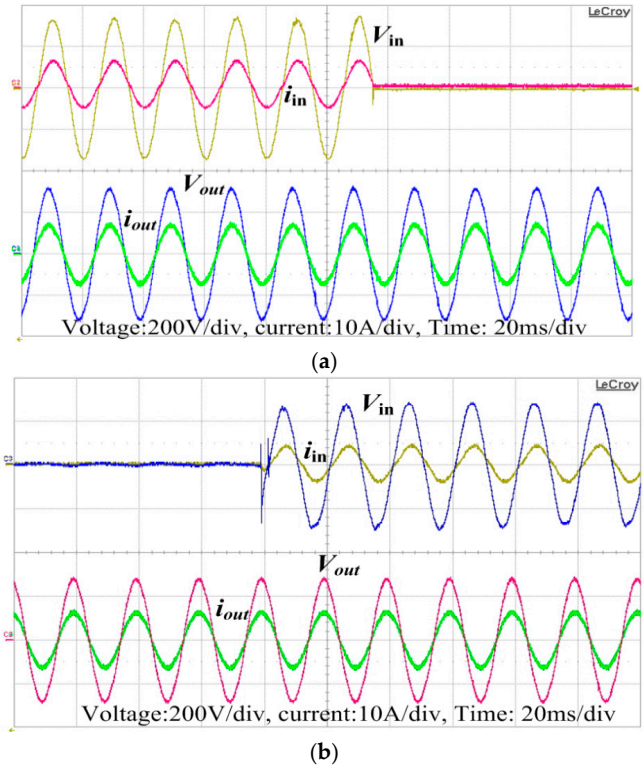


Figure 10. Transition between two modes of operation, Input voltage V_{in} and current I_{in}, Output voltage V_{out} and current I_{out}. (**a**) Grid to battery mode and (**b**) Battery mode to grid mode.

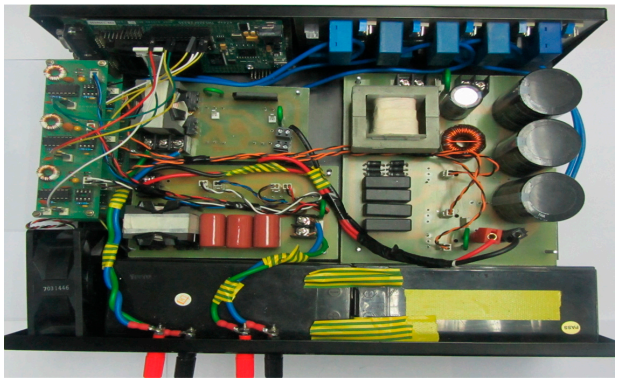


Figure 11. Laboratory prototype.

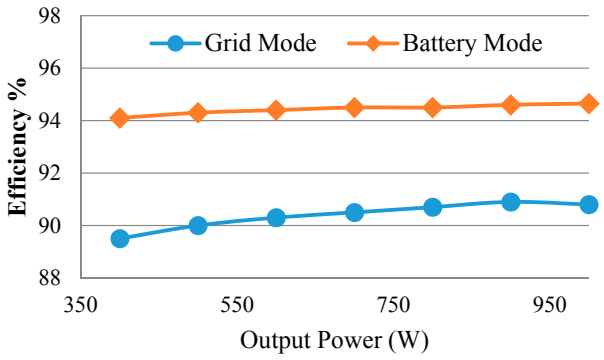


Figure 12. Efficiency graph of UPS in grid and battery mode.

Table 6. Comparison of the proposed system.

UPS Topology / Properties	Efficiency	Power Ratings	System Specification	Battery Bank	Size & Weight
An On-Line UPS System With Power Factor Correction and Electric Isolation Using BIFRED Converter [10]	-	150 VA	110 V	48 V	Small
Two-Stage Uninterruptible Power Supply With High Power Factor [6]	84%	150 VA	120 V	60 V	Small
A UPS With 110-V/220-V Input Voltage and High-Frequency Transformer Isolation [9]	86%	2 kVA	110/220 V	96 V	High
Novel AC UPS With High Power Factor and Fast Dynamic Response [8]	-	300 VA	110 V	48 V	-
Proposed UPS System	91%	1 kVA	220 V	24 V	Medium

5. Conclusions

A single phase high-frequency transformer isolated online UPS has been proposed in this paper. A single-stage AC-DC converter provides galvanic isolation, efficient power conversion, and excellent power factor correction. Besides, the AC-DC converter also charges the battery bank of the UPS system during grid mode of operation. When there is a grid interruption, the low battery bank voltage is raised to high dc-link voltage using a boost converter which reduces the battery bank significantly. The boost converter provides high voltage gain with less number of active switches. A new inverter control of cascaded PR and SM control is used which provides regulated sinusoidal output voltage with low THD for both linear and non-linear load. Overall, the volume of the system is minimized by reducing the size, weight, and battery bank of the system. The experimental results show good dynamic and steady state performance.

Authors Contribution

All the authors contributed in finalizing the Paper. The main idea of the paper was presented by Muhammad Aamir while Wajaht Ullah Tareen and Kafeel Ahmed Kalwar helped in the control of the circuit. Mudasser Ahmed Memon prepared the format of the paper. Saad Mekhilef is the head of research team.

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Conflicts of Interest: The authors declare no conflict of interest.

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