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A Dual Half-Bridge Converter with Adaptive Energy Storage to Achieve ZVS over Full Range of Operation Conditions

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Abstract: The phase-shifted full-bridge (PSFB) converter is widely employed in high-power applications. However, circulating current, duty-cycle loss, secondary voltage oscillation, and narrow zero-voltage-switching (ZVS) range are the main drawbacks of the conventional PSFB converter. This paper proposes a novel full-bridge converter to improve the performance of the conventional PSFB converter. The proposed converter contains two paralleled half-bridge inverters and an auxiliary inductor on the primary side. The rectifier stage is composed of six diodes connected with the form of full-bridge rectification. This structure allows the stored energy for ZVS operation to change adaptively with duty-cycle. The power can be transferred from the primary side to the secondary side during the whole period. Therefore, the requirement of output filter inductance is reduced and the circulating current is removed. The proposed converter is a good candidate for high power, high voltage and variable input voltage applications. The operation principle and performance are verified on a laboratory prototype.

Keywords: phase-shifted full-bridge (PSFB); adaptive energy storage; circulating current; duty-cycle loss; zero-voltage-switching (ZVS)

1. Introduction

The traditional full-bridge DC/DC converter with phase-shifted control can achieve zero-voltage-switching (ZVS) without any additional devices. The switching loss can be significantly reduced. Hence, the converter can achieve high efficiency and power density. These advantages make the phase-shifted full-bridge (PSFB) converter well-suited for high efficiency, power density, and reliability applications [1–6]. However, the drawback of the PSFB converter is the dependency of the ZVS characteristic on the load condition: ZVS is lost as load current decreases. Loss of ZVS at light loads results in low efficiency and high electro-magnetic interference (EMI) due to the increase of switching losses [5]. Another drawback is the existence of circulating current, which will significantly increase conduction loss [6]. Extending ZVS range and reducing circulating current are two key areas to improve the PSFB converter's performance.

Many studies have been proposed to overcome the drawbacks of the traditional PSFB converter. Generally, the ZVS range can be extended by utilizing energy stored in the auxiliary circuits [7–10]. However, the auxiliary circuits lead to higher circulation current and more conduction loss. The zero-voltage and zero-current-switching (ZVZCS) full-bridge converters are another solution to the problems [11–14]. In these converters, metal–oxide–silicon field-effect transistors (MOSFETs) as leading-leg switches are turned on with ZVS, while insulated gate bipolar translators (IGBTs) as lagging-lag switches are turned off with ZCS. The ZVS operation is achieved over a wide

range of load conditions, and circulating current can be removed by ZCS operation. Generally, these ZVZCS converters result in high secondary-voltage stress and increase the ripple of output voltage. The dual half-bridge converters are a novel solution to extend the ZVS range and remove circulating current [15–17]. However, these converters require the specified leakage and magnetizing inductances, which makes the design of transformers complex.

This paper proposes a new dual half-bridge converter with a simple auxiliary circuit. Since the required energy for ZVS increases as duty-cycle decreases, the proposed converter can achieve ZVS operation for all of the primary switches over the entire load range. In addition, the energy from the primary side can be transferred to the output side during the whole switching period, so the output filter requirement is reduced. The proposed converter is well suited for the high-output-voltage applications. Because of these applications, a large filter inductor is required to reduce the ripple current, which results in low efficiency and power density. The operation principle and theoretical analysis are presented to verify these advantages. Experimental results demonstrate the performance of the proposed converter.

2. Operation Principle

The circuit diagram of the proposed converter is shown in Figure 1. The converter is composed of two half-bridge inverters (HBIs) in parallel, which are driven with phase-shifted control. The transformers of T_1 and T_2 have the same characteristics with turns ratio of 1:n. L_{lk1} and L_{lk2} are the leakage inductances of T_1 and T_2, respectively. Q_1, Q_3, C_{dc1}, and T_1 form the lagging-HBI. Q_2, Q_4, C_{dc2}, and T_2 form the leading-HBI. The auxiliary inductor L_{aux} is used to adaptively adjust the energy for ZVS operation. Two full-bridge rectifiers are employed at the rectifier stage.

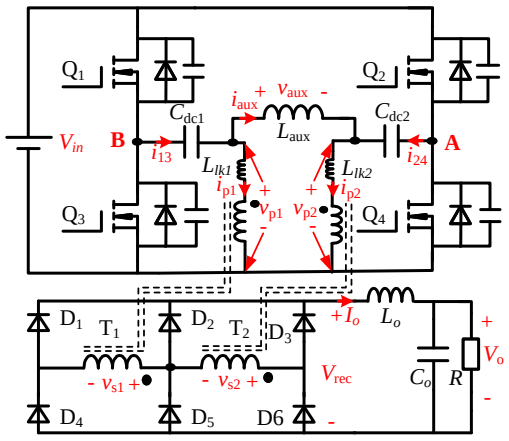


Figure 1. Proposed dual half-bridge converter.

For the convenience of circuit analysis, the following assumptions are made:

(1) The blocking capacitors C_{dc1}, C_{dc2} are considered as two constant voltage sources of $0.5V_{in}$.
(2) All the output capacitances of MOSFETs have the same values, C_{oss}.L_{lk1} and L_{lk2} also have the same values, L_{lk}.
(3) The output filter inductor L_o is large enough to be treated as a constant current source during a switching period.

Figure 2 shows the key waveforms of the proposed converter in the steady state. D means the duty-cycle and T_s is the switching period. All the primary switches' duty-cycles keep constant (50%) if the dead-time is ignored. The output voltage is regulated by adjusting the phase-shift time $0.5DT_s$ between leading-HBI and lagging-HBI. The operating sequence during each switching period can be divided into two half cycles—t_0–t_8 and t_8–t_{15}. Due to the symmetrical structure, only the first half

cycle is given. This half cycle can be divided into eight operating modes, whose topological states are shown in Figure 3.

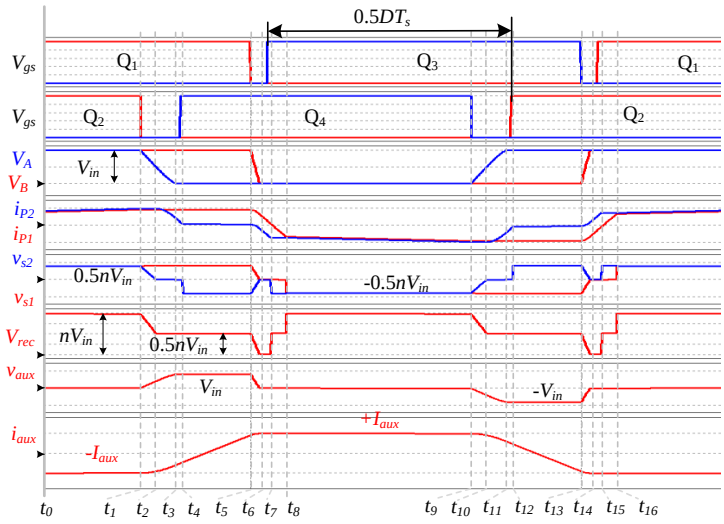


Figure 2. Key operating waveforms.

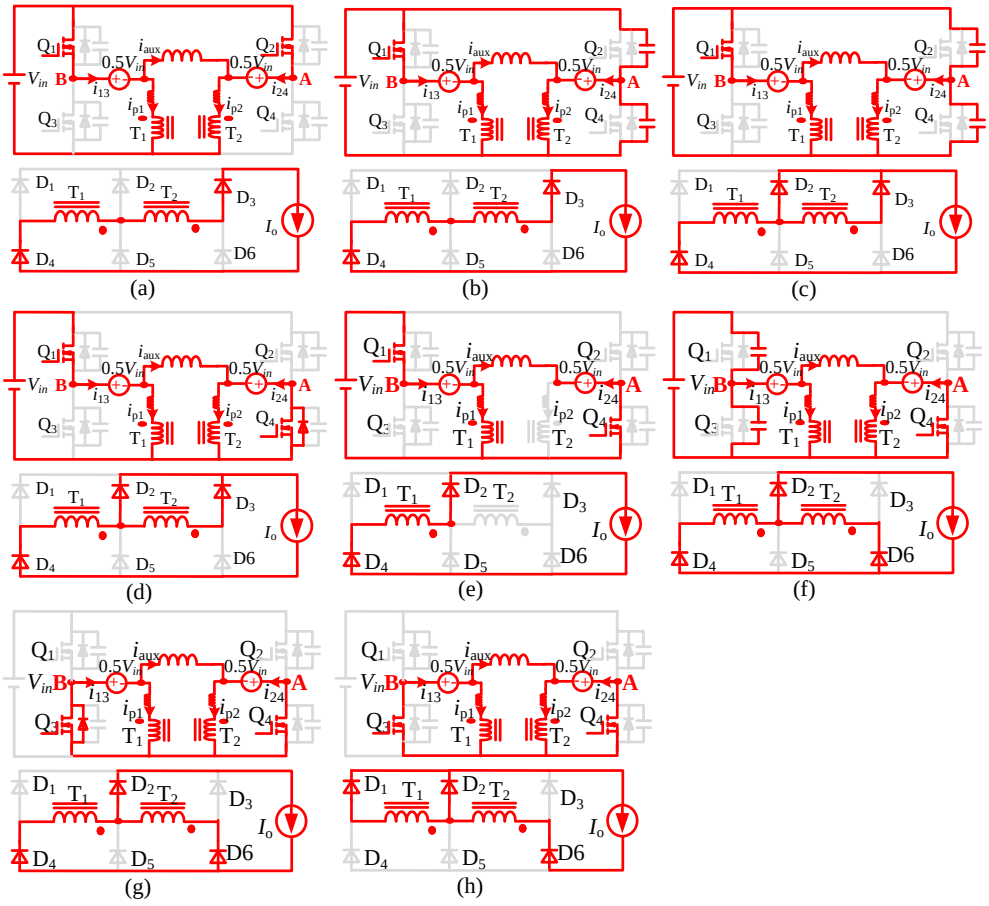


Figure 3. Topological stages of the proposed converter: (**a**) Mode 1 [t_0-t_1]; (**b**) Mode 2 [t_1-t_2]; (**c**) Mode 3 [t_2-t_3]; (**d**) Mode 4 [t_3-t_4]; (**e**) Mode 5 [t_4-t_5]; (**f**) Mode 6 [t_5-t_6]; (**g**) Mode 7 [t_6-t_7]; (**h**) Mode 8 [t_7-t_8].

Mode 1 [t_0-t_1]: Q_1 and Q_2 are on. The primary voltages of T_1 and T_2 are $0.5V_{in}$, which leads to the current of L_{aux} keeping negative maximum. The output current I_o flows through D_3 and D_4. Several primary currents are expressed as follows:

$$\begin{aligned} i_{aux}(t) &= -I_{aux} \\ i_{13}(t) &= nI_o - I_{aux} \\ i_{24}(t) &= nI_o + I_{aux} \end{aligned} \tag{1}$$

Mode 2 [t_1-t_2]: Q_2 is turned off at time t_1. The voltage across junction capacitances of Q_2 and Q_4 are charged and discharged linearly by the constant current source $i_{24}(t_1)$. The voltage of point A $V_A(t)$ decreases from V_{in} to $0.5V_{in}$. $v_{s1}(t)$ keeps $0.5nV_{in}$ and $v_{s2}(t)$ falls from $0.5V_{in}$ to zero. Thus, $V_{rec}(t)$ decreases from nV_{in} to $0.5V_{in}$. The voltage of L_{aux} starts to increase from zero. The voltages in this mode are expressed as:

$$\begin{aligned} V_A(t) &= V_{in} - \tfrac{i_{24}(t_1)}{2C_{oss}}(t - t_1) \\ V_{rec}(t) &= nV_{in} - \tfrac{ni_{24}(t_1)}{2C_{oss}}(t - t_1) \end{aligned} \tag{2}$$

Mode 3 [t_2-t_3]: When $V_A(t)$ becomes $0.5V_{in}$ in *Mode 2*, $v_{s2}(t)$ falls to zero and D_2 starts to conduct. $v_{s2}(t)$ is maintained at zero since D_2 and D_3 are in conducting state during this mode. The resonance between L_{lk2} and the junction capacitances occurs. The capacitances are charged or discharged by the energy stored in L_{lk2}. $V_A(t)$ decrease from $0.5V_{in}$ to zero with a resonance waveform. The voltage of L_{aux} continuously increases. The currents and voltages are expressed as follows:

$$\begin{aligned} i_{p2}(t) &= i_{24}(t_1)\cos\omega(t - t_2) - I_{aux} \\ V_A(t) &= 0.5V_{in} - i_{24}(t_1)\sqrt{\tfrac{L_{lk}}{2C_{oss}}}\sin\omega(t - t_2) \end{aligned} \tag{3}$$

where $\omega_1 = \frac{1}{2\sqrt{L_{lk}C_{oss}}}$.

Mode 4 [t_3-t_4]: $V_A(t)$ reaches zero at time t_3 and the parasitic diode of Q_4 starts to conduct. Q_4 can be turned on with zero voltage in this mode. $v_{s2}(t)$ is maintained at zero and the commutation between D_2 and D_3 is progressed during this mode. The voltage of L_{aux} rises to V_{in}. The primary current of T_2 is expressed as:

$$i_{p2}(t) = i_{p2}(t_3) - \frac{V_{in}}{2L_{lk}}(t - t_3) \tag{4}$$

Mode 5 [t_4-t_5]: *Mode 5* begins when $i_{p2}(t)$ falls to zero. The commutation between D_2 and D_3 is completed at t_4. $v_{s2}(t)$ becomes $-0.5nV_{in}$ and T_2 stops to transfer the power from input side to output side. The voltage of L_{aux} and $V_{rec}(t)$ are continuously maintained at V_{in} and $0.5nV_{in}$, respectively. The current of L_{aux} is given by:

$$i_{aux}(t) = -I_{aux} + \frac{V_{in}}{L_{aux}}(t - t_4) \tag{5}$$

Mode 6 [t_5-t_6]: Q_1 is turned off at t_5. At the same time, the commutation between D_4 and D_6 isprogressed. The resonance of junction capacitances and leakage inductances occurs. $V_B(t)$ is decreased from V_{in} to zero and $V_{rec}(t)$ falls to zero. The current of L_{aux} can be considered to increase to the positive maximum ($+I_{aux}$). The primary currents of T_1 and T_2 are expressed as follows:

$$\begin{aligned} i_{p1}(t) &= (nI_o + I_{aux})\cos\omega_1(t - t_5) - I_{aux} \\ i_{p2}(t) &= -(nI_o + I_{aux})[1 - \cos\omega_1(t - t_5)] \\ V_B(t) &= V_{in} - \sqrt{\tfrac{L_{lk}}{C_{oss}}}(nI_o + I_{aux})\sin\omega_1(t - t_5) \end{aligned} \tag{6}$$

Mode 7 [t_6-t_7]: *Mode 7* begins when $V_B(t)$ falls to zero. The body diode of Q_3 starts to conduct and Q_3 can be turned on with zero voltage. $v_{s1}(t)$ and $v_{s2}(t)$ are maintained zero in this mode. The voltage across L_{lk1} or L_{lk2} equals to $-0.5V_{in}$. The commutation between D_4 and D_6 is continually progressed. The currents are expressed as follows:

$$\begin{aligned} i_{p1}(t) &= -i_{p1}(t_6) + \tfrac{V_{in}}{2L_{aux}}(t - t_6) \\ i_{p2}(t) &= -i_{p2}(t_6) + \tfrac{V_{in}}{2L_{aux}}(t - t_6) \end{aligned} \tag{7}$$

Mode 8 [t_7-t_8]: *Mode 8* begins when $i_{p1}(t)$ falls to zero and D_4 is naturally turned off. At the same time, $v_{s2}(t)$ becomes $-0.5nV_{in}$ and $v_{s1}(t)$ becomes zero since the commutation between D_1 and D_2 starts. The voltage across L_{lk1} is $-0.5V_{in}$ and $i_{p1}(t)$ decreases linearly.

Mode 8 ends when $i_{p1}(t)$ reaches nI_o and D_2 is naturally turned off. The commutation between D_1 and D_2 ends at t_8. The power is transferred from the primary side to the secondary side through T_1 and T_2. The voltage across L_{aux} is zero and i_{aux} is maintained at the positive maximum.

3. Analysis of the Proposed Converter

3.1. Voltage Gain Analysis

Since the durations of duty-cycle loss and dead-time are very narrow, they can be ignored to simplify analysis. Figure 4a shows the simplified rectifier output voltage in the proposed converter. The voltage gain is derived from the volt-second balance of the output filter inductor, and it can be expressed as follows:

$$G = \frac{V_o}{V_{in}} = \frac{n(1+D)}{2} \tag{8}$$

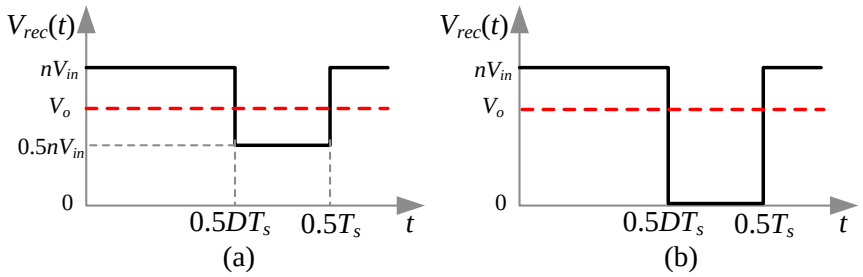


Figure 4. Idealized rectifier voltage: (**a**) proposed converter; (**b**) conventional converter.

The rectifier output voltage waveform in the conventional full-bridge converter is shown in Figure 4b. It can be noted that the energy from the primary side cannot be transferred to the secondary side during freewheel period. For the proposed converter, the energy can always be transferred to the output side during the whole period. Therefore, the filter requirement can be significantly less and the power loss can also be reduced.

As shown in Figure 4b, the voltage of the output filter inductor is $nV_{in} - V_o$ during the duty-cycle period, while the value is $-V_o$ during the freewheeling period. The output filter inductor for the conventional full-bridge converter is calculated based on the given current ripple.

$$L_{con} = \frac{D(nV_{in} - V_o)}{4f_s\Delta I_{out}} = \frac{V_o}{4f_s\Delta I_{out}}(1 - D) \tag{9}$$

where ΔI_{out} is the current ripple of L_o. In general, ΔI_{out} is set at 20 percent of full load current.

For the proposed converter, the voltage applied on L_o is $0.5nV_{in} - V_o$ during the freewheeling period. The filter inductor for the proposed converter is calculated as

$$L_{pro} = \frac{D(nV_{in} - V_o)}{4f_s\Delta I_{out}} = \frac{V_o}{4f_s\Delta I_{out}}\frac{D(1-D)}{1+D} \tag{10}$$

Figure 5 shows the relationship between the required value of filter inductor and duty-cycle. It can be noted that the filter inductance of the proposed converter is much smaller than that of the traditional full-bridge converter. Therefore, the proposed converter benefits from the reduction of the inductor's size and copper loss.

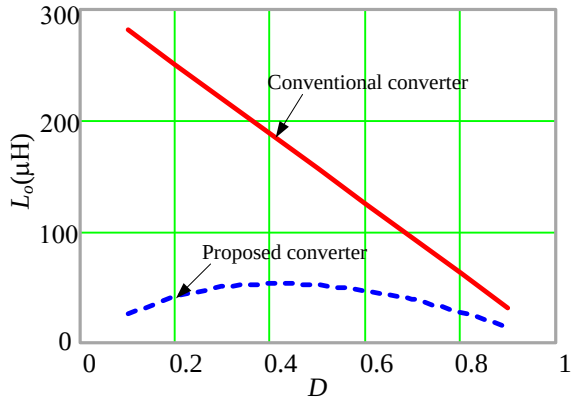


Figure 5. Filter inductance versus duty-cycle.

3.2. ZVS Characteristics

For the ZVS of leading-HBI switches, the transition is accomplished in *Mode 2* and *Mode 3*. During *Mode 2*, the output filter inductor takes part in the transition and the voltage of leading-leg is decreased from V_{in} to $0.5V_{in}$. Then, the transformer is shorted and the remaining voltage falls by the resonance between junction capacitances and leakage inductance of the transformer during *Mode 3*. The required energy for ZVS can be obtained according to (3)

$$\frac{1}{2}L_{lk2}(nI_o + I_{aux})^2 > C_{oss}(0.5V_{in})^2 \tag{11}$$

When the lagging-HBI switch is turned off during *Mode 6*, the transformers are shorted and only the energies stored in the leakage inductances can be available for lagging-leg transition. According to the Equation (6), the ZVS condition of lagging-leg switches can be expressed as

$$\frac{1}{2}(L_{lk1} + L_{lk2})(nI_o + I_{aux})^2 > C_{oss}{V_{in}}^2 \tag{12}$$

According to Equations (11) and (12), the ZVS energies are related to I_{aux}. If the durations of duty-cycle loss and dead-time are ignored, I_{aux} can be calculated as

$$I_{aux} = \frac{V_{in}}{4L_{aux}f_s}(1-D) \tag{13}$$

According to Equation (13), I_{aux} and duty-cycle have an inverse relationship. When D is low (e.g., increasing the input voltage or decreasing the load current), the maximum value of auxiliary inductor current will increase. Sufficient energy can be stored in the leakage inductances to achieve ZVS operation. Therefore, the proposed converter can achieve ZVS over the full range of load conditions.

4. Experimental Results

A prototype was built to demonstrate the performance of the proposed converter. The components used in the prototype are shown in Table 1. The circuit parameters of the prototype are given as follows:

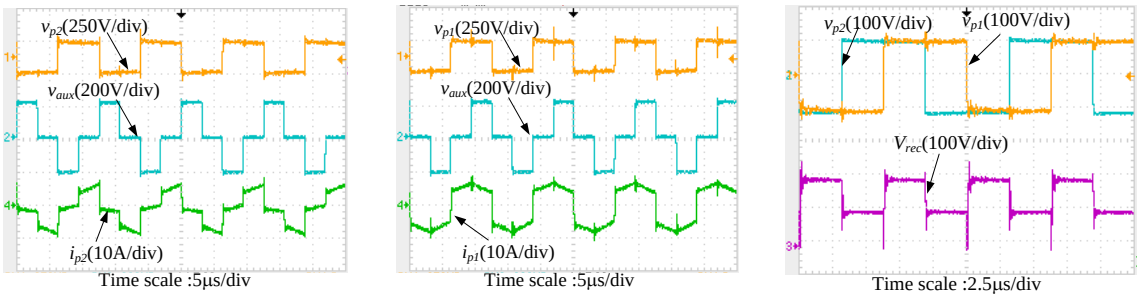
(1) Input voltage: V_{in} = 200–300 V
(2) Output voltage: V_o = 150 V
(3) Maximum output current I_o(max) = 5 A
(4) Switching frequency: f_s = 80 kHz

Table 1. Components list.

Main switches (Q_1–Q_4)	SPW20N60C3
Rectifier diodes (D_1–D_6)	IDH08SG60C
Blocking capacitor ($C_{dc1}C_{dc2}$)	10 μF
Main transformers (T_1 T_2)	Core PQ3535 Turns ratio n = 0.9 L_{lk1} = L_{lk2} = 12 μH
Output inductor (L_o)	60 μH

The digital-signal-processor (DSP) TMS320F28027 (Texas Instruments, Dallas, TX, USA) was adopted for the digital control of the proposed converter. SPW20N60C3 (Infineon Technologies, Munich, Germany) were used as the primary switches, and the effective output capacitance was 160 pF [18]. The rectifier was formed by IDH08SG60C (Infineon Technologies, Munich, Germany). The input power was evaluated through DC Power Supply 62150H, and the output power was measured through DC Electronic Load 63204, manufactured by the Chroma Company (Taiwan, China).

Figure 6 shows the key waveforms of the proposed converter at V_{in} = 230 V, I_o = 5 A. It can be noted that the experimental waveforms coincide well with the theoretical analysis described in Figure 3.



(**a**) (**b**) (**c**)

Figure 6. Key experimental waveforms of the proposed converter at V_{in} = 230 V and I_o = 5 A: (**a**) leading-half-bridge inverter (HBI); (**b**) lagging-HBI; (**c**) primary voltages of two HBIs and rectifier voltage.

Figure 7 shows the key waveforms of the auxiliary inductor when the proposed converter operates at different duty-cycles. As shown in Figure 7, both the maximum current value of the auxiliary inductor and the available energy for ZVS operation are increased when duty-cycle is decreased. This characteristic is helpful to realize the ZVS under all kinds of operation conditions and can reduce the conduction loss caused by the auxiliary circuit.

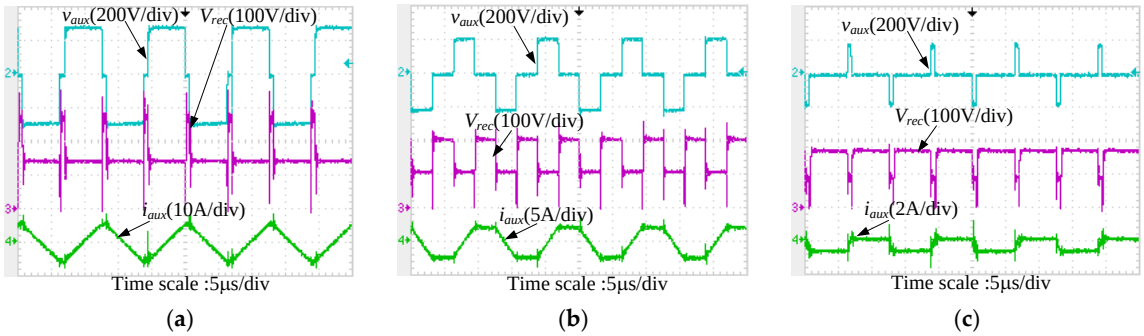


Figure 7. Experimental waveforms at different input voltages: (**a**) V_{in} = 310 V, D = 0.1; (**b**) V_{in} = 250 V, D = 0.5; (**c**) V_{in} = 190 V, D = 0.9.

Figures 8 and 9 show the gate-source and drain-source voltage waveforms at I_o = 1 A and I_o = 50 mA, respectively. It can be noted that all the switches in the proposed converter can achieve ZVS operation over the entire load current and input voltage ranges.

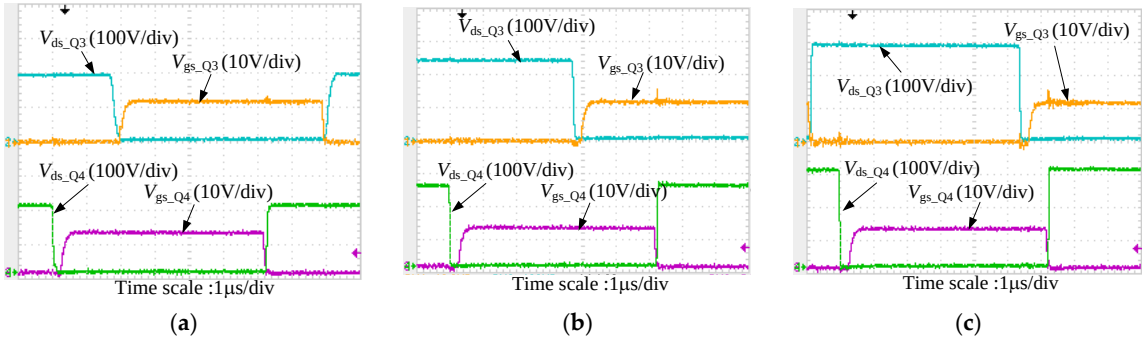


Figure 8. Zero-voltage-switching (ZVS) waveforms at I_o = 1 A: (**a**) V_{in} = 200 V; (**b**) V_{in} = 250 V; (**c**) V_{in} = 300 V.

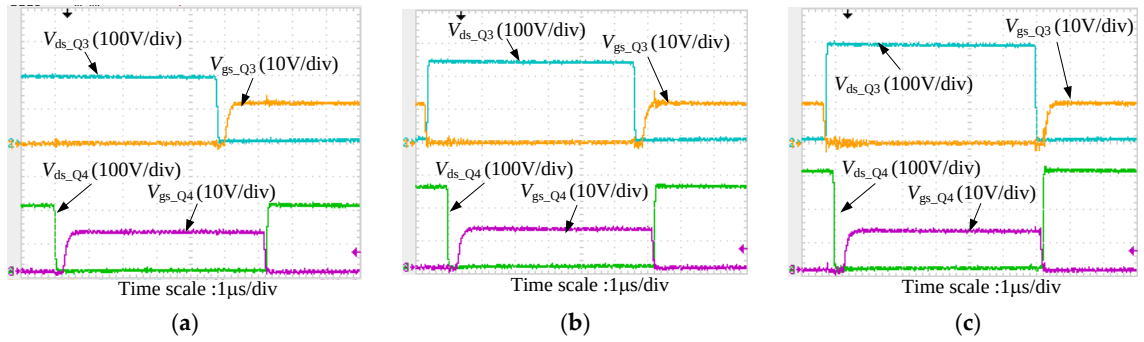


Figure 9. ZVS waveforms at I_o = 50 mA: (**a**) V_{in} = 200 V; (**b**) V_{in} = 250 V; (**c**) V_{in} = 300 V.

In order to compare the performances, a conventional PSFB converter was built with an external inductance of 20 μH to achieve the ZVS operation over a load range from 50% to 100%. Figure 10 shows the experimental efficiencies of the proposed converter and the conventional converter under different load currents. At heavy loads, both converters could achieve ZVS, while the additional components in the proposed converter increased the conduction losses. Therefore, the efficiency of the proposed converter was a little lower than that of the conventional converter. At light loads, the switching losses were dominant and the conventional converter failed to obtain ZVS. The proposed converter

could maintain the ZVS operation and achieve higher efficiency at light loads, as shown in Figure 10. The efficiency improvement was determined by the saved switching losses.

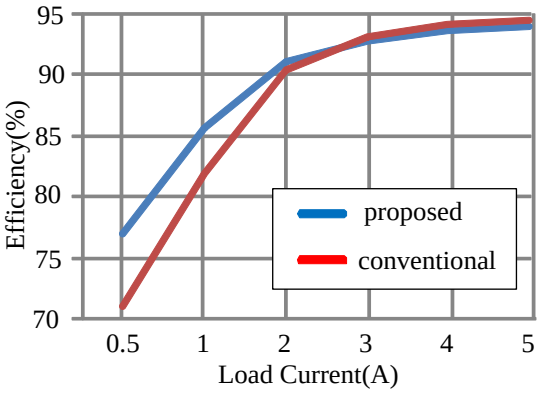


Figure 10. Comparison of the converter efficiency.

5. Conclusions

A dual half-bridge converter with an auxiliary inductor was proposed to solve the drawbacks of the conventional PSFB converters. The proposed converter can transfer the power from the primary side to the secondary side during the whole period. Therefore, the circulating current is removed and the filter requirement is reduced. The ZVS energy can be changed with the duty-cycle, which is helpful for the realization of ZVS under the whole range of operation conditions. The experimental results coincide with the theoretical analysis. The proposed converter is a good candidate for high power, high voltage, and variable input voltage applications.

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Author Contributions: Lei Zhao was responsible for the theoretical derivation and paper writing. Haoyu Li and Xuemei Zheng proposed the main idea and analysis method. Chuangyu Xu carried out the simulation and verification.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Kim, Y.D.; Cho, K.M.; Kim, D.-Y.; Moon, G.-W. Wide-range ZVS phase-shift full-bridge converter with reduced conduction loss caused by circulating current. *IEEE Trans. Power Electron.* **2013**, *28*, 3308–3316. [CrossRef]
2. Hu, S.; Li, X.; Lu, M.; Luan, B.-Y. Operation modes of a secondary-side phase-shifted resonant converter. *Energies* **2015**, *8*, 12314–12330. [CrossRef]
3. Kim, J.W.; Kim, D.Y.; Kim, C.E.; Moon, G.W. A simple switching control technique for improving light load efficiency in a phase-shifted full-bridge converter with a server power system. *IEEE Trans. Power Electron.* **2014**, *29*, 1562–1566. [CrossRef]
4. Kim, D.Y.; Kim, C.E.; Moon, G.W. Variable delay time method in the phase-shifted full-bridge converter for reduced power consumption under light load conditions. *IEEE Trans. Power Electron.* **2013**, *28*, 5120–5127. [CrossRef]
5. Zhao, L.; Li, H.; Hou, Y.; Yu, Y. Operation analysis of a phase-shifted full-bridge converter during the dead-time interval. *IET Power Electron.* **2016**, *9*, 1777–1783. [CrossRef]
6. Chen, B.Y.; Lai, Y.S. Switching control technique of phase-shift-controlled full-bridge converter to improve efficiency under light-load and standby conditions without additional auxiliary components. *IEEE Trans. Power Electron.* **2010**, *25*, 1001–1012. [CrossRef]
7. Borage, M.; Tiwari, S.; Kotaiah, S. A passive auxiliary circuit achieves zero-voltage-switching in full-bridge converter over entire conversion range. *IEEE Trans. Power Electron.* **2005**, *3*, 141–143. [CrossRef]

8. Borage, M.; Tiwari, S.; Bhardwaj, S.; Kotaiah, S. A full-bridge DC-DC converter with zero-voltage-switching over the entire conversion range. *IEEE Trans. Power Electron.* **2008**, *4*, 1743–1750. [CrossRef]
9. Safaee, A.; Jain, P.; Bakhshai, A. A ZVS pulse width modulation full-bridge converter with a low-RMS-current resonant auxiliary circuit. *IEEE Trans. Power Electron.* **2016**, *31*, 4031–4047. [CrossRef]
10. Jang, Y.; Jovanovic, M.M. A new PWM ZVS full-bridge converter. *IEEE Trans. Power Electron.* **2007**, *22*, 987–994. [CrossRef]
11. Gu, B.; Lai, J.S.; Kees, N.; Zheng, C. Hybrid-switching full-bridge DC–DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers. *IEEE Trans. Power Electron.* **2013**, *28*, 1132–1144. [CrossRef]
12. Wu, X.; Xie, X.; Zhao, C.; Qian, Z.; Zhao, R. Low voltage and current stress ZVZCS full bridge DC-DC converter using center tapped rectifier reset. *IEEE Trans. Ind. Electron.* **2008**, *55*, 1470–1477. [CrossRef]
13. Wang, J.; Ji, B.; Wang, H.; Chen, N.; You, J. An inherent zero-voltage and zero-current-switching full-bridge converter with no additional auxiliary circuits. *J. Power Electron.* **2015**, *15*, 610–620. [CrossRef]
14. Seok, K.; Kwon, B. An improved zero-voltage and zero-current-switching full-bridge PWM converter using a simple resonant circuit. *IEEE Trans. Ind. Electron.* **2001**, *48*, 1205–1209. [CrossRef]
15. Lee, I.O.; Moon, G.W. Soft-switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage applications. *IEEE Trans. Power Electron.* **2013**, *28*, 112–122. [CrossRef]
16. Lee, I.O.; Moon, G.W. Phase-shifted PWM converter with a wide ZVS range and reduced circulating current. *IEEE Trans. Power Electron.* **2013**, *28*, 908–919. [CrossRef]
17. Ye, Z.Y. Dual half-bridge DC-DC converter with wide-range ZVS and zero circulating current. *IEEE Trans. Power Electron.* **2013**, *28*, 3276–3286. [CrossRef]
18. *SPW20N60C3 Datasheet*; Infineon Technologies AG: Munich, Germany, 2010.