Management System for Large Li-Ion Battery Packs with a New Adaptive Multistage Charging Method [†]

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Abstract: Among the wide diversity of existing technologically mature batteries, lithium-ion (Li-ion) batteries have become popular because of their longevity, high energy density, high efficiency and lack of memory effect. Differential charging of cells with age has turned balancing management systems into an important research subject. This paper proposes a new battery management system (BMS) to improve the capacity usage and lifespan of large Li-ion battery packs and a new charging algorithm based on the traditional multistage method. The main advantages of the proposed system are its versatility and ability to implement different charging and balancing methods in a very accessible way. The combination of charging methods with balancing methods represents an evolution when compared with other works in the literature.

1. Introduction

The longevity of a battery charge is nowadays a big issue for people who are usually outdoors. Electric Vehicles (EV), a worldwide growing market, are pretty dependent on battery capacity and usage, for EVs will only go as far as their battery allows [1,2]. Home battery-powered devices that can store energy from either local renewable sources or from the grid are also a promising technology highly dependent on battery usage patterns [3].

The need to interconnect multiple cells in series in order to obtain the required voltage levels, coupled with the existence of intrinsic and extrinsic differences between cells, results in a lack of uniformity that reduces usable capacity, lifetime and performance. Although parallel cells are self-balanced, this does not happen when they are in a series configuration [4,5].

This intrinsic (internal) non-homogeneity between cells is due mainly to small variations in the manufacturing process, such as different capacities, volume, internal impedance and different rates of self-discharge, characteristics that worsen with usage and battery age. The main extrinsic (external) factor is temperature non-homogeneity along the battery pack, which leads to different rates of self-discharge and consequent declines in performance.

Some battery balancing methods proposed in the literature aim to create a system capable of applying a charging algorithm [6]. The dissipative resistors method adopted in this paper is based on the most frequently used balancing system due to its simplicity, cost, efficiency, volume, weight, robustness and reliability [7].

Typically, Li-ion cells are designed with a working voltage range between 3 V and 4.2 V. If the voltage drops below the lower boundary, a deep state of discharge can occur, damaging the cell. Also, if the voltage reaches values above 4.2 V the cell can be destroyed due to overheating [8]. Thus, it is really important to know the voltage of each cell and undertake precautions to prevent severe damage [9,10].

The current manuscript presents a battery management system (BMS) capable of monitoring a theoretically infinite energy storage system. This monitoring system is important when balancing and charging the cells as it requires information about individual cell and pack voltages. In addition, the acquisition unit diagnoses the battery conditions, such as static fault detection, minimum and maximum cell voltages and temperature. The only limitation of this system lies in the voltage battery pack: about 700 V corresponding to 168 cells connected in series.

Methodologies to charge batteries can be found in the literature, but there are only a few methodologies for charging large Li-ion battery packs. Thus, it is imperative to monitor and manage the voltage of each individual cell, otherwise cell voltage can reach dangerous levels [8].

This paper proposes an algorithm that combines charging with balancing methods, based on the multistage method. One of the most relevant proposed innovations deals with the criterion for switching between current levels. This transition is made based on the calculation of the error between the actual cell voltage and the desired voltage. The implemented algorithm also considers the charging current, allowing for the estimation of the state of the charge. Another important feature is the introduction of a balancing procedure in the algorithm, allowing an equalization of the cells that is of extreme importance for large Li-ion battery packs.

This paper is organized as follows: Section 2 presents and evaluates cell balancing and cell charging methods presented in the literature. Section 3 describes the hardware related to the proposed BMS. Section 4 presents the developed software. Section 5 explains the designed and implemented algorithm. Section 6 shows the results obtained by the proposed system. Section 7 concludes the paper and discusses the results.

## 2. Background

2.1. Balancing Methods

There are two kinds of methods to balance Li-ion batteries, active and passive. Active cell balancing methods can present different topologies, which can be classified in two groups based on the use of capacitors or the use of converters. This second group can be further divided into two subtypes: isolated and non-isolated. Depending on the topology of the electronic circuit, it is possible to balance at different levels: cell-to-cell, cell-to-pack, pack-to-cell and cell-to-pack-to-cell [11,12].

The cell balancing circuits based on capacitors use a capacitor in parallel with a chosen cell or pack to transfer energy from higher voltage to lower voltage cells or packs. In this group, different topologies can be adopted, from the simplest (like the switched capacitor) to the more complex (like the modularized switched capacitor) [6,12–17]. In the literatures, additional methods are proposed, such as the double-tiered switched capacitor [12], the automatic switched capacitor [15], the single switched capacitor [13,14], the chain structure of switched capacitor [16], and the series-parallel switched capacitor [17]. Figure 1a presents a modularized switched capacitor capable of transferring energy from cell to cell in the first-tier capacitors, and from pack to pack in the second-tier capacitors.

In the cell balancing circuits based on converters, the battery pack is the energy source for the converter that will then charge the chosen cells. The isolated converter balancing circuit is based on the use of isolated DC-DC converters and can have various topologies, like with multi-winding transformer [6,12,14,18], multiple transformers [12,18], and single switched transformer. Figure 1b shows an example of an isolated converter [19,20]. The non-isolated converter balancing circuits are based on non-isolated DC-DC converters such as the buck, boost, buck-boost [18], or Cuk [14,18]. Other examples of topologies based on non-isolated DC-DC converters are the full-bridge DC-DC [12,18]

and the quasi-resonant converters [18]. All these topologies can be unidirectional or bidirectional. Figure 1c presents an example of a non-isolated converter [21].

In passive cell balancing methods, the cells are balanced by discharging when the battery is not being used, or by providing an alternative path for the current to flow while it is being charged. There are a few topologies for passive methods, such as the fixed shunt resistor and the shunt resistor [12,14]. Another topology, and the most common method, is the switched shunt resistor, presented in Figure 1d. Other topologies are presented in [6], such as the dissipative shunting resistor, analog dissipative shunting, PWM controlled shunting, resonant converter, boost shunting and complete shunting. The cell balancing is made by using semiconductors controlled to be turned on or off, allowing the current to flow through the resistors connected to each cell [6,12,14,18].
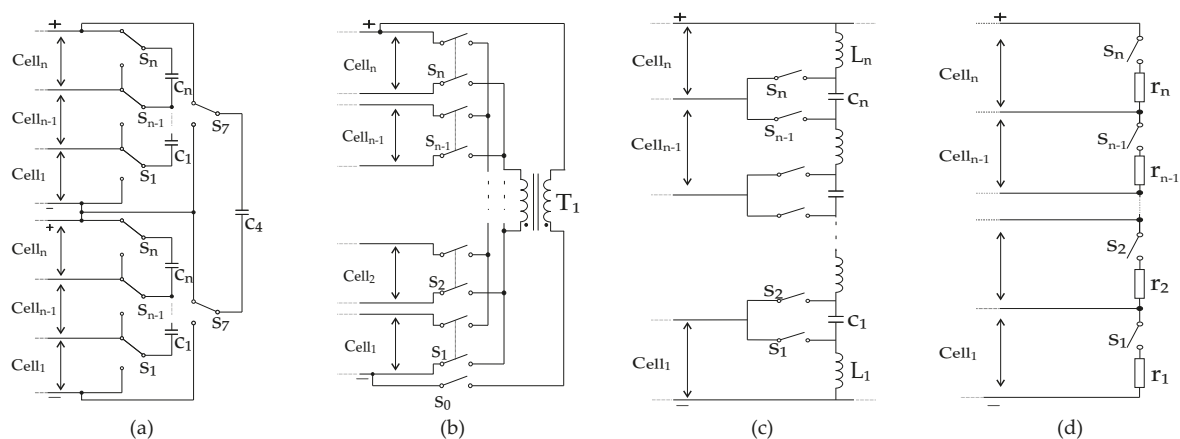
Figure 1. Several balancing topologies: (**a**) Modularized switched capacitor; (**b**) Switch matrix transformer; (**c**) Cuk converter; and (**d**) Switched shunt resistor.

A trend that is emerging in the literature is the use of dynamic (reconfigurable) topologies. Kim, Qiao and Qu [22] proposed a dynamic topology that allows cells to be deactivated (bypass), in case of an imbalance or failure. The application of this methodology can be performed during charging and discharging periods. Another methodology that involves dynamic topologies consists in reconfiguring the battery pack connections in real time. For example, Kim and Shin [23] proposed a topology called Dependable, Efficient, Scalable Architecture (DESA) that enables online reconfiguration depending on the charge level.

Although these methodologies are described in the literature as fast and efficient in terms of balancing, they require a high number of switches that must handle high currents. This exponentially increases cost and size, limiting the use of these methodologies for high power applications [24].

Figure 2 compares the main characteristics of different balancing methods. Due to its simplicity, cost, efficiency, volume, weight, robustness, and reliability [12] and the fact that it is widely used in the automotive industry, the work presented herein used the dissipative resistors method. This method has the advantage of not requiring complex control, as in active methods [25]. It should be noted that for large Li-ion battery packs passive methods are the most appropriate balancing methods, as others fail in terms of dimension and implementation costs. Table 1 presents a more detailed view of several balancing topologies introduced in literature, in order to offer a more intuitive analysis of several of the previously presented topologies.
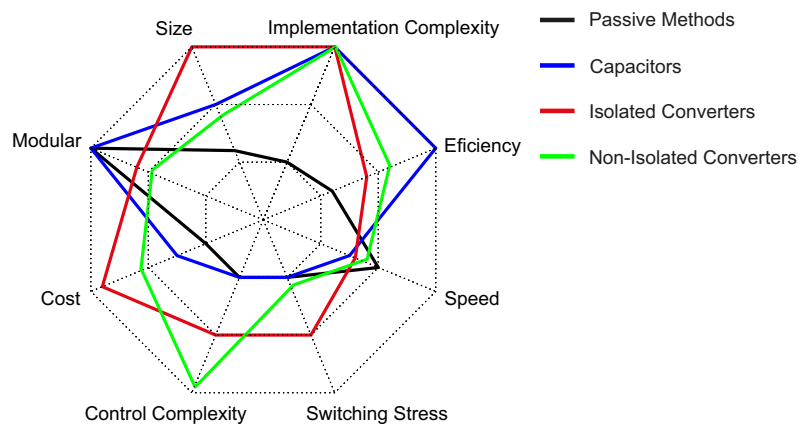
Figure 2. Comparison of balancing methods.

Table 1. Comparative table of the main characteristics of the balancing topologies (based on [6,12,18]).

| Balancing Topologies	Equalization Speed	Control Complexity	Implementation Complexity	Size	Components to Balance an *n* Cells, *m* Module
Fixed Shunt Resistor	Satisfactory	Very Simple	Very Simple	Good	*n* Resistors
Switched Shunt Resistor	Good	Simple	Very Simple	Good	*n* Resistors, *n* Switches
Complete Shunting	Fast	Simple	Medium	Good	4*n* Switches
Switched Capacitor	Normal	Medium	Simple	Normal	*n* − 1 Capacitors, 2*n* Switches
Single-Switched Capacitor	Good	Complex	Simple	Satisfactory	1 Capacitor, 2*n* Switches
Double-tiered Switched Capacitor	Good	Medium	Simple	Good	*n* Capacitors, 2*n* Switches
Modularized Switched Capacitor	Good	Complex	Medium	Normal	*n* − 1 Capacitors, 2*n* + 2*m* Switches
Multiple Transformers	Good	Medium	Simple	Bad	*n* Transformers, 1 Switch, *n* Diodes
Single Switched Transformer	Satisfatory	Complex	Medium	Bad	*n* + 3 Switches, 1 Transformer
Cuk Converter	Fast	Complex	Simple	Bad	2*n* − 2 Inductors, *n* − 1 Capacitors, 2*n* − 2 Switches
Buck Converter	Excellent	Complex	Excellent	Bad	*m* Inductores, *m* Capacitors, 2*m* Switches
Full-bridge Converter	Fast	Complex	Medium	Very Bad	*m* Capacitors, 4*m* Switches

2.2. Charging Methods

The Constant Current/Constant Voltage (CC/CV) charging algorithm is widely referenced in the literature because of its simplicity and ease of implementation. However, when applied to a large Li-ion package, this type of charging suffers from some implementation limitations. This algorithm is characterized by three phases of operation, as illustrated in Figure 3a.

The first phase, called the trickle charge (TC), corresponds to a cell voltage below the $V_{trickle}$ critical value. In this condition, the cell should be charged with a reduced current, typically with a value of C/10 where C is the nominal capacity of the cell. As soon as the cell voltage exceeds the $V_{trickle}$ value, the charging algorithm switches to the second phase. At this stage the cell is subjected to a constant charging current (CC), with a fixed and predetermined value, varying between 0.5 C and 3.2 C depending on their specifications. When the cell voltage reaches the V_{charge} value (typically 4.2 V), the algorithm switches to the third charging phase. At this stage the cell is subjected to a constant

voltage (CV). When the current reaches a default value, typically 0.1 C, or the maximum charging time, the process is complete [26,27]. To mitigate the disadvantages of this method (mainly the charging time), some variants can be found in the literature, for example, the double-loop control charger (DL-CC/CV), the boost charger (BC-CC/CV), the fuzzy-logic control (FL-CC/CV), the grey-predicated control (GP-CC/CV) and the phase-locked loop control (PLL-CC/CV) [26].

Optimal ion conductivity control (OIC), proposed in [28], is an algorithm to improve the performance of the CC/CV method. This method controls ion conductivity, one of the electrochemical characteristics relevant to an optimal charging control strategy. This control scheme measure online the battery impedance and tracks its saturation points, resulting in better efficiency, less charging time, and less temperature rising rate. Another methodology in the literature is multistage charging consisting of multiple charging stages with different current levels, as shown in Figure 3b. This method establishes different current levels and the conditions for changing stages. The most used criterion to switch between stages (threshold crossing criterion) is a defined cell voltage limit, reducing the current and making the voltage readings more realistic, because the voltage drop across the internal resistance of the cell is smaller [26].
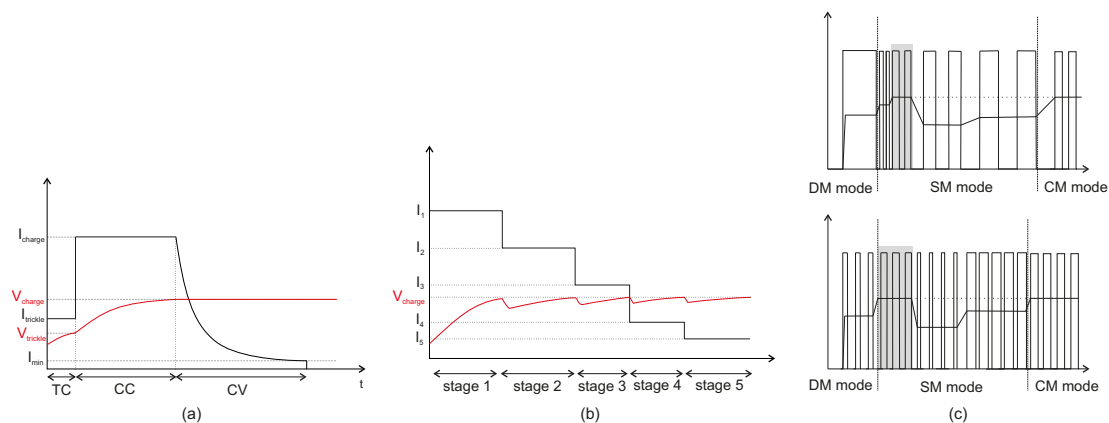
Figure 3. Charging methods: (**a**) CC/CV charging method; (**b**) multistage charging method; and (**c**) pulse charging method (above variable frequency pulse charge and below variable duty pulse current).

Some authors choose optimization algorithms to find the most optimal stages based on different approaches, such as the PSO algorithm and fuzzy controllers in [29,30]. However, despite the use of optimization algorithms, the threshold crossing criterion continues to focus on the cell voltage limit.

Another charging method, the Pulse Charging Method, is characterized by the use of a pulsed current and can be subdivided into two methodologies: the Variable Frequency Pulse Charge (VFPC) and the Variable Duty Pulse Current (VDPC), as illustrated in Figure 3c [31]. The VFPC optimizes the frequency of the current pulse in order to minimize the impedance of the cell and consequently to maximize the transference of energy. This energy transference maximization can be achieved in two different ways: by setting the pulse amplitude and varying pulse width, or vice versa. Chen [32] proposed a VFPC charging algorithm composed of three modes of operation: detection mode (DM), search mode (SM), and charge mode (CM). Briefly, the algorithm starts its operation in the DM mode and detects the state of the cell, applying a constant voltage to the cell in order to monitor the charging current. Once this mode is finished, the algorithm switches to the SM mode of operation, discovering the optimal frequency. As soon as the frequency is "optimized" the algorithm enters the CM mode of operation, repeating this process until the cell is charged. Also, in [33], the same author proposes a similar method based on the VDPC methodology.

A comparison of the various charging methods is shown in Figure 4. The multistage charging method has the best relationship between efficiency, simplicity of control, and charging time. The pulse charging method is the worst in terms of implementation and control complexity.
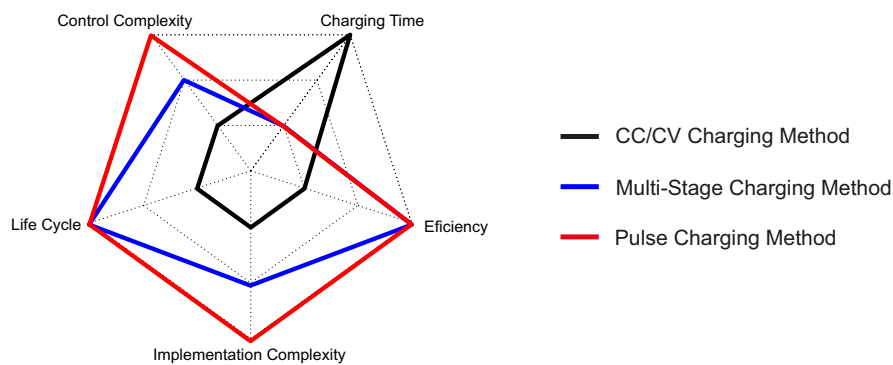
Figure 4. Comparison of charging methods.

3. Hardware Development

3.1. System Topology

A new hardware setup was implemented to make the system presented in [34] more robust and versatile. This is theoretically capable of supporting infinite power and allows the implementation of different charging and balancing algorithms in a simpler and more effective way. The topology used can be represented by the block diagram in Figure 5. Thus, it is possible to divide the system into three fundamental units: control and processing unit, acquisition and balancing unit and power unit.
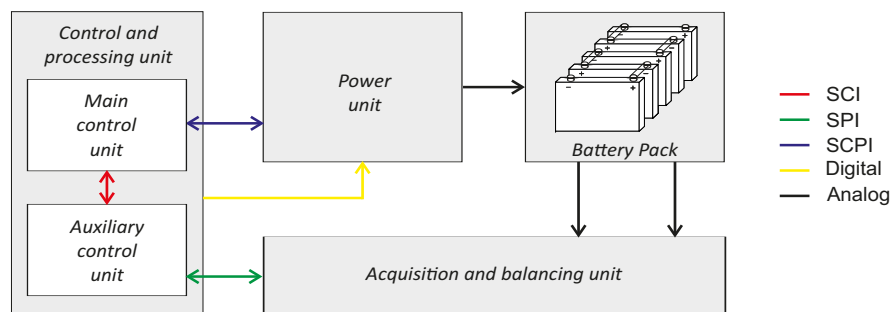
Figure 5. Block diagram of the hardware topology.

3.1.1. Control and Processing Unit

The control and processing unit is composed of a centralized architecture with two subsystems. One is the main control unit containing the software developed in Matlab. This choice allows greater flexibility and speed in the development of new combined charging and balancing methodologies.

The other subsystem (auxiliary control unit) consists of the TMS320F28069 microcontroller. This microcontroller is a 32-bit floating-point used in mathematical tasks with some complexity, since it is capable of performing parallel processing. It has a clock frequency of 90 MHz, with a RAM of 100 kb and 2 kb of ROM and a flash memory of 256 kb. It also has 16 PWM channels and 16 channels of 12-bit ADC, and the I^2C, USB, CAN, SCI and SPI communication protocols.

The auxiliary unit provides greater versatility in the interconnections between the main control unit (Matlab) and the other units by using the two asynchronous communication modules (serial communications interface; SCI) and the two synchronous communication modules (serial peripheral interface; SPI).

The main control unit communicates directly with the power system (Programmable DC SL 500-5.2 source) through the Standard Commands for Programmable Instruments (SCPI) asynchronous serial communication protocol. All other communications are performed from the auxiliary control system by the asynchronous RS-232 serial communication protocol.

3.1.2. Acquisition and Balancing Unit

The acquisition unit is centered on the ISL94212 device (Intersil, Milpitas, CA, USA), enabling it to be connected in a chain of up to a maximum of 14 devices (168 cells in series and *n* in parallel). This unit also performs extensive diagnostic functions (static fault detection functions, oscillator check function, cell overvoltage, cell undervoltage, V_{BAT} or VSS connection test, open wire test, overtemperature indication, reference check function, register checksum and EEPROM MISR checksum). Each device has capacity for 12 cells, constituting a stack of the battery pack.

Figure 6 presents the system developed to monitor and control a 24SnP system (24 cells in series and *n* in parallel). In this work, a 24S1P system was implemented resulting in a nominal power of approximately 230 W/h.

The position of each device in the chain is defined by COMMS SELECT 1 and COMMS SELECT 2 inputs of each device, where the main device takes the first position of the chain, working as master for communication purposes. This device communicates with the main control unit through the auxiliary control system via SPI.
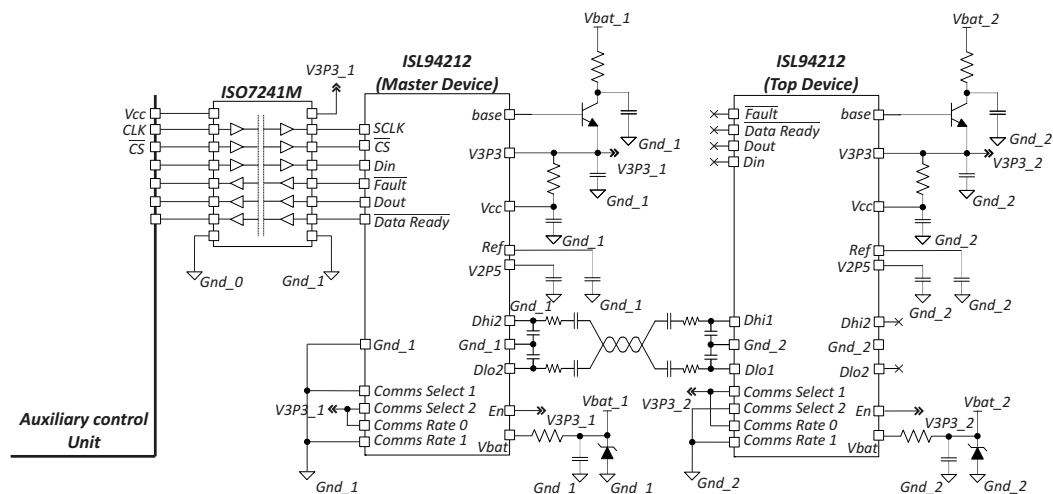

Figure 6. Electrical circuit of ISL94212 devices forming the chain.

Another feature of the ISL94212 device is the possibility to easily implement low-cost balancing methods with external circuits, by providing analog-digital converters (ADC's) to monitor the chain voltage with a resolution of ±180 mV and the individual cell voltage with a resolution of ±10 mV. The device also has outputs dedicated to the activation/deactivation of switches (MOSFET) required for the realization of balancing methods.

Using the Switched Shunt Resistor passive balancing method (in this case R_{bal} = 33 Ω), as shown in Figure 7, the device, through the programming of internal registers, offers three operating modes: timed balance mode, auto balance mode, and manual balance mode. In the timed balance mode, the main control unit defines the duration of balancing (between 0.33 and 42.33 min), as well as the instant when the balancing of the cells begins. In manual balance mode, the main control unit defines the beginning and the end of the balancing period. Finally, in the auto balance mode, the device performs balancing autonomously, depending on the state of charge at time *t*, the desired state of charge, the impedance of the balancing circuit, and the sampling time.

The ISL94212 device only allows the monitoring of four temperature sensors, therefore a system has been implemented to enable the use of a larger number of sensors (in this case 12 sensors, 1 sensor for each 2 cells), as shown in Figure 8. Given the limitations of the auxiliary control circuit, which only provides 16 analog ports, the analog multiplexer CD74HC4067 was used, allowing circuit expansion if desired. The temperature value is extrapolated through the Steinhart-Hart equation using Semitec's 10 k Ultimate Thinness NTC thermistor.
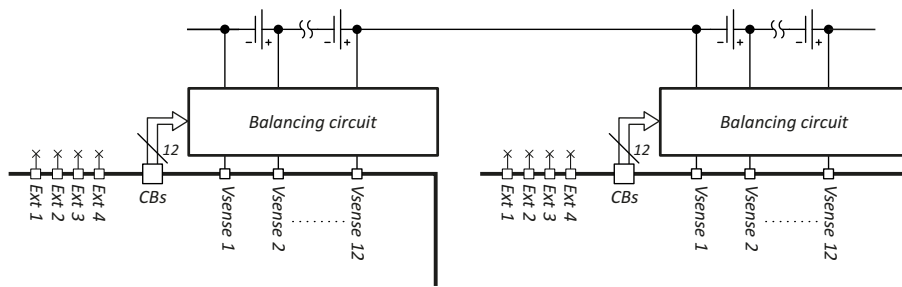
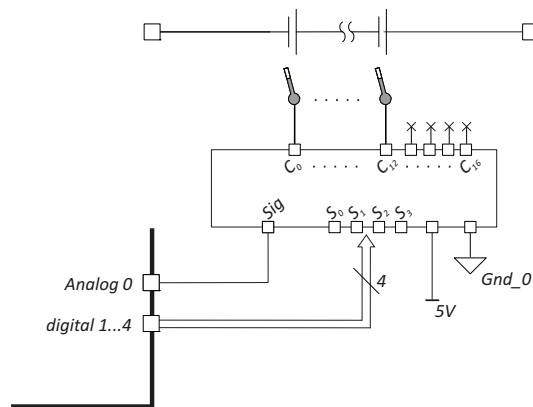**Figure 7.** Representation of the balancing circuit.

Figure 8. Representation of the electric circuit of the temperature acquisition system.

3.1.3. Power Unit

The power unit used in this work is based fundamentally on the DC SL 500-5.2 programmable power supply, which communicates directly with the main control unit via the SCPI asynchronous communication protocol.

To ensure that current only flows in one direction, a diode (whose voltage drop is compensated through the V_{sense} inputs of the programmable power supply) has been introduced in the power unit circuit. An isolated switching MOSFET drive circuit was designed (Figure 9) in order to implement the Variable Frequency Pulse Charge (VFPC) and Variable Duty Pulse Current charge (VDPC) methods described previously. This circuit, based on TLP152 optical couplers, allows a maximum switching frequency of 250 kHz. Also, an isolated DC-DC converter was used to adjust the MOSFET trigger voltage, as well as to reduce noise in the main control unit.
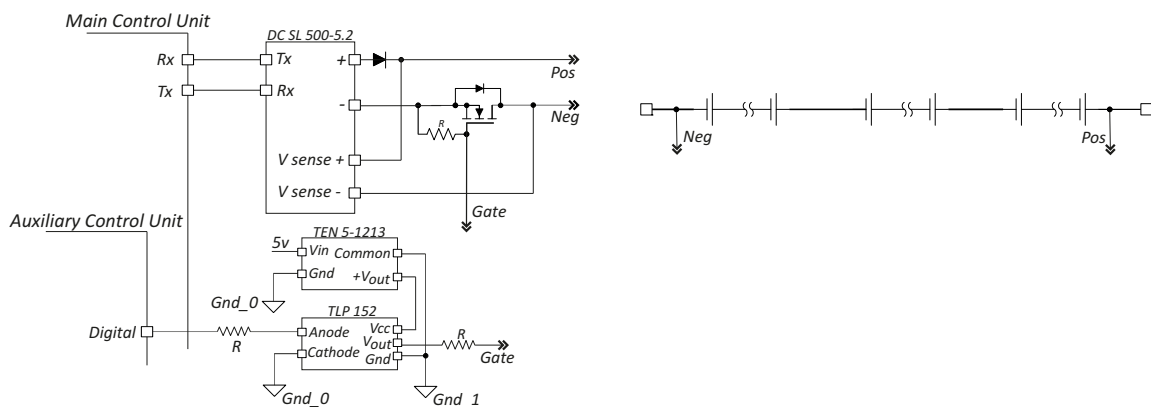

Figure 9. Power circuit command system.

4. Software Development

4.1. Auxiliary Control Unit

All algorithms implemented in the auxiliary control unit were developed in C language in Code Composer Studio version 6 (Texas Instruments, Dallas, TX, USA). The algorithm consists of a main program, shown in Figure 10, where in a first step all variables are initialized and the peripherals and interrupts are configured. After the initial settings, the unit remains in an infinite loop, waiting for the communications frame from the main control unit via SCI serial communication protocol. The first byte of the communications frame is interpreted by the auxiliary unit, allowing the selection of one among four implemented functions.
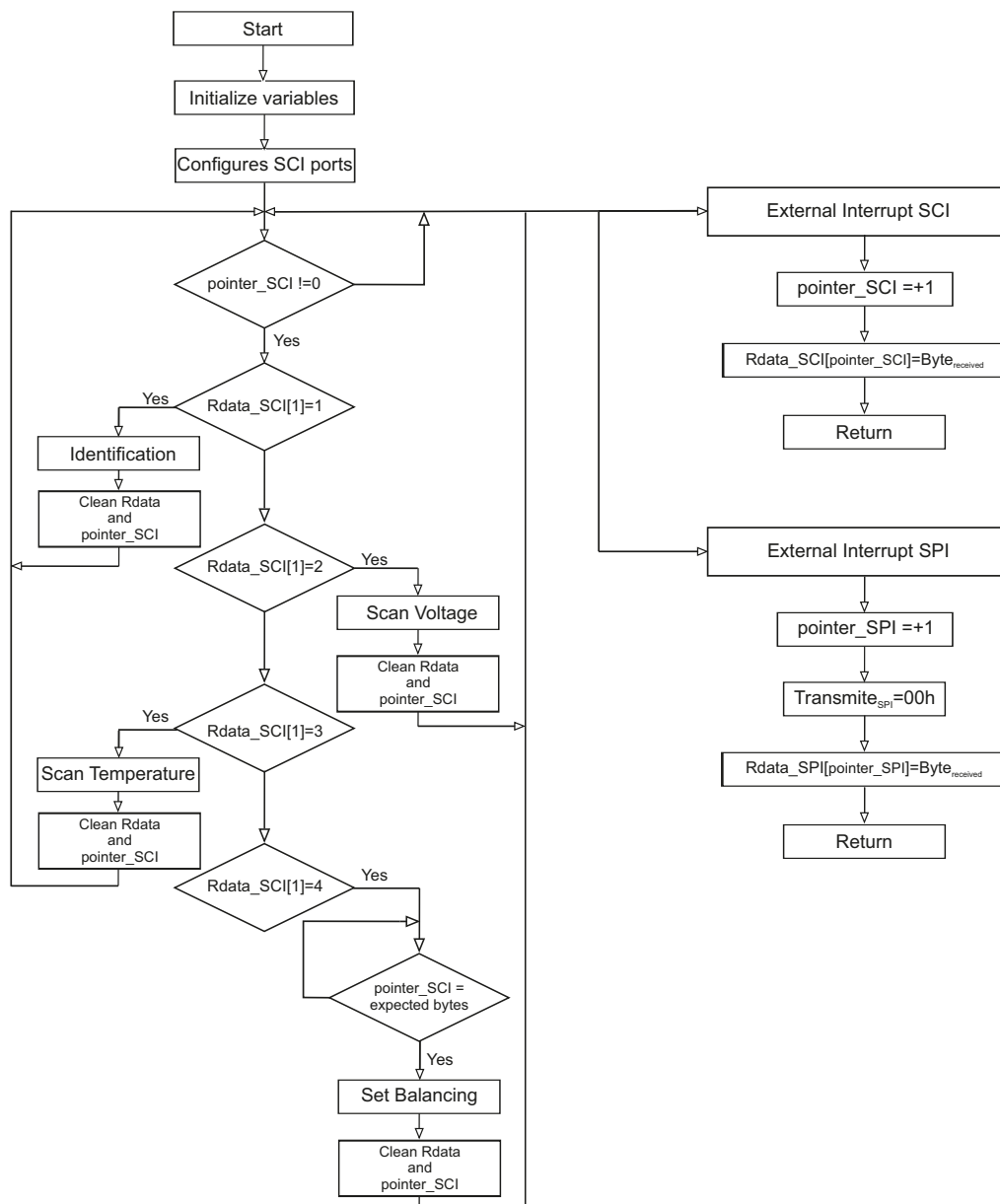

Figure 10. Flowchart of the main program implemented in the auxiliary control unit.

Table 2 presents a brief description of the functions implemented, the size of the communications frame from the main control unit, and the command byte.

Table 2. Brief description of the functions implemented in the auxiliary control unit.

Function	Dimension	Command Byte	Description
Identification	1	01 h	Responsible for identifying the number of devices used
Scan Voltage	1	02 h	Responsible for reading the voltage of the cells
Scan Temperature	1	03 h	Responsible for reading the temperature of the cells
Set Balancing	8 (by device)	04 h	Responsible for the selection of the cells and the duration of the balancing time

There are two interrupt routines in the algorithm: the SCI interrupt routine, associated with the asynchronous communication module SCI, which is responsible for reading the communications frame from the main control unit; and the SPI interrupt routine, a hardware falling edge-triggered interrupt routine associated with the GPIO20. The GPIO20 is configured as an input, associated with the output of the master device (data ready), which indicates that the data is available on the serial communications port (SPI).

4.1.1. Identification Function

The identification function is responsible for identifying the number of devices and their positions in the chain (ISL94212 devices). Briefly, this process starts by transmitting a 3-byte frame to the master device. Once this device is addressed, it responds with a 4-byte frame, which indicates the success of the process, and also states its position in the chain. This process is repeated until the addressed device is at the top of the chain. When the device at the top of the chain is identified, the identification process is complete. This routine returns one byte representing the number of devices in the chain.

4.1.2. Voltage Scan Function

The voltage scan function is responsible for reading the voltage of the battery pack cells. The initialization of this process is carried out as previously described, by requesting sampling of the voltages. Afterwards, there is a request for the value of the readings corresponding to a 40-byte communications frame. Once this is received it is directed to the main control unit, returning 40-bytes for each device forming the chain.

4.1.3. Temperature Scan Function

The temperature scan function is responsible for obtaining the temperature of the battery pack cells. Cyclically this process selects the desired read channel through inputs S1, S2, S3 and S4 of the analog multiplexer. Once the desired channel is selected, the ADC is forced to read from the auxiliary control unit. Since the ADC is 12 bits, the conversion value is decomposed into a 2-byte frame and directed to the main control unit via SCI. This process is repeated for all devices, returning 24 bytes to the main control unit.

4.1.4. Balance Set Function

The balance set function is responsible for defining the duration of the balancing process and the cells to be balanced. The process is initialized with a frame of 8 bytes per device, derived from the main control unit, with the values of the registers necessary for the configuration.

Briefly, the function is initiated by configuring the Balance Setup Register of device *i*, which sets the balancing mode to timed balance mode. If device *i* responds with a 4-byte frame (ACK) that means that the process was successful and the Balance Time Register is set up with the duration of the balancing process.

After the previous process is complete, the Balance Status Register is set up and defines the cells of device *i* subjected to balancing. The balancing process is initiated with the Enable Balance command. The function is repeated for all the devices of the pack.
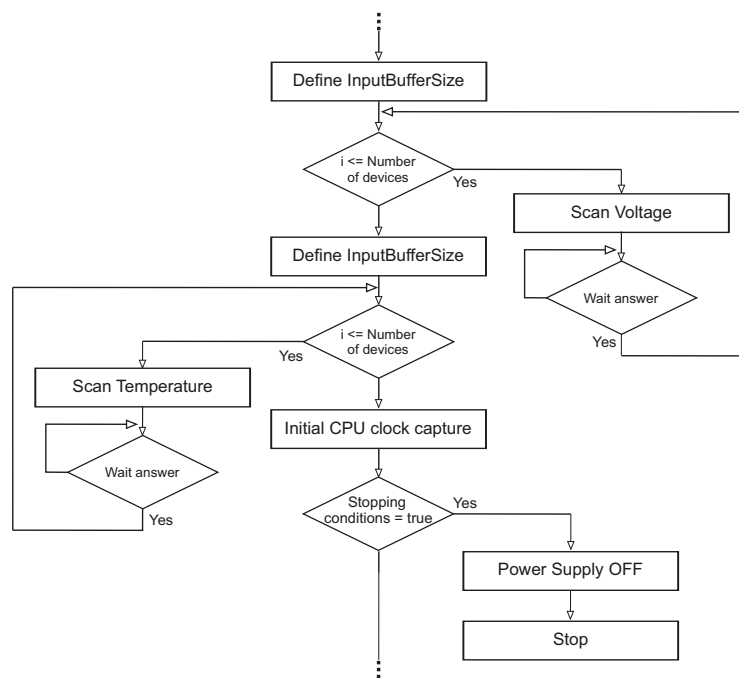
4.2. Main Control Unit

All algorithms implemented in the main control unit were developed in Matlab software. The main flowchart of the proposed algorithm can be divided into four segments. The first segment is shown in Figure 11 and includes the initial configuration as well as the definition of the number of devices in the pack. First all variables are initialized, the SCI communication ports are configured, and the duration time of the balancing process is defined. After the initial configuration, the command byte (01 h) is sent, which triggers the identification function in the control auxiliary unit. The main control unit waits for the return of this routine: a byte corresponding to the number of devices present. If the response is non-zero, the algorithm proceeds to the second segment. If the answer is zero, the algorithm makes two more attempts. If after the third attempt the answer is still zero, an error message is shown and the process is interrupted.
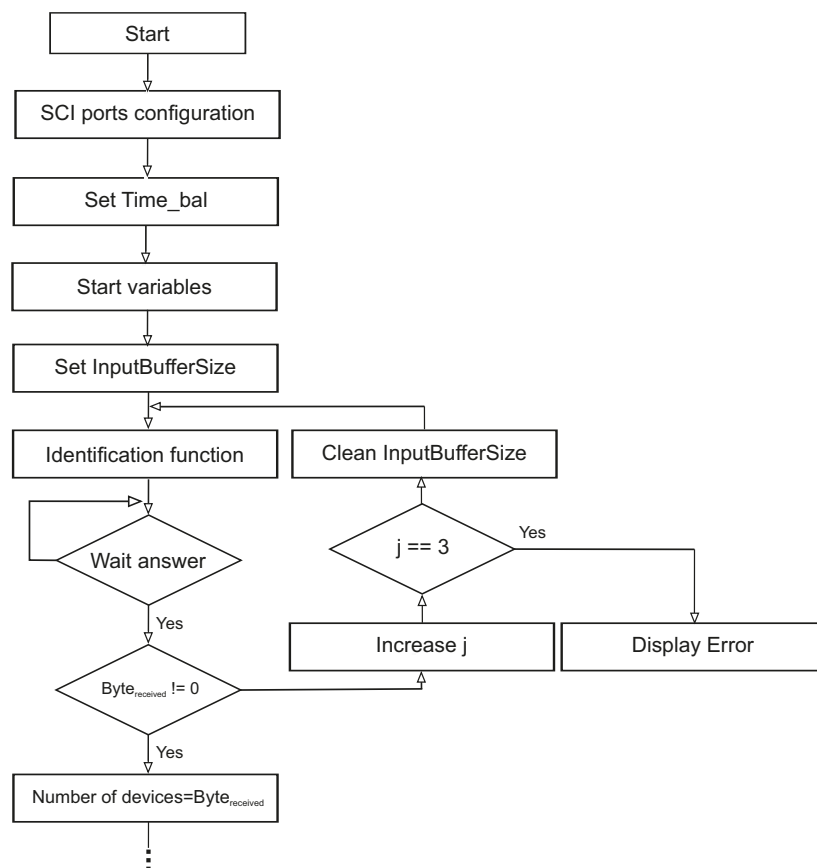
Figure 11. Flowchart of the program implemented in the main control unit—First Segment.

The second segment of the algorithm, shown in Figure 12, is responsible for the acquisition of pack cell voltages and temperatures. The first byte sent corresponds to the command (02 h) that will trigger the scanning voltage function. After the previous process is completed, the second byte corresponding to the command (03 h) is sent in order to trigger the scan temperature function.

With the initial readings are completed, the algorithm remains in an infinite loop until the stopping criteria, detailed later (Section 5), is met. When this occurs, the algorithm communicates with the power unit via SCPI with the STOP command. If the stopping criteria are not met, the algorithm executes the remaining code, described in the following segments, until a new check.

Figure 12. Flowchart of the program implemented in the main control unit—Second Segment.

The third segment of the algorithm, shown in Figure 13, defines the voltage of the power unit as calculated by:

$$dv \times N \times N_d \tag{1}$$

where: dv is the desired voltage (4.2 V), N represents the number of cells and N_d is the number of devices. Since cell balancing influences voltage readings, there is a five second lag between the balancing process (one minute in this work) and the acquisition of the cell voltages. Thus, the acquisition of the voltages is carried out at a frequency determined by the following equation:

$$1/(T_b + 5) \tag{2}$$

where T_b is the balancing time.

Once these readings are obtained, the algorithm proceeds to the third segment.

Figure 14 shows the last segment of the algorithm, which is responsible for determining the cells to be balanced. For this, a line vector is defined with a dimension given by the following equation:

$$N \times N_d, \tag{3}$$

This vector is formed by ones if the balancing criterion is met and zeros otherwise (detailed later in Section 5). When the vector is complete, the algorithm proceeds to the functions related to cell balancing.

The balancing process has two inherent functions: The Get Frame Balance Time Register function and the Get Trama Balance Status Register function. The first function sets the duration of the balancing process, configured within a 0.33 to 42.33 min by setting the [14:8] bits of the Balance Time Register of each device. Initially, the algorithm determines the number of times that T_b is divisible by 0.33 min (time base). The second function contains the information of the cells to be balanced through the Balance Time Register of each device. The algorithm decomposes the balancing vector, calculated in the fourth segment of the main flowchart, and performs the concatenation of the bytes. Once these bytes are determined the communications frame is built and transmitted to the auxiliary control unit, and the algorithm performs the second segment in order to re-check the stopping criteria.
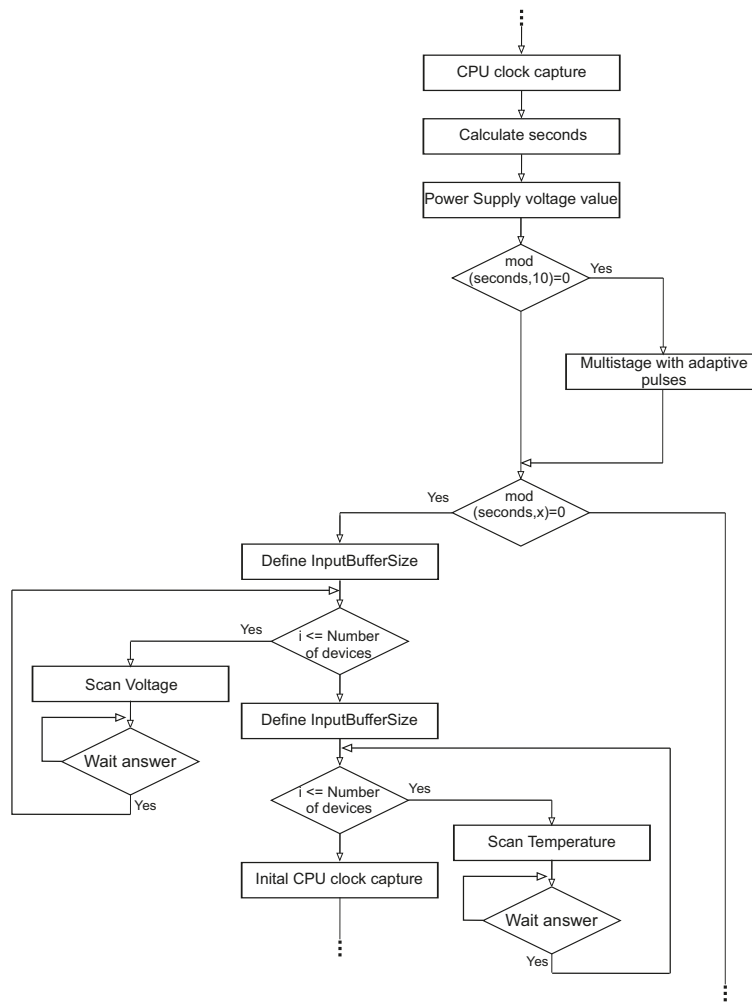
Figure 13. Flowchart of the program implemented in the main control unit—Third Segment.
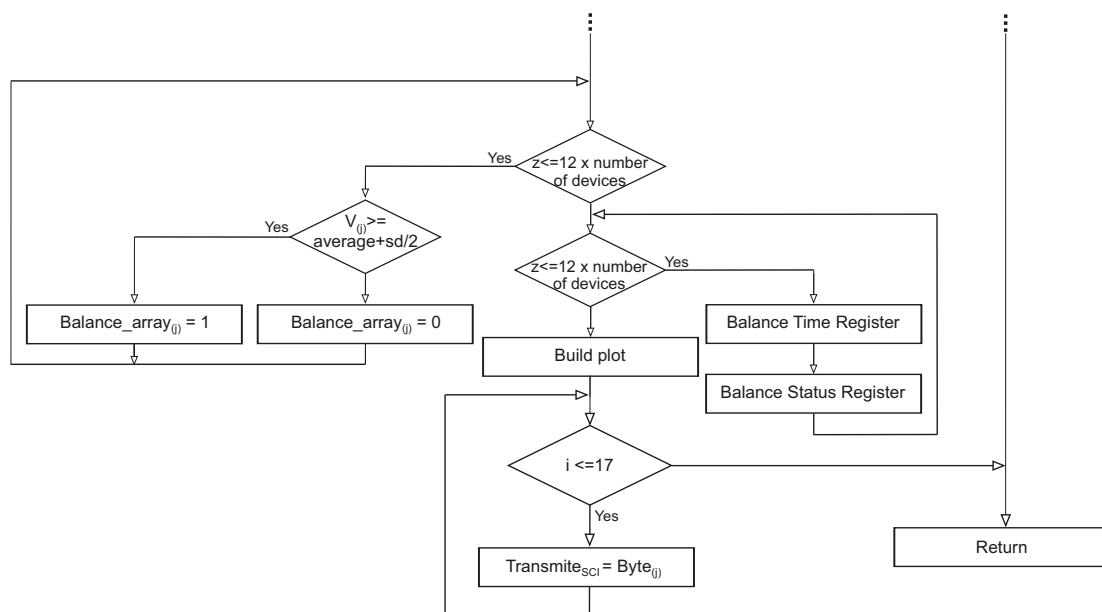

Figure 14. Flowchart of the program implemented in the main control unit—Fourth Segment.

5. Proposed Methodology

When referring to large Li-ion battery packs it is essential to have communication between the charger and the BMS, otherwise, the charger does not provide any protection, but rather a false sense of security that can lead to pack damage. The charger alone, without individual cell voltages values, becomes a reckless solution for the protection of a large Li-ion battery pack [8].

As the charger does not consider the balancing current value it may harm the battery pack in terms of its total capacity. In order to avoid exceeding the battery safe voltage limits, some batteries are used between 20% and 80% of their capacity. With a good charging and balancing management system, it is possible to use batteries between 5% and 95% of their capacity, which represents a substantial increase in use of the available energy [35].

Concerning the charging method, the proposed system was based on the multistage method, since it presents less chemical reaction stress and shorter charging time [30]. It also has a relationship between efficiency, simplicity of control, and charging time that is better than the other methods in the literature. It is also important to note that this is the most adequate method for large Li-ion battery packs because of its versatility.

Five current levels were chosen for this work. The choice of the number of levels was based on the study carried out by [36], where the authors evaluate the effect of different numbers of levels in relation to charging time and efficiency. According to the experimental results, the difference between applying a different number of charging current levels is almost negligible when the number of charging current levels is more than five. Therefore, gradual decreasing five-stage charging levels were chosen.

Another fundamental aspect is determining the value of the current levels; in this work, they were determined based on the battery conditions, the capacity, the balancing methodology, and the balancing current.

Therefore, the most important levels are the highest and lowest. In order to choose the highest current level the capacity of the batteries was taken into account, which according to the cell manual [37] is 1.5 A. For the lowest current level, the methodology and balancing current were considered, and it was set at 0.2 A. The remaining levels were interpolated as a function of the error.

The algorithm described was formulated mathematically through the following equations:

$$\text{Min } f_k(\gamma_k), \tag{4}$$

Subject to:

$$V_{i,k} \leq 4.25, \tag{5}$$

$$\frac{1}{N}\sum_{i=1}^{N} V_{i,k} \geq dv \quad \& \quad \frac{1}{N}\sum_{i=1}^{N} V_{i,k} - 0.01 \leq V_{i,k} \leq \frac{1}{N}\sum_{i=1}^{N} V_{i,k} + 0.01, \tag{6}$$

where:

$$f_k(\gamma_k) = \begin{cases} 1.5 & if & \gamma_k \geq 0.3 \\ 0.8 & if & 0.3 > \gamma_k > 0.15 \\ 0.6 & if & 0.15 \geq \gamma_k > 0.1 \\ 0.4 & if & 0.1 \geq \gamma_k > 0.02 \\ 0.2 & if & \gamma_k \leq 0.02 \end{cases}, \tag{7}$$

with:

$$\gamma_k = dv - \max(V_{i,k}). \tag{8}$$

In addition to the charging equations, it is also necessary to take into account the balancing equation. The decision on which cells to balance is based on the following equation:

$$V_{i,k} \geq \xi_k + \frac{\delta_k}{2}. \tag{9}$$

In the previous equations, the variables are:

f_k: Function to be minimized at instant k;
γ_k: Error between voltages at instant k;
$V_{i,k}$: Voltage in cell i at instant k;
dv: Desired voltage (4.2 V);
N: Number of cells;
δ_k: Standard deviation at cell voltages at instant k;
ξ_k: Mean voltage in the cells at the instant k.

Expressions (4)–(9) are interpreted as follows:

- Expression (4) represents the mathematical formulation of the proposed algorithm, which is related to the minimization of the error of the voltages in the cells to 4.2 V and consequently the minimization of the charging time.
- Expression (5) represents a stopping criterion, whereby if any cell exceeds 4.25 V the charging is terminated.
- Expression (6) represents the second stopping criterion of the algorithm. If expression (5) represents a safety condition, (6) represents a premise whereby acceptable charge results are considered, that is, when the mean value of the voltages of the cells is greater than or equal to 4.2 V and all cells are within the acceptable voltage limits, charging is interrupted and considered to have been successfully completed. Both stopping criteria were selected according to the cell manual [37].
- Expression (7) represents the values the function takes for each possible error value.
- Expression (8) represents the error between the desired voltage (4.2 V) and the maximum voltage of the cells.
- Equalization of the cells (balancing) is performed through a statistical analysis expressed by Equation (9). This represents the condition by which cells are selected for balancing. If the condition is true for a particular cell, it will be equilibrated, as shown in Figure 15.
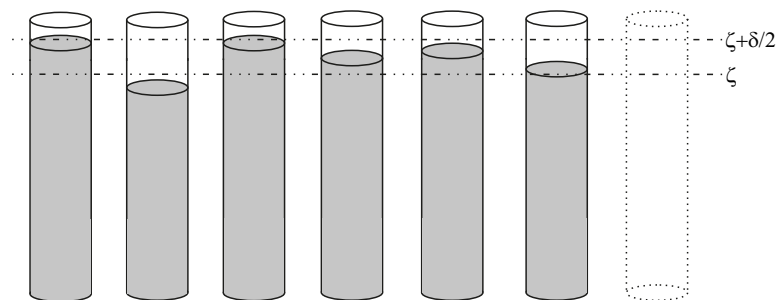

Figure 15. Graphic representation of the implemented balancing methodology.

6. Experimental Results

To test the implemented algorithm, two different types of cells were used, UR18650F-SCUD-3 cells (SANYO, Moriguchi, Japan) with a large number of charge/discharge cycles (case 1) and ICR18650-26H 2600 mAh cells (SAMSUNG, Seoul, Korea) with no charge/discharge cycles (case 2). Figure 16 illustrates the implemented hardware.

Figure 17 shows the evolution of the charging current throughout the entire process, for both case studies. The proposed methodology, when compared to the traditional Multistage charging methodology, optimizes the transition between levels and minimizes the voltage drop in the internal resistance of the cells during charging. This occurs because the common criterion used with the traditional Multistage Charging Method is as in Figure 3b, where change of stage occurs as soon as

the voltage of one of the cell reaches the value of 4.2 V. However, during charging, the cell voltage is greater than its real voltage due to a voltage drop in its internal resistance, which tends to zero as the current tends to zero. In the proposed method, this voltage drop is progressively attenuated during charging, which results in a reduction in charging time.

It is also important to analyze the differences between the two case studies in relation to the current. Thus, it is noteworthy that the proposed methodology behaves differently according to the battery condition. In case 1, due to the condition of the cells which results in a higher internal resistance, cell voltage decreases greatly during the transition between the current levels. This demands a current level correction, in order to reduce the error. In case 2, with the cells with no charge/discharge cycles, the cell voltage decays considerably less, thus the proposed algorithm approaches the traditional multistage method.

Therefore, the proposed algorithm perceivably adapts to the condition (number of charge/discharge cycles) of the cells used in the charging process. With the process of transition between current levels proposed in this article, there is a reduction in the charging time.
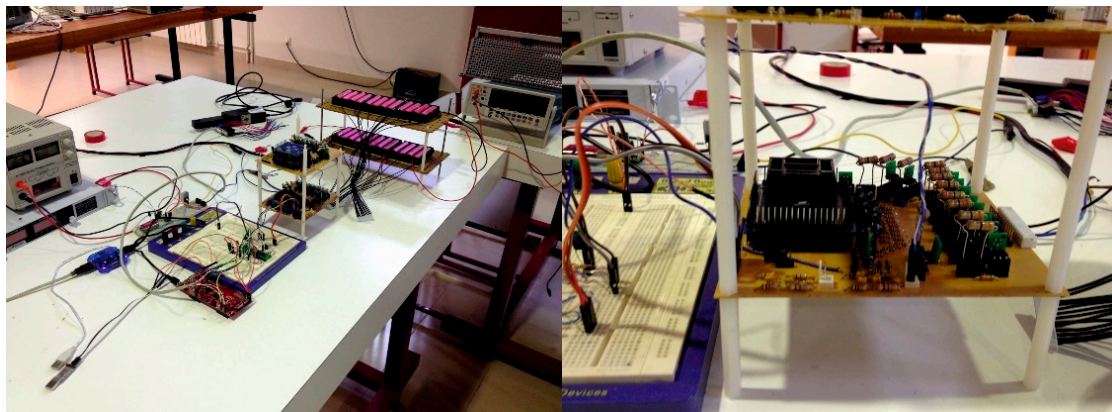

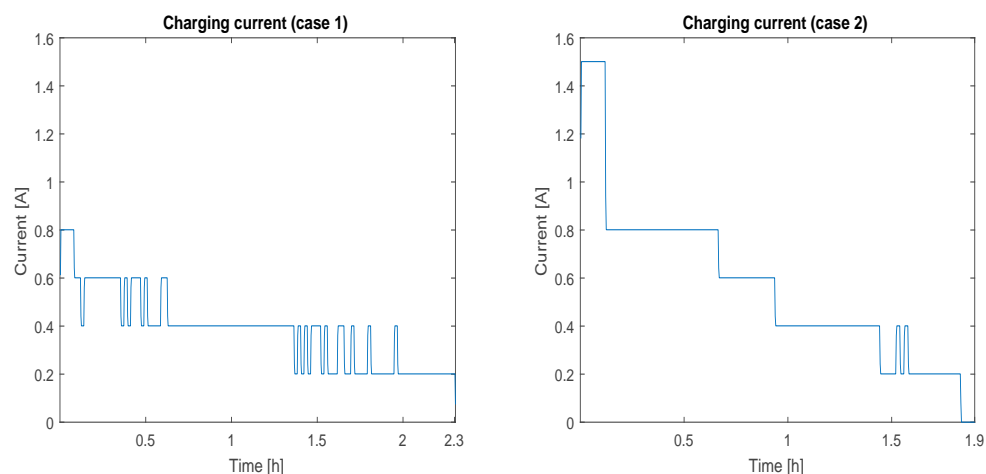**Figure 16.** Practical implementation.

Figure 17. Current profile during charging.

Figure 18 shows the evolution of the error of the voltage as a function of the charging time, corresponding to the charging process in Figure 17. These results reveal that the error decreases during the charging process, thus validating the measured voltage as the correct one.

As described above, a more pronounced oscillation is noted in case 1, resulting in the need for a greater adjustment in the transition between current levels.
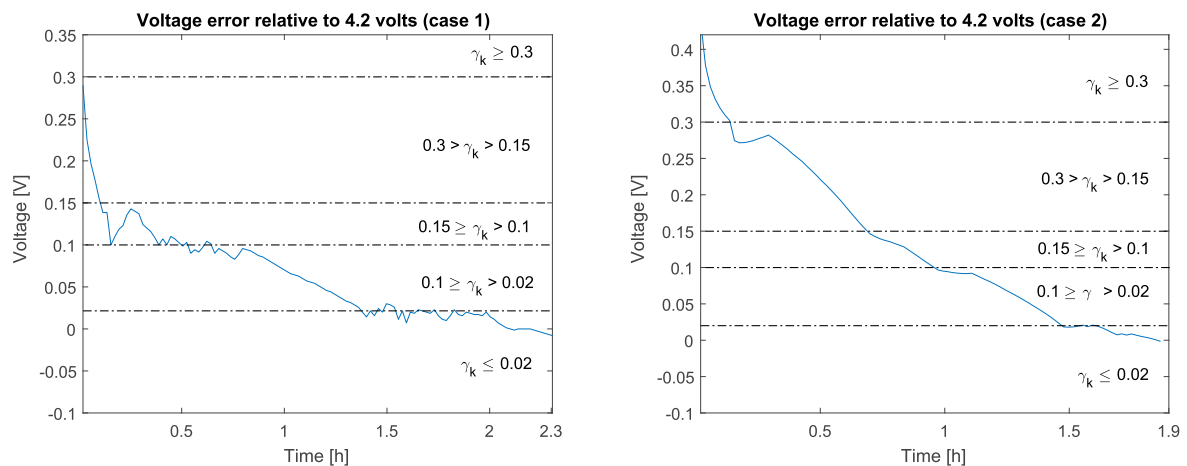
Figure 18. Error profile during charging.

Regarding the voltage present in each cell, it is possible to prove that at the end of the charging process the premises imposed by the algorithm were fulfilled, and all cells were within the desired limits. It is also relevant that although each cell has a distinct condition (greater internal resistance), the algorithm can overcome these differences, allowing the success of the charging process, as shown in Figure 19. This figure also illustrates that in case 1 there are greater variations in the voltage of the cells, resulting in the need for greater adjustment in the transition between current levels.
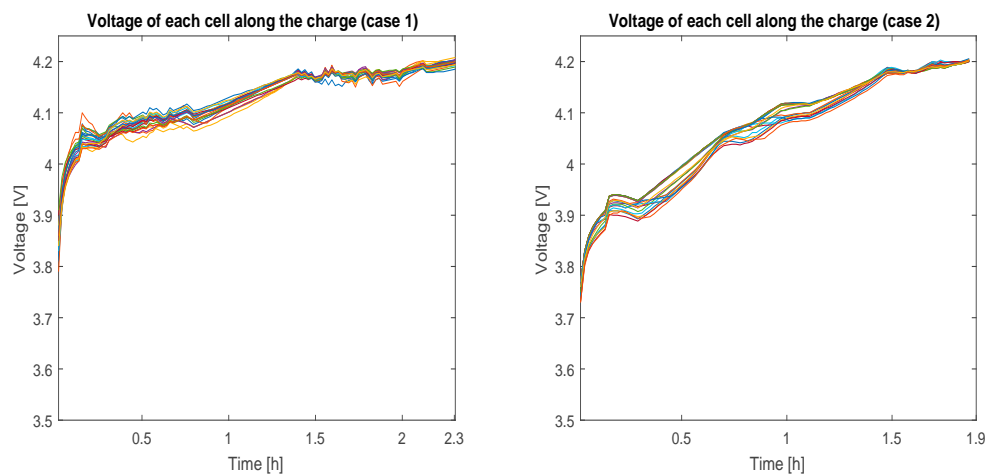

**Figure 19.** Voltage profile per cell during charging.

Figure 20 illustrates the evolution of the mean voltage (red line), the individual cell voltages, as well as a region defined by the mean voltage $\pm$ the standard deviation (gray area). It should be noted that the gray area decreases with time, i.e., the difference between voltages decreases during charging, which implies a correct order of balancing. We can also observe that the stopping criterion was reached is the two cases, that is, the mean voltage is equal to 4.2 V and all the cells were within the established limits (4.2 ± 0.01 V).

In the worst-case scenario, if there is a positive imbalance when one or more cells are positively distanced from the mean value, the algorithm maintains the minimum charge level, balancing the imbalanced cells until all are within the limits, resulting in a longer charging time. Inversely, if there is a negative imbalance, the algorithm maintains the minimum charge level until all the cells are within the limits established in the stopping criterion.
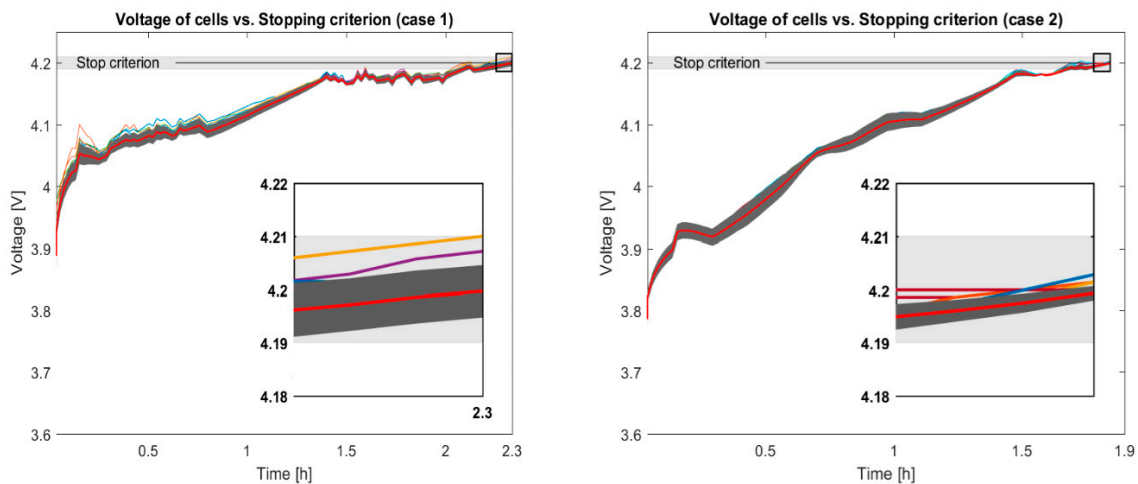
Figure 20. Voltage profile per cell vs. stopping criterion. The red line represents mean voltage, the gray area represents the mean of the voltages ± the standard deviation.

Figure 21 illustrates the behavior of each cell regarding one balancing process. A correct balancing order for the various cells is evident, in both of cases, proving a convenient formulation of the algorithm. Also, regarding the balancing process, even while charging, the top balancing is more effective, this happens because charging the current level occurs at a point close to the balancing current level, thus the cells are set to balance charge at significant lower rate than the rest, leading to cell equalization.
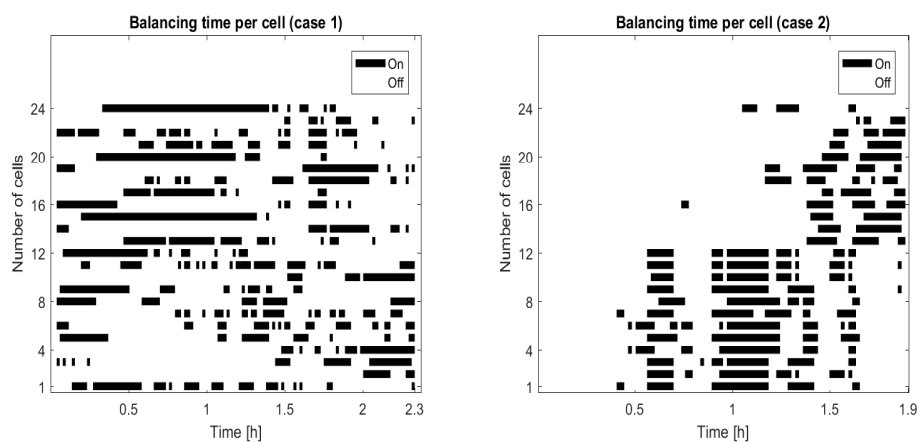
Figure 21. Balancing time per cell during charging.

It was also performed a charge for case 2 with the traditional Multistage method and with the proposed method for comparison purposes, considering the same charging conditions, Figure 22.

Through Figure 22 it is possible to perceive that the proposed algorithm has improvements regarding the charging efficiency. With regard to voltage deviation, a greater imbalance is observed in the traditional multistage method (0.0143 V) when compared with the proposed approach (0.01 V). The improvements over the multistage method are achieved due to a smoother transition between levels, achieving a voltage profile with fewer oscillations. In the traditional algorithm, the conditions of the battery influence the behavior in the transitions between current levels. This occurs due to the fact that the cells have a low internal resistance, and therefore, do not suffer sudden variations in voltage during the transitions between levels. With respect to charging time, with the proposed method the results show a reduction up to 7.2% (about 8 min).
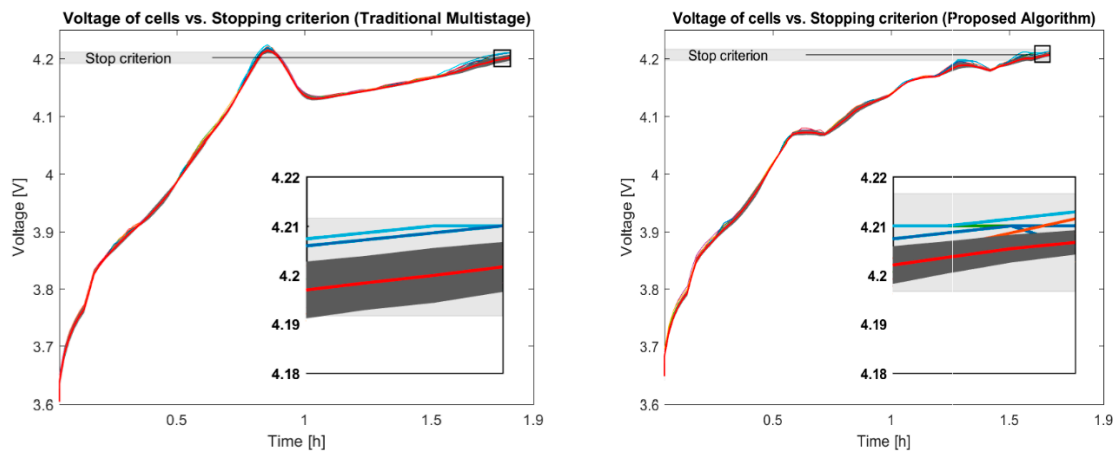
Figure 22. Voltage profile per cell vs. stopping criterion considering the traditional multistage method and the proposed method. The red line represents mean voltage, the gray area represents the mean of the voltages $\pm$ the standard deviation.

Concerning the temperature increasing during the charging process, the traditional algorithm presents a temperature increase of $\Delta T = 5.78\ °C$, whereas the proposed algorithm shows a temperature increase of $\Delta T = 4.6\ °C$, Figure 23. These results correspond to a 20.4% reduction for the proposed algorithm.

By these results, the proposed method when compared with the traditional Multistage is verified to improve the charging efficiency.
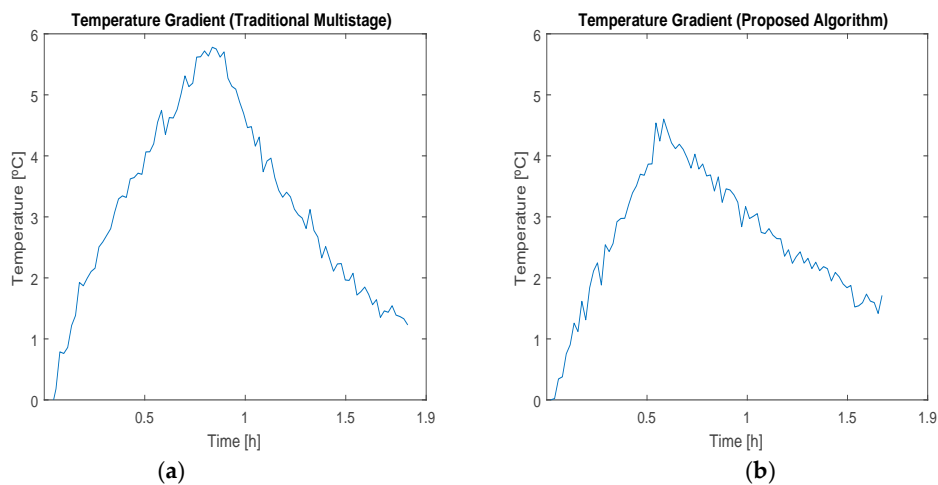
Figure 23. Temperature gradients during battery charging with (**a**) the traditional Multistage method and (**b**) the proposed method.

7. Conclusions

In this paper, a new algorithm is proposed combining charging and balancing with the objective of increasing the useful life of large Li-ion battery packs. The system is able to manage multiple battery packs with only a single voltage restriction, allowing a maximum of 168 cells in series. Since it has no restriction regarding the number of cells in parallel we can consider this system is theoretically an infinite power system.

The proposed algorithm presents an improvement over the multistage method, showing smoother voltage transitions when changing the current level, which in turn shortens the charging time. This advantage occurs because in the proposed charging method the current level changes according

to the difference between 4.2 V and the cell voltages, and not by default as in the traditional method. It is important to note that the proposed algorithm can adapt to the conditions of the used batteries. It was also possible to prove that the proposed algorithm presents better results regarding the charging time, the temperature increase and the voltage deviation when compared with the traditional multistage approach. After several tests, it was possible to prove that, with the existing BMS, top balancing is more efficient for the adopted profile in balancing current. For correct and safe charging, it is essential to have communication between the charger and the BMS.

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Conflicts of Interest: The authors declare no conflict of interest.

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