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A Self-Tuning Filter-Based Adaptive Linear Neuron Approach for Operation of Three-Level Inverter-Based Shunt Active Power Filters under Non-Ideal Source Voltage Conditions

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Abstract: This paper presents a self-tuning filter (STF)-based adaptive linear neuron (ADALINE) reference current generation algorithm to enhance the operation of a three-phase three-level neutral-point diode clamped (NPC) inverter-based shunt active power filter (SAPF) under non-ideal (unbalanced and/or distorted) source voltage conditions. SAPF is an effective and versatile mitigation tool for current harmonics. As for its controller, ADALINE-based reference current generation algorithm have widely been applied and proven to work effectively under balanced and purely sinusoidal source voltage conditions. However, no work has been conducted to study its performance under non-ideal source voltage conditions. In this work, a STF-based fundamental voltage extraction algorithm is integrated with an ADALINE algorithm, serving as synchronizer algorithm to ensure in-phase operation of the generated reference current with the non-ideal source voltage. Hence, it completely eliminates any dependency on conventional synchronizer algorithms such as phase-locked loop (PLL) and zero-crossing detector (ZCD). Additionally, the proposed STF-based ADALINE algorithm implements the modified Widrow-Hoff (W-H) weight updating algorithm for fast generation of reference current. Both simulation and experimental works are performed to verify design concept and effectiveness of the proposed algorithm. Comparative study with another recently reported algorithm is performed to investigate the performance improvement achieved by SAPF while using the proposed algorithm.

Keywords: artificial neural network (ANN); current harmonics; multilevel inverter; non-sinusoidal supply voltage; reactive power compensation; total harmonic distortion (THD)

1. Introduction

In power distribution system, harmonic currents generated by extensive usage of nonlinear loads are a major power quality problem which has attracted tremendous research interests. Harmonic currents are the main culprits to power factor (PF) degradation and they potentially cause other severe problems which include malfunction of sensitive devices, overheating of equipment, errors in measuring instruments and capacitor overloading [1,2]. Hence, for efficient operation of power system, minimization of harmonic contents in power system has been made compulsory.

For that purpose, various harmonic mitigation tools which include traditional passive filters, active power filters and hybrid power filters have been implemented [3,4]. Nevertheless, among the existing mitigation tools, the shunt-typed active power filter (SAPF) [3–5] is the most effective against current harmonics problems. Besides, it can also perform PF correction [6–9] by means of reactive

power compensation, while mitigating the harmonic currents. A typical SAPF works by first analyzing the severity of harmonic distortion in an operating power system and then injects a suitable amount of harmonic compensation current (injection current) in opposite direction back to the harmonic-polluted power system. The injected injection current allows the harmonic-polluted source current to regain its sinusoidal characteristic with fundamental frequency and working in-phase with the operating power system.

Most SAPFs apply a standard two-level voltage source inverter (VSI) [10–12] in their circuit configurations. However, three-level inverters which are famous for their unique ability in producing output waveforms with lower harmonic distortion [13–15], are recognized as better alternative. For a three-level neutral-point diode clamped (NPC) inverter, it is important to equally maintain the voltage across its splitting DC-link capacitors at half of its overall DC-link voltage [1,15,16]. This is due to the fact that a balanced injection current can effectively be generated only when the voltage across each of its splitting DC-link capacitor is balanced. Besides, if the voltages are unbalanced, the switching devices may fail to work due to over-stresses, and it may even cause unnecessary increment to the total harmonic distortion (THD) [2].

In a typical SAPF control system, the reference current generation algorithm is the first algorithm to operate and it is mainly responsible for providing the SAPF with a reference current, so that an appropriate injection current can be generated by the SAPF. By providing an accurate reference current, the SAPF should be able to mitigate harmonics optimally [17,18]. As a result, for the purpose of generating the reference current, various methods have been applied in previous research works, which include instantaneous power (pq) theory [1,19,20], synchronous reference frame (SRF) [17,21,22], fast Fourier transform (FFT) [23], synchronous detection (SD) [24], dq-axis with Fourier (dqF) [25], wavelet-based approach [26] and artificial neural network (ANN) [18,27,28]. Among the aforementioned methods, ANN-based reference current generation algorithms possesses the best features in providing quick and accurate estimation of reference current. They are well-known for their unique self-adapting, parallel computing and fault tolerance features [29,30]. Specifically, they perform by accurately estimates time-varying current components (needed for generating reference current), complete with magnitude and phase angle [31].

In the context of reference current generation algorithm, ANN-based approaches are available in several distinct architectures: adaptive linear neuron (ADALINE), back propagation network (BPN), radial basis function (RBF) and multilayer perceptron (MLP) [32,33]. Nevertheless, the ADALINE-based approach is the most preferred for generating reference currents due to its advantageous features such as simple structure and low computational burden [30]. In operation, an ADALINE-based approach is controlled by using suitable weight updating algorithm, especially the Widrow-Hoff (W-H) algorithm, which is exceptionally simple and fast in minimizing the average square errors between the actual and estimated signals [27]. However, the traditional W-H algorithm needs to learn the characteristic of multiple harmonic components which greatly increases the required iteration and learning time [27,34]. To further improve the performance of ADALINE-based reference current generation algorithms, a modified W-H weight updating algorithm is proposed to learn the characteristics of a single fundamental component instead of multiple harmonic components, by applying a suitable learning rate [27,34,35]. As a result, the modified W-H algorithm only needs to update two fundamental component weights which greatly enhances its iteration and estimation speeds.

Under balanced-sinusoidal source voltage conditions, the modified W-H ADALINE-based algorithm has widely been applied in SAPF applications and it is proven (both by simulation and experimentally) to be effective in generating reference currents. However, the algorithm requires an additional implementation of a synchronizer algorithm such as phase-locked loop (PLL) [34] and zero-crossing detector [27] for coordinating the phase of the generated reference current so that it works in-phase with the phase of the operating power system. The need for additional PLL and ZCD circuits greatly complicates the structure of ADALINE-based algorithm and it may further complicate

the overall design process. Further improvement has been performed on this particular algorithm to reduce its complexity: by replacing the conventional synchronizer algorithms (PLL and ZCD) with an ADALINE-based fundamental voltage extraction algorithm. The proposed algorithm is known as unified ADALINE-based fundamental component extraction algorithm [30,31]. The algorithm is designed for dual functionality. The first function is to generate a reference current and the second function is to coordinate the phase of the generated reference current. Hence, in the unified ADALINE algorithm, two similar modified W-H ADALINE-based algorithms are applied: the first one is for extracting the fundamental current component (reference current generation) and the second one is for extracting the fundamental voltage component (phase coordination). Since both processes apply similar modified W-H ADALINE-based algorithms, no additional design effort is needed.

However, in practical conditions, the main source voltages are most likely to be non-ideal (unbalanced and/or distorted), and this will potentially degrade the effectiveness of a SAPF which is normally designed to work under ideal (balanced and purely sinusoidal) source voltage conditions. In this case, the conventional PLL and ZCD may perform poorly and are particularly prone to errors, depending on the degree of distortion in the source voltages [5]. Meanwhile, in the unified ADALINE algorithm, the synchronizing phase is actually obtained by dividing the sinusoidal source voltage with its magnitude (unity representation of the source voltage). Hence, when the source voltage is unbalanced and/or distorted, the unified ADALINE algorithm will most likely fail to function appropriately. Therefore, the design of reference current generation algorithm must take into account various non-ideal conditions of the source voltages, to further enhance effectiveness and flexibility of SAPF in current harmonics mitigation. However, no further studies have been conducted to investigate the performance of modified W-H ADALINE-based algorithm under non-ideal source voltage conditions.

Presently, in order to cope with unbalanced and distorted source voltage conditions, there are actually three available techniques, namely optimization algorithms [36,37], adaptive notch filters (ANFs) [38] and self-tuning filters (STFs) [5,39,40]. Optimization algorithms are least preferred as complex iterative approaches are commonly required to solve the formulated optimization problem. Meanwhile, ANF is also not appropriate as it requires careful tuning of the damping ratio and adaptation gain in order to work appropriately. Besides, both the optimization algorithm and ANF are restricted to simulation studies only.

The better alternative is by using STF. Presently, for reference current generation algorithm, STF is only found to be adapted in pq theory [39,41] and SRF [42] algorithms. By incorporating the advantages of STF, both pq theory and SRF algorithms which are initially designed to work with balanced-sinusoidal source voltage, gain the ability to operate effectively under unbalanced and distorted source voltage conditions. The STF is only dedicated for extracting fundamental component directly from the non-ideal source voltage in α - β domain [39]. Once the fundamental component is extracted, further derivation processes are still needed to transform the extracted fundamental component into an effective synchronization signal. Since the application of STF is still restricted to pq theory and SRF algorithms, hence, it would be interesting to apply STF in other types of reference current generation algorithms. Besides, further study is still needed to confirm suitability and adaptability of STF with other control algorithms.

Therefore, this paper presents a STF-based ADALINE algorithm for better operation of SAPFs under unbalanced and distorted source voltage conditions. In the proposed algorithm, a simple yet effective STF-based fundamental voltage extraction algorithm is implemented, serving as a synchronizer algorithm to ensure in-phase operation of the generated reference current with the source voltage. By using the STF-based fundamental voltage extraction algorithm, the dependency on conventional synchronizer algorithms is eliminated and at the same time, the SAPF gains the ability to work effectively under unbalanced and distorted source voltage conditions. The design concept and effectiveness of the proposed STF-based ADALINE algorithm are verified using MATLAB-Simulink (R2012a, MathWorks, Natick, MA, USA). A comparative study with the recent ADALINE approach

(unified ADALINE algorithm [30,31]) is also performed to investigate performance improvement achieved by SAPF while using the proposed algorithm. Various source voltage conditions (balanced, unbalanced and distorted) are created to test performance of each algorithm. Additional experimental study is also conducted to further validate effectiveness and feasibility of the proposed algorithm.

The remainder of the paper is organized as follows: in Section 2, the working principle and control algorithms of the proposed SAPF are described. Next, Section 3 describes the features of the proposed reference current generation algorithm, and highlights the modifications and improvements performed. In Sections 4 and 5, the important findings of this work are presented and thoroughly discussed. Finally, Section 6 concludes and highlights the significant contributions of this work.

2. Working Principle and Control Algorithms of Shunt Active Power Filter (SAPF)

The block diagram in Figure 1 shows the circuit configuration of SAPF and the control algorithms applied to manage its mitigation operation. A three-level NPC inverter which operates as the SAPF is installed at point of common coupling (PCC) between three-phase source and nonlinear rectifier load. Its operation is managed by of four main control algorithms which include reference current generation, neutral-point voltage deviation control, DC-link capacitor voltage regulation, and current control algorithms.

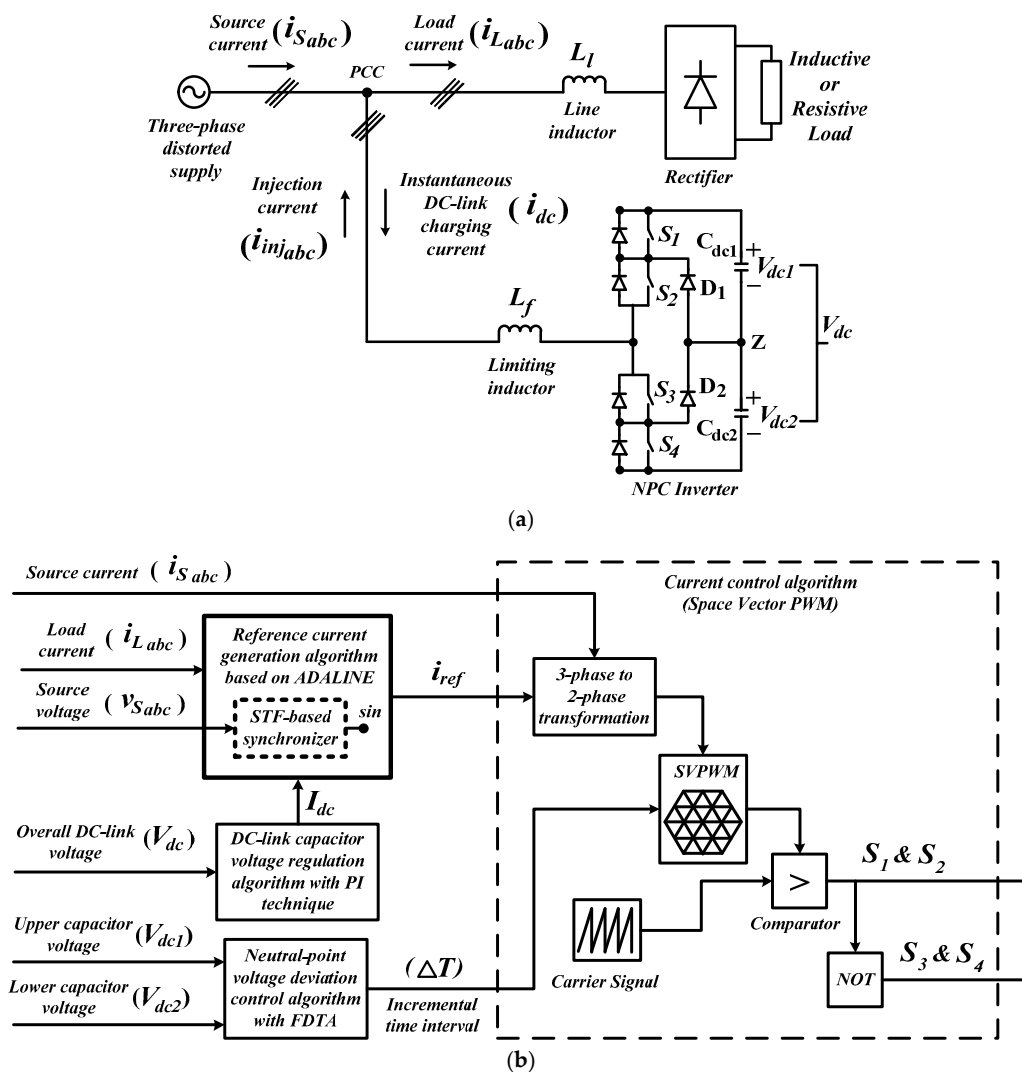


Figure 1. Block diagram of (a) three-level NPC inverter-based SAPF and (b) the applied control algorithms.

Based on Figure 1a, it is clear that the connected SAPF operates by injecting $i_{inj\ abc}$ at PCC. At the same time, it draws the necessary i_{dc} to maintain V_{dc} at constant level. According to Kirchhoff's current law (KCL), the overall current relationship of Figure 1a can be expressed as:

$$i_{S\ abc} = i_{L\ abc} - i_{inj\ abc} + i_{dc} \quad (1)$$

Under the presence of nonlinear loads, $i_{L\ abc}$ can actually be decomposed into two components: fundamental component $i_{1L\ abc}$ and harmonic component $i_{H\ abc}$. Note that, the presence of $i_{H\ abc}$ in the power system is the prime cause of distortion in the source current $i_{S\ abc}$ and it also causes $i_{S\ abc}$ to displace away from source voltage $v_{S\ abc}$. Hence Equation (1) can be rewritten as:

$$i_{S\ abc} = [i_{1L\ abc} + i_{H\ abc}] - i_{inj\ abc} + i_{dc} \quad (2)$$

In order to effectively recover the sinusoidal shape of $i_{S\ abc}$, $i_{H\ abc}$ must be removed from the power system. This can simply be achieved by making $i_{inj\ abc}$ equal to $i_{H\ abc}$. Eventually, the $i_{S\ abc}$ will regain its sinusoidal characteristic and working in-phase with $v_{S\ abc}$. Hence, Equation (2) is now expressed as:

$$i_{S\ abc} = i_{1L\ abc} + i_{dc} \quad (3)$$

As highlighted in Figure 1b, the algorithm to be discussed in this paper is the reference current generation algorithm. Meanwhile, for neutral-point voltage deviation control algorithm, fuzzy-based dwell time allocation (FDTA) [43] technique is applied. Basically, the FDTA technique continuously delivers the required incremental time interval ΔT signal to adjust the switching duration of each switching device according to the instantaneous voltage error ($V_{dc1} - V_{dc2}$) between the two splitting DC-link capacitors. This ensures equal inflow and outflow of current at neutral-point Z (refer to Figure 1a), and thus achieving voltage balancing of DC-link capacitors. Next, for effective regulation of overall DC-link capacitor voltage, proportional-integral (PI) technique [44] is applied. It delivers the required magnitude I_{dc} of instantaneous DC-link charging current i_{dc} so that the similar amount of charging current can be drawn by the SAPF to regulate its switching losses. Finally, to manage switching operation of the SAPF, a 25 kHz three-level space vector PWM (SVPWM) current control algorithm [45–47] is applied. Basically, it generates PWM switching pulses S_{1-4} based on the reference current signal i_{ref} which is delivered by reference current generation algorithm, and ΔT signal.

3. Self-Tuning Filter (STF)-Based Adaptive Linear Neuron (ADALINE) Algorithm

The proposed STF-based ADALINE algorithm is developed by referring to the recent unified ADALINE algorithm, as successfully implemented in [30,31]. Hence, for effective presentation on the working principle of the proposed STF-based ADALINE algorithm, and also for showing proper comparison, significant features of the unified ADALINE algorithm are first described. Next, by referring to the unified ADALINE algorithm, the STF-based ADALINE algorithm is elaborated, highlighting the improvements made.

3.1. Unified ADALINE Algorithm

The working principle of the unified ADALINE algorithm is shown in Figure 2. Basically, the algorithm consists of two similar fundamental component extraction algorithms: ADALINE-based fundamental current extraction and ADALINE-based fundamental voltage extraction algorithms. The current extraction algorithm is applied to extract amplitude $I_{Lfund_mag}(k)$ of the measured load current $i_L(k)$ and meanwhile the voltage extraction is applied to extract synchronization phase $\sin(k\omega\Delta t + \theta)$ from the measured source voltage $v_S(k)$.

Hence, as an overall, the unified ADALINE algorithm performs according to three consecutive processes. First, the required fundamental component of load current $i_{Lfund_est}(k)$ and source voltage $v_{Sfund_est}(k)$ signal are estimated. Second, amplitudes of the estimated fundamental components are

computed. Third, the required reference current $i_{ref}(k)$ is derived by using the computed amplitudes ($I_{Lfund_mag}(k)$ and $V_{Sfund_mag}(k)$) and I_{dc} .

According to Fourier series theory, any periodic signal can be expressed as a summation of sine and cosine components, with each component having a suitable coefficient. Hence, the harmonic-polluted load current can be expressed as:

$$i_L(k) = \sum_{n=1,2,3,\dots}^N [W_{nsin_c} \sin(nk\omega\Delta t) + W_{ncos_c} \cos(nk\omega\Delta t)] \quad (4)$$

where W_{nsin_c} and W_{ncos_c} represent the amplitudes (weights) of sine and cosine components of the fundamental load current respectively, k is the k th sample, Δt is the sampling time, ω is the fundamental frequency, and n is the order of harmonics to maximum N order.

For fundamental current extraction ($n = 1$), Equation (4) can be rewritten as:

$$i_{Lfund}(k) = W_{1sin_c} \sin(k\omega\Delta t) + W_{1cos_c} \cos(k\omega\Delta t) \quad (5)$$

and thus the amplitude $I_{Lfund_mag}(k)$ of $i_{Lfund}(k)$ can be calculated as:

$$I_{Lfund_mag}(k) = \sqrt{W_{1sin_c}^2 + W_{1cos_c}^2} \quad (6)$$

The algorithm employs the modified W-H weight updating approach. Basically, the W-H weight updating algorithm performs by continuously update the two weight $W(k)$ factors of the fundamental load component. In each iteration, the error $e(k)$ between the estimated $i_{Lfund_est}(k)$ and the actual measured $i_L(k)$ signals is first computed, and is then used to update the weights for the subsequent iterations $W(k+1)$. Concurrently, the updating process minimizes the error $e(k)$. After a few iterations, the estimated $i_{Lfund_est}(k)$ will adapt itself to the measured $i_L(k)$. However, updating only two weight elements leads to large error $e(k)$ between the estimated $i_{Lfund_est}(k)$ and actual measured $i_L(k)$. Hence, a suitable learning rate γ is applied to solve this issue. This approach greatly simplifies complexity of the designed algorithm. At the same time, it enhances iteration speed and provides fast and accurate estimation of the required fundamental load current $i_{Lfund_est}(k)$. As an overall, the complete weight updating process can be summarized as:

$$W(k+1) = W(k) + \frac{\gamma e(k) Y(k)}{Y(k)^T Y(k)} \quad (7)$$

where $W = \begin{bmatrix} W_{1sin_c} \\ W_{1cos_c} \end{bmatrix}$ represents the weight factor, $Y = \begin{bmatrix} \sin(k\omega\Delta t) \\ \cos(k\omega\Delta t) \end{bmatrix}$ represents the fundamental sine and cosine components and $e(k) = i_L(k) - i_{Lfund_est}(k)$ is the error between the measured and estimated signal.

Based on [30], the γ value should be set according to the following requirement:

$$0 < \gamma < 1 \quad (8)$$

and the best γ value reported for fundamental current extraction is 0.0006.

On the other hand, for fundamental voltage extraction, Equation (5) can be rewritten in term of source voltage expression which is given as

$$v_{Sfund}(k) = W_{1sin_v} \sin(k\omega\Delta t) + W_{1cos_v} \cos(k\omega\Delta t) \quad (9)$$

where W_{1sin_v} and W_{1cos_v} represent the amplitudes (weights) of sine and cosine components of the fundamental source voltage respectively. Hence, the required amplitude $V_{Sfund_mag}(k)$ of $v_{Sfund}(k)$ can be calculated as:

$$V_{Sfund_mag}(k) = \sqrt{W_{1sin_v}^2 + W_{1cos_v}^2} \quad (10)$$

Similarly, the modified W-H weight updating approach as shown in Equation (7) is applied to compute the required weights of the fundamental source voltage. Meanwhile, according to [30], the best γ value reported for fundamental voltage extraction is 0.01.

As mentioned above, the voltage extraction algorithm is applied to extract synchronization phase $\sin(k\omega\Delta t + \theta)$ from $v_S(k)$. Hence, with the availability of $V_{Sfund_mag}(k)$, $\sin(k\omega\Delta t + \theta)$ is obtained according to:

$$\sin(k\omega\Delta t + \theta) = \frac{v_S(k)}{V_{Sfund_mag}(k)} \quad (11)$$

Since $\sin(k\omega\Delta t + \theta)$ is obtained by processing the source voltage directly, hence the synchronization phase obtained by using Equation (11) will be in accordance with the phase of the operating system. In this manner, dependencies on conventional synchronization algorithm such as PLL and ZCD can be neglected. Once $\sin(k\omega\Delta t + \theta)$ is available, together with $I_{Lfund_mag}(k)$ and I_{dc} (from DC-link capacitor voltage regulation algorithm), the desired reference current is generated according to:

$$i_{ref}(k) = (I_{Lfund_mag}(k) + I_{dc}) \sin(k\omega\Delta t + \theta). \quad (12)$$

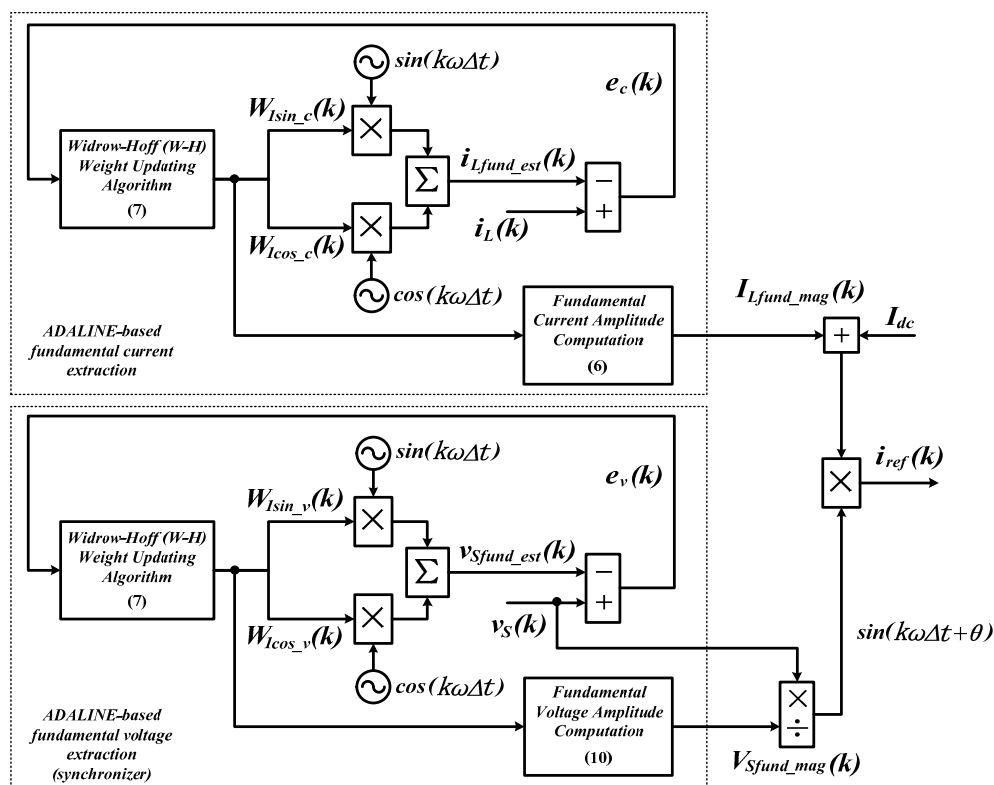


Figure 2. Control structure of unified ADALINE algorithm [30].

3.2. STF-Based Fundamental Voltage Extraction Algorithm (Synchronizer Algorithm)

Despite the fact that the ADALINE-based fundamental voltage extraction algorithm has been reported in [30] to be simple and effective in generating the required synchronization phase under sinusoidal source voltages, the algorithm still possesses shortcomings and weaknesses which significantly limits its flexibility and applications. According to Equation (11), the synchronization phase generated by ADALINE-based fundamental voltage extraction algorithm is actually unity representation of the actual source voltage. Hence, if the actual source voltage is unbalanced and/or

distorted, the synchronization phase will be unbalanced and/or distorted as well. In other words, the applied ADALINE-based fundamental voltage extraction algorithm is incapable of generating an appropriate synchronization phase when the source voltage is non-ideal. This greatly limits flexibility of the unified ADALINE algorithm in reference current generation, as unbalances and distortion in the main supply voltage are unavoidable in real practical system. Hence, a synchronization algorithm which is able to deal with unbalanced and distorted source voltage is compulsory and worth implementing.

The block diagram in Figure 3 shows control structure of the proposed STF-based ADALINE algorithm. Basically, the proposed algorithm works in a similar manner to the unified ADALINE algorithm where it also comprises of two fundamental component (current and voltage) extraction parts. However, as clearly shown in Figures 2 and 3, the proposed algorithm implements a new STF-based fundamental voltage extraction algorithm to overcome the limitations of the conventional ADALINE-based fundamental voltage extraction algorithm. The improvement is performed to ensure effective operation of SAPF under non-ideal source voltage. Specifically, the STF-based fundamental voltage extraction algorithm performs according to three consecutive processes as follows:

- (1) Extract the fundamental (sinusoidal) source voltage $v_{Sfund}(k)$ from the measured source voltage $v_S(k)$,
- (2) Compute the magnitude $V_{Sfund_mag}(k)$ of fundamental source voltage $v_{Sfund}(k)$, and
- (2) Divide $v_{Sfund}(k)$ directly with the computed magnitude $V_{Sfund_mag}(k)$.

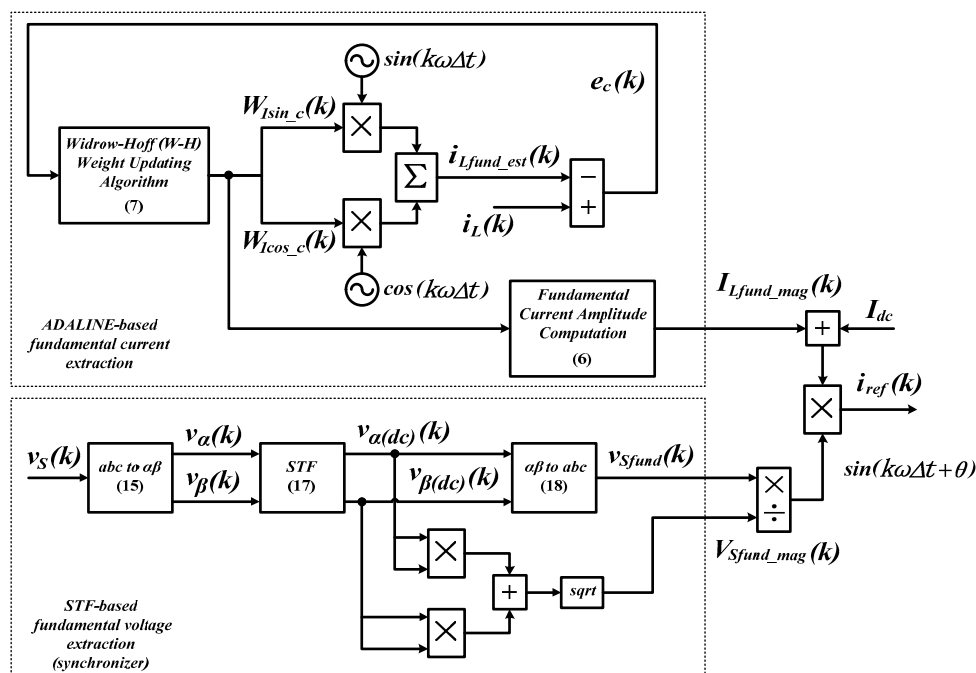


Figure 3. Control structure of the proposed STF-based ADALINE algorithm.

The extraction of $v_{Sfund}(k)$ is conducted in the $\alpha\beta$ domain via Clarke’s transformation where the measured three-phase voltages are first transformed into their respective two-phase $\alpha\beta$ representation by using a transformation matrix $T_{\alpha\beta}$ given as follows:

$$T_{\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta_1(t) & \cos\theta_2(t) & \cos\theta_3(t) \\ \sin\theta_1(t) & \sin\theta_2(t) & \sin\theta_3(t) \end{bmatrix} \quad (13)$$

where:

$$\theta_{ph}(t) = \theta(t) + \frac{2\pi}{3}(ph - 1), \quad ph = 1, 2, 3 \quad (14)$$

and $\theta(t)$ is an angular arbitrary function and is considered as $\theta(t) = 0$.

Hence, by applying $T_{\alpha\beta}$, the source voltage $v_{S\alpha\beta}$ in $\alpha\beta$ domain can be obtained as follows:

$$\begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix}. \quad (15)$$

Under non-ideal source voltage conditions, source voltages which are expressed in $\alpha\beta$ domain can actually be decomposed into fundamental and distorted components as follows:

$$\begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = \begin{bmatrix} v_{S\alpha(dc)} + v_{S\alpha(ac)} \\ v_{S\beta(dc)} + v_{S\beta(ac)} \end{bmatrix} \quad (16)$$

where $v_{S\alpha(dc)}$ and $v_{S\beta(dc)}$ refer to the fundamental (*dc*) components of source voltage in $\alpha\beta$ domain, and meanwhile $v_{S\alpha(ac)}$ and $v_{S\beta(ac)}$ represent the distorted (*ac*) components of source voltage in $\alpha\beta$ domain. The fundamental components of source voltage are the main signals required for generating the synchronization phases.

To accurately extract the fundamental components under non-ideal source voltage conditions, STF technique which is implemented and clearly described in [39], is employed. Generally, the STF performs by processing the source voltage signals in $\alpha\beta$ domain according to the transfer function (after performing Laplace transformation) expressed as follows [5,39,41]:

$$\begin{bmatrix} v_{S\alpha(dc)}(s) \\ v_{S\beta(dc)}(s) \end{bmatrix} = \frac{K}{s} \begin{bmatrix} v_{S\alpha}(s) - v_{S\alpha(dc)}(s) \\ v_{S\beta}(s) - v_{S\beta(dc)}(s) \end{bmatrix} + \frac{2\pi f_c}{s} \begin{bmatrix} -v_{S\beta(dc)}(s) \\ v_{S\alpha(dc)}(s) \end{bmatrix} \quad (17)$$

where K is a constant gain parameter and f_c is the cutoff frequency. It is important to note that the performance of STF is influenced by the selected K values. Nevertheless, for effective operation of STF in extracting dc components of source voltage, K and f_c are commonly set at 100 and 50 Hz, respectively [40,41].

With the extracted fundamental components $v_{S\alpha(dc)}$ and $v_{S\beta(dc)}$, inverse Clarke's transformation as expressed in Equation (18) is applied to transform the extracted fundamental components of source voltage in $\alpha\beta$ domain back into its three-phase representation $v_{Sfund}(k)$:

$$\begin{bmatrix} v_{Sfund\ a} \\ v_{Sfund\ b} \\ v_{Sfund\ c} \end{bmatrix} = T_{\alpha\beta}^T \begin{bmatrix} v_{S\alpha(dc)} \\ v_{S\beta(dc)} \end{bmatrix} \quad (18)$$

At the same time, $v_{S\alpha(dc)}$ and $v_{S\beta(dc)}$ are used to calculate the required amplitude $V_{Sfund_mag}(k)$ of $v_{Sfund}(k)$ according to the following approach:

$$V_{Sfund_mag}(k) = \sqrt{v_{S\alpha(dc)}^2 + v_{S\beta(dc)}^2}. \quad (19)$$

With the availability of $v_{Sfund}(k)$ and $V_{Sfund_mag}(k)$, $\sin(k\omega\Delta t + \theta)$ can be obtained according to the following approach:

$$\sin(k\omega\Delta t + \theta) = \frac{v_{Sfund}(k)}{V_{Sfund_mag}(k)}. \quad (20)$$

By using Equation (20), the synchronization phase can accurately be generated under any type of non-ideal source voltages and thus granting the proposed STF-based ADALINE algorithm the ability to work effectively under non-ideal source voltages.

4. Simulation Results

Simulation model of the proposed SAPF and its control algorithms are developed and tested in MATLAB-Simulink. To evaluate the performance of the proposed STF-based ADALINE algorithm, four cases of source voltage conditions are considered: in case 1, balanced-sinusoidal source voltage, in case 2, balanced-distorted source voltage containing only odd-order harmonics, in case 3, balanced-distorted source voltage containing both odd-order and even-order harmonics, and in case 4, unbalanced-distorted source voltage. The source voltages applied are expressed as follows:

Case 1: Balanced-sinusoidal source voltage:
(THD = 0.00%)

$$v_{Sa} = 326\sin(\omega t) \quad (21)$$

$$v_{Sb} = 326\sin(\omega t - 120^\circ) \quad (22)$$

$$v_{Sc} = 326\sin(\omega t + 120^\circ) \quad (23)$$

Case 2: Balanced-distorted source voltage containing only odd-order harmonics:
(THD = 32.17%)

$$v_{Sa} = 326\sin(\omega t) + 80\sin(3\omega t) + 60\sin(5\omega t) + 30\sin(7\omega t) + 10\sin(9\omega t) \quad (24)$$

$$v_{Sb} = 326\sin(\omega t - 120^\circ) + 80\sin(3(\omega t - 120^\circ)) + 60\sin(5(\omega t - 120^\circ)) + 30\sin(7(\omega t - 120^\circ)) + 10\sin(9(\omega t - 120^\circ)) \quad (25)$$

$$v_{Sc} = 326\sin(\omega t + 120^\circ) + 80\sin(3(\omega t + 120^\circ)) + 60\sin(5(\omega t + 120^\circ)) + 30\sin(7(\omega t + 120^\circ)) + 10\sin(9(\omega t + 120^\circ)) \quad (26)$$

Case 3: Balanced-distorted source voltage containing both odd-order and even-order harmonics:
(THD = 33.17%)

$$v_{Sa} = 326\sin(\omega t) + 8\sin(2\omega t) + 80\sin(3\omega t) + 5\sin(4\omega t) + 60\sin(5\omega t) + 2\sin(6\omega t) + 40\sin(7\omega t) \quad (27)$$

$$v_{Sb} = 326\sin(\omega t - 120^\circ) + 8\sin(2(\omega t - 120^\circ)) + 80\sin(3(\omega t - 120^\circ)) + 5\sin(4(\omega t - 120^\circ)) + 60\sin(5(\omega t - 120^\circ)) + 2\sin(6(\omega t - 120^\circ)) + 40\sin(7(\omega t - 120^\circ)) \quad (28)$$

$$v_{Sc} = 326\sin(\omega t + 120^\circ) + 8\sin(2(\omega t + 120^\circ)) + 80\sin(3(\omega t + 120^\circ)) + 5\sin(4(\omega t + 120^\circ)) + 60\sin(5(\omega t + 120^\circ)) + 2\sin(6(\omega t + 120^\circ)) + 40\sin(7(\omega t + 120^\circ)) \quad (29)$$

Case 4: Unbalanced-distorted source voltage:
(THD_a = 14.71%, THD_b = 17.48% and THD_c = 26.66%)

$$v_{Sa} = 326\sin(\omega t) + 30\sin(3\omega t - 120^\circ) + 20\sin(5\omega t + 120^\circ) + 30\sin(7\omega t) + 10\sin(9\omega t - 120^\circ) \quad (30)$$

$$v_{Sb} = 286\sin(\omega t - 120^\circ) + 40\sin(3\omega t) + 20\sin(5\omega t + 120^\circ) + 20\sin(7\omega t - 120^\circ) + 10\sin(9\omega t + 120^\circ) \quad (31)$$

$$v_{Sc} = 246\sin(\omega t + 120^\circ) + 50\sin(3\omega t) + 40\sin(5\omega t) + 10\sin(7\omega t - 120^\circ) + 10\sin(9\omega t + 120^\circ) \quad (32)$$

Two types of nonlinear rectifier loads are constructed for the simulation study: the first type composes of a three-phase uncontrolled bridge rectifier with 50 Ω resistor and 50 mH inductor

connected in series (inductive), and meanwhile the second type composes of similar rectifier with a series connected 25Ω resistor (resistive). Table 1 highlights the parameter specifications of the proposed SAPF. The proposed algorithm is evaluated in term of current harmonics mitigation performance (THD value) demonstrated by SAPF. Moreover, the performance demonstrated by the SAPF while using the proposed algorithm is compared with the existing unified ADALINE algorithm, to investigate the improvements achieved.

Table 1. Parameter specifications for the proposed SAPF.

Parameter	Value	Unit
Fundamental source voltage (line to line)	400 (rms)	V
Fundamental frequency	50	Hz
DC-link capacitor	3300 (each)	μF
Overall DC-link reference voltage	880	V
Limiting inductor	5	mH
Switching frequency	25	kHz

4.1. Balanced-Sinusoidal Source Voltage (Case 1)

Under case 1 source voltage conditions, the simulation waveforms of SAPF which include three-phase source voltage v_S , load current i_L , injection current i_{inj} , and source current i_S , obtained for inductive and resistive loads are shown in Figures 4 and 5 respectively. Meanwhile, the THD values of source current i_S recorded before and after connecting SAPF are tabulated in Table 2.

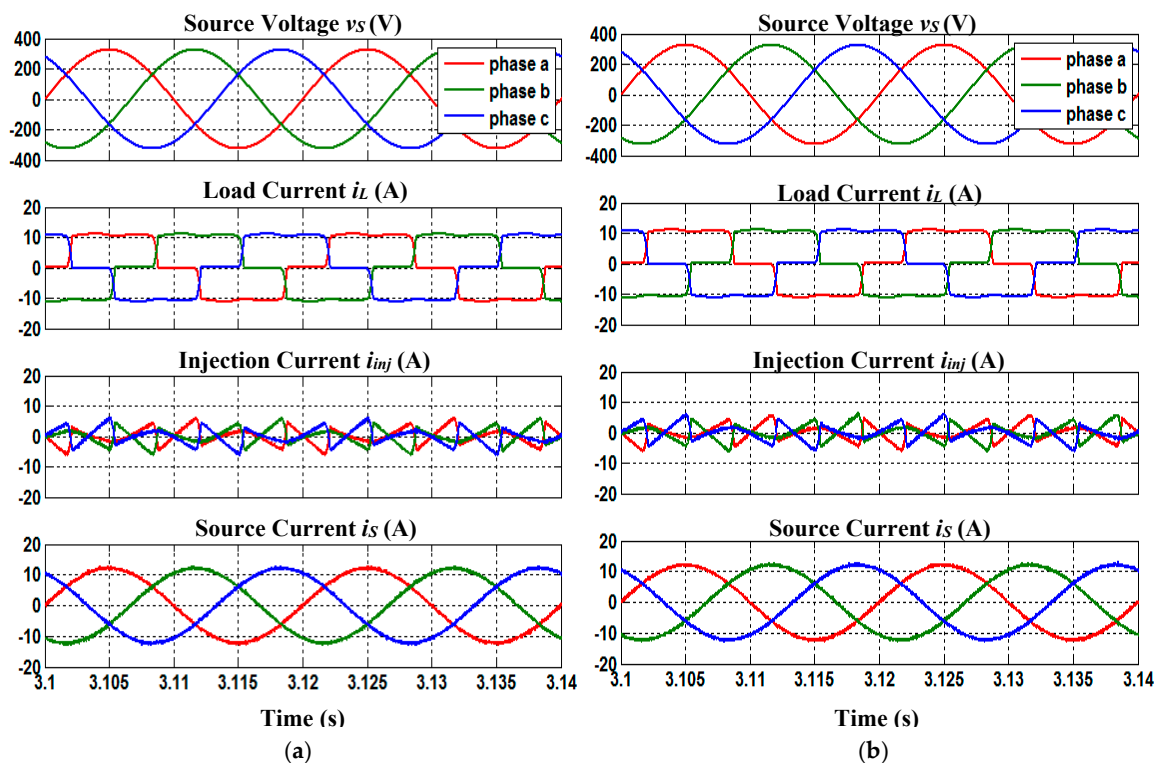


Figure 4. Simulation waveforms of SAPF under case 1 condition which include three-phase source voltage v_S , load current i_L , injection current i_{inj} and source current i_S , for inductive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

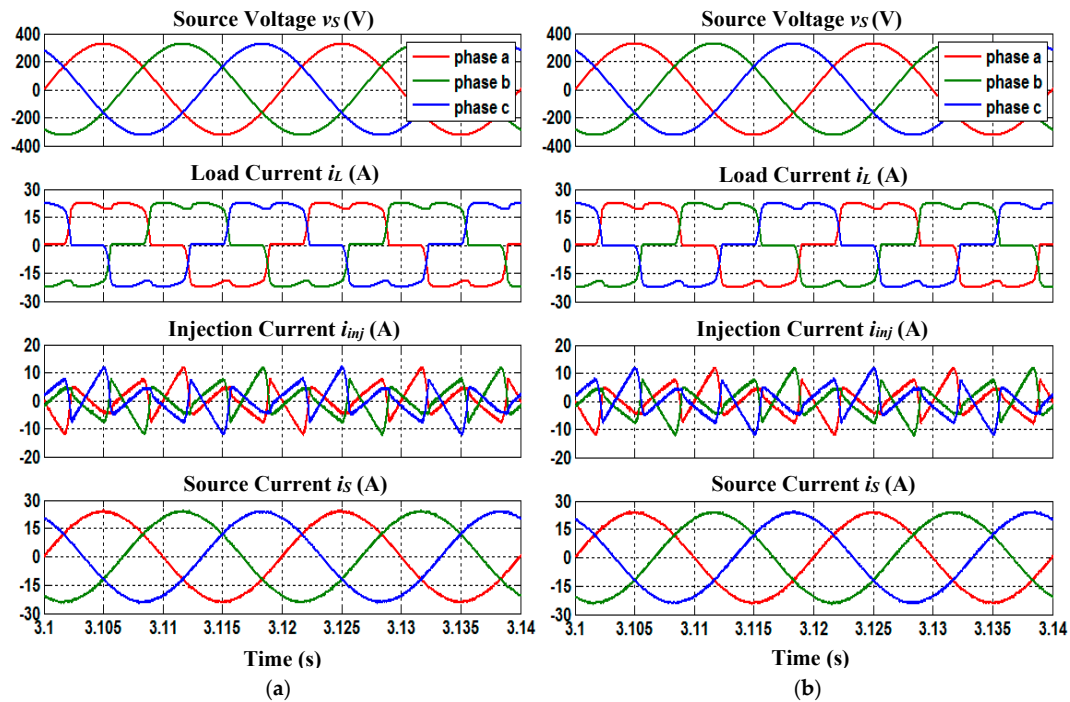


Figure 5. Simulation waveforms of SAPF under case 1 condition which include three-phase source voltage v_s , load current i_L , injection current i_{inj} and source current i_s , for resistive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

Table 2. THD values of source current i_s before and after connecting SAPF, obtained under case 1 condition (Simulation Result).

Reference Current Generation Algorithm	Total Harmonic Distortion, THD (%)					
	Phase a		Phase b		Phase c	
	Inductive	Resistive	Inductive	Resistive	Inductive	Resistive
Before Connecting SAPF						
N/A	27.34	27.01	27.34	27.01	27.34	27.01
After Connecting SAPF						
STF-based ADALINE	2.60	1.29	2.57	1.28	2.57	1.31
Unified ADALINE	3.28	1.38	3.34	1.39	3.26	1.42

Based on Table 2, it can be observed that under balanced-sinusoidal source voltage condition, both reference current generation algorithms are able to provide effective mitigation of harmonic currents for both nonlinear loads, where the recorded THD values are below 5%, complying with the limit set by IEEE Standard 519-2014 [48]. However, the THD values resulting from the STF-based ADALINE algorithm are 0.09–0.77% lower than with the unified ADALINE algorithm, thereby showing superiority of the proposed algorithm over the existing algorithm under balanced-sinusoidal source voltage condition.

Moreover, it is also important to note that for both nonlinear loads, the mitigated source current i_s resulting from both reference current generation algorithms is working in phase with the source voltage v_s . In other words, both reference current generation algorithms are able to improve the power factor to almost unity. Specifically, taking phase a as example, the PF recorded before connecting SAPF is 0.95 (both inductive and resistive loads) and both reference current generation algorithms have corrected the PF to 0.99 (both inductive and resistive loads).

Other than that, the behavior of all DC-link voltages throughout mitigation operation of SAPF is also studied to verify correct operation of SAPF. Based on Figure 6, under balanced-sinusoidal

source voltage condition, it is obvious that all DC-link capacitor voltages of the SAPF are properly regulated and maintained at their respective desired value. Besides, voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) of the SAPF are observed to have equally maintained at half of its overall DC-link voltage V_{dc} . Concurrently, the voltage deviation at neutral-point of the SAPF has also been minimized. Therefore, it can be confirmed from the findings that the operation of SAPF is correct and valid. The findings obtained also confirm the effectiveness of DC-link capacitor voltage regulation algorithm with PI technique and neutral-point voltage deviation control algorithm with FDTA technique applied in the proposed SAPF.

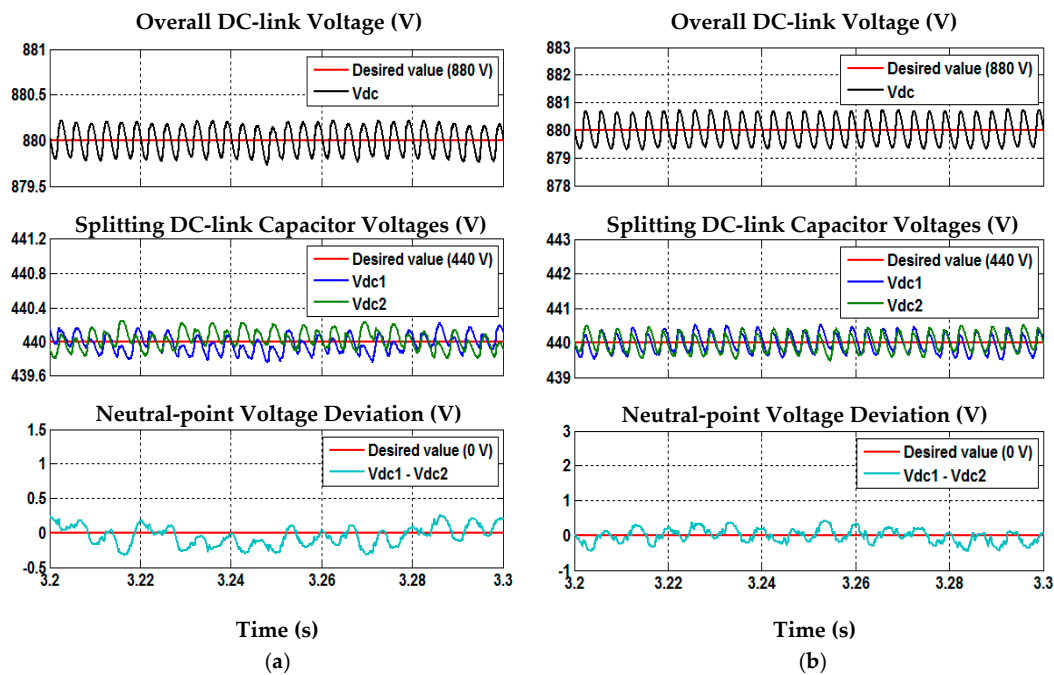


Figure 6. Simulation waveforms of SAPF while using STF-based ADALINE algorithm under case 1 condition which include overall DC-link voltage V_{dc} , splitting DC-link capacitor voltages V_{dc1} and V_{dc2} , and neutral-point voltage deviation Vd ($V_{dc1} - V_{dc2}$), for (a) inductive and (b) resistive loads.

4.2. Balanced-Distorted Source Voltage Containing Only Odd-Order Harmonics (Case 2)

Under case 2 source voltage condition, the simulation waveforms of SAPF which include three-phase source voltage v_s , load current i_L , injection current i_{inj} , and source current i_s , obtained for inductive and resistive loads are shown in Figures 7 and 8 respectively. Meanwhile, performance comparison in term of the resulting THD values of source current i_s , between STF-based ADALINE and unified ADALINE algorithms is summarized in Table 3.

Table 3. THD values of source current i_s before and after connecting SAPF, obtained under case 2 condition (Simulation Result).

Reference Current Generation Algorithm	Total Harmonic Distortion, THD (%)					
	Phase a		Phase b		Phase c	
	Inductive	Resistive	Inductive	Resistive	Inductive	Resistive
Before Connecting SAPF						
N/A	33.54	25.56	33.54	25.56	33.54	25.56
After Connecting SAPF						
STF-based ADALINE	3.19	2.00	3.19	1.96	3.21	1.97
Unified ADALINE	21.12	20.71	21.73	21.18	20.89	20.48

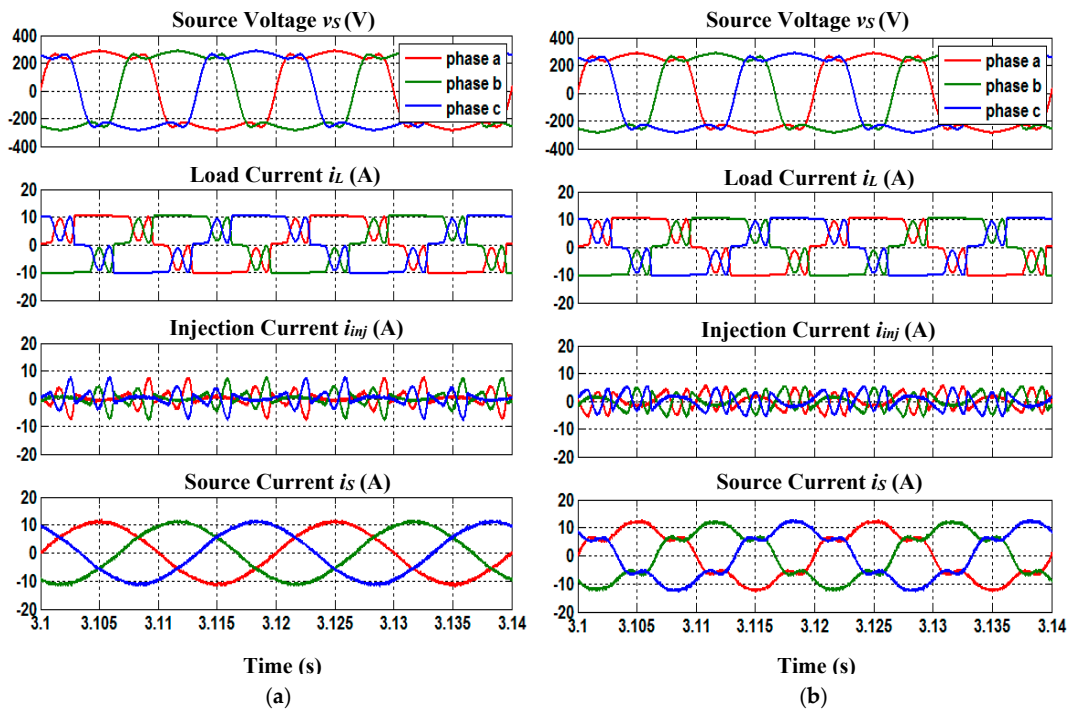


Figure 7. Simulation waveforms of SAPF under case 2 condition which include three-phase source voltage v_s , load current i_L , injection current i_{inj} and source current i_s , for inductive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

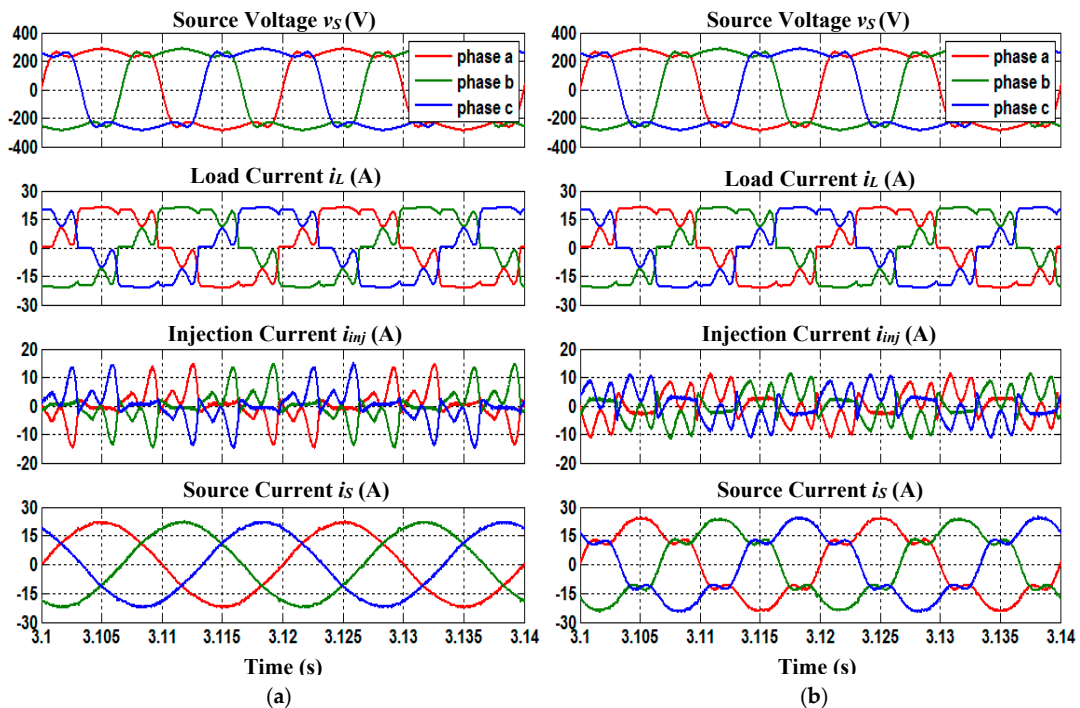


Figure 8. Simulation waveforms of SAPF under case 2 condition which include three-phase source voltage v_s , load current i_L , injection current i_{inj} and source current i_s , for resistive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

Based on Table 3, it can be observed that SAPF utilizing the STF-based ADALINE algorithm effectively maintains the THD values of source current i_s below the allowable THD limit of 5%.

For instance, SAPF utilizing the STF-based ADALINE algorithm is observed to have effectively reduced the high THD values of source current i_S (phase a) from 33.54% (inductive) and 25.56% (resistive) to 3.19% and 2.00% respectively. In contrast, SAPF utilizing the unified ADALINE algorithm fails to comply with the 5% THD limit as high THD values (phase a) of 21.12% (inductive) and 20.71% (resistive) are recorded.

In addition, for both nonlinear loads, the mitigated source current i_S resulting from both reference current generation algorithms is observed to be working in phase with the source voltage. However, due to superior effectiveness of the STF-based ADALINE algorithm in minimizing the THD values of source current i_S , PFs recorded for both nonlinear loads by using STF-based ADALINE algorithm are better (closer to unity) as compared to the one obtained by using unified ADALINE algorithm. Specifically, by referring to phase a, the PFs recorded before connecting SAPF are 0.94 (inductive) and 0.93 (resistive), and they have been corrected to 0.99 (both inductive and resistive loads) by SAPF utilizing STF-based ADALINE algorithm, and 0.97 (both inductive and resistive loads) by SAPF utilizing unified ADALINE algorithm.

Similarly, under case 2 source voltage condition, the behavior of all DC-link voltages throughout mitigation operation of SAPF is also studied to verify correct operation of SAPF. Based on Figure 9, under harmonic-distorted (only odd-order harmonics) source voltage condition, it is obvious that all DC-link capacitor voltages of the SAPF are properly regulated and maintained at their respective desired value. Besides, voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) of the SAPF are observed to have equally maintained at half of its overall DC-link voltage V_{dc} . At the same time, the voltage deviation at neutral-point of the SAPF has also been minimized. Therefore, once again it can be confirmed from the findings that the operation of SAPF is correct and valid. The findings obtained also confirm the effectiveness of DC-link capacitor voltage regulation algorithm with PI technique and neutral-point voltage deviation control algorithm with FDTA technique applied in the proposed SAPF.

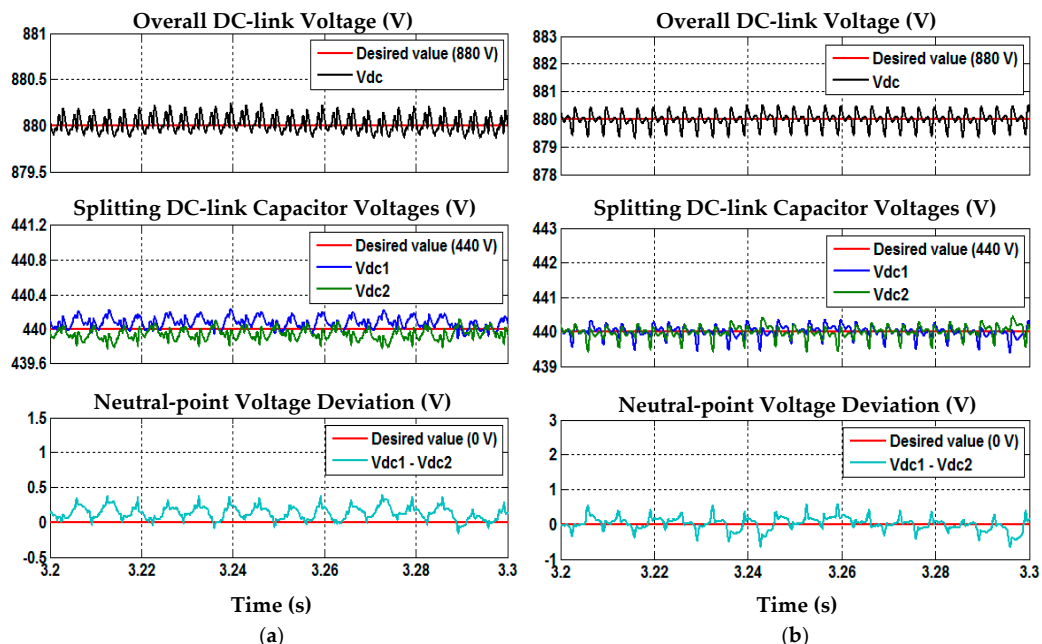


Figure 9. Simulation waveforms of SAPF while using STF-based ADALINE algorithm under case 2 condition which include overall DC-link voltage V_{dc} , splitting DC-link capacitor voltages V_{dc1} and V_{dc2} , and neutral-point voltage deviation Vd ($V_{dc1} - V_{dc2}$), for (a) inductive and (b) resistive loads.

4.3. Balanced-Distorted Source Voltage Containing Both Odd-Order and Even-Order Harmonics (Case 3)

Under case 3 source voltage condition, the simulation waveforms of SAPF which include three-phase source voltage v_S , load current i_L , injection current i_{inj} , and source current i_S , obtained for

inductive and resistive loads are shown in Figures 10 and 11 respectively. Meanwhile, performance comparison in term of the resulting THD values of source current i_s , between STF-based ADALINE and unified ADALINE algorithms is summarized in Table 4.

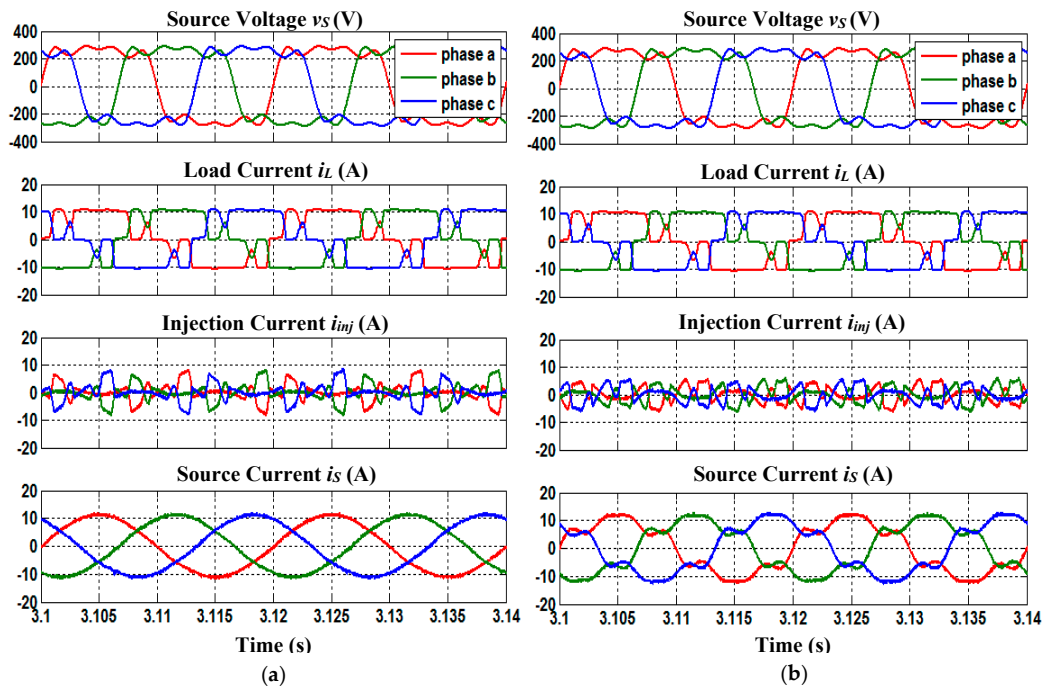


Figure 10. Simulation waveforms of SAPF under case 3 condition which include three-phase source voltage v_s , load current i_L , injection current i_{inj} and source current i_s , for inductive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

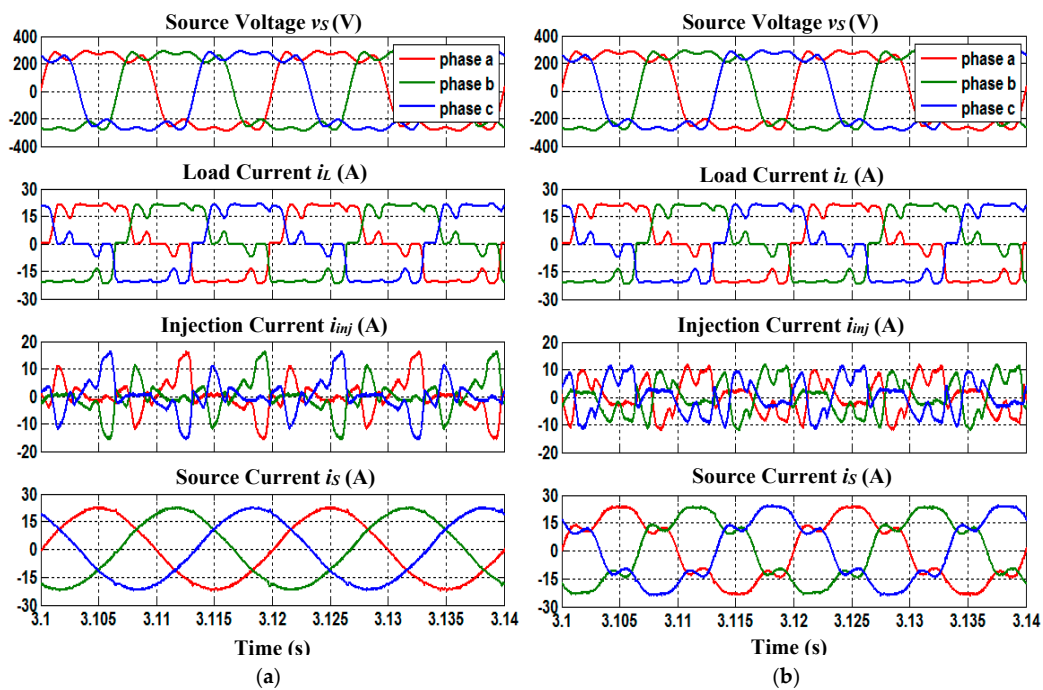


Figure 11. Simulation waveforms of SAPF under case 3 condition which include three-phase source voltage v_s , load current i_L , injection current i_{inj} and source current i_s , for resistive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

Based on Table 4, SAPF utilizing the STF-based ADALINE algorithm is also found to perform effectively in maintaining the THD values of the source current i_s below the allowable THD limit of 5%. Specifically, the high THD values of source current i_s (phase a) have been reduced from 39.86% (inductive) and 37.70% (resistive) to 3.95% and 3.10%, respectively, by using STF-based ADALINE algorithm. On the other hand, SAPF utilizing the unified ADALINE algorithm fails to comply with the 5% THD limit where high THD values (phase a) of 22.59% (inductive) and 22.36% (resistive) are recorded.

Table 4. THD values of source current i_s before and after connecting SAPF, obtained under case 3 condition (Simulation Result).

Reference Current Generation Algorithm	Total Harmonic Distortion, THD (%)					
	Phase a		Phase b		Phase c	
	Inductive	Resistive	Inductive	Resistive	Inductive	Resistive
Before Connecting SAPF						
N/A	39.86	37.70	39.86	37.70	39.86	37.70
After Connecting SAPF						
STF-based ADALINE	3.95	3.10	3.89	3.13	3.94	3.06
Unified ADALINE	22.59	22.36	23.01	22.86	22.27	22.05

In addition, it can also be observed that for both nonlinear loads, the mitigated source current i_s resulting from both reference current generation algorithms is working in phase with the source voltage. Nevertheless, owing to superior effectiveness of the STF-based ADALINE algorithm in providing minimum THD values of source current i_s , it outperforms the ability unified ADALINE algorithm in improving PF performances. Specifically, taking phase a as example, the PF recorded before connecting SAPF is 0.92 (both inductive and resistive loads) and it has been corrected to 0.99 (both inductive and resistive loads) by SAPF utilizing STF-based ADALINE algorithm, and 0.97 (both inductive and resistive loads) by SAPF utilizing unified ADALINE algorithm.

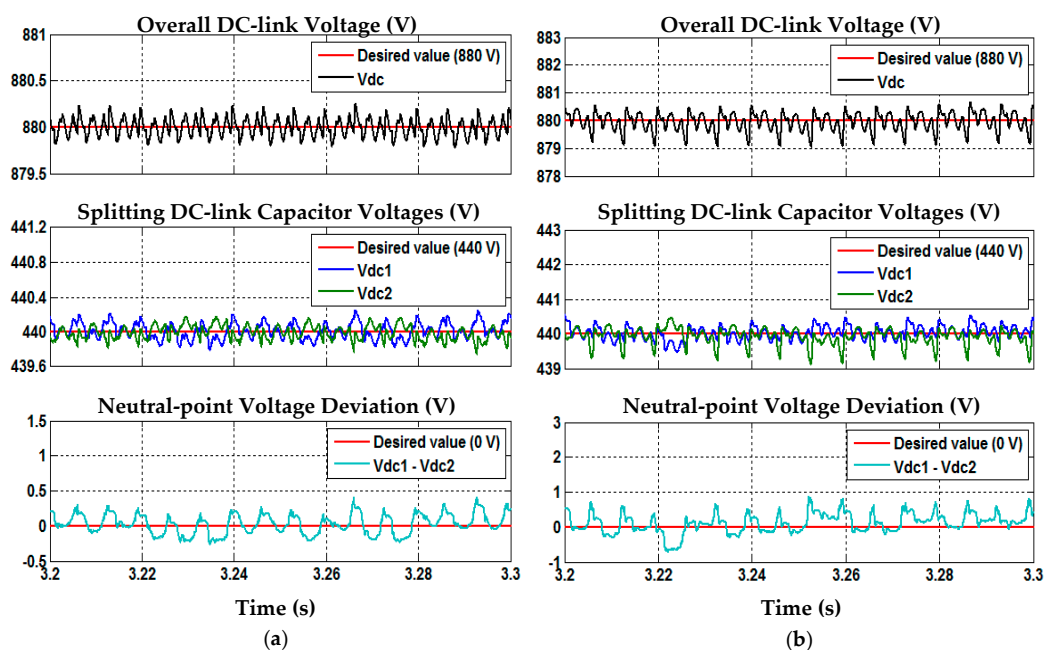


Figure 12. Simulation waveforms of SAPF while using STF-based ADALINE algorithm under case 3 condition which include overall DC-link voltage V_{dc} , splitting DC-link capacitor voltages V_{dc1} and V_{dc2} , and neutral-point voltage deviation Vd ($V_{dc1} - V_{dc2}$), for (a) inductive and (b) resistive loads.

Similarly, under case 3 source voltage condition, the behavior of all DC-link voltages throughout mitigation operation of SAPF is also studied to verify correct operation of SAPF. As seen in Figure 12, under harmonic-distorted (both odd-order and even-order harmonics) source voltage conditions, it is obvious that all DC-link capacitor voltages of the SAPF are properly regulated and maintained at their respective desired value. Besides, voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) of the SAPF are observed to have equally maintained at half of its overall DC-link voltage V_{dc} . Concurrently, the voltage deviation at neutral-point of the SAPF also has been minimized. In other words, SAPF utilizing STF-based ADALINE algorithm is observed to have performed correctly and effectively under the influence of case 3 source voltage condition. At the same time, the observation from Figure 12 also proves effectiveness of DC-link capacitor voltage regulation algorithm with PI technique and neutral-point voltage deviation control algorithm with FDTA technique applied in the proposed SAPF.

4.4. Unbalanced-Distorted Source Voltage (Case 4)

Under case 4 source voltage condition, the simulation waveforms of SAPF which include three-phase source voltage v_S , load current i_L , injection current i_{inj} , and source current i_S , obtained for inductive and resistive loads are shown in Figures 13 and 14 respectively. Meanwhile, performance comparison in term of the resulting THD values of source current i_S , between STF-based ADALINE and unified ADALINE algorithms is summarized in Table 5.

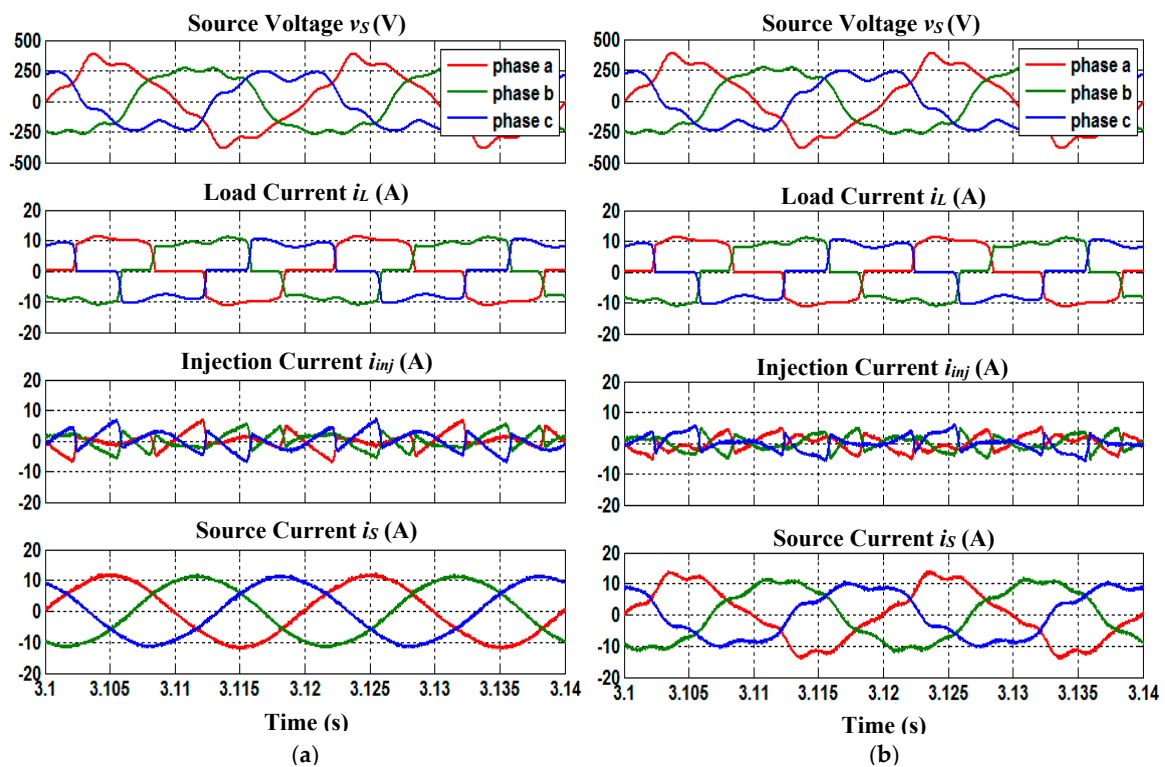


Figure 13. Simulation waveforms of SAPF under case 4 condition which include three-phase source voltage v_S , load current i_L , injection current i_{inj} and source current i_S , for inductive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

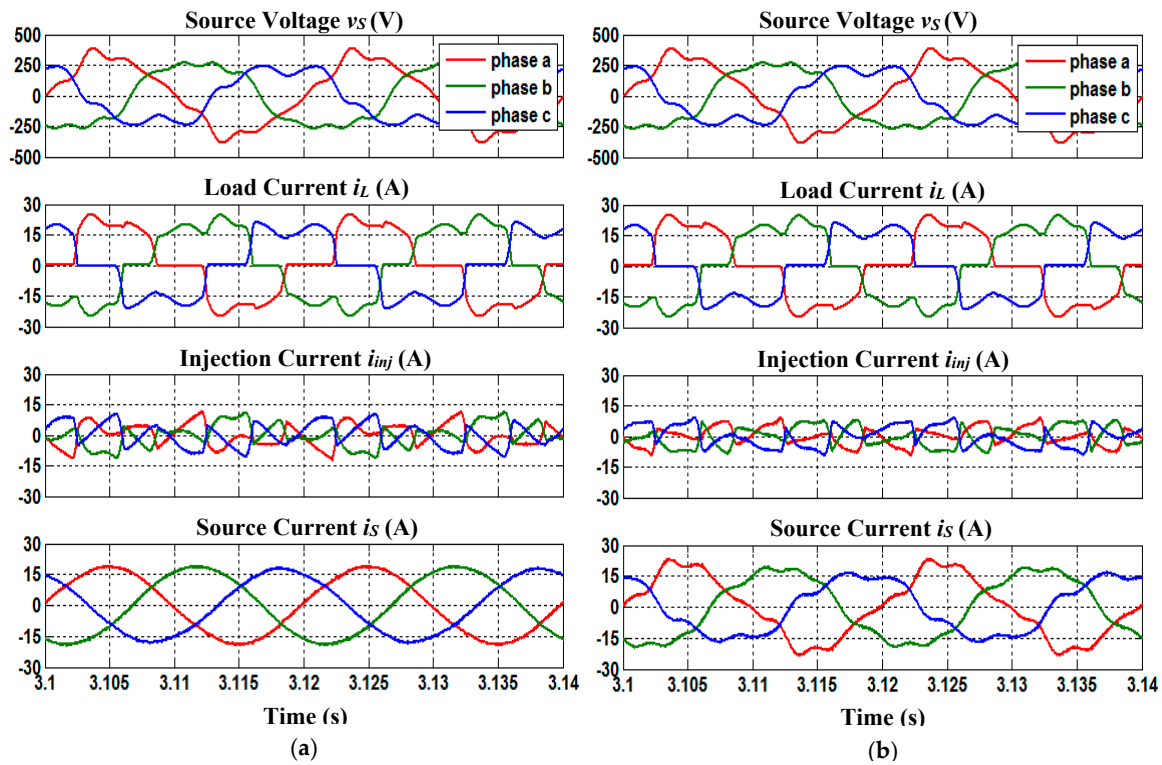


Figure 14. Simulation waveforms of SAPF under case 4 condition which include three-phase source voltage v_s , load current i_L , injection current i_{inj} and source current i_s , for resistive load, obtained by using (a) STF-based ADALINE and (b) unified ADALINE algorithms.

Table 5. THD values of source current i_s before and after connecting SAPF, obtained under case 4 condition (Simulation Result).

Reference Current Generation Algorithm	Total Harmonic Distortion, THD (%)					
	Phase a		Phase b		Phase c	
	Inductive	Resistive	Inductive	Resistive	Inductive	Resistive
Before Connecting SAPF						
N/A	31.95	34.04	26.57	23.98	34.16	35.53
After Connecting SAPF						
STF-based ADALINE	3.31	2.86	2.60	1.87	2.74	2.27
Unified ADALINE	17.82	17.49	11.49	11.31	16.99	16.55

In this case, SAPF utilizing the STF-based ADALINE algorithm is also found to perform effectively in maintaining the THD values of the source current i_s below the allowable THD limit of 5%. For instance, SAPF utilizing the STF-based ADALINE algorithm effectively reduces the high THD values of source current i_s (phase a) from 31.95% (inductive) and 34.04% (resistive) to 3.31% and 2.86% respectively. In contrast, SAPF utilizing the unified ADALINE algorithm fails to comply with the 5% THD limit where high THD values (phase a) of 17.82% (inductive) and 17.49% (resistive) are recorded.

Besides that, for both nonlinear loads, the mitigated source current i_s resulting from both reference current generation algorithms is found to be working in phase with the source voltage. Nevertheless, since STF-based ADALINE algorithm is superior to unified ADALINE in terms of the resulting THD values, hence PFs recorded for both nonlinear loads by using the STF-based ADALINE algorithm are closer to unity as compared to that obtained by using the unified ADALINE algorithm. Specifically, the PF (phase a) recorded before connecting SAPF is 0.94 (both inductive and resistive loads) and it

has been corrected to 0.99 (both inductive and resistive loads) by SAPF utilizing STF-based ADALINE algorithm, and 0.98 (both inductive and resistive loads) by SAPF utilizing unified ADALINE algorithm.

Furthermore, as shown in Figure 15, under unbalanced-distorted source voltage conditions, all DC-link capacitor voltages of the SAPF are also observed to be properly regulated and maintained at their respective desired value. Besides, voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) of the SAPF are observed to have equally maintained at half of its overall DC-link voltage V_{dc} . Concurrently, the voltage deviation at neutral-point of the SAPF also has been minimized. Hence, SAPF utilizing STF-based ADALINE algorithm is once again proven to operate correctly and effectively. Besides, it is also clear from Figure 15 that the applied DC-link capacitor voltage regulation with PI technique and neutral-point voltage deviation control algorithm with FDTA technique is working effectively even though the source voltage is unbalanced and distorted.

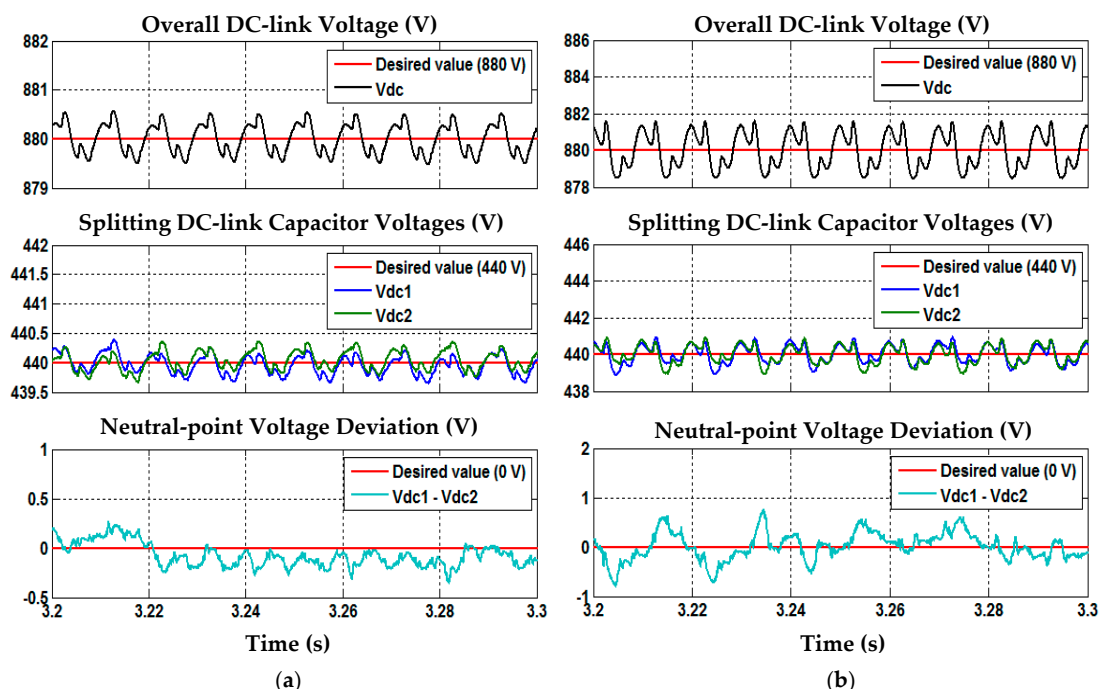


Figure 15. Simulation waveforms of SAPF while using STF-based ADALINE algorithm under case 4 condition which include overall DC-link voltage V_{dc} , splitting DC-link capacitor voltages V_{dc1} and V_{dc2} , and neutral-point voltage deviation Vd ($V_{dc1} - V_{dc2}$), for (a) inductive and (b) resistive loads.

As an overall, based on all the simulation results obtained, it is clear that SAPF utilizing the proposed STF-based ADALINE algorithm is able to perform effectively under various source voltage conditions (both ideal and non-ideal), by maintaining the THD values of the mitigated source current i_s within the allowable THD limit of 5%. This is due its superior ability in generating an accurate synchronization phase even under non-ideal source voltage conditions. With an accurate synchronization phase, an accurate reference current can effectively be generated to govern the operation of SAPF, regardless of the degree of unbalances and distortion in the source voltage. In addition, for all four cases of source voltage conditions, SAPF utilizing STF-based ADALINE algorithm is also able to improve PF performance to almost unity, thereby proving its ability to perform power factor correction.

On the other hand, the existing unified ADALINE algorithm which applies unity representation of the actual source voltage as synchronization phase, only works effectively under ideal (balanced-sinusoidal) source voltage condition but fails to operate appropriately under non-ideal (unbalance and/or distorted) source voltage conditions. This is simply because the required synchronization phase cannot accurately be generated just by considering unity representation of the

actual source voltage. For instance, if the actual source voltage is unbalanced and/or distorted, the generated synchronization phase will be unbalanced and/or distorted as well.

Moreover, under different source voltage conditions (both ideal and non-ideal), all DC-link capacitor voltages of SAPF are observed to have properly regulated and maintained at their respective desired values. Voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) of the SAPF are observed to have equally maintained at half of its overall DC-link voltage V_{dc} . At the same time, the voltage deviation at neutral-point of the SAPF also has been minimized. Hence, based on these encouraging findings, it can be confirmed that the design concept and working principle of SAPF utilizing STF-based ADALINE algorithm in harmonics mitigation are correct and valid.

5. Experimental Verification

A laboratory prototype was developed to validate practically the effectiveness of the proposed STF-based ADALINE algorithm. The experimental setup for the proposed SAPF is shown in Figure 16. A total of twelve insulated-gate bipolar transistors (IKW30N60T, Infineon Technologies, Munchen, Germany) and six diodes (VS-30EPF12, Vishay Intertechnology Inc., Malvern, PA, USA) are assembled to form the three-phase three-level NPC inverter. The switches are driven by gate drive optocoupler (HCPL-3120, Agilent Technologies, Santa Clara, CA, USA) driver IC. All control algorithms are built in a TMS320F28335 digital signal processor (DSP, Texas Instrument, Dallas, TX, USA) board. The nonlinear loads (both inductive and resistive) applied in experimental work are set similar to the simulation work. Similar analysis which has been performed in the simulation work is considered for experimental analysis. Moreover, additional analysis to determine the operational efficiency of the SAPF is also conducted to further evaluate performance of the proposed SAPF. Basically, the operational efficiency ζ of the SAPF can be determined according to the following approach [49]:

$$\zeta = \frac{1}{\left(\frac{\Delta P}{P_L} + 1\right)} \times 100\% \quad (33)$$

where P_L is the real power consumed by the nonlinear load before connecting the SAPF and ΔP is the extra real power consumed by the SAPF itself after connecting it at PCC for harmonics mitigation.

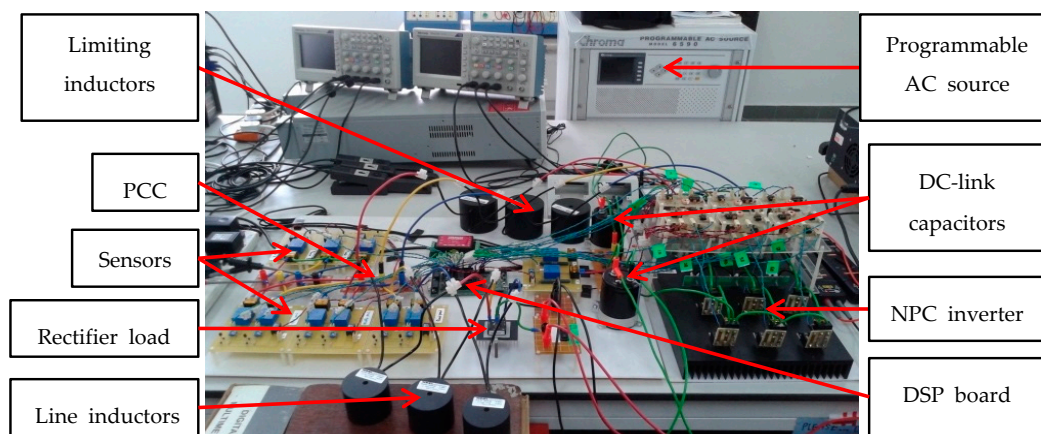


Figure 16. The hardware setup.

For experimental testing, two distinct source voltage conditions are considered:

- Case A: balanced-sinusoidal source voltage, and
- Case B: unbalanced-sinusoidal source voltage.

For case A, the supplied voltage is set at 50 Hz, 100 Vrms (line to line). Meanwhile, for case B, 50 Hz voltage supply with magnitude $v_{Sa} = 53$ Vrms, $v_{Sb} = 36$ Vrms, and $v_{Sc} = 45$ Vrms is applied.

Both source voltages are supplied from a three-phase programmable AC source (Chroma 6590, Chroma ATE INC., Taipei, Taiwan). Next, the desired overall DC-link reference voltage is set at 220 V. The experimental work is designed for maximum rated power of 1 kW.

Experimental waveforms of SAPF utilizing STF-based ADALINE algorithm which include three-phase source voltage v_S , three-phase source current i_S , phase b voltage and currents, and DC-link voltages, obtained under case A condition for inductive and resistive loads are shown in Figures 17 and 18, respectively. Meanwhile, all the THD values recorded from the experimental work are summarized in Table 6.

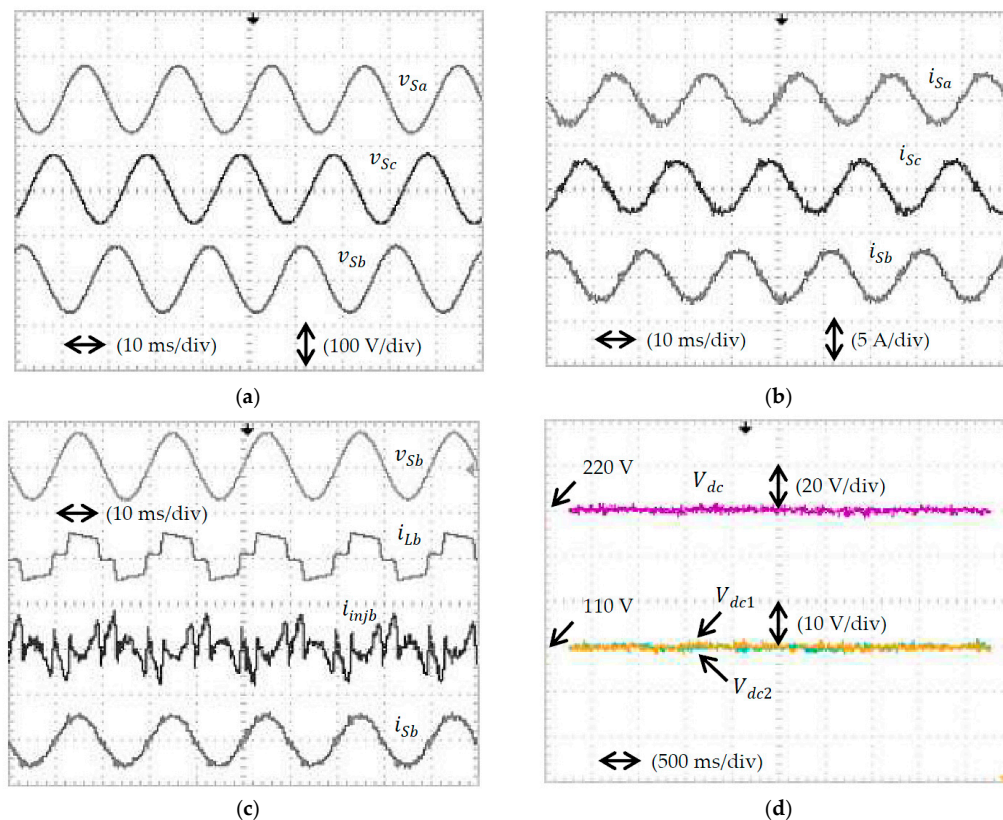


Figure 17. Experimental waveforms of SAPF while using STF-based ADALINE algorithm, obtained for inductive load under case A condition which include (a) three-phase source voltage v_S ; (b) three-phase source current i_S ; (c) phase b source voltage v_{Sb} (100 V/div), load current i_{Lb} (5 A/div), injection current $i_{inj b}$ (2 A/div), and source current i_{Sb} (5 A/div); and (d) DC-link voltages.

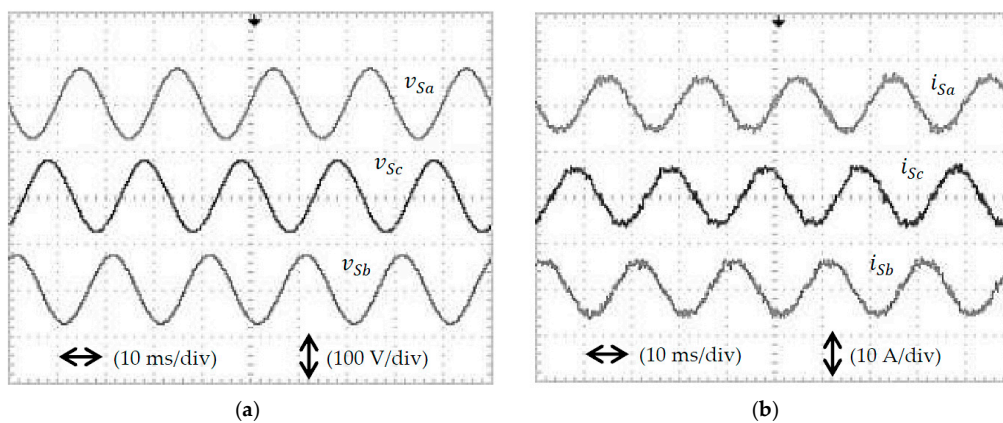


Figure 18. Cont.

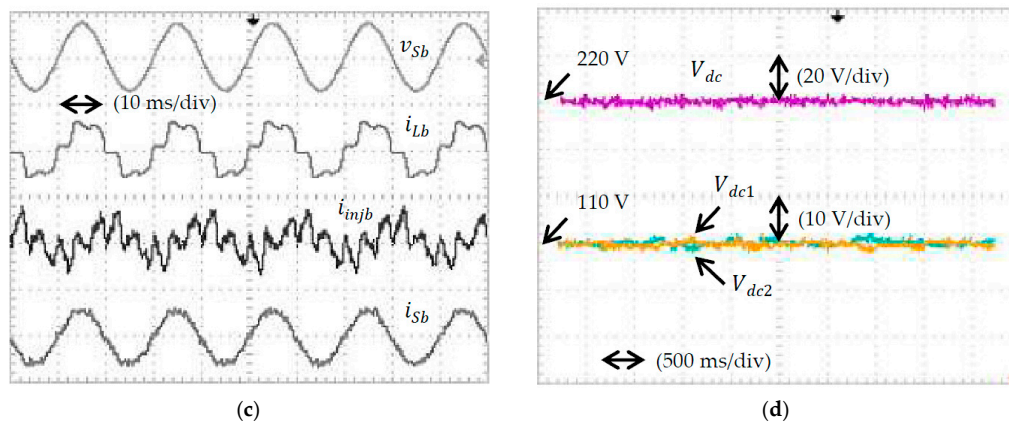


Figure 18. Experimental waveforms of SAPF while using STF-based ADALINE algorithm, obtained for resistive load under case A condition which include (a) three-phase source voltage v_S ; (b) three-phase source current i_S ; (c) phase b source voltage v_{sb} (100 V/div), load current i_{Lb} (10 A/div), injection current i_{injb} (5 A/div), and source current i_{sb} (10 A/div); and (d) DC-link voltages.

Table 6. THD values of source current i_S before and after mitigation by SAPF with STF-based ADALINE algorithm, obtained under cases A and B conditions (Experimental Result).

Cases of Source Voltage Conditions	Total Harmonic Distortion, THD (%)					
	Phase a		Phase b		Phase c	
	Inductive	Resistive	Inductive	Resistive	Inductive	Resistive
Before Connecting SAPF						
Case A	26.10	24.83	25.88	24.85	26.27	25.06
Case B	22.73	21.65	27.32	26.33	23.40	22.18
After Connecting SAPF						
Case A	3.48	3.21	3.65	3.31	3.54	3.25
Case B	3.52	3.35	4.15	3.91	3.84	3.66

Based on Figures 17b and 18b, under balanced-sinusoidal source voltage condition, it is clear that SAPF utilizing the STF-based ADALINE algorithm shows effective mitigation of the harmonics generated by both inductive and resistive loads where the THD values of the mitigated source current i_S for both nonlinear loads are effectively maintained below 5%. For instance, the high THD values of source current i_S (phase a) have been reduced from 26.10% (inductive) and 24.83% (resistive) to 3.48% and 3.21% respectively. Moreover, as shown in Figures 17c and 18c, the mitigated source current i_S obtained for each nonlinear load seems to work in phase with the source voltage v_S and thus achieving almost unity power factor. Specifically, taking phase a as example, the PF recorded before connecting SAPF is 0.95 (inductive) and 0.94 (resistive), and they have been corrected 0.99 (both inductive and resistive loads) by SAPF utilizing the STF-based ADALINE algorithm.

Furthermore, it can be observed from Figures 17d and 18d that for both nonlinear loads, all DC-link capacitor voltages are properly regulated and maintained at their respective desired values. Voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) are also observed to have equally maintained at half of the overall DC-link voltage V_{dc} . Therefore, it can be confirmed that the design concept and operation of SAPF utilizing the STF-based ADALINE algorithm in harmonics mitigation are correct and valid under ideal (balanced-sinusoidal) source voltage condition.

On the other hand, experimental waveforms of SAPF utilizing the STF-based ADALINE algorithm which include three-phase source voltage v_S , three-phase source current i_S , phase b voltage and currents, and DC-link voltages, obtained under case B condition for inductive and resistive loads are

shown in Figures 19 and 20, respectively. It is clear from Figures 19a and 20a that the source voltage supplied in this case is unbalanced and sinusoidal.

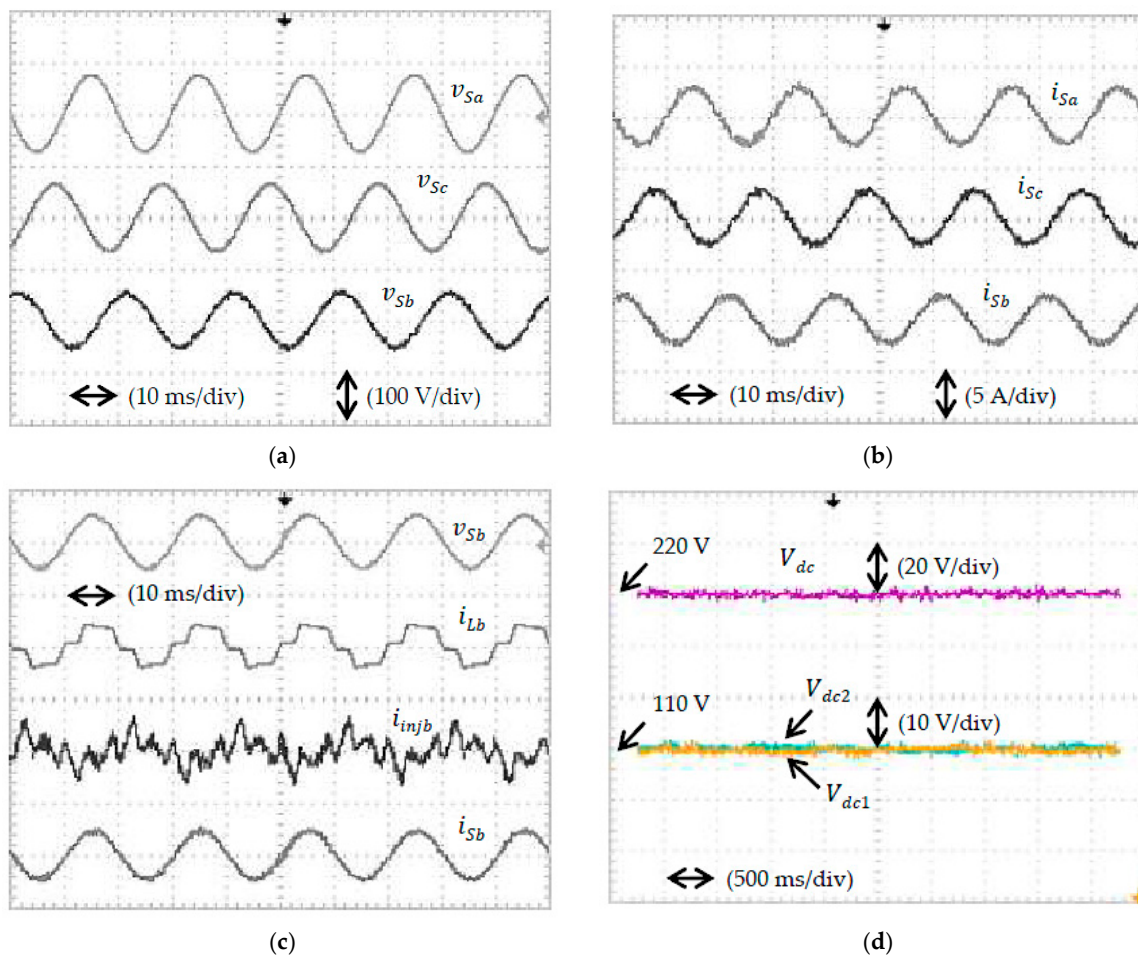


Figure 19. Experimental waveforms of SAPF while using STF-based ADALINE algorithm, obtained for inductive load under case B condition which include (a) three-phase source voltage v_s ; (b) three-phase source current i_s ; (c) phase b source voltage v_{sb} (100 V/div), load current i_{Lb} (5 A/div), injection current i_{inj_b} (2 A/div), and source current i_{sb} (5 A/div); and (d) DC-link voltages.

Nevertheless, as can be observed from Figures 19b and 20b, even though the supplied source voltage is unbalanced, SAPF utilizing the STF-based ADALINE algorithm is still capable of effectively mitigating harmonics generated by both inductive and resistive loads, where the THD values of the mitigated source current i_s recorded for both nonlinear loads are below 5%. For instance, the high THD values of source current i_s (phase a) have been reduced from 22.73% (inductive) and 21.65% (resistive) to 3.52% and 3.35% respectively. Moreover, as shown in Figures 19c and 20c, the mitigated source current i_s obtained for each nonlinear load seems to work in phase with the source voltage v_s and thus achieving almost unity power factor. Specifically, taking phase a as example, the PF recorded before connecting SAPF is 0.95 (inductive) and 0.94 (resistive), and they have been corrected 0.99 (both inductive and resistive loads) by SAPF utilizing the STF-based ADALINE algorithm.

Furthermore, it can be observed from Figures 19d and 20d that for both nonlinear loads, all DC-link capacitor voltages are properly regulated and maintained at their respective desired values. Voltages across both splitting DC-link capacitors (V_{dc1} and V_{dc2}) are also revealed to have equally maintained at half of the overall DC-link voltage V_{dc} . Therefore, once again it can be confirmed that

the design concept and operation of SAPF utilizing the STF-based ADALINE algorithm in harmonics mitigation are correct and valid under non-ideal (unbalanced) source voltage condition.

After confirming the correct operation of SAPF in harmonics mitigation, it is also important to determine its operational efficiency. Under balanced-sinusoidal source voltage condition, SAPF utilizing the proposed STF-based ADALINE algorithm is operating at efficiency of 94% (inductive load) and 97% (resistive load). Meanwhile, under unbalanced-sinusoidal source voltage conditions, SAPF utilizing the proposed STF-based ADALINE algorithm is operating at efficiency of 91% (inductive load) and 95% (resistive load).

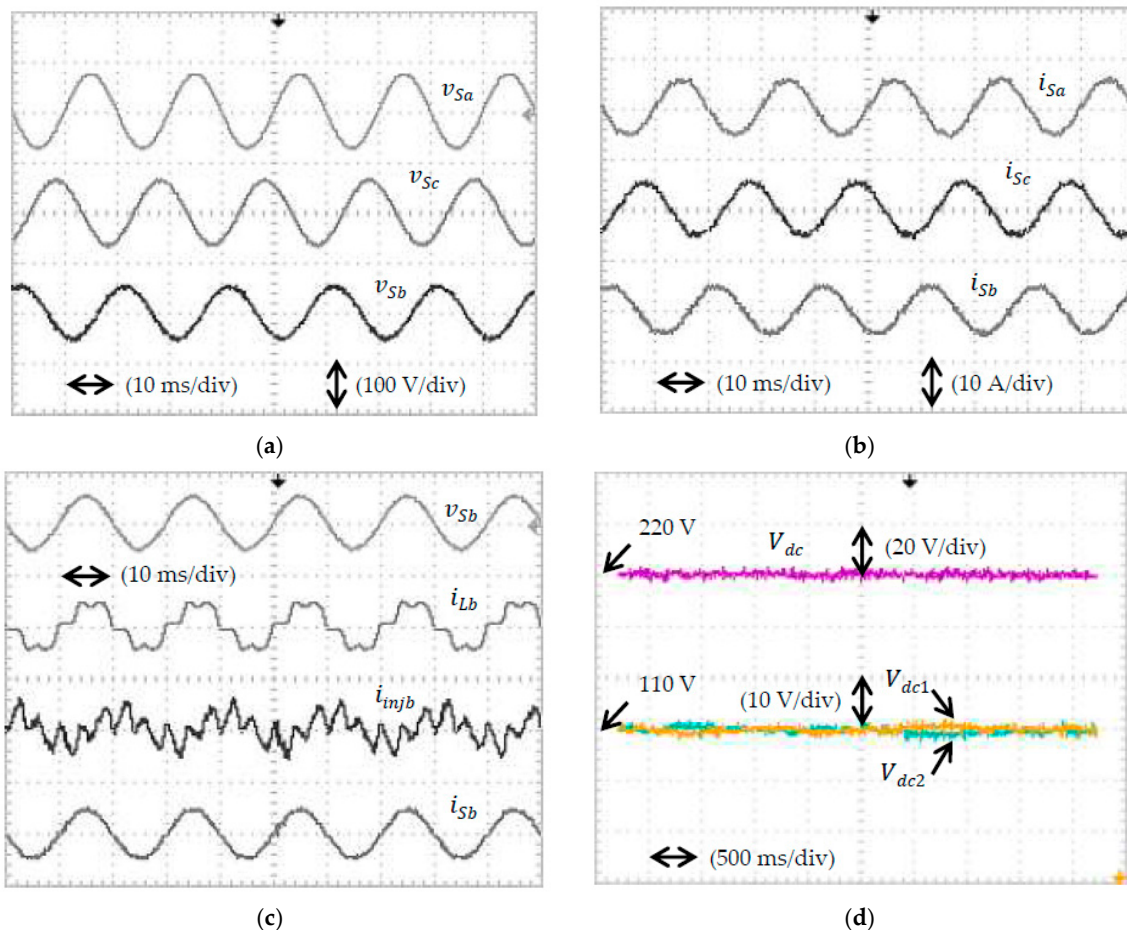


Figure 20. Experimental waveforms of SAPF while using STF-based ADALINE algorithm, obtained for resistive load under case B condition which include (a) three-phase source voltage v_s ; (b) three-phase source current i_s ; (c) phase b source voltage v_{sb} (100 V/div), load current i_{Lb} (10 A/div), injection current $i_{inj b}$ (5 A/div), and source current i_{sb} (10 A/div); and (d) DC-link voltages.

6. Conclusions

In this paper, an ADALINE-based reference current generation algorithm with integration of the STF approach (STF-based ADALINE) is proposed to enhance the operation of three-phase three-level NPC inverter-based SAPF in current harmonics mitigation. In this algorithm, a new STF-based fundamental voltage extraction algorithm which operates as a synchronizer is formulated to ensure in-phase operation of SAPF with the operating power system, by coordinating phases of the generated reference current with respect to angular position of the operating power system. Comprehensive analyses under various source voltage conditions (balanced, unbalanced and distorted) are performed to evaluate performance of the newly proposed algorithm in comparison with the recent unified ADALINE algorithm. From the simulation findings, the mitigation performance of SAPF while using

the proposed STF-based ADALINE algorithm is revealed to be superior to that of unified ADALINE algorithm. In addition, the proposed algorithm is also proven to work effectively with different types of nonlinear rectifier loads and various scenarios of source voltage conditions (balanced, unbalanced and distorted). The minimum THD values recorded for mitigated source current clearly show advantages of the proposed STF-based ADALINE algorithm over the existing unified ADALINE algorithm especially in dealing with non-ideal source voltage conditions. Furthermore, the encouraging findings obtained from the experimental work have confirmed effectiveness and feasibility of proposed algorithm in generating reference current for effective operation of SAPF under both ideal and non-ideal source voltage conditions.

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