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A Modular AC-DC Power Converter with Zero Voltage Transition for Electric Vehicles

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Abstract: A study of the fundamental of operation of a three-phase AC-DC power converter that uses Zero-Voltage Transition (ZVT) together with Space Vector Pulse Width Modulation (SVPWM) is presented. The converter is basically an active rectifier divided into two converters: a matrix converter and an H bridge, which transfer energy through a high-frequency transformer, resulting in a modular AC-DC wireless converter appropriate for Plug-in Electric Vehicles (PEVs). The principle of operation of this converter considers high power quality, output regulation and low semiconductor power loss. The circuit operation, idealized waveforms and modulation strategy are explained together with simulation results of a 5 kW design.

Keywords: PEV's; AC-DC converter; ZVT; SVPWM; matrix converter; H bridge

1. Introduction

AC-DC power converters are typically used in Plug-in Electric Vehicles (PEVs) that require high reliability, reduced total harmonic distortion (THD) of the drawn currents and output regulation to charge batteries or supercapacitors with high performance and satisfy stringent power quality and density standards [1–3]. Electric Vehicle (EV) systems need to consider power quality regulations that typically include the harmonic emission during the charging and transient states, which have been analyzed with different standards and methods as the works described in [4,5]. Moreover, high-frequency switching techniques can increase the power quality, density and energy transfer reliability of AC-DC power converters without altering the basic topology configuration, keeping output controllability and reliability [6]; however, high AC line currents, drawn by the converter to rapidly charge the storage devices distributed along the traction DC link of the EV, may endanger the EV charger operator or impair the charger connector and, therefore, the supply drawn currents are limited to gain reliability causing slow energy transfer [7].

An available method of ensuring operator reliability with high currents, obtaining a simple way of connecting the charge uses wireless power transfer [8–10]. This is a twofold method, since the technique commonly uses a transformer to effectively isolate the power transfer from the user, and provides possible circuit splitting since the transformer is operated as an intermediary between two modules. For example, the converter presented in [11] uses a Medium-Frequency-Transformer for wind power conversion applications; however, the system uses an indirect matrix converter with three output phases that increases the circuit complexity and the magnetic components. EVs typically us two modules, where the first module is located on a charging station and the other on board the vehicle, improving the power density of the converter and increasing the EV distance range since the on-board

section may be free of heavy devices [12]. The use of a single-phase high-frequency transformer was proposed in [13] as a wireless device to convert power from the utility to a DC-link capacitor bank; however, the circuit incurs in the use of several power stages required to generate high-frequency power signals from the utility supply to the transformer, limiting the efficiency of the converter and causing high complexity.

This paper presents the principle of operation of a modular AC-DC converter with Zero-Voltage Transition (ZVT), whose aim is to produce high-quality current waveforms, output regulation and soft switching of the semiconductor devices through the use of an off-board current-feed matrix converter and an on-board high-frequency H bridge, in such a way that the size of the converter located inside the vehicle becomes reduced in contrast with other topologies, [14–16]. The method potentially exhibits the following advantages: first, the current-feed matrix converter is used for straightforward generation of low-ripple, AC line currents without the need of several power stages; second a high-frequency transformer is used to isolate the matrix converter from the H bridge and regulate the output voltage; and third, the circuit uses a ZVT technique together with Space Vector Pulse Width Modulation (SVPWM) to achieve soft commutation of the power semiconductors and generate high-quality sinusoidal currents. Simulation results obtained in Saber with a 5 kW model are provided in the article, demonstrating the correspondence with the developed theoretical background and idealized waveforms to verify its feasibility.

2. ZVT AC-DC Converter

2.1. Circuit Description

The topology arises from the idea of splitting a conventional active rectifier in two modules as is shown in Figure 1. The off-board module of the converter is a three-phase current fed matrix converter that generates a single phase high-frequency current. This converter is intended to be located outside the electric vehicle in the charging station. The matrix converter has six bi-directional switches (Q_1–Q_6) and is fed by the line current of inductors L. The primary side of a high-frequency transformer is connected at the output of the matrix converter to allow wireless power transfer between the matrix converter and the second module.

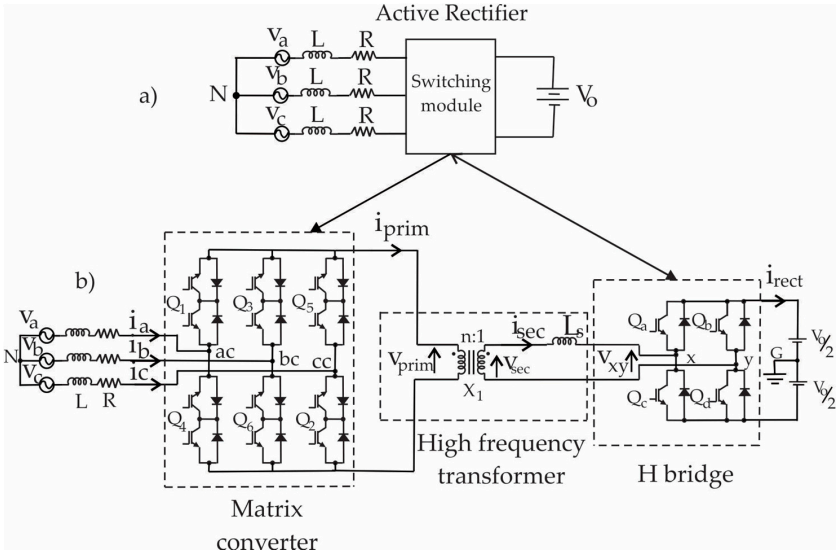

Figure 1. (**a**) Conventional active rectifier; (**b**) Circuit diagram of the proposed modular AC-DC converter.

The on-board module uses the secondary side of the high-frequency transformer and a series inductor, L_s, partially formed by the transformer leakage inductance and an additional inductor,

together with an H bridge to regulate the output voltage, V_o. The H bridge inverts the output voltage with a phase-shifted Pulse Width Modulation (PWM) technique, such that a quasi-square with a $\pm nV_o$ amplitude is generated on the primary side of the transformer, $v_{prim.}$ In this way, the conventional SVPWM technique is modified to obtain three-level PWM voltage waveforms which are used to control the line currents together with the supply voltage.

2.2. Principle of Operation

The control strategy used in the AC-DC converter is based in a SVPWM technique allowing DC output voltage regulation using an index modulation, being easy to implement with a fast response compared to other methods of PWM [17–19]. The conventional SVPWM technique is modified with a ZVT strategy, in such a way that the semiconductor devices are soft switched. The fundamental of operation of the SVPWM technique with ZVT is described below assuming negligible output voltage ripple and lossless components. Figure 2a–c show the active rectifier switching states, S_a, S_b and S_c, of a conventional SVPWM scheme for one switching period in the first sector, which ranges from 0° to 60°, where 1 and 0 indicate on and off states respectively. These switching states are splitted to define the switching states of the H bridge and those of the matrix converter.

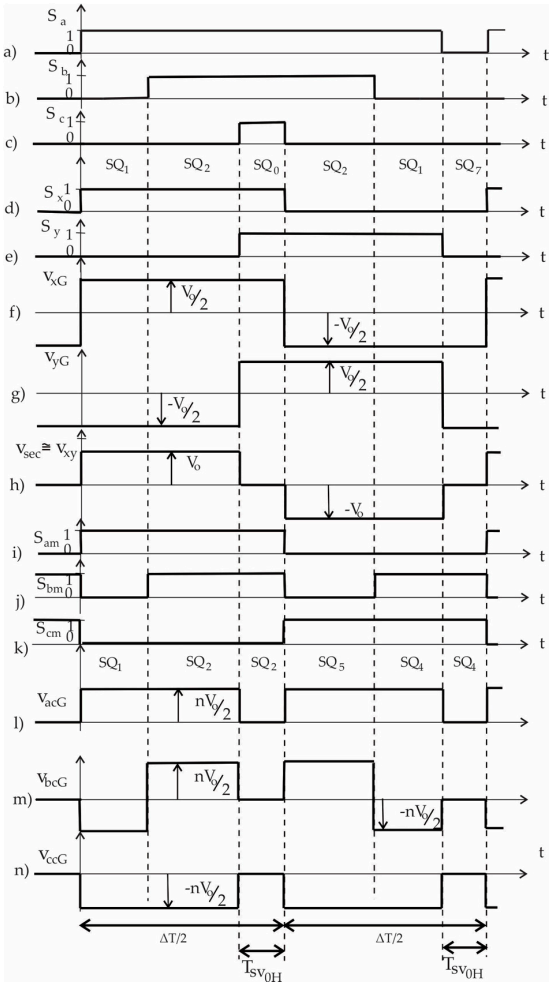

Figure 2. Derivation of the transistor switching states of the modular active rectifier of Figure 1b together with their voltage converter waveforms: (**a**) switching state S_a; (**b**) switching state S_b; (**c**) switching state S_c; (**d**) switching state S_x; (**e**) switching state S_y; (**f**) voltage v_{xG}; (**g**) voltage v_{yG}; (**h**) voltage v_{sec}; (**i**) switching state S_{am}; (**j**) switching state S_{bm}; (**k**) switching state S_{cm}; (**l**) voltage v_{acG}; (**m**) voltage v_{bcG}; (**n**) voltage v_{ccG}.

The H-bridge switching states S_x and S_y are presented in Figure 2d,e, with a duty cycle of 50% and a short-circuit period, T_{SV0H}, that generates the voltages v_{xG} (Figure 2f), and v_{yG} (Figure 2g) referred to the G node of the DC rail. The H-bridge voltage (Figure 2h), $v_{xy} = v_{xG} - v_{yG}$, clamps the secondary side of the transformer to zero Volts when the H bridge is in the short-circuit state. During the first semi cycle, $\Delta T/2$, the voltage in the secondary side of the transformer, v_{sec}, is clamped to V_o and the switching states of the matrix converter legs, S_{am}, S_{bm} and S_{cm} (Figure 2i–k) are equal to S_a, S_b and S_c respectively. When S_a, S_b and S_c are equalized in the three inverters legs, a short-circuit occurs; which is caused in the modular version through the H bridge during T_{SV0H}, such that the matrix converter retains the last switching state combination. During the second semi cycle, a mirrored state sequence occurs, since the output voltage in the H bridge becomes $v_{\text{sec}} = -V_o$ and the switching states in the matrix converter are the complement of S_a, S_b and S_c. The H-bridge short-circuit is caused again and the matrix converter retains the last switching states when S_a, S_b and S_c are equal. In this way, the neutral combination is again caused by the H bridge instead of the matrix converter.

The matrix converter voltages referred to the DC rail node G, v_{acG}, v_{bcG} and v_{ccG} are shown in Figure 2l–n, which are the product of the primary voltage v_{prim} ($v_{prim} = nv_{sec}$) and the individual switching state of each leg. When the short-circuit is caused by the H bridge, the matrix converter voltages are clamped to zero Volts.

2.3. SVPWM Technique

Six active voltage space vectors, sv_1 to sv_6, are obtained at the central nodes of the matrix converter shown in Figure 1b by using six switching states combinations, $\boldsymbol{SQ_1}$ to $\boldsymbol{SQ_6}$, which are listed in Table 1, with respect to the states of S_{am}, S_{bm} and S_{cm}. These space vectors are plotted in the bi-dimensional α-β plane of Figure 3 using the Clarke transform [20]. sv_1 to sv_6 are generated using the switching states of the matrix converter together with its output voltage $\pm nV_o$. A neutral space vector, sv_0, is produced by using any state combination of the matrix converter together with the H-bridge short-circuit. sv_0 is located at the origin of the α-β plane.

Table 1. Switching states vectors of matrix converter.

Switching State Combination	S_{am}, S_{bm} and S_{cm} States
$\boldsymbol{SQ_1}$	(1, 0, 0)
$\boldsymbol{SQ_2}$	(1, 1, 0)
$\boldsymbol{SQ_3}$	(0, 1, 0)
$\boldsymbol{SQ_4}$	(0, 1, 1)
$\boldsymbol{SQ_5}$	(0, 0, 1)
$\boldsymbol{SQ_6}$	(1, 0, 1)

An arbitrary averaged voltage vector, $v_{cav} = V_{cpk}\angle\theta_c$, can be generated at the converter input using a Volts-seconds balance to control the input line currents together with the supply voltages. Since the matrix converter output voltage reverses its biasing during half of the switching cycle, the Volts-seconds balance utilises the operating sector and its opposite sector of the α-β plane. For example, during the first semi cycle of a switching period in sector S_1, v_{cav} is determined by:

$$v_{cav} = a_1 sv_1 + a_2 sv_2 + a_0 sv_0 \tag{1}$$

where $\alpha_1 = \frac{T_{sv1}}{\frac{\Delta T}{2}}$, $\alpha_2 = \frac{T_{sv2}}{\frac{\Delta T}{2}}$ and $\alpha_0 = \frac{T_{sv0H}}{\frac{\Delta T}{2}}$.

Whereas, during the second semi cycle, v_{cav} is defined by:

$$v_{cav} = a_4 sv_4 + a_5 sv_5 + a_0 sv_0 \tag{2}$$

where $\alpha_4 = \frac{T_{sv4}}{\frac{\Delta T}{2}}$, $\alpha_5 = \frac{T_{sv5}}{\frac{\Delta T}{2}}$, since $v_{prim} = -nV_o$.

The same procedure applies for the rest of the sectors. Table 2 summarizes the switching states according to the sector location of θ_c together with the biasing of v_{prim}.

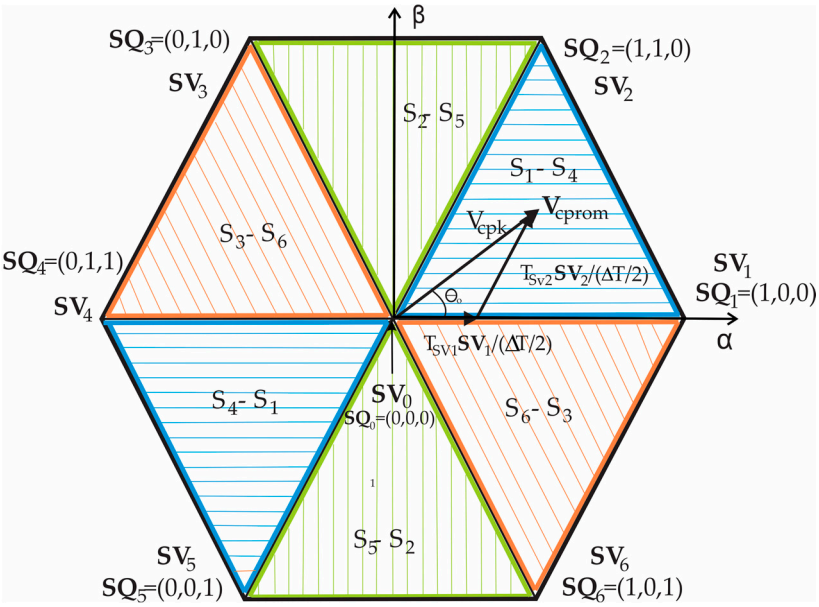

Figure 3. Space Vector Bi-dimensional plane.

Table 2. Switching states vectors.

Angle θ_c	Sector	v_{prim} (+)	v_{prim} (−)
		Switching State	**Switching State**
1–60°	S_1	SQ_1, SQ_2	SQ_4, SQ_5
61–120°	S_2	SQ_2, SQ_3	SQ_5, SQ_6
121–180°	S_3	SQ_3, SQ_4	SQ_6, SQ_1
181–240°	S_4	SQ_4,SQ_5	SQ_1, SQ_2
241–300°	S_5	SQ_5, SQ_6	SQ_2, SQ_3
301–360°	S_6	SQ_6, SQ_1	SQ_3, SQ_4

v_{xy} and v_{sec} are shown in Figure 4a,b respectively for straight comparison to describe the generation of the secondary transformer current, i_{LS}, shown in Figure 4c. During the first semicycle, i_{LS} is assumed positive together with v_{sec} clamped to V_o. The slope of i_{Ls} is negative since the converter voltage is greater than the AC supply voltage even when the matrix converter switches from SQ_1 to SQ_2; whilst during the H-bridge short circuit the matrix switching state SQ_2 is retained, such that the slope of i_{LS} is inverted. A current reversal occurs in i_{Ls} since v_{xy} is clamped to $-V_o$ and v_{sec} to zero during an overlap period T_{ovl} that is calculated with Equation (3):

$$T_{ovL} = \frac{nI_{primpk}L_s}{V_o} \tag{3}$$

where I_{primpk} is the peak magnitude of the current in the primary side of the transformer, i_{prim}.

In this way, the ZVT is performed in the semiconductor devices during the current reversal to obtain soft commutation. The overlap period finishes when i_{LS} reaches the same magnitude with an opposite sign, such that the first semi cycle becomes to an end. The second semi cycle is a mirror of the first since the complementary switching states of SQ_1 and SQ_2, SQ_4 and SQ_5 respectively, are used to operate the matrix converter and because the H bridge has clamped v_{xy} to $-V_o$.

i_{Ls} is equal to ni_{prim}, where i_{prim} depends on the switching of the line currents. Table 3 lists the equivalence of i_{prim} respective to the line currents and the matrix switching states.

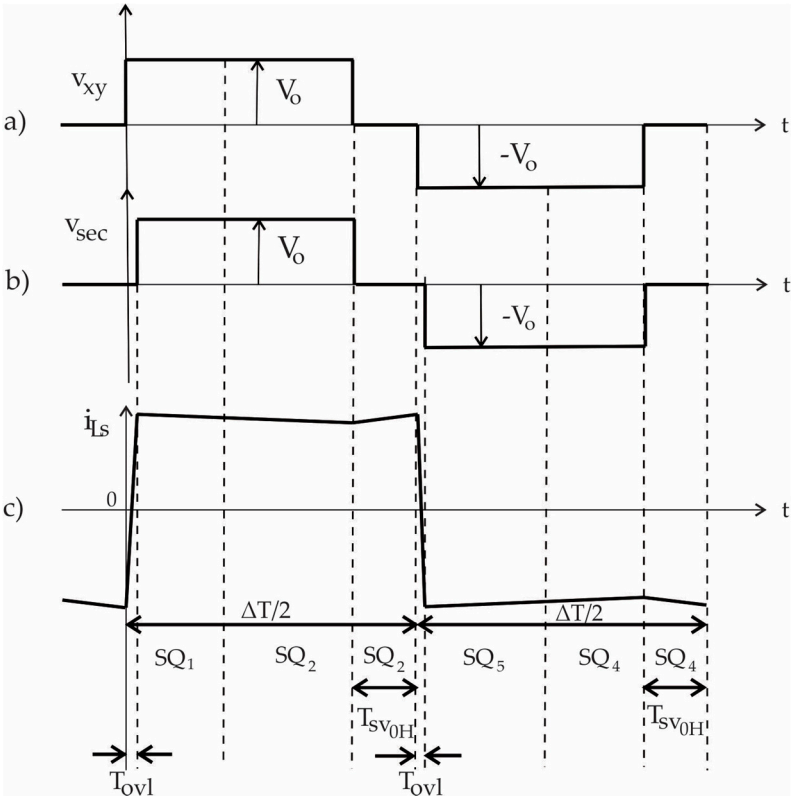

Figure 4. Ideal wavfeorms: (**a**) Voltage v_{xy}; (**b**) voltage v_{sec}; and (**c**) current through the transformer, i_{LS}.

Table 3. i_{LS} magnitude for each switching state.

Switching State	i_{prim}
SQ_1	$i_{prim} = i_a - i_b - i_c$
SQ_2	$i_{prim} = i_a + i_b - i_c$
SQ_3	$i_{prim} = i_b - i_a - i_c$
SQ_4	$i_{prim} = i_b + i_c - i_a$
SQ_5	$i_{prim} = i_c - i_b - i_a$
SQ_6	$i_{prim} = i_a - i_b + i_c$

3. ZVT AC-DC Converter

A block diagram for the AC-DC operation of the circuit of Figure 1b is shown in Figure 5. In this figure θ_c and the index modulation, M_a, are the inputs required for the SVPWM scheme. Since the converter of Figure 1b is divided into two parts, a sequenced operation is used and described below:

(a) The conventional active rectifier switching states are generated using M_a and θ_c. These are equivalent to the control signals of Figure 2a–c.

(b) S_{am}, S_{bm} and S_{cm}, shown in Figure 2i–k, are generated and multiplexed to assign the control signals for each bi-direccional switch.

(c) S_x and S_y, shown in Figure 2d,e, are generated from the active periods of the conventional active rectifier.

(d) An overlap is required to turn on and off the bidirectional switches during the reversal of current i_{LS}.

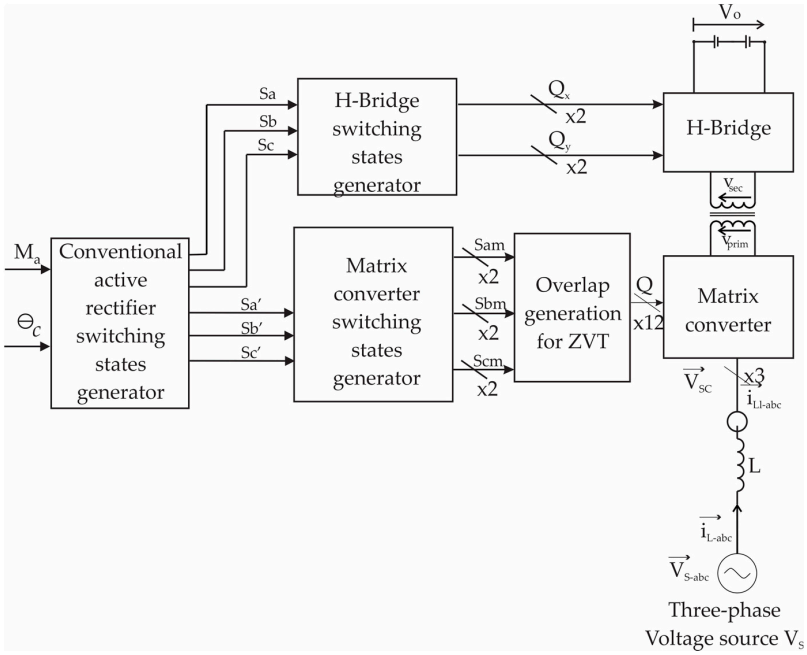

Figure 5. Block diagram for AC-DC operation of the modular converter of Figure 1b.

3.1. H-Bridge and Matrix Converter Switching States

The derivation of the H-bridge and matrix converter control switching states is described using the block diagram of Figure 6, which are obtained from the switching states of the conventional active rectifier, as described in Section 2.2. Firstly, S_a, S_b and S_c are generated using θ_c and M_a. The conventional SVPWM active periods, T_a, T_b and T_c, are compared with a high-frequency carrier triangular waveform to produce three digital signals, PWM_a, PWM_b and PWM_c, which are shown in Figure 7. These signals are multiplexed with respect to the sector location to derive the switching states S_a, S_b and S_c, (Figure 7e–g). The H-bridge switching states, Q_a, Q_c, Q_b an Q_d, are obtained with a sequential circuit using S_a, S_b and S_c as inputs.

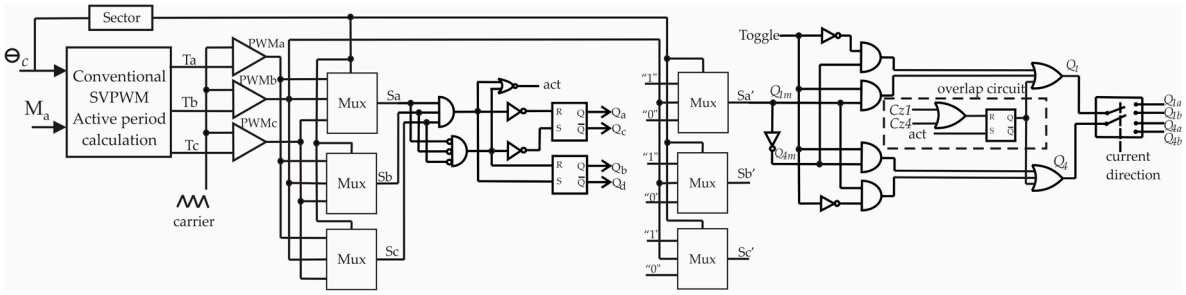

Figure 6. Block diagram to generate the switching states for the matrix converter and the H bridge.

Other set of multiplexers are utilized to derive three digital signals, S_a', S_b' and S_c', that produce the active switching states by using off and on states instead of the short and long pulse trains of PWM_a and PWM_c respectively, as is shown in Figure 7h–j. S_a', S_b' and S_c' are also multiplexed with respect to the sector location and are processed to derive the switching state of each matrix converter leg. The digital circuit to generate the matrix converter control signals for the first leg, Q_{1a}, Q_{1b}, Q_{4a} and Q_{4b}, is shown at the right-hand of Figure 6. This circuit commutates the switching states to the opposite side of the α-β plane, sending the complement states when v_{sec} is clamped to negative voltage. The same circuit is used to generate the control signals for the second and third matrix converter legs.

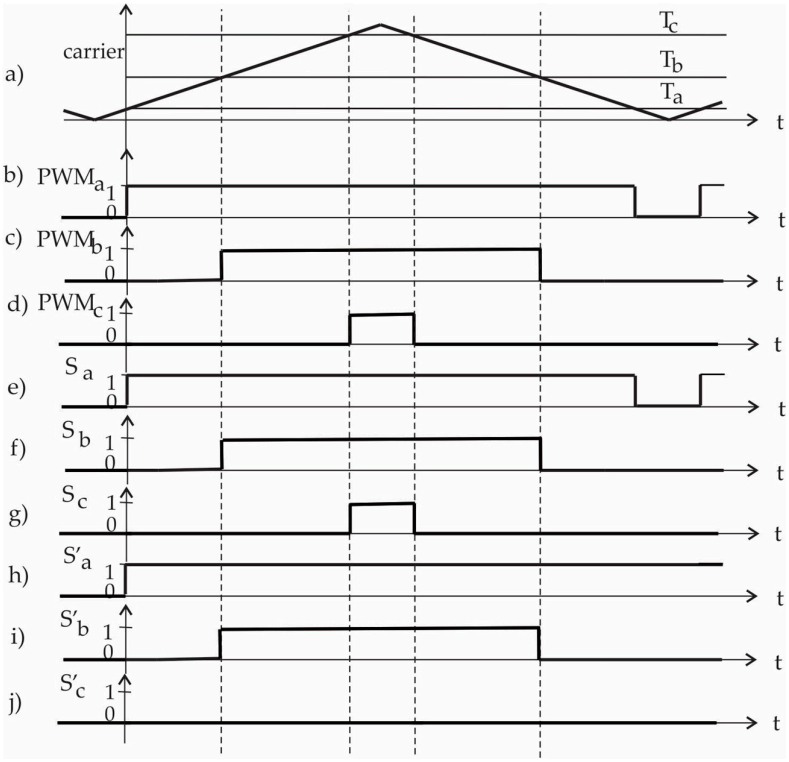

Figure 7. Generation of PWM signals, and conventional active rectifier switching states. (**a**) High-frequncy triangular carrier signal; (**b**) digital signal PWM_a; (**c**) digital signal PWM_b; (**d**) digital signal PWM_c; (**e**) switching state S_a; (**f**) switching state S_b; (**g**) switching state S_c; (**h**) digital signal S'_a; (**i**) digital signal S'_b; (**j**) digital signal S'_c.

3.2. Neutral-to-Active Switching Transition in the Matrix Converter

Since each bi-directional switch in the matrix converter is built with two semiconductor devices with a common collector configuration that allows the current flow in both directions, an overlap in all the matrix converter legs is required to commutate the flowing of current in one direction to the opposite direction during the negative biasing of v_{sec}. Figure 8 shows the switching sequence of Q_{1a}, Q_{1b} and Q_{4a}, Q_{4b} to turn off Q_1 and turn on Q_4.

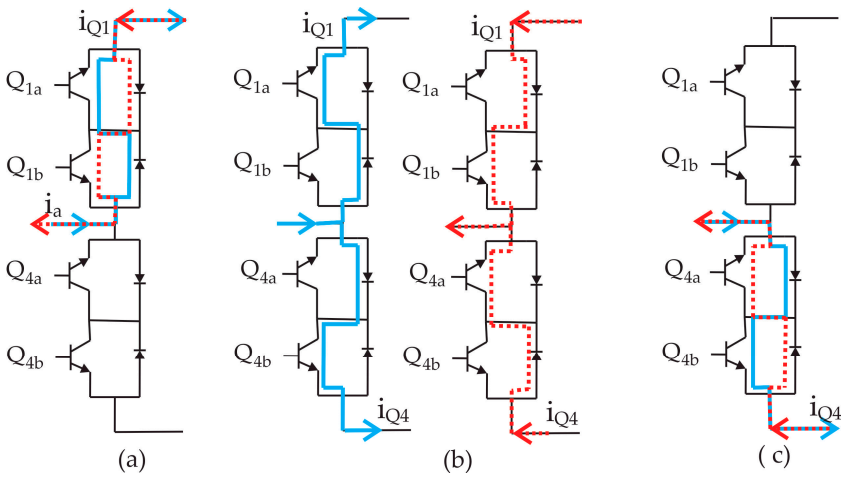

Figure 8. Switching sequence in the on-to-off transition from neutral-to-active switching state. (**a**) initial current flow; (**b**) overlap time; (**c**) current flow in the opposite direction.

In Figure 8a, Q_{1a} and Q_{1b} are conducting the current in the blue or red arrow direction, i_{Q1}. When Q_1 and Q_4 are commutated to the on and off states respectively, Q_{1b} is turned off and Q_{4b} is turned on when the current is flowing in the blue arrow direction; and Q_{1a} is turned off and Q_{4a} is turned on when the current is flowing in the red arrow direction (Figure 8b). Finally, when the current flow stops due to the biasing inversion of v_{sec} through the corresponding arrow, the transistors of Q_4 are turned on, (Figure 8c), and, therefore, the current in Q_4, i_{Q4}, flows in the opposite direction through the matrix converter leg.

The logic circuit that generates the overlap in the first matrix converter leg is included in the right-hand of Figure 6. This diagram shows the zero crossing detector signals C_{z1} and C_{z2} that are used to indicate the end of the overlap.

3.3. Active-to-Active Switching Transition in the Matrix Converter

The transition between two active vectors takes place twice in a switching period. In Figure 2a the transition occurs from $\boldsymbol{SQ_1}$ to $\boldsymbol{SQ_2}$ during the first semi cycle; whereas in the second semi cycle, the transition occurs from $\boldsymbol{SQ_5}$ to $\boldsymbol{SQ_4}$. The transition between adjacent active vectors implies a switching state change in one matrix converter leg. By instance, the state of the second matrix leg, S_{bm} in Figure 2, switches from the off to the on state producing an active-to-active transition. The turn on-to-off sequence of Q_3 and Q_6 is shown in Figure 9.

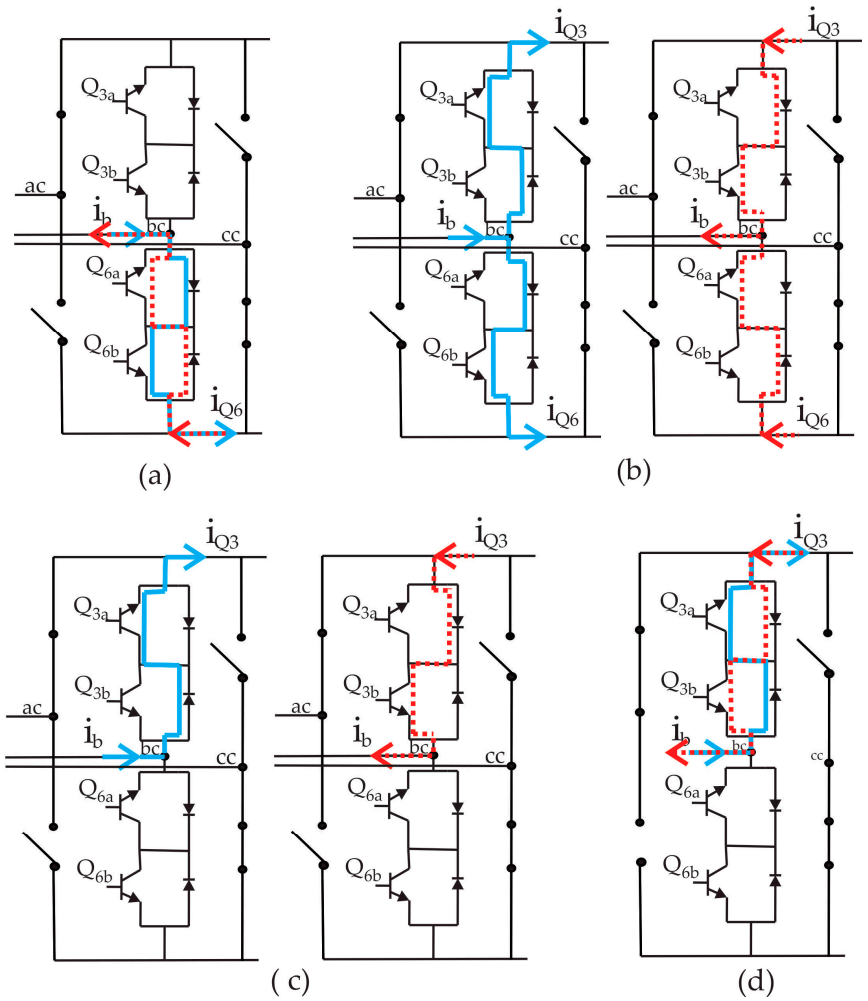

Figure 9. Switching sequence in the on-to-off transition from active-to-active switching state. (**a**) initial current flow; (**b**) overlap time; (**c**) current flow in the opposite direction; (**d**) bidirectional switch in on state.

In Figure 9a, Q_{6a} and Q_{6b} are firstly turned on and the current flows in the red or blue arrow direction, i_{Q6}; then, in Figure 9b Q_{6a} and Q_{3a} are turned off and on respectively to allow the current reversal in the matrix converter leg when the current is flowing in the blue arrow direction; or Q_{6b} and Q_{3b} are turned off and on respectively to allow the current reversal when the current is flowing in the red arrow direction. In this figure, the transistors of Q_6 are turned on for a period of time t_D longer than the turning off time of the semiconductor device, t_r, to guarantee that the current stops flowing through it. This bidirectional switch configuration comes to an end when the transistor of Q_6 is turned off as shown in Figure 9c. Lastly, the sequence finishes by turning on transistors of Q_3, as shown in Figure 9d, with i_{Q3} flowing in the opposite direction.

4. Steady-State Analysis and Parameters Selection

A steady-state analysis of the AC-DC modular converter is derived using the generalized diagram of Figure 10, where v_s is the three-phase source voltage vector, L is the line inductor, v_L is the line inductor voltage vector, v_{cav} is the converter voltage vector, n:1 is the transformer turns ratio that links the off-board AC-AC module with the AC-DC module; V_o is the DC output voltage and R is the output load.

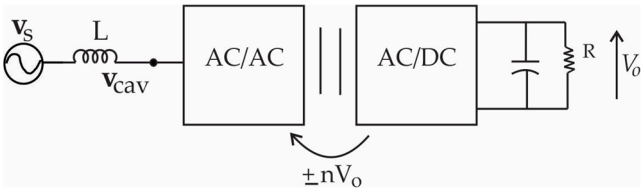

Figure 10. Generalized diagram for steady-state analysis

Assuming a vectorial current control to drive the phase and magnitude of the line current $\boldsymbol{i}_L$ and produce high power factor, a phasorial diagram is shown in Figure 11 which describes the behavior of the AC-DC converter of Figure 1. In this diagram, v_s, v_L and v_{cav} are defined by:

$$v_s = V_{spk}\angle 0^\circ, \tag{4}$$

$$v_L = V_{Lpk}\angle 90^\circ, \tag{5}$$

$$v_{cav} = V_{cpk}\angle \varphi^\circ \tag{6}$$

In Figure 11 the amplitudes of v_{cav} and v_L are defined by:

$$V_{cpk} = \frac{V_{spk}}{\cos\varphi} \tag{7}$$

$$V_{Lpk} = V_{cpk}\sin\varphi \tag{8}$$

Whereas the current $\boldsymbol{i}_L$ is obtained with Equation (9):

$$i_L = \frac{v_L}{\omega L} \tag{9}$$

Considering the phasorial diagram of Figure 11, v_L is calculated using Equation (10):

$$v_L = v_s - v_c \tag{10}$$

Equations (9) and (10) are used to derive the amplitude of i_L, I_{Lpk}, which is defined by:

$$I_{Lpk} = \frac{V_{spk} tg\varphi}{\omega L} \tag{11}$$

where $\omega = 2\pi f$. Assuming ideal conditions, a power balance is derived:

$$P_{in} = P_{out} \tag{12}$$

where P_{in} and P_{out} are the input and output power converter respectively and are equivalent to Equation (13):

$$\frac{3V_{spk}I_{Lpk}}{2} = \frac{V_o^2}{R} \tag{13}$$

Substituting Equation (11) in (13), the power balance becomes:

$$\frac{3V_{spk}{}^2 tg\varphi}{2\omega L} = P_o \tag{14}$$

According to Figure 11, the AC-DC converter can operate under two extreme conditions; a minimum supply voltage, V_{spkmin}, obtaining a maximum phase, φ_{max}, with a maximum power demand at the output, P_{omax}; and a maximum supply voltage, V_{spkmax} obtaining a minimum phase, φ_{min}, with a minimum power demand at the output, P_{omin}. Therefore, φ_{max} and φ_{min} are obtained using Equations (15) and (16) respectively:

$$\varphi_{max} = tg^{-1}\frac{2P_{omax}\omega L}{3V_{spkmin}^2} \tag{15}$$

$$\varphi_{min} = tg^{-1}\frac{2P_{omin}\omega L}{3V_{spkmax}^2} \tag{16}$$

Considering P_{omax} = 5 kW, P_{omin} = 500 W, V_{spkmin} = 144 V and V_{spkmax} = 216 V, φ_{max} and φ_{min} are obtained for different values of L. Figure 12 is used to select the optimal L that allows an appropriate range of phase control. L was judged to be 3 mH, in such a way that φ can be ranged from 0.46° to 10.3°.

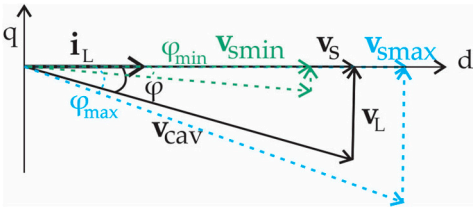

Figure 11. Phasorial diagram for the AC-DC converter operation.

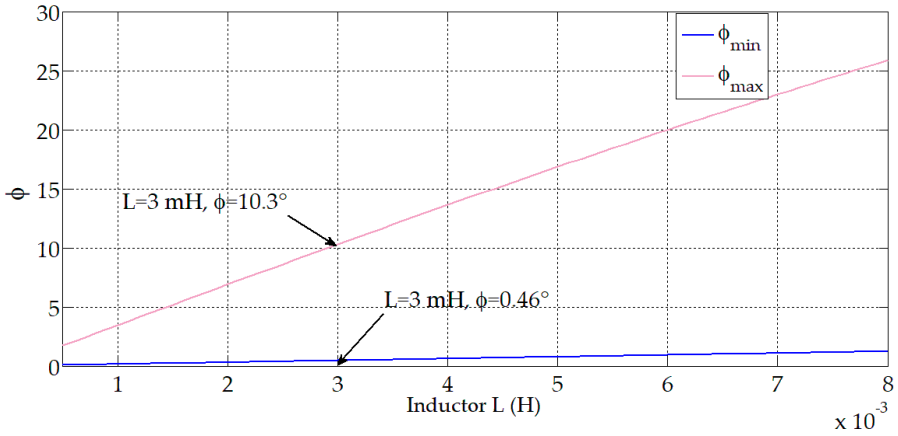

Figure 12. φ_{min} and φ_{max} obtained for different values of L.

The voltage V_{cpk} is expressed in function of the modulation index, M_a, when the converter operates with a SVPWM scheme [14], as follows:

$$V_{cpk} = M_a n V_o \frac{\sqrt{3}}{4} \tag{17}$$

The minimum and maximum converter voltages, V_{cpkmin} and V_{cpkmax}, are utilized to obtain the minimum and maximum modulation indexes, M_{amin} and M_{amax} respectively, which are shown in (18) and (19):

$$M_{amin} = \frac{4V_{cpkmin}}{\sqrt{3}nV_o} \tag{18}$$

$$M_{amax} = \frac{4V_{cpkmax}}{\sqrt{3}nV_o} \tag{19}$$

where V_{cpkmin} = 144.004 Volts and V_{cpkmax} = 219.53 Volts were calculated using Equation (7) for V_{spkmin} and V_{spkmax} respectively. An optimal value for n was determined by using Equations (18) and (19) and ranging n from 2 to 10, such that the results are plotted in Figure 13. n was selected to be 5 since M_a can be set between 0.66 and 1 to control the amplitude of the converter input voltage. It was judged in this work that n should be 5 to allow the converter an appropriate SVPWM operation and leave a small upper range of M_a for the ZVT effects since the maximum value of M_a is 1.16 for SVPWM [20].

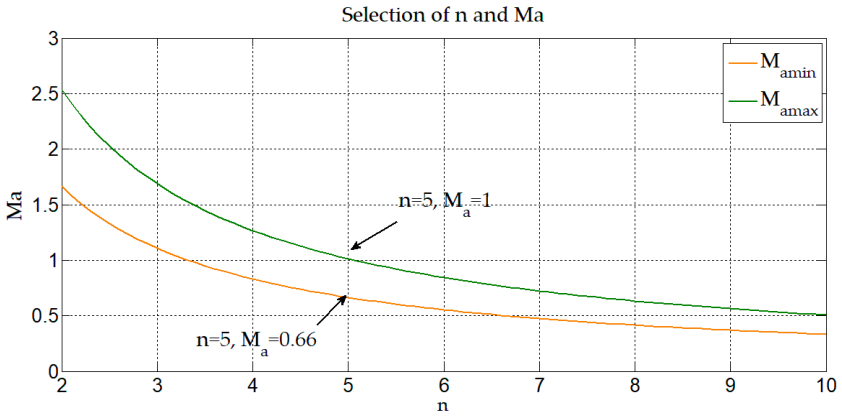

Figure 13. M_{amin} and M_{amax} obtained for different n.

Equations (14) and (17) show that there is a compromise between the selection of the parameters n, φ and L to reach a wide range of M_a within the conventional active rectifier operation range.

5. Numerical Verification

To verify the principle of operation of the modular AC-DC converter and the SVPWM with ZVT control strategy, a simulation in Saber was performed using ideal components and the parameters listed in Table 4.

Table 4. Simulation Parameters.

Parameter	Value
Source voltage v_a, v_b and v_c	180 V peak
Source frequency	60 Hz
Switching fequency	7.2 kHz
Input inductor L	3 mH
Index modulation M_a	0.628
Input resistor R	0.1 Ω
Leakage Inductance L_s	50 μH
Turns ratio n	5:1
Output voltage V_o	100 V
Output Power P_o	5 kW

5.1. Verification of the Modified SVPWM

A Saber simulation was performed synchronizing the operation of the divided rectifier control signals with the fundamental frequency of the supply, using the scheme of Figure 14. I_{Lpk} is the current reference used to define θ_c and M_a for the SVPWM operation of the rectifier and cause high power factor as shown in Figure 11. The converter voltage was phase shifted to align the line currents with the supply using the vectorial control system of Figure 14. A reference current of I_{Lpk} = 19.54 A was used to obtain a 100 V, 5 kW output with high power factor supply. The component of V_{cav} in the q axis, V_{cavq}, was determined using Equation (7) and the phasorial diagram of Figure 11, V_{cavq} = 22.1 V, such that $V_{cavd} = V_{spk}$ = 180 V, therefore, the phase between v_s and v_{cav} was $\varphi = 7°$.

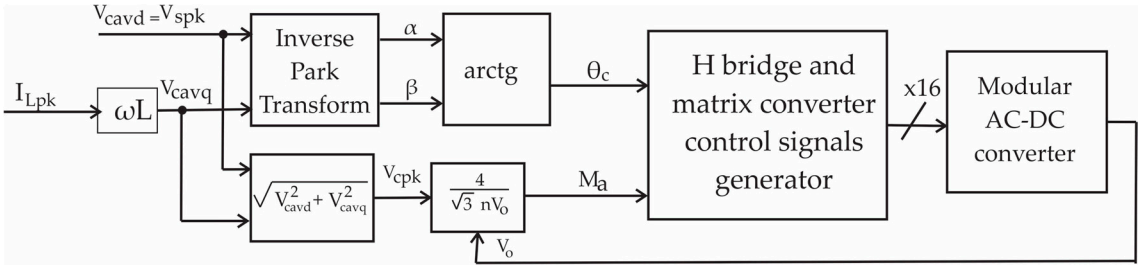

Figure 14. General scheme used in simulation.

To confirm the correct operation of the scheme shown in Figure 14, Figure 15 shows a Saber result plot of the supply and converter phases, θ_S and θ_C, for current references of 9.4 A and 19.54 A and cause 2.5 kW and 5 kW respectively. In Figure 15a a phase shift of 3° is obtained, whereas in Figure 15b the phase shift becomes of 7° since the current reference was increased. The effectiveness of the SVPWM rectifier operation of the circuit of Figure 1b was verified analyzing the Saber simulation results of the line currents and input voltages of the converter. Figure 16a shows Saber results of the source voltage v_{aN} and the line current i_a. The resultant line current i_a is sinusoidal with a 3.3% ripple. Figure 16b shows the five-level converter voltage, v_{acN}, to verify the correct operation of the space vector strategy. The current and voltage in the primary side of the transformer, i_{prim} and v_{prim} are shown in Figure 16c, where i_{prim} is the rectified version of the line currents, but, inverted in one quadrant of the switching cycle producing a high-frequency AC square current.

The operation of the H bridge was verified contrasting the conventional SVPWM states with the phase-shifted control signals of the H bridge. Figure 17 plots the Saber results of $S_{a,}$ S_b and S_c (Figure 17a–c, respectively) in contrast to S_x and S_y (Figure 17d,e). The H-bridge input voltages v_{xG} and v_{yG} are shown in Figure 17f,g, respectively, and its difference v_{xy} is shown in Figure 17h. In the latter figure, v_{xy} is a $\pm V_o$ quasi-square waveform, whose zero level is effectively produced by the H-bridge overlap, which can be used to produce the neutral vectors required by the conventional rectifier states in a switching cycle.

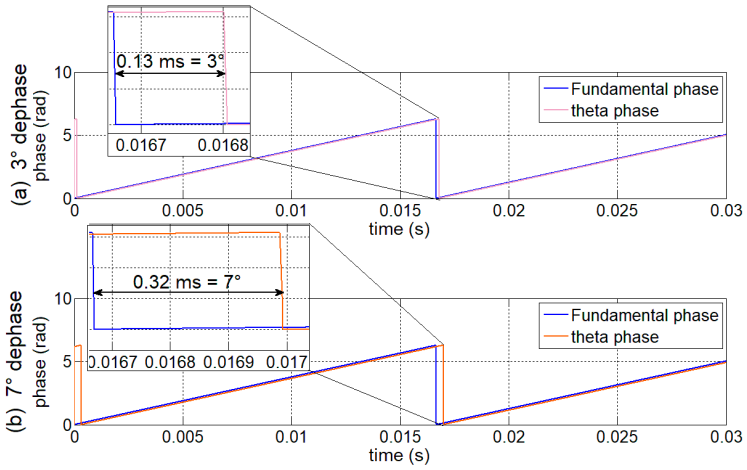

Figure 15. Variation of φ: (**a**) $\varphi = 3°$; (**b**) $\varphi = 7°$.

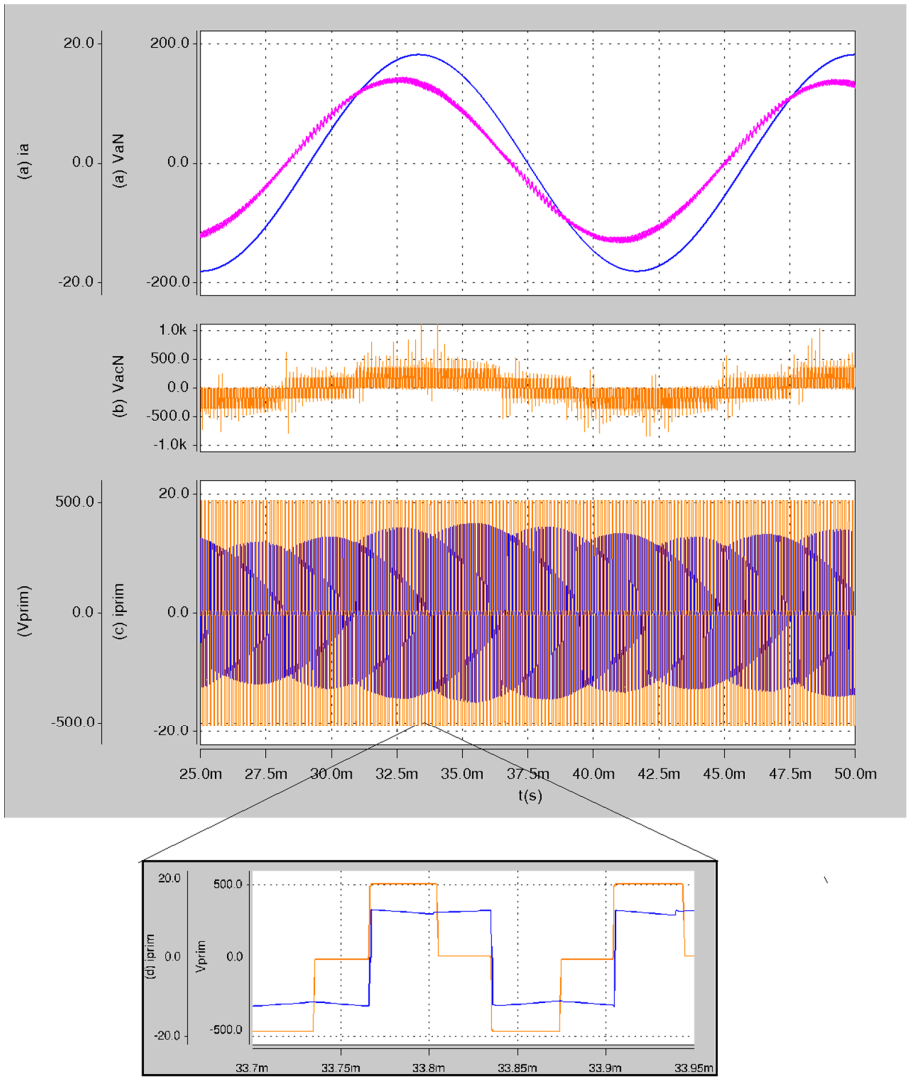

Figure 16. Simulation results (**a**) Supply voltage v_{aN} and line current i_a; (**b**) converter voltage in phase a; and (**c**) High-frequency current and voltage in the primary side of the transformer. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

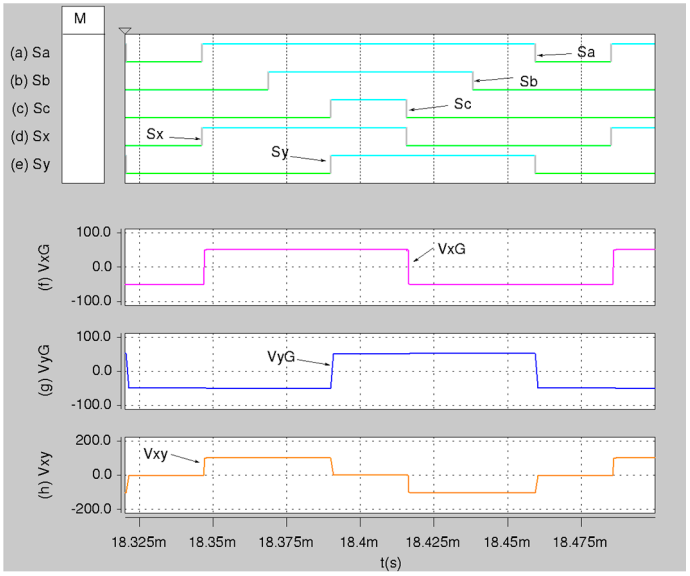

Figure 17. Simulations results: conventional switching states (**a**) S_a, (**b**) S_b and (**c**) S_c; H-bridge switching states (**d**) S_x and (**e**) S_y and voltages (**f**) v_{xG} (**g**) v_{yG} and (**h**) v_{xy}. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

The SVPWM strategy for the divided AC-DC converter of Figure 1b was verified by contrasting a switching cycle of the states S_{am}, S_{bm} and S_{cm} with S_a, S_b and S_c. The upper plot of Figure 18 shows S_a, S_b and S_c together with S_{am}, S_{bm} and S_{cm}; whilst the three-phase input converter voltages with respect to the G node of the DC link, v_{acG}, v_{bcG} and v_{ccG}, are shown in the lower plots of Figure 18 (Figure 18g–i) for straightforward comparison with those plotted in Figure 2. In these plots v_{acG} and v_{ccG} are positive and negative rectified waveforms of v_{xy}; furthermore, v_{bcG} becomes a fully AC waveform due to the state reversals of the matrix converter leg since this switching cell utilizes the active-to-active switching transition.

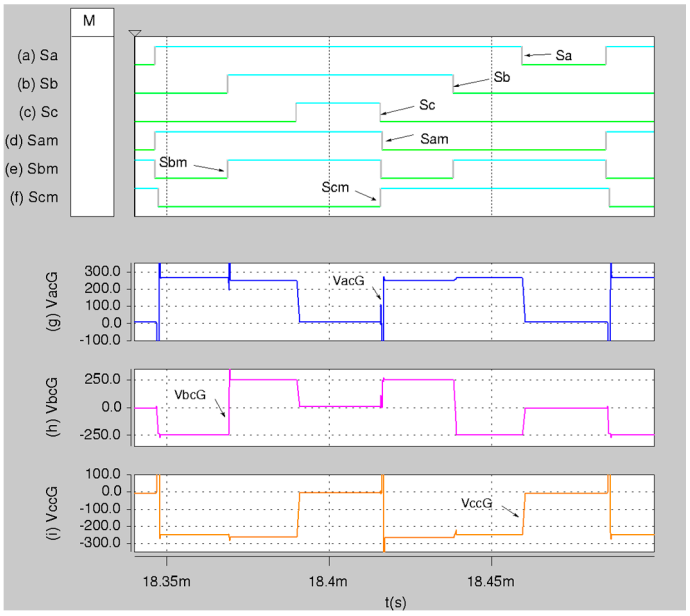

Figure 18. Simulations results: (**a**) conventional switching states S_a; (**b**) S_b; and (**c**) and S_c; (**d**) matrix converter switching states S_{am}; (**e**) S_{bm}; and (**f**) S_{cm}; (**g**) Voltage v_{acG}; (**h**) v_{bcG}; and (**i**) v_{ccG}. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

5.2. ZVT Verification

The effects of the ZVT in the transistors of the matrix converter were initially verified analyzing the quasi-square voltages v_{xy} and v_{sec} together with the transformer secondary current, $i_{sec} = i_{Ls}$, as shown in Figure 19 for direct comparison with Figure 4. In Figure 19a,b, during the first semi cycle, v_{xy} and v_{sec} are clamped to V_o such that i_{Ls} (Figure 19c) has a smooth negative slope; however, this slope becomes positive when the H bridge is in its overlap state to produce a neutral voltage vector at the converter AC input. A expanded portion of the first semi cycle of i_{Ls} is shown in Figure 19d.

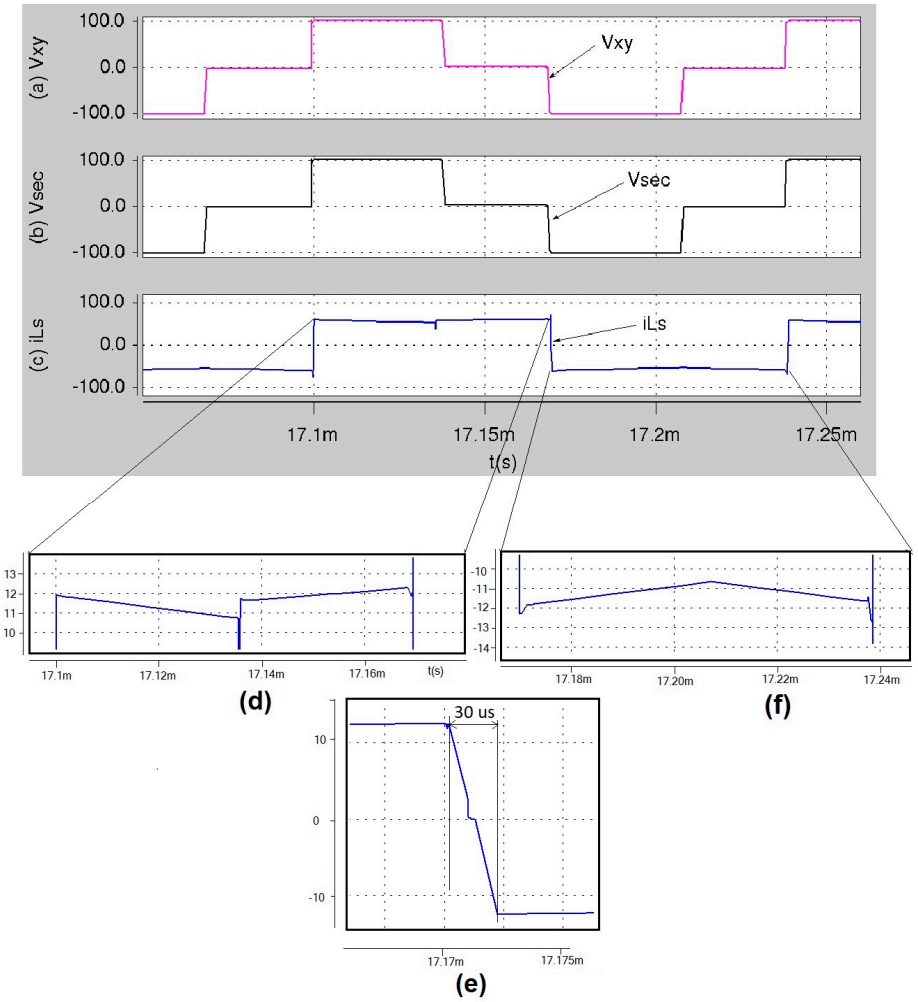

Figure 19. Simulation results: (**a**) voltage v_{xy}; (**b**) v_{sec}; (**c**) current i_{Ls}; (**d**) Expanded portion of the first semicycle; (**e**) expanded portion of T_{ovL}; and (**f**) expanded portion of the second semicycle. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

At the beginning of the second semicycle, i_{Ls} is reversed in an overlap period of $T_{ovL} = 3$ µs, as shown in the expanded portion of Figure 19e, which was confirmed using Equation (3), since v_{xy} and v_{sec} are now clamped to $-V_o$ and zero respectively; whereas the rest of the second semicycle i_{Ls} becomes a mirrored wave of the first, which is shown in the expanded portion of Figure 19f. i_{Ls} is an AC trapezoidal waveform that is shaped by the switched operation of the H bridge and the matrix converter, which needs to be controlled to ensure stability and prevent saturation by the aid of a DC blocking capacitor, or a peak current control [21], since a high-frequency transformer is used in the proposed converter.

A zero-voltage switching transition is achieved in the matrix converter legs due to the zero-voltage biasing of its bidirectional switches whilst i_{Ls} is being reversed. This was verified analyzing the voltage

and current waveforms in the first matrix leg switches Q_1 and Q_4 when an i_{LS} reversal occurs. Figure 20 depicts the simulated switching transition result described in Figure 8 to turn on Q_4 and turn off Q_1.Initially in Figure 20, the switches of Q_1, Q_{1a} and Q_{1b}, and those of Q_4, Q_{4a} and Q_{4b}, are in the on and off states respectively. Later in Figure 20a, Q_{1a} and Q_{4a} have an overlap period that cause to the voltage of Q_4, v_{Q4}, decrease to zero, and then i_{Q4} increases as shown in Figure 20b, achieving a ZVT turn on in Q_4 during the current reversal. Whereas i_{Q4} increases, i_{Q1} falls to set Q_1 to the off state, as shown in Figure 20c, which depicts a hard switch off transition. During the overlap, v_{sec} is clamped to zero and then biased to $-V_o$ at the end of the overlap, whilst the current reversal in i_{Ls} occurs (Figure 20d).

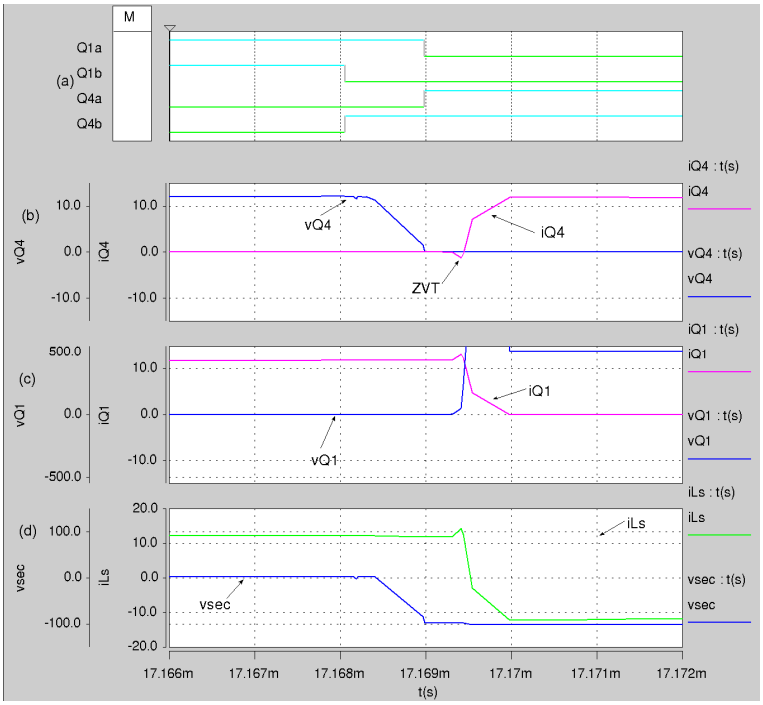

Figure 20. Simulation results to verify ZVT during the switching transition to turn on Q_4, (**a**) control signals Q_{1a}, Q_{1b}, Q_{4a}, Q_{4b}; (**b**) i_{Q4} and v_{Q4}; (**c**) i_{Q1} and v_{Q1}; and (**d**) v_{sec} and i_{Ls}. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

Figure 21a shows the simulated results of the opposite switching transition to turn on Q_1 and turn off Q_4. Mirrored waveforms are obtained for i_{Q1}, i_{Q4}, v_{Q1} and v_{Q4} in contrast to Figure 20. The ZVT is shown in Figure 21b when i_{Q1} becomes positive during the zero voltage in Q_1. v_{sec} is clamped to $+V_o$ whilst i_{Ls} is reversed.

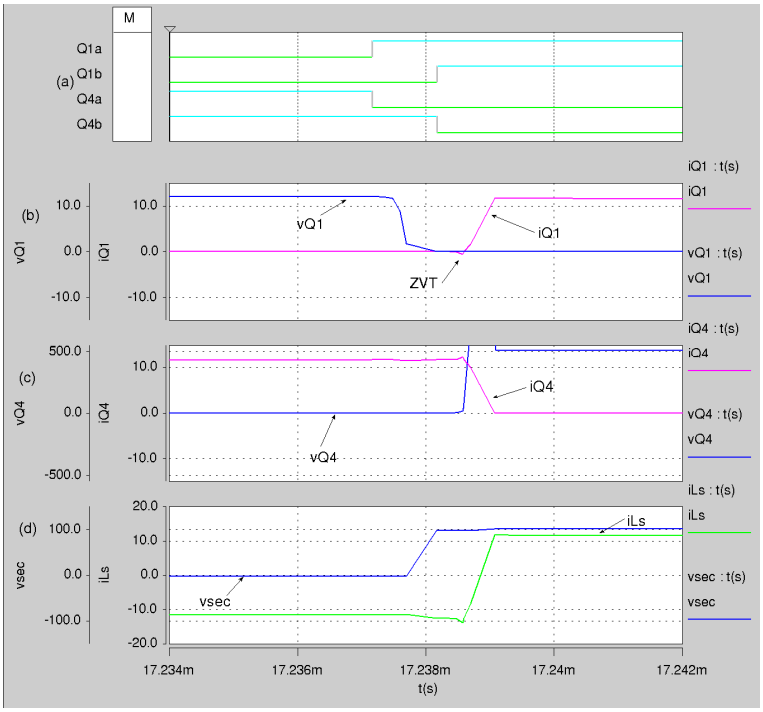

Figure 21. Simulation results to verify ZVT during the switching transition to turn on Q_1, (**a**) control signals Q_{1a}, Q_{1b}, Q_{4a}, Q_{4b}; (**b**) i_{Q1} and v_{Q1}; (**c**) i_{Q4} and v_{Q4}; and (**d**) v_{sec} and i_{Ls}. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

5.3. Steady-State Power Balance Verification

To verify the input-to-output active power balance, the DC output power was calculated by the aid of the H-bridge output current i_{rect}. The current i_{Ls} and i_{rect} are shown in Figure 22a,b, respectively. In these figures i_{Ls} is seen to be rectified by the H bridge since i_{rect} may become either $\pm i_{Ls}$, during the $\pm V_o$ clamping of v_{xy} respectively or zero when the H bridge is in its short-circuit state. The average or i_{rect}, I_{rect}, was calculated using the simulation results shown in Figure 22, and it was found that I_{rect} = 50 A and, therefore, the output power is 5 kW, since the Saber simulation was performed assuming a constant DC output voltage of V_o = 100 Volts. In this fashion, the output power equalizes the active supply power, demonstrating the principle of operation of the AC-DC divided converter of Figure 1b.

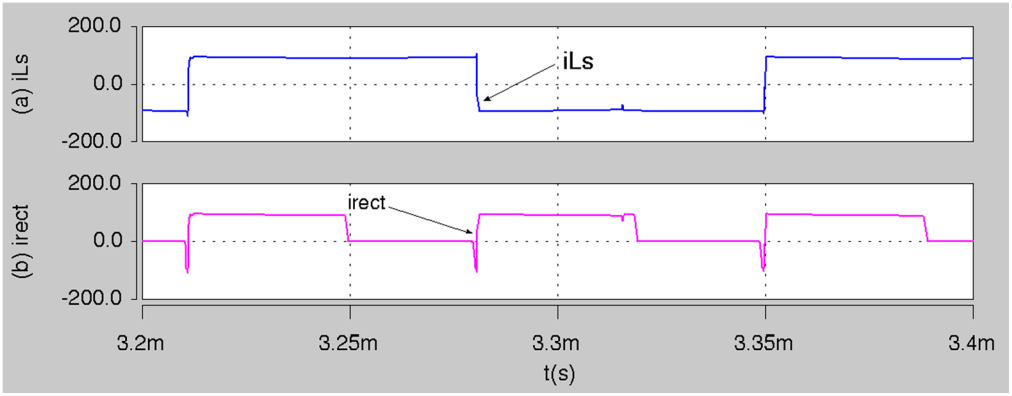

Figure 22. Simulations results for (**a**) i_{Ls}; (**b**) i_{rect}. Supply: 127 V, 60 Hz, Output: 100 V, 5 kW.

To verify the high-quality supply currents the harmonic content in the line current i_a was calculated, as shown in Figure 23; the measured current THD was 4.43%, being the power rated

at 5 kW. Two main current harmonic clusters were found at the harmonic order of n = 242 and n = 488, corresponding to the frequencies of 14.5 kHz and 29.28 kHz, which were increased in amplitude since four switching transitions take place between space vector combinations during a switching period.

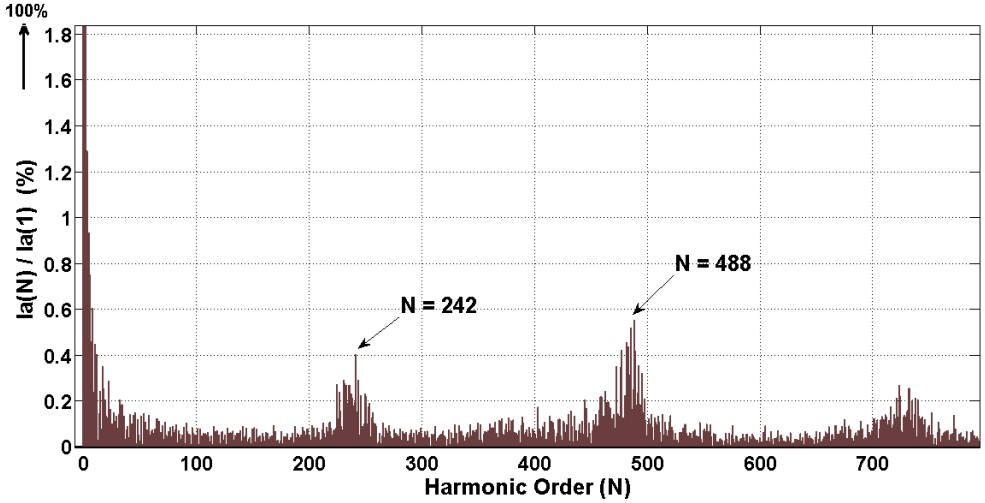

Figure 23. Harmonic content for line current i_a.

The low order harmonic content of the input current was compared with the Standard EN61000-3-2 [22], for the limits of Class A converters. Figure 24 shows that the components are within the standard limits; for example, for n = 3, the amplitude is 0.39 A, 2% of the fundamental, that is less than limit, 2.3 A.

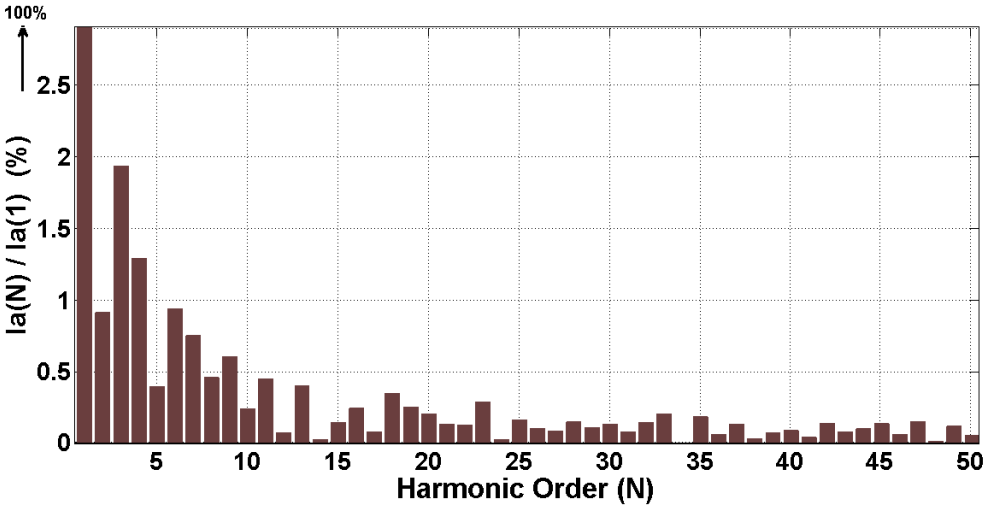

Figure 24. Low Harmonic content for line current i_a for comparison with Standard EN 61000-3-2.

6. Comparison of the Proposed Converter with Other AC-DC Topologies

Table 5 presents a detailed comparison of the proposed topology with four other AC-DC converters of different levels. The first row of this table is referred to the charging power levels for EVs, which are currently three according to the International Electrotechnical Commission standard IEC61851 [23]. Level 1 is for small on-board battery chargers with typical use in home or office; Level 2 is for medium power battery chargers that can be used in private or public outlets, and Level 3 is generally designed for a recharging station for commercial and public transportation. The proposed topology is intended for Level 3 applications, which justifies the use of a three-phase voltage supply.

Table 5. Comparison with three other AC-DC converters.

Factor \ Topology	Proposed AC-DC Modular Converter	Three-Phase PFC Rectifier with DC-DC Converter, [14]	AC-DC Matrix Converter, [14]	Isolated On-Board Vehicle Battery Charger Utilizing SiC Power Devices, [15]	Inductively Coupled Multi-Phase Resonant Wireless Converter, [16]
Level	3	2	2–3	1–2	1
Supply voltage phases	3	3	3	1	1
Switching Devices	16 (4 on board)	12	12	6	6
THD	4.40%	<5%	<1%	4.20%	<5%
Switching losses	Virtual 0 W (ZVT)	241.1 W	165.2 W	0 W (using ZVT)	0 W (using ZVT)
Switching Frequency	7.2 kHz	10 kHz	10 kHz	250 kHz	83–88 kHz
Capability to reverse power flow	Yes	No	Yes	No	No
Possibility to split the converter	Yes	No	No	No	Yes
Output Power	5–20 kW	22.6 kW	20.4 kW	6.1 kW	1 kW
Efficiency	95.8% (estimated)	97.72%	96.80%	94%	93.34%
Total Volume On-Board Converter	1700 cm^3 (Estimated)	8430 cm^3	6668.5 cm^3	1742 cm^3	5250 cm^3 (Estimated)
Power Density	10 kW/dm^3 (Estimated)	3.8 kW/dm^3	4.3 kW/dm^3	5 kW/dm^3	192 W/dm^3 (Estimated)
Advantages over others	Reduces the size of the converter located on-boar the vehicle. The SVPWM together with ZVT generate high-quality sinusoidal currents with null switching losses	Eliminates harmonics, improves the power factor, great simplicity, stable and reliable operation	The volume of the reactive components is reduced. Passive components are not needed in intermediate steps	The switching frequency is increased, the size and weight is reduced	Full-range regulation from zero to full power without switching losses
Major Drawbacks	The efficiency can be reduced by using the transformer	Need to be followed by a step-down DC-DC converter. Passive components are required in intermediate steps	The converter is on-board the vehicle. When the switching devices reach the temperature of 145°, the maximum output power decreases	The conversion is made by three steps with intermediate passive components. Not suitable for high power applications	Not suitable for high power applications. More than transformers are used, increasing the losses

Table 5 shows that the number of switching devices used in the proposed converter is slightly higher in contrast to the topologies described in [14–16]; however, only four of them are located on-board the vehicle. The use of the bidirectional switches in the matrix converter allows the possibility power flow reversal through the converter, being more suitable to future smart grids. The implementation of the proposed AC-DC modular converter is considering the use of high-frequency, nanocrystal magnetic materials for the transformer core. In this fashion, higher power capability may be obtained with distributed gapped cores, such as the used in [15], increasing the efficiency limit by the actual wireless coupling techniques used in actual AC-DC chargers for wireless electric vehicles [22].

7. Conclusions

The splitting of a conventional active rectifier into a matrix converter and an H bridge linked through a high-frequency transformer resulted in an AC-DC modular converter topology ideal for high power density applications. The converter portion on board makes the topology particularly attractive for PEV's; nevertheless, the technique is suitable for other applications. A SVPWM technique with ZVT was proposed for the described converter which allows symmetric generation of virtually square current waves that are attractive for high-frequency wireless transmission of high power.

The topology was verified using a numerical prediction performed in Saber which resulted in high-quality supply currents with a current THD of 4.43%. An input-to-output power balance was verified ensuring reliable power transmission. The high-frequency switching of 7.2 kHz allowed ZVT of the semiconductor devices, since a short overlap period was caused by a simple sequential logic circuitry which aids to the reduction of the switching power losses of typical SVPWM schemes; nevertheless, semiconductor current monitoring is required to obtain correct switching behavior of the matrix converter.

Future aims of research of this topology consider its practical development at higher switching frequencies, allowing further reduction of size and weight, possibility of wireless power transmission, which would be particularly attractive for reliable and risk free charging of electric vehicles. Furthermore, the application of the proposed topology could be examined for other power electronic topologies.

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Author Contributions: Jazmin Ramirez-Hernandez and Ismael Araujo-Vargas developed the principle of operation of the proposed AC-DC converter. The topology of the AC-DC converter was proposed by Marco Rivera. The numerical simulation results were obtained by Jazmin Ramirez-Hernandez using the Synopsis Saber Software, which was validated by Ismael Araujo-Vargas. Furthermore, the paper writing was done by Jazmin Ramirez-Hernandez and revised by Ismael Araujo-Vargas with a technical revision scope of Marco Rivera. All authors were involved and contributed in each part of the article for its final depiction as a research paper.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

C_{z1}, C_{z2}	Zero crossing detector signals
i_a, i_b, i_c	Line current in phase *a*, *b* and *c* respectively
$\boldsymbol{i_L}$	Three-phase line current vector
i_{LS}	Current through the leakage inductance
i_{Q1}, i_{Q4}, i_{Q3}, i_{Q6}	Current through switches Q_1, Q_4, Q_3 and Q_6 respectively
i_{prim}	Current in the primary side of the transformer
i_{sec}	Current in the secondary side of the transformer
I_{primpk}	Peak magnitude of the current in the primary side of the transformer
i_{rect}	H-bridge output current
I_{rect}	Peak magnitude of H-bridge output current

L	Line inductor
L_s	Transformer leakage inductance
M_a	Modulation index
M_{amin}, M_{amax}	Minimum and maximum modulation index variation
n	Transformer turns ratio
P_{in}, P_{out}	Input and output power
P_{omin}, P_{omax}	Minimum and maximum output power variation
PWM_a, PWM_b, PWM_c	Digital signals obtained from the comparison between conventional active periods and a high-frequency carrier triangular waveform
Q_1-Q_6	Bi-directional switches in the matrix converter
Q_a, Q_b, Q_c, Q_d	H-bridge control signals
Q_{1a}, Q_{1b}, Q_{4a}, Q_{4b}	Control signals in the first matrix converter leg
Q_{3a}, Q_{3b}, Q_{6a}, Q_{6b}	Control signals in the second matrix converter leg
R	Output load
S_a, S_b, S_c	Conventional active rectifier switching states
S_a', S_b', S_c'	Intermediate signals to obtain the matrix converter switching states
S_{am}, S_{bm}, S_{cm}	Matrix converter switching states
S_x, S_y	H-bridge switching states
sv_1 to sv_6	Active voltage space vectors
sv_0	Neutral voltage space vector
$\boldsymbol{SQ}_1$ to $\boldsymbol{SQ}_6$	Vector of matrix converter switching states combinations
S_1 to S_6	Sectors in the α-β plane
T	Switching period
T_a, T_b, T_c	Conventional SVPWM active periods
t_D	Overlap period required in the active-to-active switching transition
T_{ovL}	Matrix converter legs overlap period
t_r	Turning off time in the semiconductor devices
T_{SV0H}	Short-circuit period in the H-bridge
T_{SV1}, T_{SV2}, T_{SV4}, T_{SV5}	Active times of the space vectors sv_1, sv_2, sv_4 and sv_5 respectively
v_a, v_b, v_c	Phase a, b and c voltages
v_{acG}, v_{bcG}, v_{ccG}	Matrix converter voltages referred to the G node
v_{cav}	Averaged converter voltage vector
V_{cpk}	Peak magnitude of the averaged converter voltage vector
v_{cavd}, v_{cavq}	Converter d-q-axis voltage
V_{cpkmin}, V_{cpkmax}	Minimum and maximum peak converter voltage variation
v_L	Line inductor voltage vector
V_{Lpk}	Peak magnitude of line inductor voltage vector
V_o	Output voltage
v_{prim}	Voltage in the primary side of the transformer
v_{Q1}, v_{Q4}	Voltages in switches Q_1 and Q_4 respectively
v_{sec}	Voltage in the secondary side of the transformer
v_s	Three-phase source voltage vector
v_{smin}, v_{smax}	Minimum and maximum three-phase source voltage vector variation
V_{spk}	Peak magnitude of the three-phase source voltage vector
V_{spkmin}, V_{spkmax}	Minimum and maximum voltage supply variation
v_{xy}	Voltage generated by the H bridge
v_{xG}, v_{yG}	H-bridge legs voltages referred to the G node
θ_c	Converter operation phase
θ_s	Source phase
φ	Phase between v_s ad v_{cav} vectors
φ_{min}, φ_{max}	Minimum and maximum phase φ variation

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