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An Input-Parallel-Output-Series Switched-Capacitor Three-level Boost Converter with a Three-Loop Control Strategy

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Abstract: There has been increasing interest for industry applications, such as solar power generation, fuel cell systems, and dc microgrids, in step-up dc-dc converters with reduced number of components, low component stress, small input ripples and high step-up ratios. In this paper, an input-parallel-output-series three-level boost (IPOS-SC-TLB) converter is proposed. In addition to achieving the required performance, the input and output terminals can share the same ground and an automatic current balance function is also achieved in the IPOS-SC-TLB converter. Besides, a capacitor voltage imbalance mechanism was revealed and a three-loop control strategy composed of output voltage loop, input current loop and voltage-balance loop was proposed to address the voltage imbalance issue. Finally both simulation and experiment studies have been conducted to verify the effectiveness of the IPOS-SC-TLB converter and the three-loop control strategy.

Keywords: three-level boost; automatic current balance; three-loop; voltage imbalance

1. Introduction

Multilevel step-up dc-dc converters are widely employed in wind farms [1–6], solar power generation systems [7–11], fuel cell systems [12–15], high-power charging stations for electric cars [16,17], and dc microgrids [18–20]. In these systems, a multilevel step-up dc-dc converter helps regulate a varying low-level input voltage to a stable high-level voltage, which usually serves as the dc link voltage of a grid-connected inverter. It is desirable to achieve both low voltage stress and low current stress across components to reduce power losses and save cost. Besides, input current ripple is another important issue that should be considered for these systems, especially for fuel cell or battery storage systems. As multilevel conversion techniques have evolved, many multilevel step-up dc-dc converters have been proposed. In terms of non-isolated multilevel step-up dc-dc converters, the three-level boost converter was firstly proposed and then adopted to combine with a three-level diode-clamped inverter to achieve medium voltage and high power [2,6]. The corresponding four-level boost converter was subsequently proposed to output higher voltage level and higher power [4]. Owing to the interleaved scheme, small input current ripple and low component stress could be easily realized in these multilevel boost converters. However, the input terminal and the output terminal in the two converters do not share the same ground, which can bring in severe EMI problem [7]. One flying-capacitor-based three-level boost converter was proposed to address this problem and good effect has been achieved [12]. However, all these multilevel boost converters face the same inherent limitation, i.e., the voltage gain is limited to be $1/(1-d)$, where d is the duty ratio. Unfortunately, practical considerations limit its output voltage to approximately four times its input voltage. To supply

a high output voltage, it must operate at extremely high duty-cycle whereas extreme duty-cycles impose inefficient small off times. Small off times will cause severe diode reverse-recovery currents, increasing electromagnetic interference (EMI) levels [9].

Another flying-capacitor-based three-level boost converter with intrinsic voltage doubler was proposed in [21,22]. In addition to the advantages of topology described in [8], the two input inductor currents of this converter could be self-balanced due to the flying-capacitor. Moreover, the voltage gain of this converter is $2/(1-d)$ instead of $1/(1-d)$. However, the voltage stresses across the output diode and the output capacitor equals to the output voltage, which is a disadvantage. On the other hand, the voltage stresses across the output diodes could be decreased by half of the output voltage in the converter with two symmetrical flying-capacitors [23]. Nevertheless, one more diode and one more capacitor are necessary, and voltage stress across the output capacitor is still very high. These shortcomings are also presented in the topologies proposed in [24,25]. In general, a list of split capacitors connected in series is a good solution to reducing voltage stress across the output capacitor. One solution is the application of a diode-capacitor voltage multiplier on a classical non-isolated boost converter, which also presents a high voltage gain and self-balanced function for capacitor voltages [26]. However, a large input current ripple and a high current stress across the single switch exist inevitably as no interleaved scheme is adopted in these converters. Modular multilevel dc-dc converter is a good choice for high voltage applications, such as high voltage direct current (HVDC) and high voltage drive areas [27–31]. However, it is not a good choice for medium-voltage applications. Reference [32] proposed a modular multilevel dc-dc converter composed of multiple buck-boost converter modules, which is suitable for medium-voltage and high-power applications. However, the output voltage of the lower module multiplying by $d/(1-d)$ serves as the input voltage of the upper module, to achieve a high voltage gain. The voltage gain is smaller than $2/(1-d)$ and all switches do not share the same ground. Recently, a switched-capacitor technique has begun to be employed in medium-voltage and high-power dc-dc converters with good performance [33–36].

To address the abovementioned issues and to achieve a reduced number of components, low component stress, small input ripples and high step-up ratio, an input-parallel-output-series switched-capacitor three-level boost (IPOS-SC-TLB) converter is proposed in this paper. In addition to achieving the required performance target, the proposed IPOS-SC-TLB converter also has automatic current balancing capability. Compared with the existing three-level boost converters, the proposed converter has the advantages of high voltage gain at full duty cycle range, small component stress, a reduced number of components, common ground for the input and output terminals, and automatic current balancing. All capacitors, diodes, switches only endure half of the output voltage, enabling components with less voltage rating used in the proposed IPOS-SC-TLB converter. Common ground for the input and output terminals not only save power supplies for designing drivers, also helps reduce EMI. Automatic current balancing capability avoid additional current-balance control strategy that is required in a multi-converter system. To address the voltage imbalance issue, a three-loop control strategy composed of an output voltage loop, an input current loop and a voltage-balance loop is developed for the IPOS-SC-TLB converter.

The remainder of the paper is organized as follows: Section 2 introduces the topology derivation and operating principle of the proposed IPOS-SC-TLB converter. Performance analysis is subsequently presented in Section 3 and the three-loop control strategy is given in Section 4. Both simulation and experimental verifications have been done in Section 5 and finally the conclusions of the paper are drawn in Section 6.

2. IPOS-SC-TLB Converter

2.1. Topology Derivation

Until now, interleaved techniques adopted in multilevel dc-dc converters can be divided into two different types: serial-interleaved (SI) techniques (Figure 1a) and parallel-interleaved (PI) techniques

(Figure 1b). As it can be seen, the total components of the two topologies are equal except the numbers of inductors and capacitors. One inductor is necessary in the SI structure while (n − 1) inductors are employed in the PI structure. The SI structure needs (n − 1) capacitors, while one capacitor is necessary in the PI structure.

A comparative analysis between the two techniques are presented in Table 1. On the one hand, (n − 1) voltage levels U_0, U_1, … U_{n-1}, are achieved due to the (n − 1) split capacitors in the SI structure while only one output voltage level U_{n-1} is achieved in the PI structure. On the other hand, the total input current flow through (n − 1) split inductors in the PI structure while through only one inductor in the SI structure. As a result, the SI structure has output voltage divider function and voltage-balance control strategy is necessary to realize voltage balance. The PI structure has input current shunt function and current-balance control strategy is necessary to balance all split inductor currents. All the drive circuits of the switches must be isolated in the SI topology, i.e., (n − 1) isolated drive sources are necessary in the SI structure. However, this drawback does not exist in the PI structure because all the switches share the same ground.

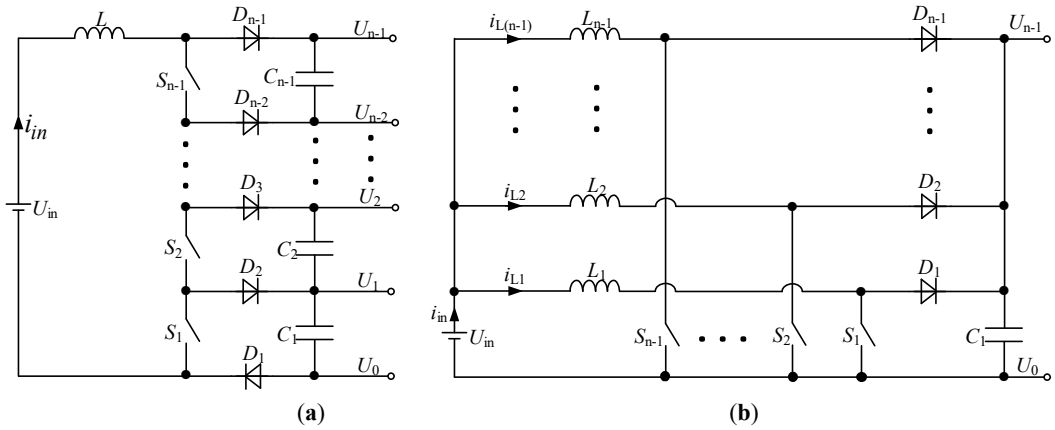

Figure 1. Two interleaved structures: (**a**) SI; (**b**) PI.

Table 1. Comparative analysis between SI and PI topologies.

Structure	Voltage Level	Function	Control
SI	U_0, U_1, … U_{n-1}	Divide voltage	Voltage-balance
PI	U_{n-1}	Shunt current	Current-balance

The conventional three-level boost converter is based on the SI structure in Figure 2a. To distinguish it from other topologies in this paper, the converter in Figure 2a is called SI-TLB. The converter in Figure 2b is named as PIB as it is based on the PI topology. The input terminal and the output terminal of SI-TLB do not share the same ground, which easily results in electromagnetic interference (EMI) problems. Moreover, the voltage stresses across all the components in a PIB converter are high since no multilevel technique is employed.

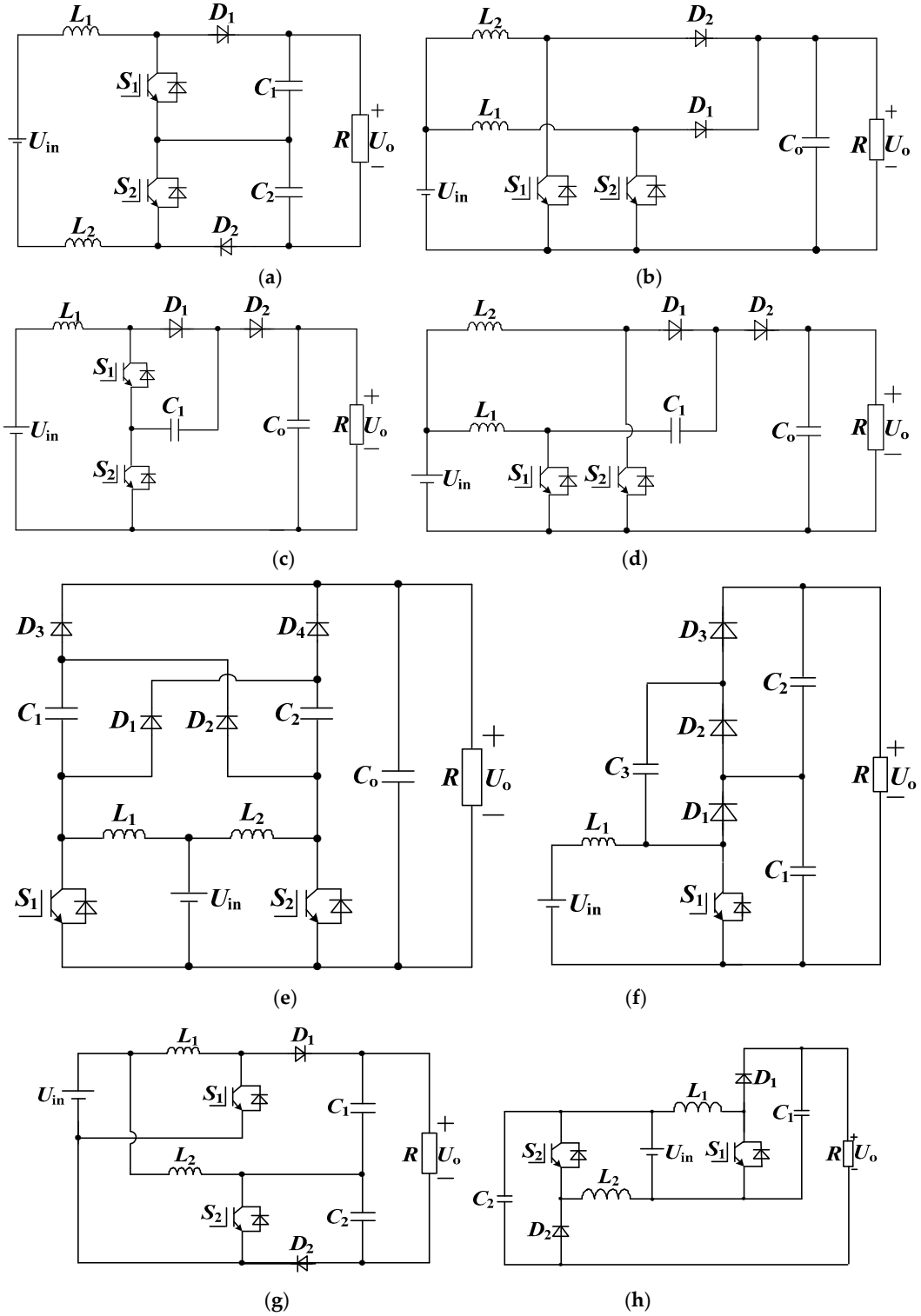

Figure 2. Development of TLB converters: (**a**) SI-TLB; (**b**) PIB; (**c**) SI-FC-TLB; (**d**) PI-FC-TLB; (**e**) PI-SFC-TLB; (**f**) SC-TLB; (**g**) IPOS-TLB1; (**h**) IPOS-TLB2.

To avoid these shortcomings mentioned above, flying-capacitor technique has been introduced into SI-TLB and PIB converters to develop new three-level boost converters. The converter called SI-FC-TLB in Figure 2c is derived by employing one flying-capacitor. The input terminal and the output terminal share the same ground and all switches and diodes are clamped at the half of the output voltage by controlling the voltage of the flying-capacitor C_f to be half of the output voltage [21,22].

However, it can be seen that SI-TLB and SI-FC-TLB both have a limited voltage gain due to the SI structure. Thus, the converter called PI-FC-TLB in Figure 2d was proposed based on PI structure and one flying-capacitor [21,22]. The voltage gain of PI-FC-TLB is as two times as that of SI-TLB and SI-FC-TLB. But the voltage stress across the output diode is high, equal to the output voltage. Also, another converter PI-SFC-TLB based on the PI structure and two symmetrical flying-capacitors in Figure 2e was proposed to reduce the voltage stresses across the output diodes [23]. However, the voltage stress across the output capacitor is still equal to the output voltage and many capacitors and diodes are necessary. As analyzed above, flying-capacitor technique introduced into multilevel boost converters based on SI structure could help solve the problem that input and output terminals do not share the same ground while flying-capacitor technique introduced into multilevel boost converters based on PI structure could help enhance voltage gains. However, there is a common disadvantage among SI-FC-TLB, PI-FC-TLB, and PI-SFC-TLB converters that the output terminal is constructed by only one output capacitor, which not only bears a high voltage stress, but also does not help reduce the voltage stress across output diodes and output capacitors. Additionally, the voltage-balance control is not easy to realize as one or more flying-capacitor voltages should be control independently. Even though the output capacitor can be replaced by two split capacitors in series in the output terminal, the two split capacitors could not be self-balanced and could not be controlled by voltage-balance control strategy either. On the other hand, a three-level boost converter based on switched-capacitor network is proposed in [26]. For simplification, the converter is name as SC-TLB, which not only has two split capacitors at the output terminal, but also has self-balancing function for capacitor voltages. As a result, there is no need to employ any voltage-balance control strategies to solve the voltage imbalance issue. However, as analyzed in Section 1, there is a big disadvantage that SC-TLB has high input current and high input current ripple since no interleaved structures are employed. As a result, high power losses are inevitable in the SC-TLB converter.

There are also two input-parallel-output-series (IPOS) boost converters shown in Figure 2g (called by IPOS-TLB1) and Figure 2h (called by IPOS-TLB2) from references [24,25]. Like the ISOS-TLB converter, the input terminal and the output terminal do not share the same ground and the voltage stress across diode D_1 is equal to the output voltage in the IPOS-TLB1 converter. Although the topology IPOS-TLB2 is simple, its voltage gain is smaller than the other topologies and the input terminal and the output terminal do not share the same ground, either.

According to the comparative analysis mentioned above, the SI structure is suitable for high input voltage and high output voltage applications while the PI structure is suitable for high input current and high output current applications. As shown in Figure 1, the input terminal, output terminal and all switches share the same ground in the PI topology. The flying-capacitor technique helps enhance the voltage gains of the converters based on the PI structure. Besides, the switched-capacitor technique, which could be deemed as an extension of flying-capacitor technique, not only increases the voltage gain, but also brings a self-balancing function for capacitor voltages. On the whole, there are three techniques could be employed in multilevel dc/dc converters, i.e., interleaved technique, flying-capacitor technique, and switched-capacitor technique. Until now, only one or two of the three techniques were employed in a single power converter.

This paper proposes an IPOS-SC-TLB converter in Figure 3 and presents a detailed analysis of the converter. IPOS-SC-TLB combines the parallel-interleaved technique, flying-capacitor technique, and switched-capacitor technique together. In Figure 3, L_1, L_2, S_1, S_2 formulate the PI structure, while L_1, S_1, D_1, C_1 form Boost I and L_2, S_2, D_3, C_2 form Boost II. Besides, C_f, D_2 and S_2, C_1 formulate a switched-capacitor network, which makes the two input terminals in parallel and the output terminals in series for Boost I and Boost II.

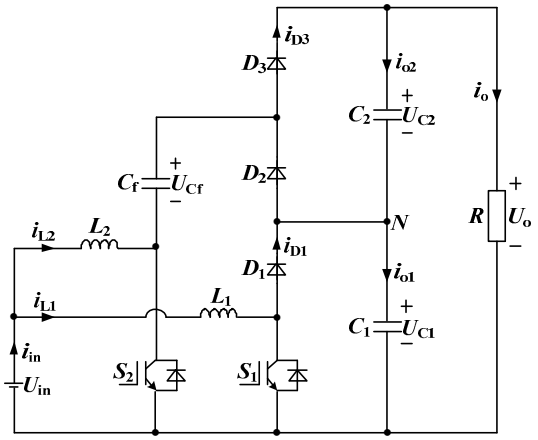

Figure 3. The proposed IPOS-SC-TLB converter.

2.2. Operating Principle

In the IPOS-SC-TLB converter, all the inductors, capacitors, switches, diodes have the same respective parameters, i.e.,

$$L_1 = L_2 = L \tag{1}$$

$$C_1 = C_2 = C \tag{2}$$

Considering the voltage drops of IGBT and diode, and the equivalent series resistor of inductor, the equivalent circuits of the IPOS-SC-TLB converter are presented in Figure 4. In the interleaved scheme, the operating stages of IPOS-SC-TLB could be divided into two modes according to duty cycle: when d is greater than 0.5 and when d is smaller than 0.5.

(1) When the duty cycle d is greater than 0.5, the IPOS-SC-TLB operates at the periodic stages of I, II, I, and III.

Stage I: Both switches S_1, S_2 are turned on and the diode D_2 is forward biased as the capacitor voltage U_{C1} is still a little bigger than the capacitor voltage U_{Cf} after the stage III. During Stage I, both the two inductors L_1, L_2 are charged by the input source U_{in}. Thus, there are:

$$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = U_{in} - I_{L1} r_L - U_S \tag{3}$$

$$U_{C1} = U_{Cf} + U_S + U_D \tag{4}$$

As the two capacitor voltages U_{C1}, U_{Cf} are charged in parallel, the voltage differences between U_{C1} and U_{Cf} are small but cannot be ignored. As a result, the current flowing through D_2 caused by the small voltage difference is labelled as I_1. The current flowing through S_1 is equal to i_{L1} while the current flowing through S_2 is the sum of i_{L2} and I_1.

Stage II: When the switch S_1 is turned on and the switch S_2 is turned off, the diode D_3 is forward. The inductor L_1 is still charged by the input source U_{in}, which also supplies energy to the load together with the inductor L_2 and the flying-capacitor C_f. Thus, there are:

$$L_1 \frac{di_{L1}}{dt} = U_{in} - I_{L1} r_L - U_S \tag{5}$$

$$L_2 \frac{di_{L2}}{dt} = U_{in} + U_{Cf} - U_D - U_{C2} - U_{C1} \tag{6}$$

According to (4) and (6), there is:

$$L_2 \frac{di_{L2}}{dt} = U_{in} - U_{C2} - U_S - 2U_D \tag{7}$$

During Stage II, the capacitor voltage U_{Cf} decreases while the capacitor voltage U_{C1} increases. As a result, the voltage difference between U_{C1} and U_{Cf} becomes bigger and bigger and finally reaches its maximum at the end of Stage II. The current flowing through the switch S_1 is still equal to i_{L1} while no currents flows through the switch S_2 and the diode D_2 during this stage.

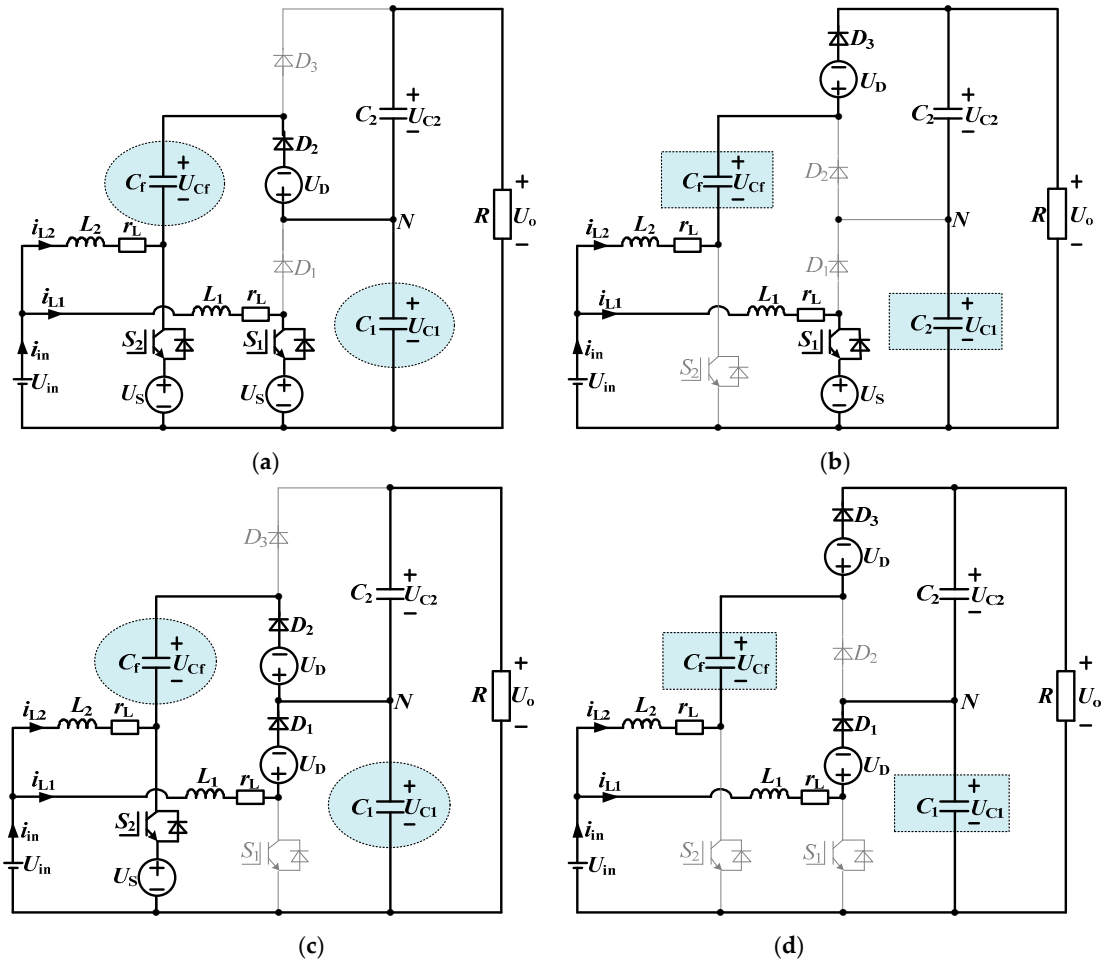

Figure 4. Equivalent circuits of the IPOS-SC-TLB converter: (**a**) stage I; (**b**) stage II; (**c**) stage III; (**d**) stage IV.

Stage I: The converter repeats Stage I and the same output results could be achieved like (3) and (4). However, as analyzed in Stage II, the voltage difference between U_{C1} and U_{Cf} reaches its maximum value, the current flowing through the diode D_2 reaches its maximum value, labelled as I_2. The current flowing through S_1 turns to be the same as i_{L1} again while the current flowing through S_2 is the sum of i_{L2} and I_2.

Stage III: When the switch S_1 is turned off while the switch S_2 is turned on, the diodes D_1, D_2 are both forward. The inductor L_2 is charged by the input source U_{in}, which also supplies energy to C_1 and C_f together with the inductor L_1. Thus, there are:

$$L_1 \frac{di_{L1}}{dt} = U_{in} - I_{L1} r_L - U_D - U_{C1} \tag{8}$$

$$L_2 \frac{di_{L2}}{dt} = U_{in} - I_{L1} r_L - U_S \tag{9}$$

During Stage III, the two capacitors C_1, C_f are connected in parallel and thus the voltage difference between them is small, which results in a small current flowing through the diode D_2. It has been

mentioned in the first Stage I, labelled as I_1. As a consequence, the current flowing through S_1 turns to be zero while the current flowing through S_2 is the sum of i_{L2} and I_1.

(2) When the duty cycle d is smaller than 0.5, the IPOS-SC-TLB converter operates at the periodic stages of IV, II, IV, and III.

Stage IV: Both switches S_1, S_2 are turned off while D_1 and D_3 are on forward biased:

$$L_1\frac{di_{L1}}{dt} = U_{in} - I_{L1}r_L - U_D - U_{C1} \tag{10}$$

$$L_2\frac{di_{L2}}{dt} = U_{in} + U_{Cf} - U_D - U_{C2} - U_{C1} = U_{in} - U_{C2} - U_S - 2U_D \tag{11}$$

As the first Stage IV begins after Stage III, the capacitor voltage U_{Cf} decreases while the capacitor voltage U_{C1} increases. During this stage, no currents pass through the two switches S_1, S_2 and the diode D_2 as they are all switched off.

Stage II: The same results could be achieved like (5)–(7) and the voltage difference between U_{C1} and U_{Cf} continues increasing during this stage. The current flowing through the switch S_1 is still equal to i_{L1} while no currents flows through the switch S_2 and the diode D_2 during this stage.

Stage IV: The converter enters into another Stage IV, where the voltage difference between U_{C1} and U_{Cf} continues increasing and reach its maximum value at the end of the stage. And no currents no currents pass through the two switches S_1, S_2 and the diode D_2.

Stage III: At the beginning of the stage III, the current flowing through the diode D_2 reaches its maximum value I_2. But later becomes a smaller value I_1 as the two capacitors C_1, C_f are charged in parallel. Thus, the current flowing through the switch S_1 is zero while the current flowing through the switch S_2 is the sum of i_{L2} and I_2 and then the sum of i_{L2} and I_1 during this stage. For any duty cycle d, two equations can be attained based on Voltage-Second Balance Principle during one switching period:

$$dT_s(U_{in} - I_{L1}r_L - U_S) + (1-d)T_s(U_{in} - I_{L1}r_L - U_D - U_{C1}) = 0 \tag{12}$$

$$dT_s(U_{in} - I_{L2}r_L - U_S) + (1-d)T_s(U_{in} - U_{C2} - U_S - 2U_D) = 0 \tag{13}$$

During the switching period, the output voltage of the converter is always described by:

$$U_o = U_{C1} + U_{C2} \tag{14}$$

According to (28), there is:

$$I_{L1} = I_{L2} = \frac{U_o}{R(1-\mathrm{d})} \tag{15}$$

Therefore, the voltage gain G and the capacitor voltages could be derived by:

$$G = \frac{U_o}{U_{in}} = \frac{2 + \frac{(2\mathrm{d}-3)U_D - U_S}{U_{in}}}{1 - \mathrm{d} + \frac{r_L(1+\mathrm{d})}{R(1-\mathrm{d})}} \tag{16}$$

The capacitor voltages are calculated by:

$$\begin{cases} U_{C1} = \frac{U_{in} - I_{L1}r_L - U_D}{1-d} \\ U_{C2} = \frac{U_{in} - dI_{L2}r_L - U_S + (2\mathrm{d}-2)U_D}{1-d} \\ U_{Cf} = \frac{U_{in} - I_{L1}r_L - (1-\mathrm{d})U_S - (2-\mathrm{d})U_D}{1-d} \end{cases} \tag{17}$$

When the parasitic parameters are ignored, there are:

$$\begin{cases} G = \frac{2}{1-d} \\ U_{C1} = U_{C2} = U_{Cf} = \frac{1}{2}U_o \end{cases} \tag{18}$$

3. Performance Analysis

3.1. Component Stress

According to the analysis mentioned above, the key voltage waveforms of the IPOS-SC-TLB converter are presented in Figure 5. The voltage stresses across all switches, diodes and capacitors are half of the output voltage:

$$U_{S1} = U_{S2} = U_{D1} = U_{D2} = U_{D3} = U_{C1} = U_{C2} = U_{Cf} = \frac{1}{2}U_o \tag{19}$$

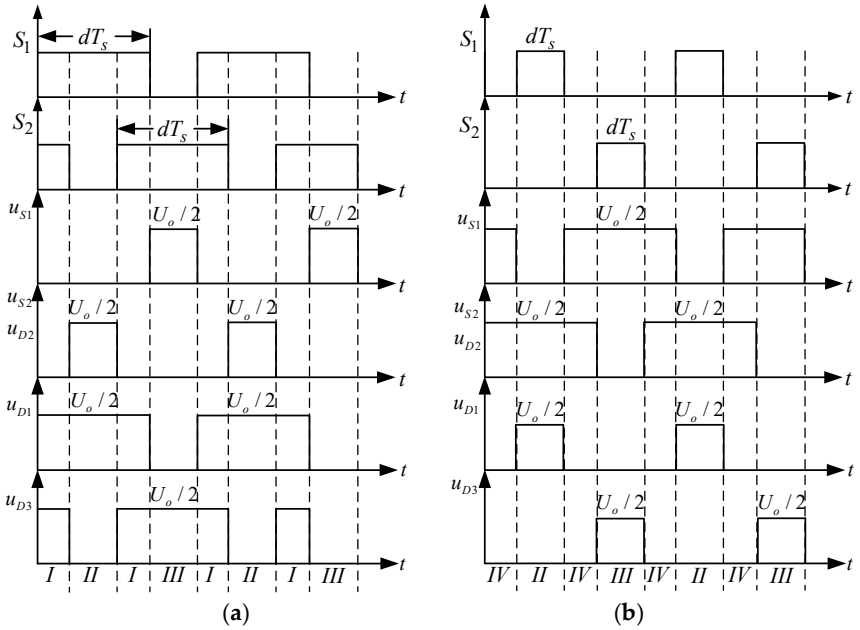

Figure 5. Key voltage waveforms: (**a**) $d > 0.5$; (**b**) $d \leq 0.5$.

The current waveforms of the IPOS-SC-TLB converter are presented in Figure 6. From Figure 6, whatever the duty cycle d is, the average current across S_1, S_2 can be obtained as follows:

$$\begin{cases} I_{S1} = dI_{L1} \\ I_{S2} = I_{L2} \end{cases} \tag{20}$$

The average currents across D_1, D_2, D_3 identical with value equal to the average output current are determined as follows:

$$I_{D1} = I_{D2} = I_{D3} = I_o = \frac{U_o}{R} \tag{21}$$

When the duty cycle d is over 0.5, the operating period of Stage II in Figure 4b can be expressed by $(1-d)T_s$ during one switching period. During Stage II, the capacitor C_2 is charged with the current expressed by:

$$i_{C2\_charged} = I_{L2} - \frac{U_o}{R} \tag{22}$$

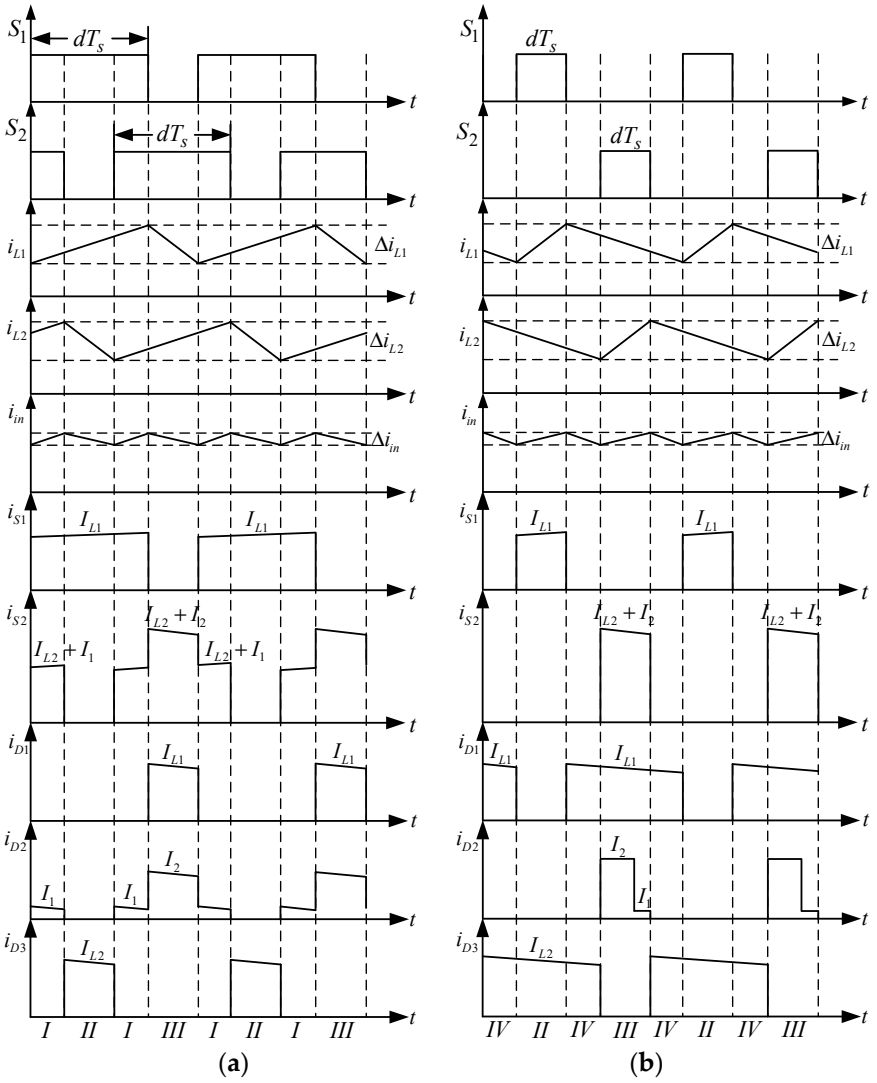

Figure 6. Key current waveforms: (**a**) $d > 0.5$; (**b**) $d \leq 0.5$.

During the remained operating period dT_s, C_2 is discharged with the current expressed by:

$$i_{C2\_discharged} = -\frac{U_o}{R} \tag{23}$$

According to Ampere-Second Balance Principle, there is:

$$(1-d)T_s(I_{L2} - \frac{U_o}{R}) + dT_s(-\frac{U_o}{R}) = 0 \tag{24}$$

We can obtain the average current of inductor L_2 by simplifying (24) as below:

$$I_{L2} = \frac{U_o}{R(1-d)} \tag{25}$$

When the duty cycle is smaller than 0.5, the same formula as (25) can be obtained. It should be noted that the average current of inductor L_2 could be also derived as below. During one whole switching period, the average charging current flowing through C_f is the same as the average current flowing through D_2. So the increased charges of C_f during one switching period is I_{D2}*T_s. In addition, when d is over 0.5, the flying-capacitor C_f is only discharged during Stage II and the average discharging current flowing through C_f is I_{L2} with the discharging time $(1-d)T_s$. When d is smaller than 0.5,

the flying-capacitor C_f is discharged during Stage II and Stage IV with the average discharging current I_{L2} and the total discharged time $(1-d)T_s$. It can be seen that the decreased charges of C_f during one switching period is I_{L2}*$(1-d)T_s$ no matter what the duty cycle d is. Therefore, by applying Ampere-Second Balance Principle on C_f, we have:

$$I_{D2} * T_s = I_{L2} * (1-d)T_s \tag{26}$$

According to (26), the same formula as (25) can be achieved. On the other hand, the average current of L_1 can be easily obtained as below:

$$I_{L1} = \frac{I_{D1}}{1-d} = \frac{U_o}{R(1-d)} \tag{27}$$

According to (20)–(27), the average currents across all switches and diodes are:

$$\begin{cases} I_{L1} = I_{L2} = \frac{U_o}{(1-d)R} \\ I_{S1} = \frac{dU_o}{(1-d)R} \\ I_{S2} = \frac{U_o}{(1-d)R} \\ I_{D1} = I_{D2} = I_{D3} = \frac{U_o}{R} \end{cases} \tag{28}$$

3.2. Switched-Capacitor Network

For two typical boost converters, their input terminals cannot be simply connected in parallel and while their output terminals are connected in series simultaneously. The flying-capacitor C_f and the diode D_2 in the proposed IPOS-SC-TLB converter are used to realize the input-parallel output-series topology. Because a switched-capacitor network is constructed and it helps support the output voltage of the Boost I for the Boost II. As shown in Figure 4, the flying-capacitor C_f is clamped with the capacitor C_1 during Stage I and Stage III, labelled as the oval areas, i.e., the two capacitor voltages are identical. During Stage II and Stage IV, the flying-capacitor C_f serves as the voltage support for the Boost II. So, it could be thought of as that the output capacitor C_2 is charged by the input source because the capacitor voltage U_{Cf} offsets the capacitor voltage U_{C1}, which are labelled as the rectangular areas. Furthermore, it can be seen from (26) that the flying-capacitor C_f could automatically balance the average currents of the two inductors L_1 and L_2. Thus, the IPOS-SC-TLB converter does not need any current-balance circuit or current-balance control strategy that is required in the conventional parallel-interleaved dc/dc converters.

3.3. Ripple Analysis

In the switched-capacitor network, the flying-capacitor C_f could be served as an energy buffer. According to (26) and (27), the increased or decreased charges on C_f is U_o*T_s/R, which could be described by another way of C_f*Δu_{Cf}, where Δu_{Cf} represents the voltage ripple of C_f. Finally, the voltage ripple of C_f is derived by:

$$\Delta u_{Cf} = \frac{U_o}{RC_f f_s} \tag{29}$$

Besides, it is easy to attain the voltage ripples of C_1 and C_2:

$$\Delta u_{C1} = \Delta u_{C2} = \frac{U_o d}{RCf_s} \tag{30}$$

Additionally, the current ripples of L_1 and L_2 could be obtained by:

$$\Delta i_{L1} = \Delta i_{L2} = \frac{U_{in}}{L}\frac{d}{f_s} \tag{31}$$

The input current ripple can be calculated by:

$$\Delta i_{in} = \begin{cases} \frac{U_{in}}{L}\frac{2d-1}{f_s} d > 0.5 \\ \frac{U_{in}}{L}\frac{d(1-2d)}{f_s(1-d)} d \leq 0.5 \end{cases} \quad (32)$$

3.4. Inrush Current Suppression

In practical application, IGBT and diode usually have some voltage drops and capacitors has equivalent serial resistors. Thus, it is inevitable to see some voltage differences between C_1 and C_f, which can be described by:

$$\Delta U = U_{C1} - U_{Cf} = U_S + U_D \quad (33)$$

U_D and U_S are assumed to be the voltage drop of one diode and the voltage drop of one IGBT. Figure 7 shows the equivalent circuit of the switched-capacitor network when S_2 turns on.

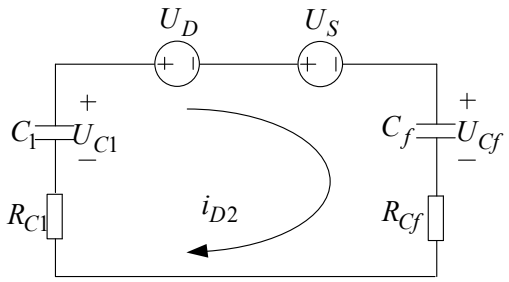

Figure 7. Equivalent circuit of the switched-capacitor network.

It can be seen that the output capacitor C_1 is connected with the flying-capacitor C_f in parallel. R_{C1}, R_{Cf} means the equivalent serial resistors of C_1 and C_f, respectively. The current i_{D2} flowing through the diode D_2 could be calculated by:

$$i_{D2} = \frac{\Delta U}{R_{C1} + R_{Cf}} \quad (34)$$

In (34), the equivalent serial resistors R_{C1}, R_{Cf} are usually very small, which are in the range of milliohms. As a result, although ΔU is small, it may bring in very high inrush current i_{D2} flowing the switched-capacitor network when S_2 is turned on and D_2 is forward instantaneously. Moreover, this will result in more conduction losses across the switch S_2 and the diode D_2.

From (10), one way to suppress i_{D2} is to reduce the voltage difference ΔU is by using wide bandgap semiconductors, such as SiC or GaN components that have smaller voltage drops compared with Si-based components. However, ΔU cannot be reduced to zero and this may still bring in a certain inrush current. Another method is to increase the impedance of the switched-capacitor network. Placing a serial resistor with high resistance could increase the impedance but extra power losses are produced. As shown in Figure 8, this paper proposes to put a small stray inductor L_s together with D_2. In this way, the loop impedance is increased by $2\pi f_s L_s$ and then the inrush current i_{D2} is reduced to:

$$i_{D2} = \frac{\Delta U}{2\pi f_s L_s + R_{C1} + R_{Cf}} \quad (35)$$

3.5. Comparative Analysis

Comparative analyses of SC-TLB, SI-TLB, SI-FC-TLB, PI-FC-TLB and the proposed IPOS-SC-TLB are presented in Table 2. *L*, *S*, *D*, and *C* represent the quantities of inductors, switches, diodes and capacitors, respectively. *DS* means the quantity of driver supplies and *G* means the voltage gains. Besides, U_{VPS}, U_{VPD}, and U_{VPC} respectively represent the voltage stresses across switches, diodes, capacitors; and I_{VPS1}, I_{VPS2}, and I_{VPD} represent the average current across switches S_1, S_2 and diodes,

respectively. "Self-balance" means the input inductor currents could be self-balanced and "same ground" means the input terminal and the output terminal share the same ground. In addition, the voltage gain comparison curves are presented in Figure 9.

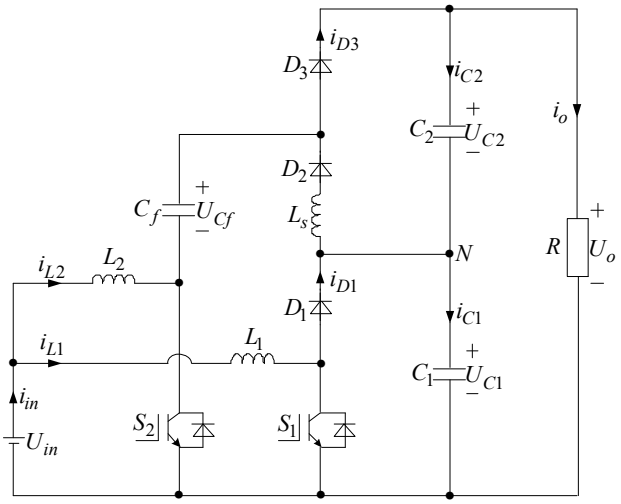

Figure 8. IPOS-SC-TLB with a small stray inductor L_s.

Among these seven TLB converters, the common performance parameters are the voltage stress across switches and the input current ripple. The TLB converters based on SI structure need two isolated drive power supplies and have a low voltage gain, while those TLB converters based on PI structure need only one power supply and show a higher voltage gain. The SI-FC-TLB and PI-FC-TLB are very similar except for different interleaved structures. From these two converters, it could be seen that the voltage stresses across the output diodes are low in the SI structure while high in the PI structure; and the average current stresses across switches are high in the SI structure while low in the PI structure. The smaller average current stress across switches should be attributed to the PI structure. Among the five converters, the quantity of components are not the most in the proposed IPOS-SC-TLB, and high voltage gain, small voltage stress and small current stress are achieved. Moreover, voltage-balance control could be easily achieved with the input terminal and the output terminal sharing the same ground. In other words, the proposed IPOS-SC-TLB converter integrates nearly all the merits of the other four TLB converters. However, there is also a disadvantage that the imbalance current between the two power switches S_1, S_2. As analyzed in Equation (28), the average current of S_2 is U_o/R higher than the average current of S_1.

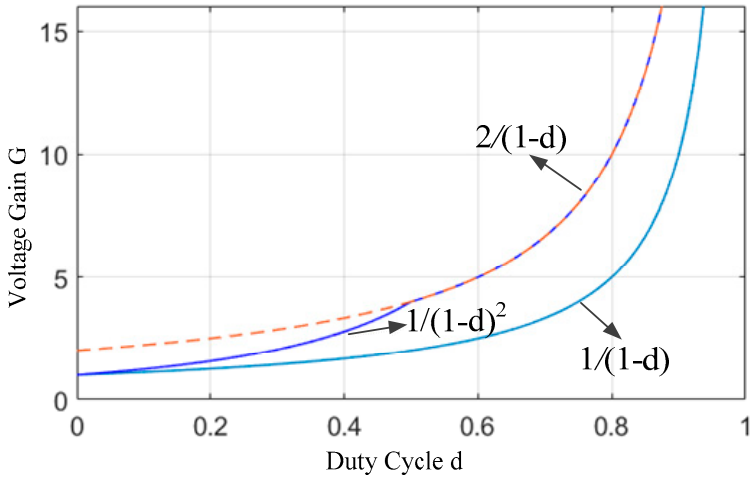

Figure 9. Voltage gain comparison.

Table 2. Comparative analysis among SC-TLB, SI-TLB, SI-FC-TLB, PI-FC-TLB, SC-TLB and the proposed IPOS-SC-TLB.

Topology	L	S	D	C	DS	G ($d \leq 0.5$)	G ($d > 0.5$)	U_{VPS}	U_{VPD}	U_{VPC}	I_{VPS1}	I_{VPS2}	I_{VPD}	Current Ripple	Self-Balance	Same Ground
SC-TLB	1	1	3	3	1	$2/(1-d)$		$0.5U_o$	$0.5U_o$	$0.5U_o$	dI_{in}	-	I_o	Large	Yes	Yes
SI-TLB	2	2	2	2	2	$1/(1-d)$		$0.5U_o$	$0.5U_o$	$0.5U_o$	dI_{in}	dI_{in}	I_o	Small	No	No
SI-FC-TLB	2	2	2	2	2	$1/(1-d)$		$0.5U_o$	$0.5U_o$	$0.5U_o$	dI_{in}	dI_{in}	I_o	Small	No	Yes
PI-FC-TLB	2	2	2	2	1	$1/(1-d)^2$	$2/(1-d)$	$0.5U_o$	U_o	U_o	$0.5dI_{in}$	$0.5dI_{in}$	I_o	Small	Yes	Yes
PI-SFC-TLB	2	2	4	3	1	$2/(1-d)$		$0.5U_o$	U_o	U_o	$(1+d)I_{in}/4$	$(1+d)I_{in}/4$	$0.5I_o$	Small	Yes	Yes
IPOS-TLB1	2	2	2	2	1	$1/(1-d)^2$	$2/(1-d)$	$0.5U_o$	U_o	$0.5U_o$	$0.5dI_{in}$	$0.5dI_{in}$	I_o	Small	No	Yes
IPOS-TLB2	2	2	2	2	2	$(1+d)/(1-d)$		$U_o/(1+d)$	$U_o/(1+d)$	$U_o/(1+d)$	$0.5dI_{in}$	$0.5dI_{in}$	I_o	Small	No	No
Proposed	2	2	3	3	1	$2/(1-d)$		$0.5U_o$	$0.5U_o$	$0.5U_o$	$0.5dI_{in}$	$0.5I_{in}$	I_o	Small	Yes	Yes

4. Three-Loop Control Strategy

4.1. Voltage Imbalance Mechanism

η_1, η_2 are labelled as the conversion efficiencies of Boost I and Boost II, respectively. Thus, there is:

$$\begin{cases} \eta_1 U_{in} I_{L1} = U_{C1} I_{D1} \\ \eta_2 U_{in} I_{L2} = U_{C2} I_{D3} \end{cases} \tag{36}$$

As the output terminals of Boost I and Boost II are connected in series, the two Boost modules have the same output current. As the average currents across C_1 and C_2 are both equal to zero during one switching period, there is:

$$I_{D1} = I_{D3} \tag{37}$$

In addition, the power losses of D_2 and S_2 produced in the switched-capacitor network are small but could not be ignored. But the power losses should be attributed to the Boost II as D_2 and S_2 help formulate the Boost II. As a result, there is:

$$\eta_1 > \eta_2 \tag{38}$$

Based on (36)–(38), we have:

$$U_{C1} > U_{C2} \tag{39}$$

As analyzed above, the two split inductor currents could be self-balanced, but the two output capacitor voltages could not be self-balanced. Considering the voltage drops of IGBT and diode, the voltage difference between C_1 and C_2 could be described by the sum of the voltage drop of one IGBT and the voltage drop of one diode. Besides, the parasitic resistances of L_1 and L_2 are labelled as r_{L} and the parasitic resistance of C_f is labelled as r_{Cf}. As the average currents across L_1 and L_2 are high, the voltage drops of parasitic resistances are large and could not be ignored. Under this condition, the two output capacitor voltages could be rewritten as:

$$U_{C1} = \frac{1}{1-d}(U_{in} - I_{L1} r_L) - U_D \tag{40}$$

$$U_{C2} = \frac{1}{1-d}[U_{in} - I_{L2}(r_L + r_{Cf})] - \Delta U - U_D \tag{41}$$

The two split inductors are designed to attain the same parameters. Owing to the automatic balanced inductor currents, the voltage difference between C_1 and C_2 could be described by:

$$\Delta U = U_{C1} - U_{C2} = \frac{I_{L2} r_{Cf}}{1-d} + \Delta U \tag{42}$$

Considering (15)–(42) is further simplified as:

$$\Delta U = U_{C1} - U_{C2} = \frac{I_{L2} r_{Cf} + \Delta U_{SC}}{1-d} = \frac{I_{in} r_{Cf}}{2(1-d)} + U_S + U_D \tag{43}$$

It can be seen from (43) that the voltage imbalance issue is related to the output characteristic and the parasitic parameters, including the average input current I_{in}, the duty cycle d, the equivalent series resistance r_{Cf} of the flying-capacitor, and the voltage drops of IGBTs and diodes. The capacitances of the two output capacitors have no effect on the voltage imbalance issue, which is quite different from the conventional three-level boost converter shown in Figure 2a.

4.2. Three-Loop Control Strategy

To address the voltage imbalance issue and to achieve stale operation of the IPOS-SC-TLB converter, a three-loop control strategy including an output voltage loop, an input current loop and a voltage-balance loop is proposed in this section. The voltage loop and the current loop respectively controls the output voltage and the input inductor currents, while the voltage-balance loop helps alleviate the voltage imbalance issue. However, the voltage loop and the voltage-balance loop will influence each other if no decoupling scheme is employed. To decouple the output voltage loop and the voltage-balance loop, the derivation analysis has been done as follows.

Duty cycles d_1, d_2 in (44) are both composed of the common duty cycle d and the voltage-balance duty cycles Δd_1, Δd_2. Also, I_{L1}, I_{L2} in (45) are both composed of the average inductor current I_L and the voltage-balance inductor current ΔI_{L1}, ΔI_{L2}:

$$\begin{cases} d_1 = d + \Delta d_1 \\ d_2 = d + \Delta d_2 \end{cases} \tag{44}$$

$$\begin{cases} I_{L1} = I_L + \Delta I_{L1} \\ I_{L2} = I_L + \Delta I_{L2} \end{cases} \tag{45}$$

In the IPOS-SC-TLB converter, the relationship of the input inductor currents and the output current could be described by:

$$\begin{cases} (1 - d_1) I_{L1} = I_o \\ (1 - d_2) I_{L2} = I_o \end{cases} \tag{46}$$

By substituting (44) and (45) into (46), there is:

$$\begin{cases} (1 - d)\Delta I_{L1} - \Delta d_1 I_L = \Delta I_o \\ (1 - d)\Delta I_{L2} - \Delta d_2 I_L = \Delta I_o \end{cases} \tag{47}$$

When the output voltage is not disturbed, the output current variation ΔI_o is equal to zero. Thus, (47) could be simplified by:

$$\begin{cases} \Delta d_1 = \frac{1-d}{I_L} \Delta I_{L1} \\ \Delta d_2 = \frac{1-d}{I_L} \Delta I_{L2} \end{cases} \tag{48}$$

When the IPOS-SC-TLB converter works at stable steady state, ΔI_{L1} and ΔI_{L2} indirectly reflect the values of Δd_1, Δd_2. According to (38), it is not difficult to deduce the following formula:

$$\Delta I_{L1} + \Delta I_{L2} = \frac{I_L}{1 - d} (\Delta d_1 + \Delta d_2) \tag{49}$$

In the three-loop control strategy, to decouple the voltage loop and the voltage-balance loop, the sum of Δd_1 and Δd_2 should be equal to zero. Thus, according to (49), there is:

$$\Delta I_{L1} + \Delta I_{L2} = 0 \tag{50}$$

Then, the reference inductor currents of Boost I and Boost II could be concluded as follows:

$$\begin{cases} {I_{L1}}^* = I_L + \Delta I_{L1} = I_L - \Delta I_L \\ {I_{L2}}^* = I_L + \Delta I_{L2} == I_L + \Delta I_L \end{cases} \tag{51}$$

According to (51), the three-loop control strategy is presented in Figure 10. The regulators of the output voltage loop and the voltage-balance loop adopt proportional-integral controller while the regulator of the current loop adopts proportional controller. The controllers can be designed based on a small-signal linearized model of the dc/dc converter, which can be developed according to the classic

average modeling method for power converters [35,36]. The inner current control loop is designed to respond faster than the outer voltage control loop so that the two control loops can be designed independently. As a result, when dealing with the inner loop, we take the outer loop as a constant input. On the other hand, the inner current control loop can be approximated as a simple lag block when we proceed with the voltage loop. The voltage-balance loop has the slowest response. When designing the controller for the voltage-balance loop, the voltage and current control loop can be considered being in steady state already. Classic Bode-plot and root-locus proportional-integral controller design procedures [36] can be used to obtain the parameters for the controllers. Nevertheless, it should be noted that due to the nonlinearity of power devices, the designed controller parameters need to be further tuned for the actual circuit. Besides, the carrier signals C_{a1}, C_{a2} are with phase-shifted 180 degrees to realize interleaved scheme for the switches S_1 and S_2.

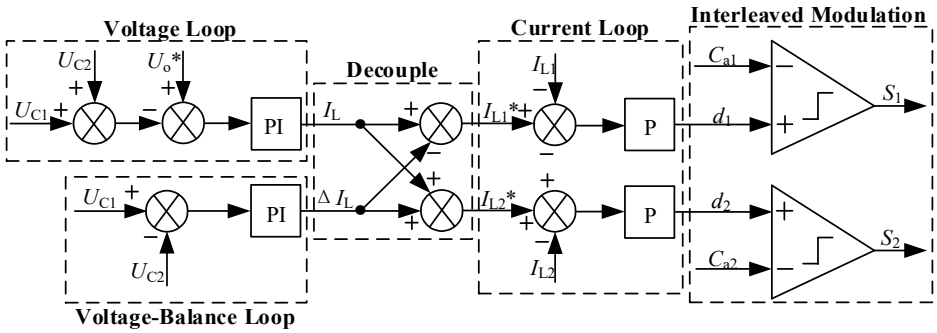

Figure 10. The three-loop control strategy.

The two sampled capacitor voltages U_{C1}, U_{C2} are added together and then compared with the output voltage reference U_o* to output the average inductor current I_L through the voltage loop regulator. ΔI_L is achieved through the voltage-balance loop regulator by comparing U_{C1} and U_{C2}. ΔI_{L2} equals to $-\Delta I_{L1}$ according to (50). The inductor current references I_{L1}*, I_{L2}* in (51) could be achieved through the decoupled scheme. Then, I_{L1}* and I_{L2}* compares with I_{L1} and I_{L2}, and pass though the two current loop regulators to output the duty cycles of Boost I and Boost II as follows:

$$\begin{cases} d_1 = d + \Delta d_1 = d - \Delta d \\ d_2 = d + \Delta d_2 = d + \Delta d \end{cases} \tag{52}$$

When U_{C1} is bigger than U_{C2}, the voltage-balance process is: ΔI_L becomes positive, which makes I_{L1}* decrease and I_{L2}* increase. As a result, d_1 decreases while d_2 increases, i.e., the turn-on time of S_1 decreases while that of S_2 increases. Thus, U_{C1} decreases while U_{C2} increases. Finally, U_{C1} equals to U_{C2} after several switching periods. When U_{C1} is smaller than U_{C2}, U_{C1} and U_{C2} could be also balanced according to a similar voltage-balance process.

5. Simulation and Experimental Verification

5.1. Simulation Verification

To verify the correctness and feasibility of the IPOS-SC-TLB converter, a simulation model adopting the proposed three-loop control strategy with 400 W output power has been implemented. The detailed simulation and experimental parameters are presented in Table 3.

Table 3. Simulation & Experimental Parameters.

Components	Parameters
Input voltage U_{in}	48 V–120 V
Output voltage U_o	400 V
Switching frequency f_s	25 kHz
Output power P_o	400 W
Switches S_1, S_2	G80N60, 2.4 V voltage drop
Diodes D_1, D_2	DSEP30-06B, 2.0 V voltage drop
Inductors L_1, L_2	915 μH, 895 μH, 0.1 ohm equivalent series resistance
Capacitors C_1, C_2, C_f	470 μF, 0.28 ohm equivalent series resistance
Driver	A3120

The input voltage varies between 48 V and 120 V, and the output voltage is controlled to be stable at 400 V. The switching frequency of the converter is set as 25 kHz. Two inductors are both chosen as about 900 μH with 0.1 ohm equivalent series resistance. Three capacitors are all set as 470 μF with 0.28 ohm equivalent series resistance. Each of the two IGBT switches has a voltage drop of 2.4 V and each of the three diodes has a voltage drop of 2.0 V. Figure 11 shows the simulation results when the input voltage is 48 V and Figure 12 shows the simulation results when the input voltage is 120 V. It can be seen that the IPOS-SC-TLB converter can output a stable dc voltage of 400 V under both the two different input voltages. The voltage difference between U_{C1} and U_{C2} is about 20 V under the input voltage 48 V and 10 V under the input voltage 120 V without voltage-balance control. However, once the voltage-balance control loop is added, U_{C1} and U_{C2} are balanced with the same voltage 200 V. Besides, in the whole experimental process, a small voltage difference between U_{C1} and U_{Cf} is about 4.4 V, which is the sum of the voltage drop of one IGBT and the voltage drop of one diode.

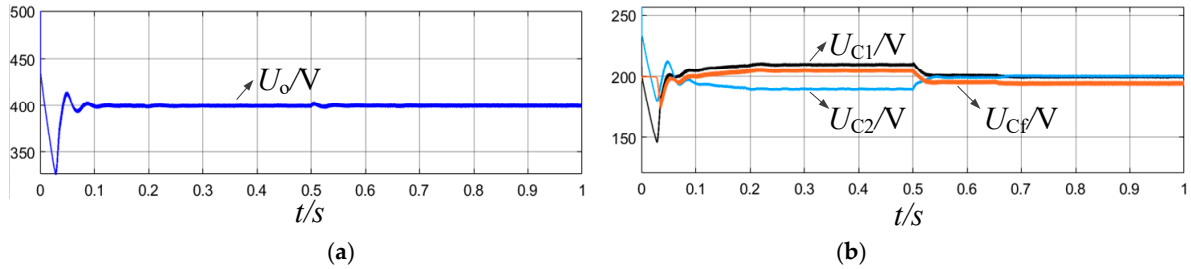

Figure 11. Simulated voltage waveforms when U_{in} is 48 V: (**a**) U_o; (**b**) U_{C1}, U_{C2}, and U_{Cf}.

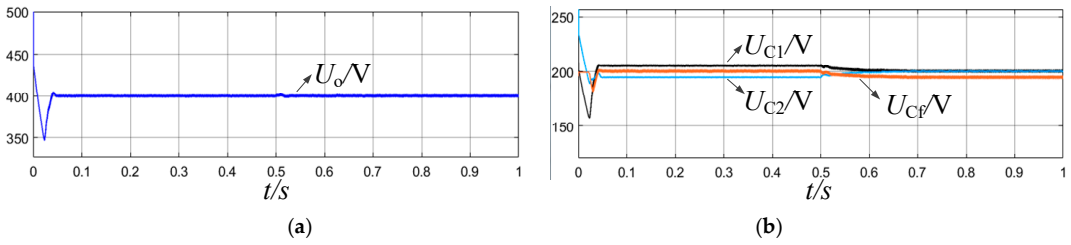

Figure 12. Simulated voltage waveforms when U_{in} is 120 V: (**a**) U_o; (**b**) U_{C1}, U_{C2}, and U_{Cf}.

More importantly, Figure 13 shows the two split inductor current waveforms of the converter without voltage-balance control and with voltage-balance control when the input voltage is 48 V. Under the condition without voltage-balance control, the average values of the two inductor currents are equal while a little different under the condition with voltage-balance control. Because the duty cycle d_1 and the duty cycle d_2 are the same under the condition without voltage-balance control but d_1 is a little smaller than d_2 under the condition with voltage-balance control. Besides, the input current ripple is smaller than the inductor current ripples, and input current ripple frequency is 50 kHz, which is two times the switching frequency 25 kHz.

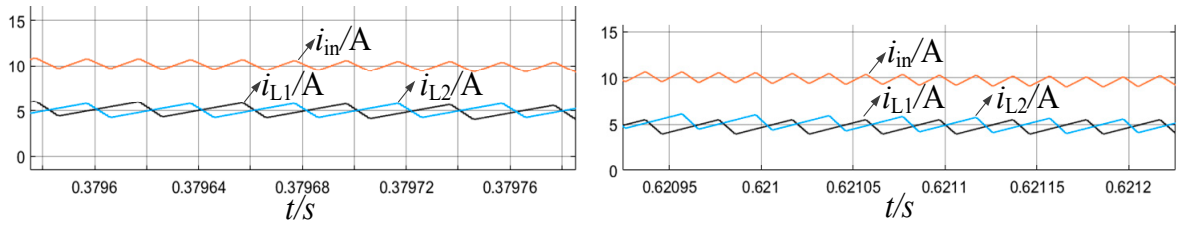

Figure 13. Simulated current waveforms when U_{in} is 48 V: (**a**) without voltage-balance control; (**b**) with voltage-balance control.

The simulated voltage waveforms and current waveforms are presented in Figure 14. The voltage stress across all power devices are half of the output voltage. The average current across every diode is 1 A, which is the same as the output current. Additionally, the average current across the switch S_2 is bigger than S_1 because the current across the diode D_2 added on the current of S_2. These results prove correctness of the theoretically derived results shown in (28). On the whole, the simulation results basically verify the effectiveness of the IPOS-SC-TLB converter and the proposed three-loop control strategy.

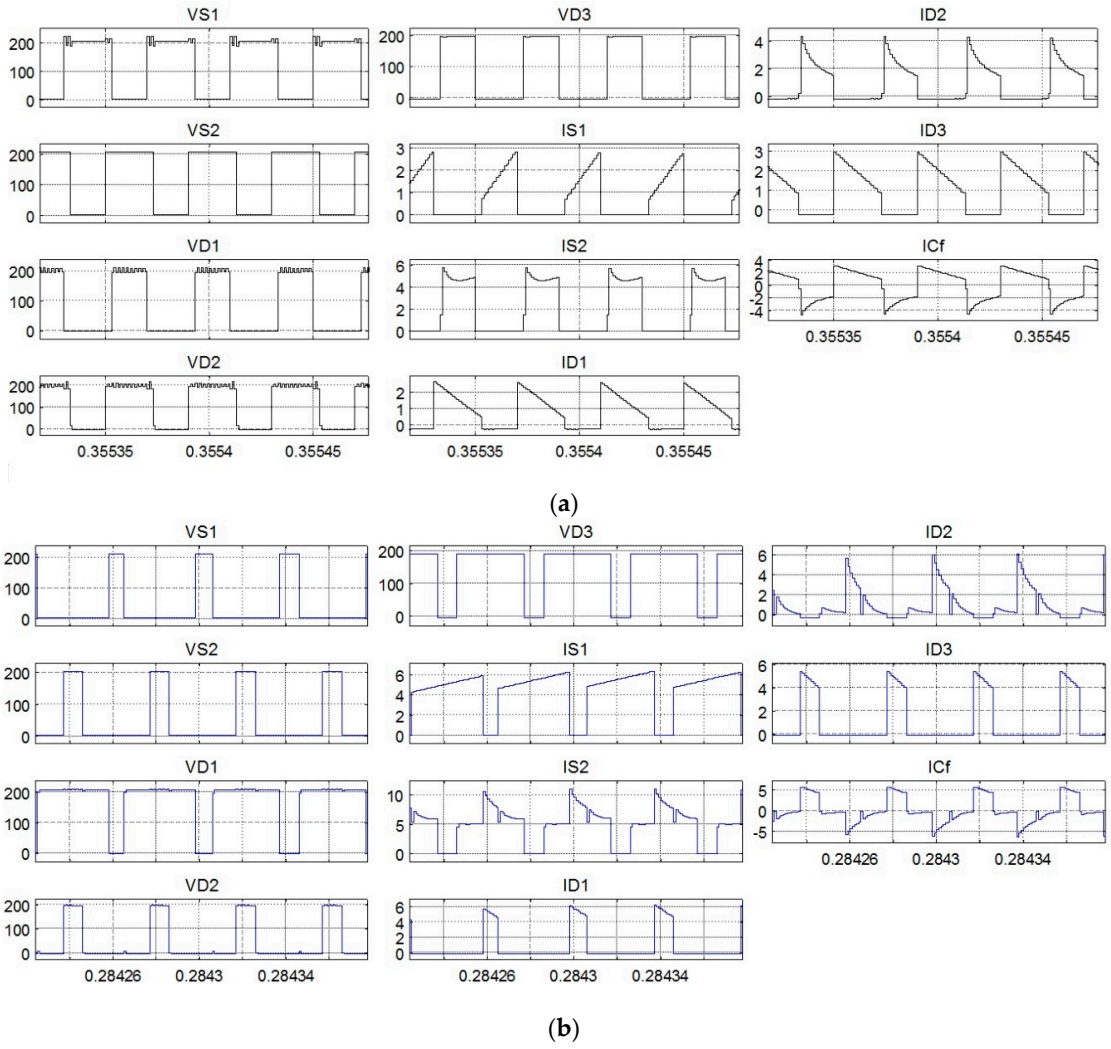

Figure 14. Simulated voltage and current waveforms: (**a**) U_{in} = 48 V; (**b**) U_{in} = 120 V.

5.2. Experimental Verification

To verify the converter and three-loop control strategy further, an experimental prototype with the same parameters shown in simulation model is built and it is given in Figure 15. It should be noted that the inductors L_1, L_2 are respectively designed to be 915 μH, 895 μH with some deviations in fact. The two switches are both selected as IGBT G80N60, which have a voltage drop of 2.4 V and the three diodes are selected as DSEP30-06B, which have a voltage drop of 2.0 V. The control loop of the converter was implemented based on Dspace 1103.

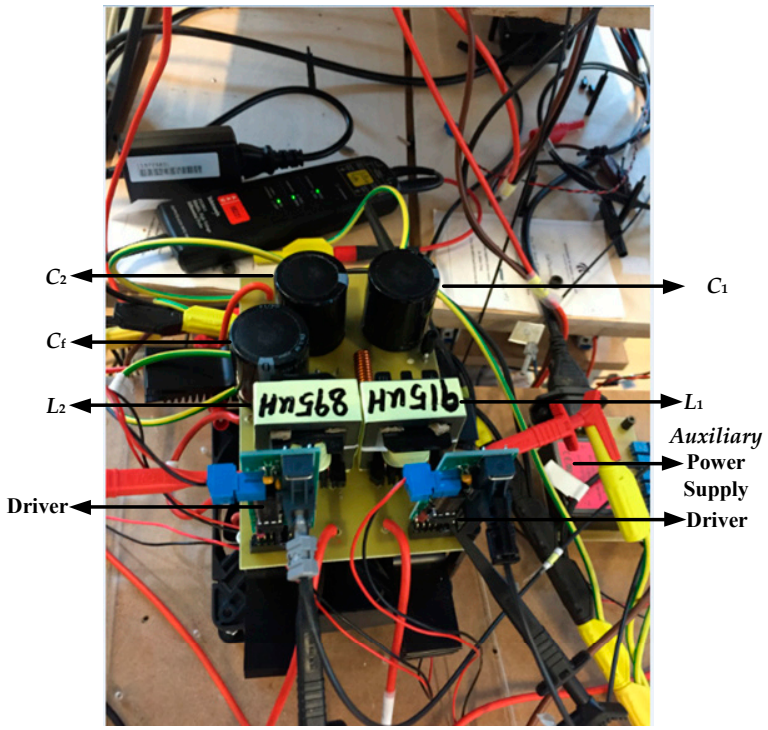

Figure 15. The experimental prototype.

The input current and capacitor voltages of the IPOS-SC-TLB converter under different input voltages are presented in Figure 16, and the corresponding capacitor voltages are presented in Figure 17. The inductor currents across L_1, L_2 and the drive signals of S_1, S_2 are presented in Figure 18. It can be seen that the output voltage is stable at 400 V and the three capacitor voltages are stable with 200 V under different input voltages. The input current is continuous with a small current ripple and the input current ripple frequency is 50 kHz, which is two times the switching frequency 25 kHz. Moreover, it is easy to observe that as the duty cycle approaches 0.50, the input current ripple becomes almost zero, which verifies (32).

To show voltage stresses across all the switches and diodes, the terminal voltage waveforms of S_1, S_2, D_1, D_2, and D_3 are presented in Figures 19–21. It should be noted that u_{S1}, u_{S2} are defined to describe the voltage difference between the drain terminal and the source terminal of S_1 and S_2, respectively. u_{D1}, u_{D2}, u_{D3} are the voltage differences between the cathode and the anode of D_1, D_2 and D_3. It can be seen that all the voltage stresses of the switches and diodes are 200 V, which is half of the output voltage 400 V. It matches with (12). In addition, the current I_{S2} is the sum of I_{S1} and I_{D2}, which matches with (20) and (21). For example, when the input voltage is 48 V, I_{S1}, I_{S2}, I_{D2} are 3.74 A, 4.78 A and 1.13 A, respectively. It is not difficult to know that the switching state of D_1 is complementary to that of D_2, and the switching state of D_1 is 180 degrees shifted from that of D_3. The switching state of S_1 is also 180 degrees shifted from that of S_2. All of these results can verify the correctness of the operating principle of the IPOS-SC-TLB converter.

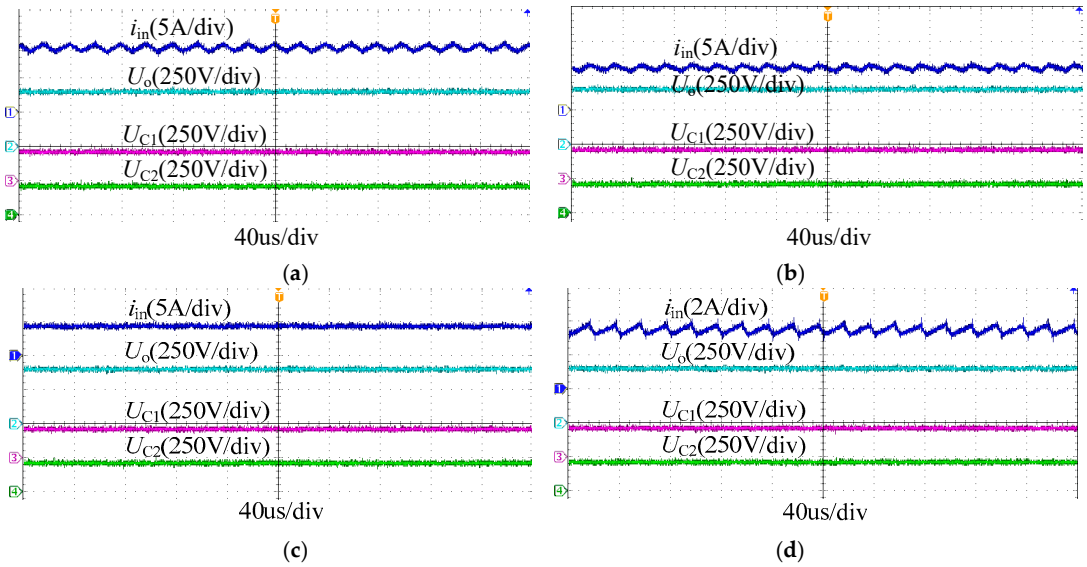

Figure 16. Input current and capacitor voltage waveforms: (**a**) U_{in} = 48 V; (**b**) U_{in} = 72 V; (**c**) U_{in} = 100 V; (**d**) U_{in} = 120 V.

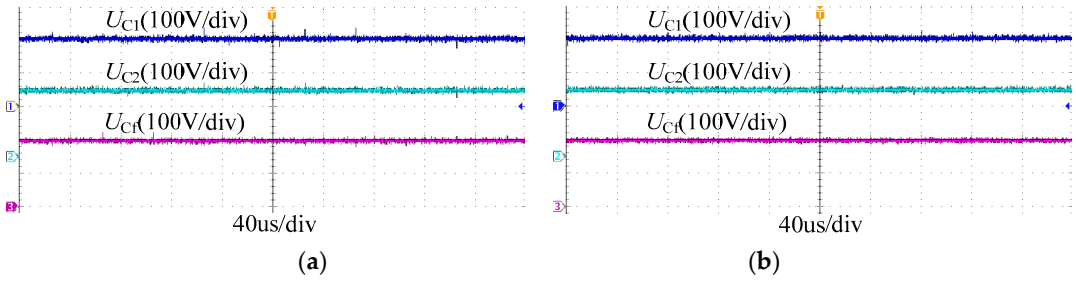

Figure 17. Capacitor voltage waveforms: (**a**) U_{in} = 48 V; (**b**) U_{in} = 120 V.

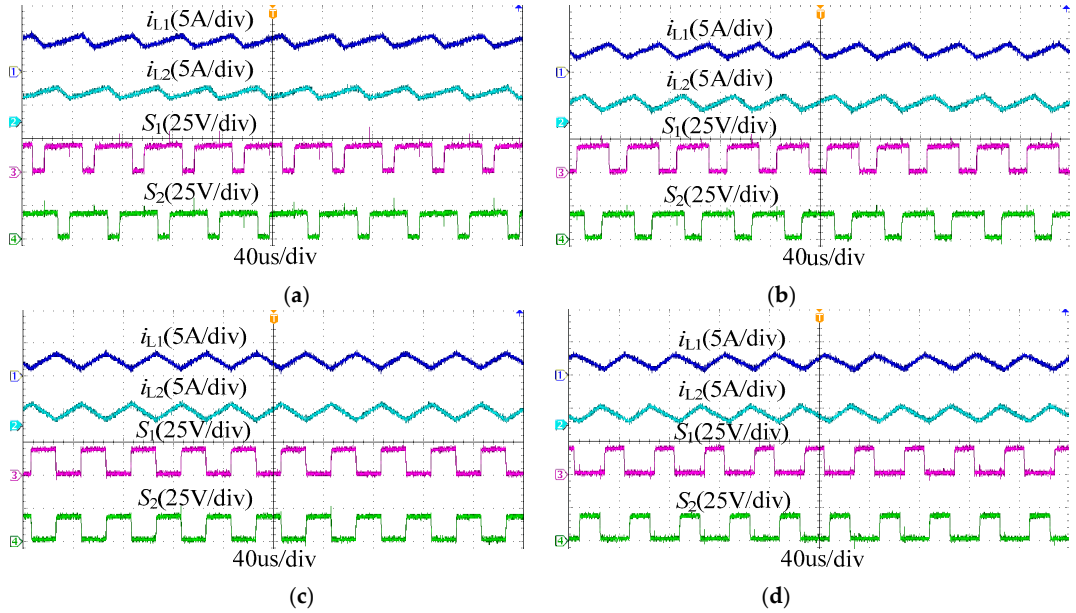

Figure 18. Inductor current and drive signal waveforms: (**a**) U_{in} = 48 V; (**b**) U_{in} = 72 V; (**c**) U_{in} = 100 V; (**d**) U_{in} = 120 V.

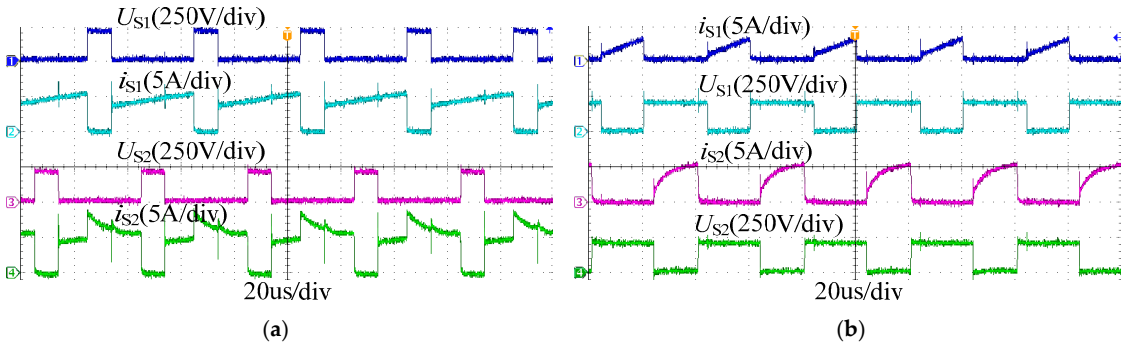

Figure 19. Tested voltage and current waveforms of S_1, S_2: (**a**) U_{in} = 48 V; (**b**) U_{in} = 120 V.

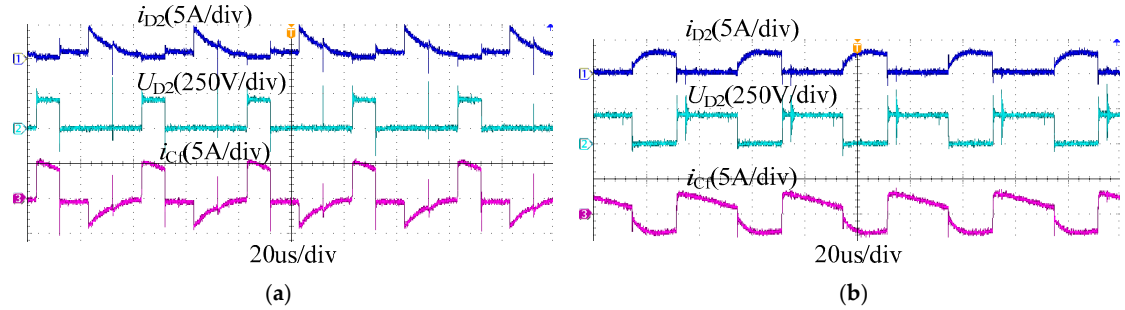

Figure 20. Tested voltage and current waveforms of D_2 and current waveform of C_f: (**a**) U_{in} = 48 V; (**b**) U_{in} = 120 V.

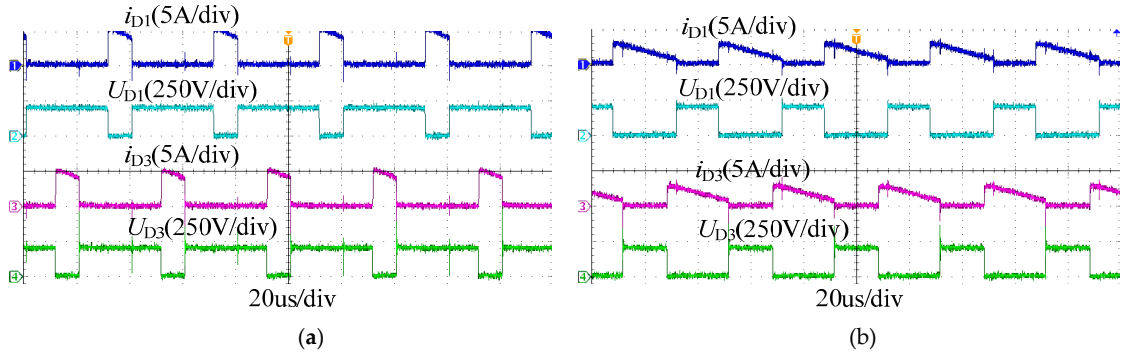

Figure 21. Tested voltage and current waveforms of D_1, D_3: (**a**) U_{in} = 48 V; (**b**) U_{in} = 120 V.

More importantly, the voltage-balance experimental waveforms of the IPOS-SC-TLB converter are presented in Figures 22 and 23. The experimental results indicate that when the voltage-balance loop is not added, there is about 13.0 V voltage difference between U_{C1} and U_{C2}. For example, when the input voltage is 48 V, the tested duty cycle is around 0.83. According to (43), the voltage difference between U_{C1} and U_{C2} is 11.26 V under the input voltage of 48 V. The tested voltage difference of 13.00 V basically matches the theoretical value 11.26 V with some voltage error. When the voltage-balance loop is added, the voltage difference becomes nearly zero.

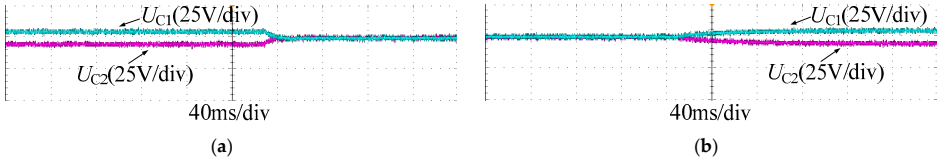

Figure 22. Voltage balance process of C_1, C_2 when U_{in} is 48 V: (**a**) from no voltage-balance control to voltage-balance control; (**b**) from voltage-balance control to no voltage-balance control.

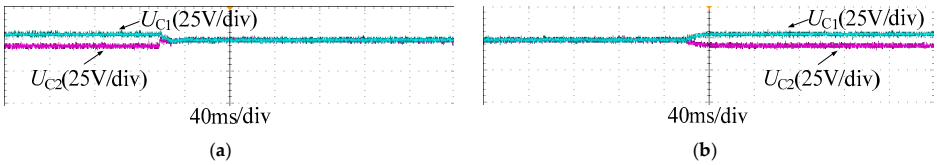

Figure 23. Voltage balance process of C_1, C_2 when U_{in} is 120 V: (**a**) from no voltage-balance control to voltage-balance control; (**b**) from voltage-balance control to no voltage-balance control.

Figure 24 shows the theoretical voltage gain and the experimental voltage gain versus duty cycle when U_{in} is 48 V. It can be seen that the theoretical voltage gain and the experimental voltage gain have the same increasing trend though some deviations exist. The experimental voltage gain basically matches the theoretical voltage gain when the duty cycle varies between 0.2 and 0.5. However, when the duty cycle is over 0.50, the experimental theoretical voltage gain is less than the theoretical voltage gain, and their difference increases with the duty-cycle increasing. This phenomenon may be due to the non-linearity of power electronic components and the fact the true values of parasitic parameters are hard to obtain.

The conversion efficiency curves versus output power for the IPOS-SC-TLB converter under different input voltages are given in Figure 25. The minimum efficiency and the maximum efficiency are 92.08% and 94.20%, respectively, at an input voltage of 48 V; 95.13% and 96.55% at the input voltage of 72 V; 96.08% and 97.32% at the input voltage 100 V; 96.62% and 98.57% at an input voltage of 120 V. It can be seen that the proposed converter is not efficient in low voltage levels, such as 48 V in the experiment. To make it efficient, the converter should be implemented with optimized design, including component selection, coupling inductor design and applying soft switching technique. For component selection, wide bandgap device (SiC, GaN) with much smaller parasitic parameters should be a good solution, which could not only reduce conduction and switching losses, but also enhance the switching frequency to reduce passive components' size and parasitic parameters as well. Coupling design for the two inductors L_1 and L_2 will help reduce size and improve efficiency of the converter. Soft switching technique applied on this converter will help enhance conversion efficiency.

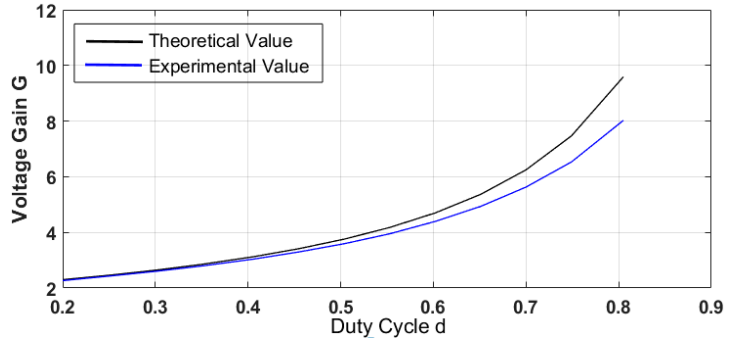

Figure 24. The theoretical voltage gain and the experimental voltage gain versus duty cycle when U_{in} is 48 V.

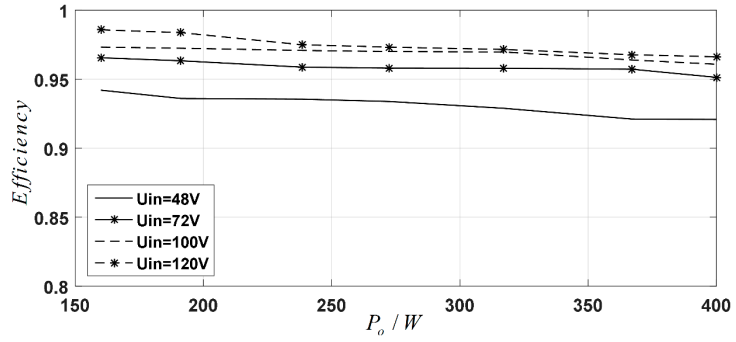

Figure 25. Efficiency curves under different input voltages.

Based on all the experimental results, the theoretical analysis of the IPOS-SC-TLB converter is correct and the three-loop control strategy is feasible. The effectiveness of the proposed IPOS-SC-TLB converter has been verified.

6. Conclusions

This paper presents an input-parallel-output-series three-level Boost converter, which can step up the input voltage to a high voltage level, as well as attaining low voltage stress, low current stress and small input current ripple. Another advantage of the proposed topology is the automatic current balancing function. There is also a disadvantage that the imbalance current between the two power switches S_1, S_2. The average current of S_2 is U_o/R higher than the average current of S_1.

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Nomenclature

List of Abbreviations

IPOS-SC-TLB	input-parallel-output-series switched-capacitor three-level boost
HVDC	high voltage direct current
SI	serial-interleaved
PI	parallel-interleaved
SI-TLB	serial-interleaved three-level boost
PIB	parallel-interleaved boost
SI-FC-TLB	serial-interleaved flying-capacitor three-level boost
PI-FC-TLB	parallel-interleaved flying-capacitor three-level boost
PI-SFC-TLB	parallel-interleaved symmetric flying-capacitor three-level boost
SC-TLB	switched-capacitor three-level boost
IPOS-TLB1	input-parallel-output-series three-level boost 1
IPOS-TLB2	input-parallel-output-series three-level boost 2

List of Symbols

U_{in}	average input voltage
U_o, I_o	average output voltage and average output current
U_o*	output voltage reference
U_{C1}, U_{C2}, U_{Cf}	average voltages of capacitors C_1, C_2, C_f
ΔU	voltage difference between C_1 and C_f,
i_{L1}, i_{L2}	currents of inductors L_1, L_2
I_{L1}, I_{L2}	average currents of inductors L_1, L_2
I_{L1}*, I_{L2}*	reference currents of inductors L_1, L_2
Δi_{L1}, Δi_{L2}	current ripples of inductors L_1, L_2
Δi_{in}	input current ripple
I_{D1}, I_{D2}, I_{D3}	average currents of diodes D_1, D_2, D_3
I_{S1}, I_{S2}	average currents of switches S_1, S_2
d	duty cycle
d_1	duty cycle of boost 1
d_2	duty cycle of boost 2
Δd	duty cycle difference

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