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Energy Storage Characteristic Analysis of Voltage Sags Compensation for UPQC Based on MMC for Medium Voltage Distribution System

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Abstract: The modular multilevel converter (MMC), as a new type of voltage source converter, is increasingly used because it is a distributed storage system. There are many advantages of using the topological structure of the MMC on a unified power quality controller (UPQC), and voltage sag mitigation is an important use of the MMC energy storage system for the power quality compensation process. In this paper, based on the analysis of the topology of the MMC, the essence of energy conversion in a UPQC of voltage sag compensation is analyzed; then, the energy storage characteristics are calculated and analyzed to determine the performance index of voltage sag compensation; in addition, the simulation method is used to verify the voltage sag compensation characteristics of the UPQC; finally, an industrial prototype of the UPQC based on an MMC for 10 kV of medium voltage distribution network has been developed, and the basic functions of UPQC have been tested.

Keywords: MMC; unified power quality controller; voltage sag; energy storage characteristics; medium voltage distribution system

1. Introduction

Ensuring power quality is one of the requirements of a power system operation. The sensitivity to the change of power characteristics of modern industrial, commercial, and residential electrical equipment such as high performance office equipment, precision experimental instruments, variable frequency speed control equipment, programmable logic controllers, various automatic production lines, and computer systems is increasing year by year. At the same time, the increasing variety and the capacity of power quality interference sources lead to more and more complex power qualities, and the resulting interference and loss is also increasing [1,2]. Therefore, in order to improve the quality of power supply, to reduce the losses caused by power quality, to protect users' interests, and to create a favorable investment environment, the adoption of advanced power-quality control technology will become one of the features of future power supplies.

Many methods have been put forward for the control of power quality, and there has been research on a wide range of power quality control technologies, including dynamic reactive power compensation technology (Static Var Compensator (SVC) and STATCOM), active power filters (APF),

and dynamic voltage restorers (DVR) [3–6], but a single power quality regulator can only partially solve the problem of power quality. With the increasing complexity of distribution network structures and power load components, various power quality problems will occur at the same time in the same distribution system or in the same electricity load. If a single type of control device is adopted for every power quality problem, the investment costs, the workload of device operations, the required maintenance, and the complexity of coordination between devices will be greatly increased, so a unified power quality controller (UPQC) can be used to solve the problem of voltage and current power qualities [7–9]. Because of the restrictions of power electronic devices, they can only be applied at lower voltage levels; however, power quality problems sometimes occur at higher voltage levels. Thus, there is an urgent need for a comprehensive power quality control system to achieve comprehensive governance.

A modular multilevel converter (MMC) is a new power electronic topology that has been developed in recent years [10]. The modular superposition technique can be applied to a high voltage level on the basis of the existing power electronic device manufacturing level. Compared to the switch tube series technology, it is easier to apply the application of higher voltage level and power requirement; the modular design can improve the redundancy of the device and increase the reliability of the device. A modular design is also conducive to a standardized scale production in order to reduce production costs; in addition, the multilevel technology can also reduce the harmonic content of the output voltage and the switching frequency of the switching device, which will then reduce the switching loss [11–13]. The applications of an MMC are becoming more and more extensive. MMC technology has obvious advantages in its application in the field of high voltage and large capacity represented by flexible DC transmission. It has been a breakthrough in the field of HVDC [14,15], and there has been a gradual shift to DC/DC converters [16,17], high-voltage DC power systems of high-power variable frequency drive [18], flexible AC transmission systems [19,20], and the development of large-scale photovoltaic grid-connected energy storage areas [21,22], These technologies have made many valuable contributions in scientific research as well as some engineering applications, showing good application prospects. The development of MMC technology enables the application of UPQC in the field of high voltage and large capacity [23].

In many power quality problems, the reliability of a power supply system for voltage sag has been an important issue [24]. With the development of microelectronics, computers, power electronics technologies, renewable energy power generation systems, user equipment, and access systems that are able to process more information, the equipment used to detect voltage sag is very sensitive, causing many troubles and huge losses for stakeholders. Therefore, voltage sag is one of the most serious and urgent power quality problems. Due to the voltage sags, the compensation is required to be real-time. At the same time, the system is also exchanged with the system, while the compensation is temporarily reduced. This requires that the response time of the compensation equipment for the voltage sags must be very rapid [25].

In a medium voltage distribution network, voltage sag is prone to occur due to the complex structure of the power grid and the wide distribution area. Meanwhile, the voltage level is relatively high, which has a significant impact on the electrical equipment and leads to a very high amount of energy required for the sags compensation [26,27]. Conventional power converters are not appropriate solutions to this problem. Because the MMC topology has unique characteristics, namely the ability to spread the energy storage unit in each module, the ease of meeting the requirements of the storage capacity, and the relative ease of manufacturing it, the MMC has the characteristics of modular, distributed energy storage, and its energy storage characteristics are an important influence on the voltage sag compensation of a UPQC.

In this paper, through the analysis of the topology and equivalent model, put forward control strategy of UPQC, the performance index of unified power quality controller using energy storage characteristics to achieve voltage sag compensation is calculated and analyzed, and the simulation results are given.

2. UPQC Based on MMC and Control Strategy

2.1. UPQC Based on MMC

An MMC is shown in Figure 1. This MMC has a total of six bridges, with each bridge arm being composed of a plurality of interconnected structures and the same submodule (SM) and an L reactor connected in series, combined with two upper and lower bridge arms to form a unit. For the purpose of modular design and manufacture, the six bridges are symmetrical; that is, the parameters of each submodule and the reactance value of each bridge arm are the same. Compared with the voltage source converter (VSC) topology structure, a significant difference is that the MMC does not have a DC capacitor between the common DC negative sides; the DC capacitor is distributed to each submodule, and the withstand voltage is low, thereby simplifying the design and manufacture [10–12].

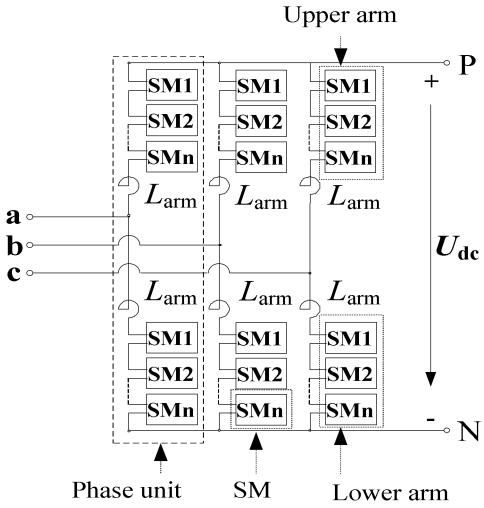


Figure 1. Modular multilevel converter (MMC) topology diagram.

Figure 2a shows a schematic diagram of the simplified topology, including the comprehensive power quality control system and the map series; the main topology of the parallel part adopts the MMC structure (see Figure 2a), and energy storage capacitor shall be borne by the SM in the MMC (see Figure 2b). The parallel part is directly connected to the power grid, and the serial part is connected with the system through the coupling transformer [6–8,23].

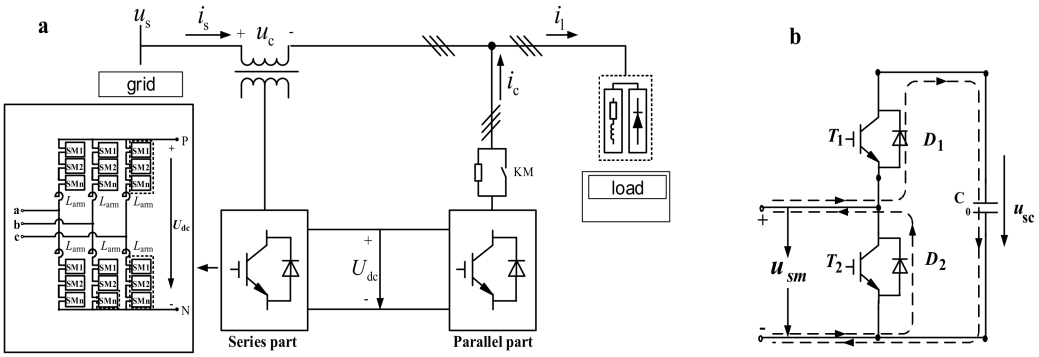


Figure 2. (**a**) Simplified schematic of MMC–UPQC (unified power quality controller) topology; (**b**) Structure of MMC submodule.

2.2. The Equivalent Model of the MMC Converter

The bridge arm of the MMC can be equivalent to a controlled voltage source, and the control amount is the switch state of each SM in the bridge arm. Therefore, the MMC accurate model can be established by the switch function [28,29].

In normal operation, the SM is either in a full voltage state or in a zero voltage state. Set S_{xpi} (x = a, b, c; i = 1, 2, . . . , n) represents the running state of the ith SM of the upper bridge arm on the phase unit of x, S_{xpi} = 1 represents open (full voltage state), while S_{xpi} = 0 represents off (zero voltage state). Similarly, Set S_{xni} (x = a, b, c; i = 1, 2, . . . , n) represents the running state of the ith SM of the lower bridge arm on the phase unit of x. The capacitance voltages of the ith SM in the upper and lower bridge arms in the phase unit of x are represented by U_{smxpi} and U_{smxni} respectively.

The single-phase schematic diagram of the MMC is set up as shown in Figure 3a. In figure, u_{x1} and u_{x2} represent the voltages of the upper and lower bridge arms in the x phase (x = a, b, c), i_{x1} and i_{x2} represent the currents of the upper and lower bridge arms in the x phase, R_1 and R_2 represent the resistances of the upper and lower bridge arms, L_1 and L_2 represent the inductances of the upper and lower bridge arms, P and N represent the positive and negative poles of the DC bus, and i_x and i_{xc} represent the line currents and circulations of the phase of x.

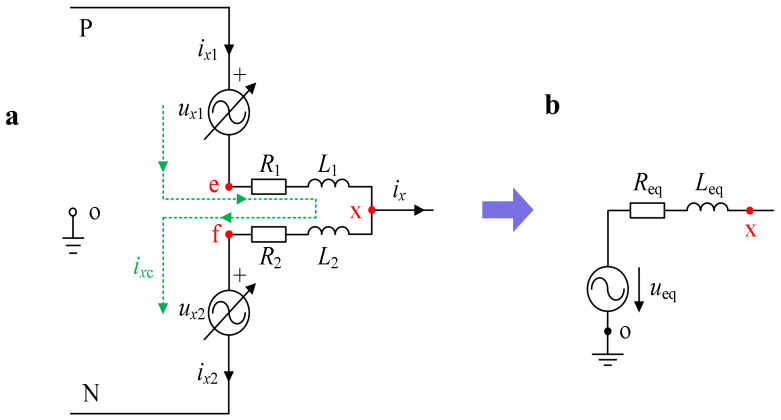


Figure 3. (**a**) Single-phase simplified schematic of MMC; (**b**) Thevenin-equivalent circuit of MMC.

First, the correlation voltage in Figure 3a is expressed by the switching functions of each module, as shown in Equations (1)–(3).

$$u_{\mathrm{eo}} = U_{\mathrm{Po}} - u_{x1} = \frac{U_{\mathrm{dc}}}{2} - \sum_{i=1}^{\mathrm{n}} U_{smxpi} \cdot S_{xpi} \tag{1}$$

$$u_{\mathrm{fo}} = U_{\mathrm{No}} + u_{x2} = -\frac{U_{\mathrm{dc}}}{2} + \sum_{i=1}^{\mathrm{n}} U_{smxni} \cdot S_{xni} \tag{2}$$

$$u_{\mathrm{ef}} = u_{\mathrm{eo}} - u_{\mathrm{fo}} = U_{\mathrm{dc}} - \sum_{i=1}^{\mathrm{n}} U_{smxpi} \cdot S_{xpi} - \sum_{i=1}^{\mathrm{n}} U_{smxni} \cdot S_{xni} \tag{3}$$

Referring to the current direction of Figure 3, the following relationship can be obtained according to KCL, where, i_{xc} is the common mode current of i_{x1} and i_{x2}:

$$i_{x1} = i_{x2} + i_x \tag{4}$$

$$i_{xc} = \frac{1}{2}(i_{x1} + i_{x2}) \tag{5}$$

By Equations (4) and (5), the expression of the available bridge arm current is shown as follows:

$$i_{x1} = i_{xc} + \frac{i_x}{2} \tag{6}$$

$$i_{x2} = i_{xc} - \frac{i_x}{2} \tag{7}$$

The pressure drop expression on the bridge arm resistance and the commutation reactance can then be derived from the bridge arm current, as shown below:

$$u_{ex} = R_1 i_{xc} + L_1 \frac{di_{xc}}{dt} + \frac{1}{2}\left(R_1 i_x + L_1 \frac{di_x}{dt}\right) \tag{8}$$

$$u_{xf} = R_2 i_{xc} + L_2 \frac{di_{xc}}{dt} - \frac{1}{2}\left(R_2 i_x + L_2 \frac{di_x}{dt}\right) \tag{9}$$

From the view of the system side, the voltage source converter can be regarded as an ideal voltage source with no inertia. The Thevenin-equivalent model of the MMC is set up as shown in Figure 3b.

The equivalent voltage source ports x and o refer to the converter from the system after disconnecting the port open circuit voltage; then, $i_x = 0$ and $R_1 = R_2 = R$, $L_1 = L_2 = L$. The pressure drop is equal to the upper and lower bridge arm resistances (see Equation (10)), and the Thevenin-equivalent voltage is in the form of Equation (11).

$$u_{ex} = u_{xf} = -\frac{1}{2}u_{ef} \tag{10}$$

$$u_{eq} = u_{xo} = u_{xf} + u_{fo} = -u_{ex} + u_{eo} = \frac{1}{2}u_{ef} + u_{fo} = -\frac{1}{2}u_{ef} + u_{eo} \tag{11}$$

Substitute the Equations (1)–(3) into Equation (11); then, the Thevenin-equivalent voltage expression can be used to switch module function, as shown below:

$$u_{eq} = -\frac{1}{2}\sum_{i=1}^{n} U_{smxpi} \cdot S_{xpi} + \frac{1}{2}\sum_{i=1}^{n} U_{smxni} \cdot S_{xni} \tag{12}$$

The equivalent impedance of the MMC equals to the value of impedance after all independent voltage sources in port x and o are zero.

$$Z_{eq} = (R_1 + j\omega L_1)//(R_2 + j\omega L_2) = \frac{1}{2}(R + j\omega L) = R_{eq} + j\omega L_{eq} \tag{13}$$

Generally, the equivalent resistance of the bridge arm is very small; thus, R_{eq} can be ignored.

2.3. Control Strategy

The equivalent circuit model of the MMC obtained from Section 2.2 can be seen as a voltage source converter (VSC); the u_{eq} voltage source is adjusted flexibly by the switching of the SM of the MMC. At present, relatively mature modulation strategies include the phase-shifted PWM, the level-shifted PWM, the SVPWM, the nearest level modulation (NLM), and others [30,31], and the corresponding modulation mode can be chosen depending on the demands.

2.3.1. Control Strategy of Parallel Side Converter

The control strategy of the parallel side of the UPQC is based on dq rotation coordinate transformation. The three-phase three wire dq0 detection algorithm that is based on the instantaneous reactive power theory is adopted to achieve the negative sequence compensation, the reactive power compensation, and the harmonic compensation. Figure 4 shows the control block diagram on the

parallel side of the UPQC. The external voltage loop of the DC common side adopts the PI regulator to control the actual DC voltage tracking expectation.

The compensation measure unit inputs the positive sequence reactive power, the negative sequence of the fundamental wave, and the superposition signal of the harmonic component of the inner loop of the current. The feedforward decoupling method is used to decouple the d and the q components of the converter, and then, the dq inverse transform is used to generate the input trigger pulse of the voltage instruction signal.

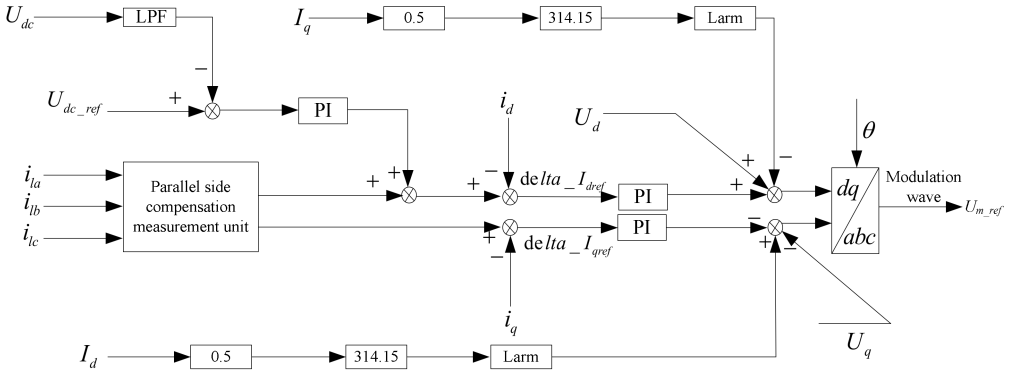


Figure 4. Block diagram of UPQC parallel side control algorithm.

The MMC converter of the UPQC adopts a carrier phase-shift modulation. In the process of modulation, it is necessary to consider the capacitance voltage balance of SMs and the circulation control problem between the phases [32]. As shown in Figure 5, the voltage balance control, the circulation current control in the phase, the voltage balance control of the SM, and the total modulation wave after the superposition of the results of Figure 4 are taken into account. Through the modulation method of the carrier phase shift, the IGBT is turned on and off in the touches, and the MMC modulation control method in series is consistent with the parallel side.

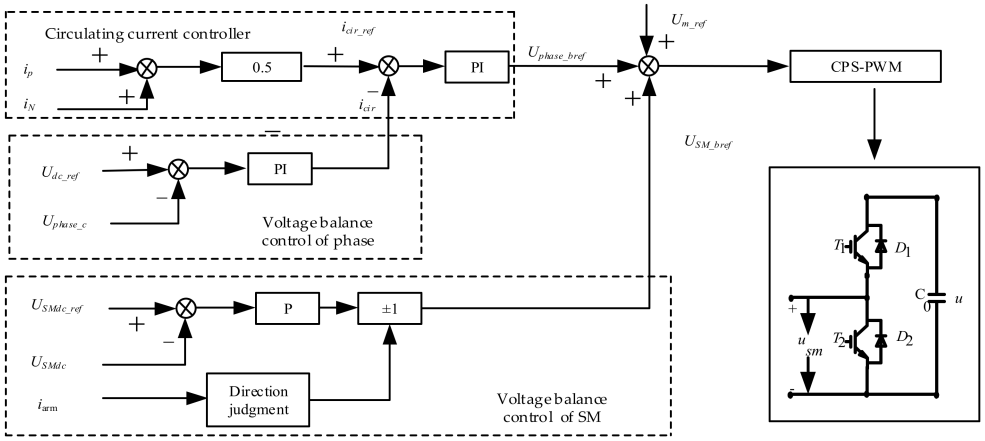


Figure 5. Block diagram of MMC control strategy.

The three-phase three line dq0 detection algorithm that is based on the instantaneous reactive power theory is used to realize the negative sequence compensation, the reactive compensation, and the harmonic compensation of the current on the parallel side of the UPQC. Figure 6 shows a block diagram of the UPQC's parallel side detection algorithm. u_{sa}, u_{sb}, and u_{sc} are three-phase power voltages, and phase angles are obtained through a phase-locked loop (PLL) unit, while i_{la}, i_{lb}, and i_{lc} are load currents. Through the compensation algorithm, the reactive compensation component,

the negative sequence compensation component, and the harmonic compensation component are obtained respectively, while the trigger pulse is generated by phase-shifted PWM.

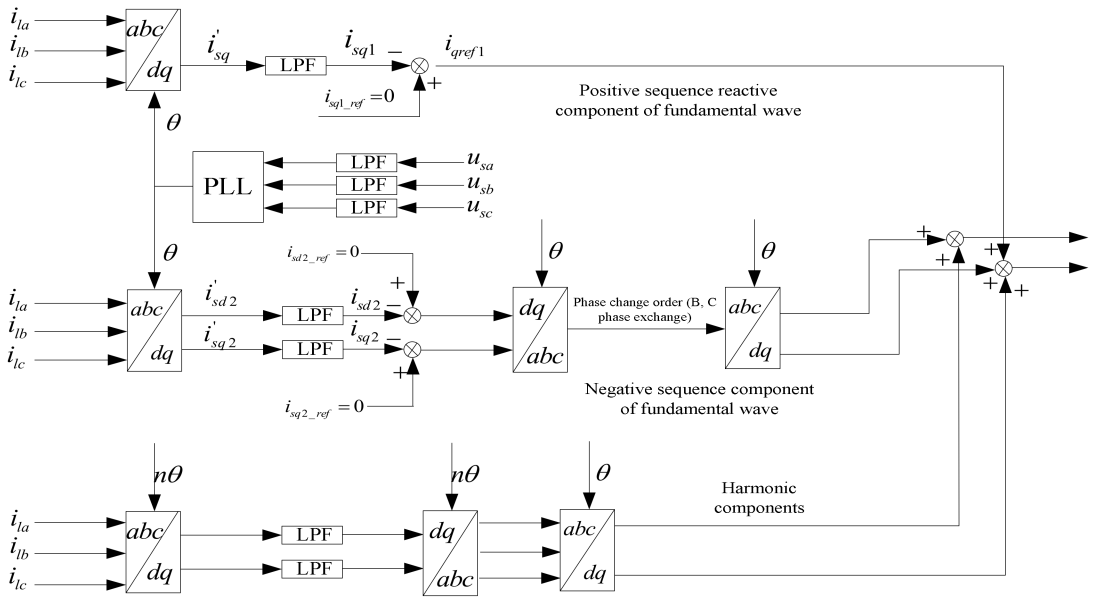


Figure 6. Block diagram of UPQC parallel side detection algorithm.

2.3.2. Control Strategy of Series Side Converter

Figure 7 shows a block diagram control algorithm on the series side of the UPQC. u_{abcCom} is the instruction voltage which is calculated by the series side compensation algorithm, while u_{abc_out} is the difference between the actual circuit system voltage and the load voltage. Because the series part of the UPQC access system passes through the transformer, the converter output voltage will have a certain phase difference to the voltage of the system side. When the voltage sags controller is designed, the feedforward PI can be used to eliminate such errors. The instruction voltage is used as a reference value, and the actual compensation voltage is tracked through the adjustment of the PI.

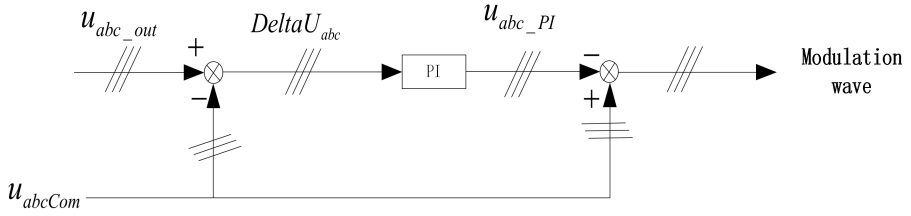


Figure 7. Block diagram of UPQC series side control algorithm.

The series side of the UPQC mainly compensates the voltage type power quality, including the voltage sags compensation, the negative sequence voltage compensation, and the harmonic voltage compensation. Figure 8 shows a block diagram of the UPQC's series side detection algorithm. Voltage sags and negative sequence voltages are based on the dq0 detection algorithm that is based on the instantaneous reactive power theory. Due to the phase error of high order harmonics, the detection algorithm of FFT is adopted.

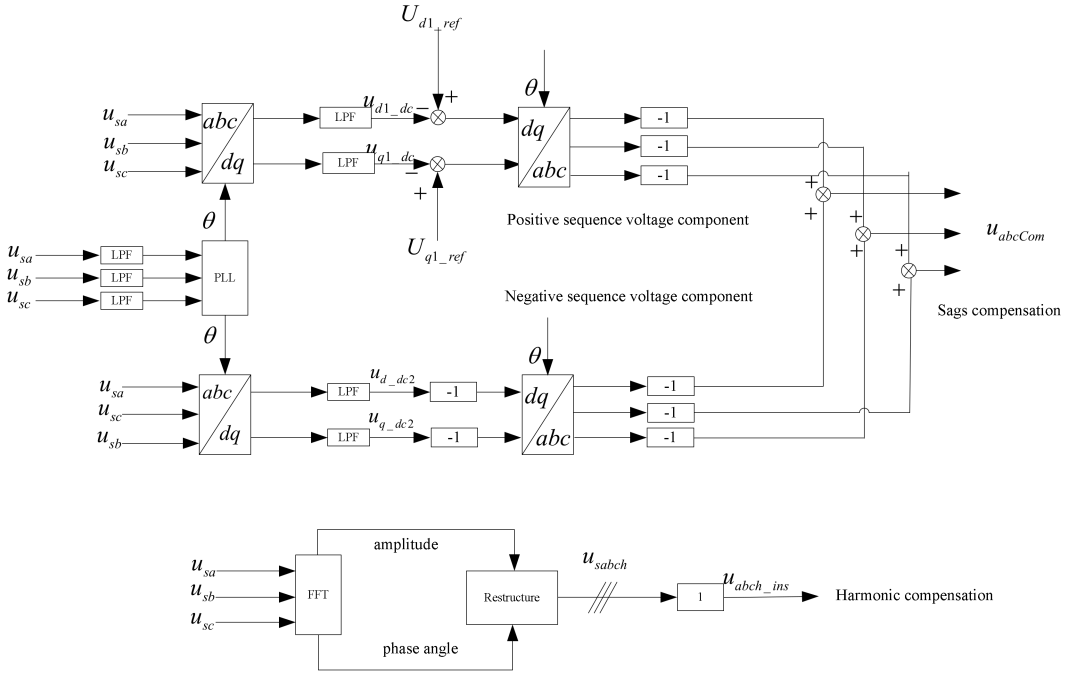


Figure 8. Block diagram of the UPQC's series side detection algorithm.

2.3.3. Analysis of Voltage Sag Compensation for the UPQC and the Coordinated Control

(1) Essential analysis of the voltage sags compensation

Voltage sag is a typical power quality problem. The voltage RMS value dropped to below 0.9 p.u., and the duration of each cycle was between 0.5 min and 1 min. The voltage sag is inversely proportional to time, i.e., the greater the sag, the shorter the duration. When voltage sags occur, the reliability of the power supply will be especially sensitive to the load, and the load may even appear to be unable to continue the work. Voltage sags cause power systems to provide an insufficient amount of energy to load to compensate for the voltage sag, as the system cannot provide energy in this part, which means that the energy must be solved through the method of external storage.

The energy of voltage sag compensation can be divided into two parts in the UPQC: the energy absorbed by the parallel side converter and the energy stored in the system. However, because the parallel side is in the direction of the load side, when the load is low, the energy of the parallel side will absorb the energy at the same time. Therefore, a better approach is not to control the voltage in the voltage sag; thus, the parallel side does not absorb energy, allowing the whole process of the compensation for voltage sag in the energy storage system to achieve the release. In the MMC, which is on the DC capacitor dispersed in each SM in the realization of the energy storage unit, the appropriate parameters can achieve voltage sag compensation because of the large number of SMs.

(2) Coordinated control of series and parallel converters in the UPQC

Due to the limited storage power of the MMC's submodule in DC capacitors, the UPQC can only provide a short duration of support (DC capacitors release energy). The UPQC parallel side absorbs the active power, and if the final energy source is still the power supply of the system side, when the voltage sag is of a significant depth, the UPQC compensation algorithm adopts the mode of a common DC bus without control during voltage sag and disconnects the parallel side unbalance compensation channel to avoid a series problem of overcurrent side converters, which is caused by the DC voltage of the parallel side support due to the parallel side converter on the load side. The decision unit is added before the modulation input instruction voltage. When voltage sag occurs, if the DC bus voltage falls to the minimum voltage of the DC bus or the voltage sag exceeds the given compensation time,

the UPQC will quit the operation. Therefore, when the system side voltage has a more serious fault sag (such as 85% voltage sag depth), because the system side voltage is very low, the power system can provide an amount of energy to the load that is far less than the load requirements (considering the voltage characteristics of load power). Most of the energy needs to be supported by UPQC in no additional storage unit under the condition that the UPQC duration voltage sag compensation will decrease with an increase in voltage sag amplitude.

3. Energy Storage Characteristics of the UPQC

The parameter design of the submodule capacitor of the MMC has been investigated in many studies, namely the aspects of instantaneous power fluctuation and filter performance, and also a combination of the two in an actual situation [33]. There has also been an attempt to use the empirical formula [34]. In the UPQC, we can see from the preceding analysis that the energy storage of the DC capacitor of a submodule is the energy source of support voltage sag compensation, and its sag compensation performance index has a significant relationship with its value. The concept of "Unit Capacitance Constant (UCC)" was proposed by Hagiwara and Akagi [34] to help design a capacitance value; this value is the total capacitance energy storage ratio and the equipment capacity in seconds. The UCC constant is defined as follows:

$$UCC = \frac{\frac{1}{2} \times N \times C_{sm} \times U_{ds}^2}{Q_{out}} \tag{14}$$

In Equation (14), C_{sm} is the equivalent capacitance, U_{dc} is the working voltage of the DC capacitor, and Q_{out} is the reactive power output. Usually, the UCC is 30–200 ms.

The DC capacitor stored energy is limited; thus, in the absence of an additional storage device, the comprehensive power quality control system has a limited ability to provide itself with the function of load quantity. The energy source is still the ultimate load of the power system either for short periods of time or when it is needed for support (DC capacitor release energy). In particular, the failure type of voltage sag is a more serious problem in the system (such as the 60% side voltage sags) because the system side voltage is very low; the power that the system can provide to the load is far less than the load requirements (considering the voltage characteristic of load power) as most of the energy is required by the power quality comprehensive control system for support. In the absence of additional storage units, the duration of the voltage sag compensation will decrease with increasing amplitude of voltage sag.

The data related to system specific calculations are shown in Table 1. The main circuit parameters are as follows: 32 modules and 384 submodules (768 IGBTs) in each bridge arm, a DC-rated voltage module for 900 V, a DC voltage of 28.8 kV in the normal operation of the power quality control system, and a capacitance of 4700 μF in each submodule. The specific data and system conditions are shown in Table 1.

Table 1. System parameters.

Variable	Value	Unit
System voltage	10	kV
Load capacity	5	MVA
Maximum compensation capacity on series side	3	MVA
Arm inductance	32	mH
Common DC operating voltage	28.8	kV
Common DC side minimum operating voltage	24	kV
Number of bridge arm modules	32	
Normal operating voltage of submodule DC	0.9	kV
Submodule DC side minimum operating voltage	0.75	kV
Submodule DC capacitance	4.7	mF

It is assumed that the load is essentially unchanged after the voltage sag occurs on the system side.

If the system voltage sags, then the load voltage must be compensated with the rated voltage, and the power of the series side is completely provided by the DC capacitor. The energy required for the compensation of the series compensation system is derived from the energy storage of the capacitor. According to the ITIC curve and the actual capacity of the compensation, different DC voltage reductions occur.

For example, in the DC side, when the voltage decreases from 28.8 kV to 24 kV, the maximum voltage of the series side can compensate for the decrease in 6 kV; thus, it can compensate for 60% sags. In addition, the compensation capacity of the series side is 3 MVA, which causes the voltage of each module to be decreased from 900 V to 750 V. The power flow is shown in Figure 9.

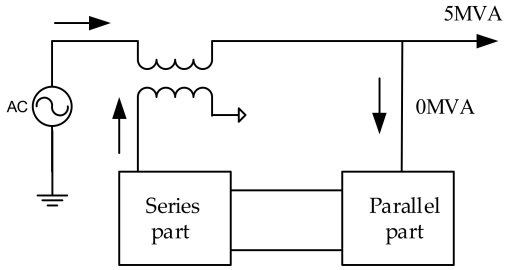


Figure 9. Power flow diagram of the UPQC.

At this time, the series side converter is equivalent to the operation of the DVR, and the DC side capacitance decreases from 28.8 kV to 24 kV when the output energy is as follows:

$$W = \frac{1}{2} \times C \times N \times (U_{SMN}^2 - U_{SM}^2) = \frac{1}{2} \times 4700 \times 10^{-6} \times 384 \times (900^2 - 750^2) = 223.34\,\text{kJ} \quad (15)$$

In Equation (15), C is the SM capacitor, N is the number of submodules, U_{SMN} is the rated voltage of the submodule, and U_{SM} is the voltage of the submodule when the DC side voltage is discharged to 24 kV.

$$\Delta t = \frac{W}{S} = \frac{W}{3 \times 10^6} = 74\,\text{ms} \quad (16)$$

Considering that the series side sag compensation system requires energy from the capacitor energy storage case, in the case of the 3 MVA series side output, the theoretical calculation for the duration of the compensation system for 60% voltage sag is 74 ms; considering the loss of switches and other components, which would slightly decrease the duration, an approximate estimate is 60 ms.

If the magnitude of the dip is below 60%, the corresponding series compensating voltage side output will be less than 6 kV, and then, the minimum DC voltage can be lower than 24 kV; the DC side capacitor can release more energy, and the duration of the compensation sag can be longer. Using the above calculation, the compensated sag amplitude and the supporting time are shown in Table 2, and the voltage sag amplitude and the support time diagram are shown in Figure 9.

Table 2. Voltage sag amplitude and theoretical support time.

Series Compensation Range	Minimum DC Voltage	Release Energy (kJ)	Support Time (ms)
60%	24	223.34	74
50%	20	378.44	151
40%	16	505.34	253
30%	16	505.34	337
20%	16	505.34	505
10%	16	505.34	1011

According to Table 2 and Figure 10, when the sag amplitude is relatively large, the support time of the UPQC sag compensation is relatively short, the sag amplitude is relatively low, and the support time for the sag compensation is relatively long. Through the above calculation, in the case of a certain loss, the choice of capacitor parameters can be achieved to suppress the 40% voltage sag for a support time of 200 ms and inhibit the voltage drop of 60% for a support time of 60 ms.

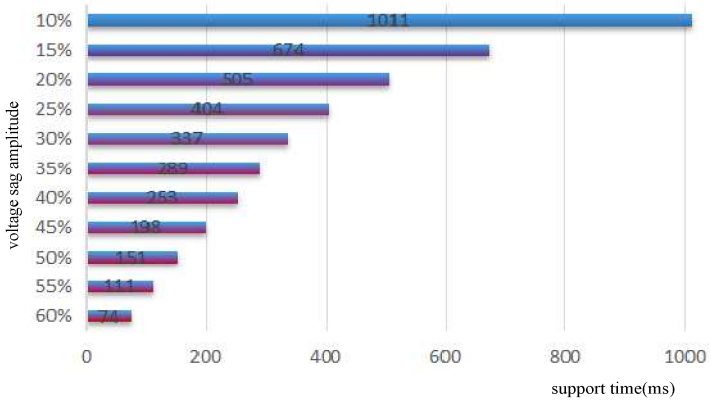


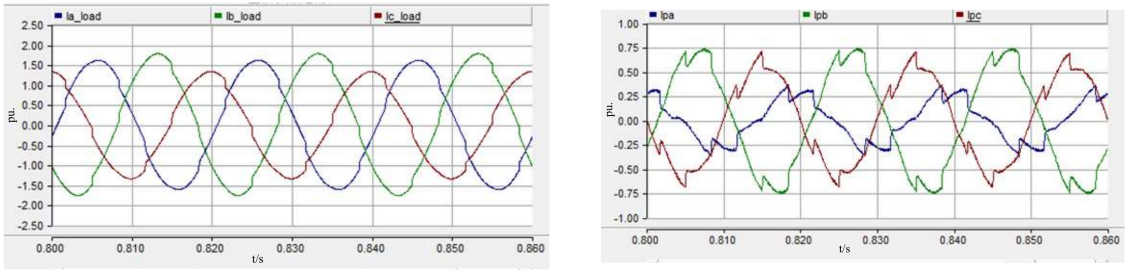
Figure 10. Voltage sag amplitude and support time.

4. Simulation Analysis and Experimental Study

4.1. Simulation Analysis

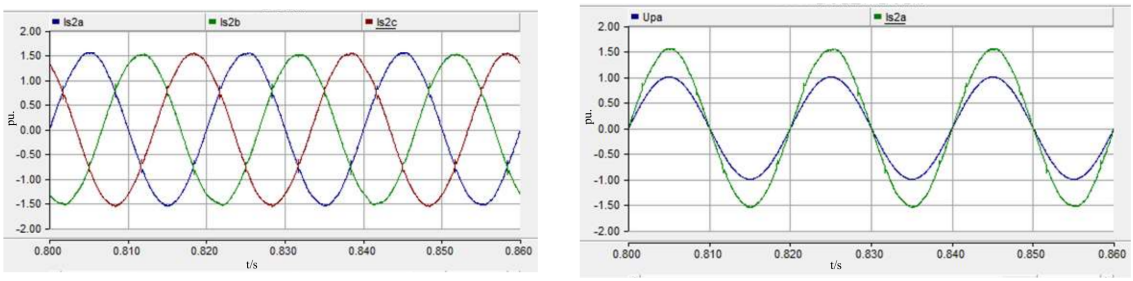
To verify the correctness of the theoretical analysis, a detailed electromagnetic transient simulation model of the UPQC based on the MMC is conducted under PSCAD/EMTDC, and the parameters of simulation are consistent with Table 1.

Figure 11 shows the waveform of the reactive compensation, the unbalanced current, and the harmonic current on the parallel side (the reactive current is 0.25 p.u., the negative sequence current is 0.25 p.u., and the harmonic current is 0.2 p.u.). (a) is the load current waveform, and it has obvious imbalance and a harmonic current; (b) is the current waveform output for the parallel side converter and the compensation of the negative sequence current, the reactive current, and the harmonic current; (c) is the current waveform of the power grid, and it has a good sinusoidal degree; and (d) is the single phase voltage of the power grid and the current waveform after compensation. It can be seen that it has the characteristics of the unit power factor.



(**a**) (**b**)

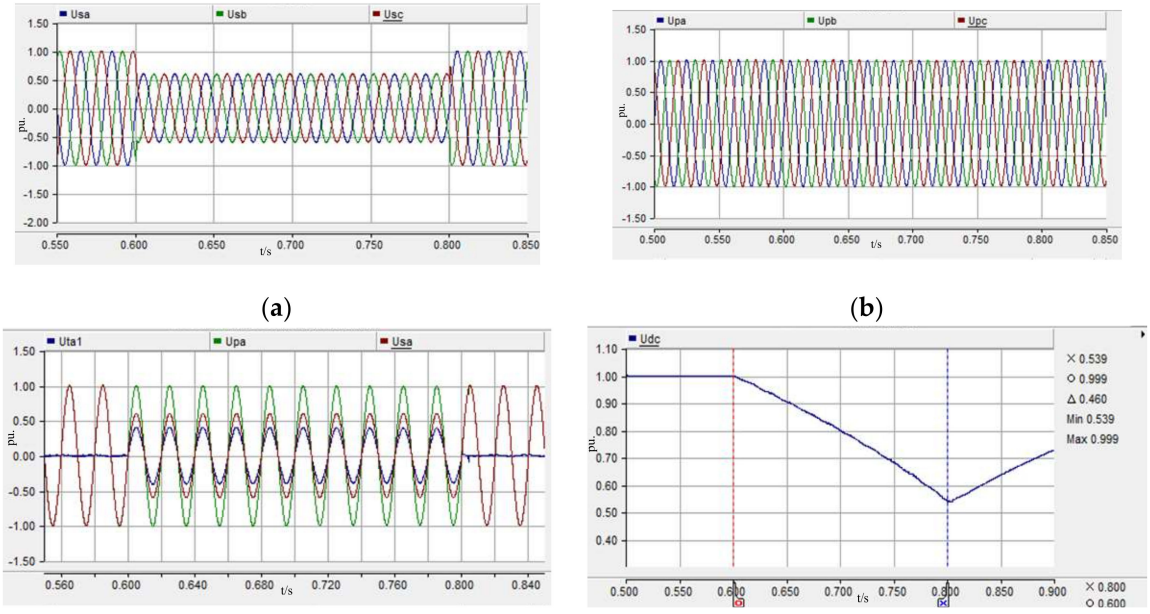
Figure 11. *Cont.*



(**c**) (**d**)

Figure 11. Comprehensive compensation for parallel side: (**a**) three-phase load current; (**b**) parallel side output current; (**c**) three-phase grid current; (**d**) voltage and current of single-phase power grid.

Figures 12 and 13 show the three-phase voltage sag of 40% and 60%, respectively. During the sag period, to avoid having overcurrent being inadequately controlled by the DC bus voltage, the series sag compensation depends mainly on the support of the energy storage in the capacitors. Figure 12 shows that for a sag of 40%, after 200 ms of sag compensation, the DC bus voltage drops to 0.57 (approximately 16 kV, to ensure the minimum DC bus voltage sag compensation of 40% control performance under the condition of good compensation); thus, the UPQC has sag 40%/200 ms support ability. Figure 13 shows that for a 60% sag, after approximately 70 ms of sag compensation, the DC bus voltage drops to 0.82 (approximately 24 kV, to ensure the minimum DC bus voltage sag compensation of 60% control performance under the condition of 60%) to achieve sag compensation in the 70 ms period. The theoretical calculation time is essentially the same as that of the simulation result.



(**a**) (**b**)

(**c**) (**d**)

Figure 12. Three-phase voltage sag of 40% (**a**) three-phase voltage of power grid; (**b**) load three-phase voltage; (**c**) grid voltage, load voltage, and compensation voltage; (**d**) DC bus voltage.

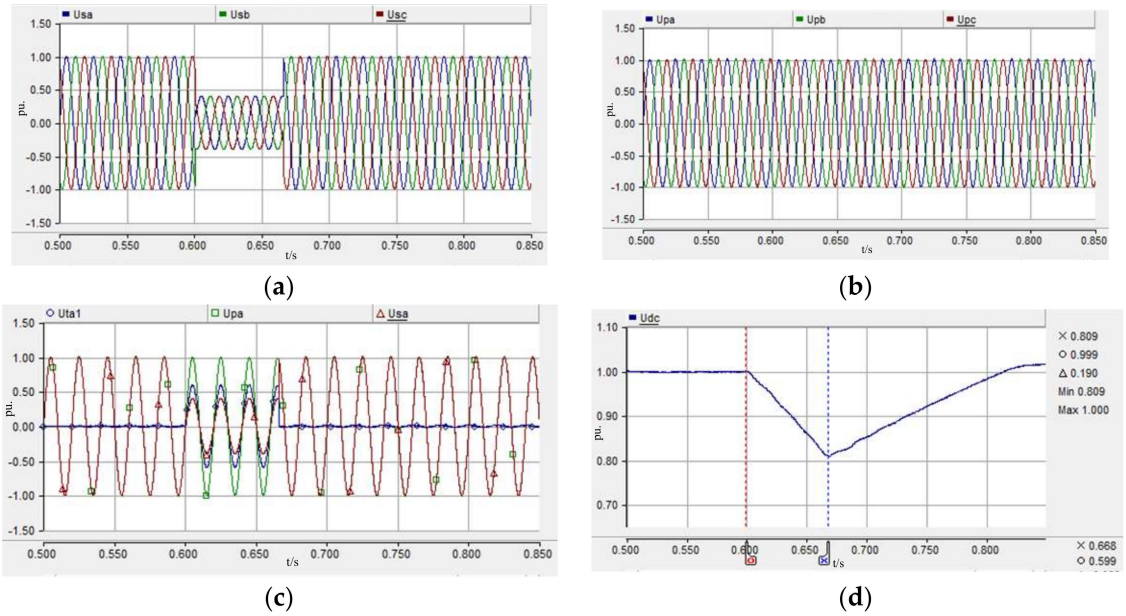


Figure 13. Three-phase voltage sag of 60%: (**a**) three-phase voltage of power grid; (**b**) load three-phase voltage; (**c**) grid voltage, load voltage, and compensation voltage; (**d**) DC bus voltage.

4.2. Experimental Study

An industrial prototype of the UPQC based on the MMC for 10 kV of a medium voltage distribution network has been developed. The topology and parameters are identical with Figure 1 and Table 1. It is installed in a 110 kV substation in Huizhou, Guangdong province, China. Preliminary experimental research has been carried out, and the basic functions of the UPQC have been tested.

The UPQC industrial prototype with a scale of 2 MVA on a series side converter and 2 MVA on a parallel converter comprises of a series side converter, parallel side converter bridge arm, reactor, filter reactor, filter capacitor, series transformer, special transformer, circuit breaker, isolating switch device, control system, monitoring system, and protection device. The series converter is connected in series to the selected outlet of the 10 kV feeder through the isolation transformer, and the parallel converter is directly connected to the 10 kV feeder.

The installation site of the UPQC prototype is all outdoors. The mobile container installation mode was adopted, while the series side converter valves, the parallel side converter valves, the high voltage switch cabinet, the low voltage control cabinet and so forth were adopted by one container. The high–low voltage equipment was separated, and the similar equipment was relatively centralized. Figure 14 is the layout of the UPQC prototype equipment, and Figure 15 is the scene picture of the UPQC device.

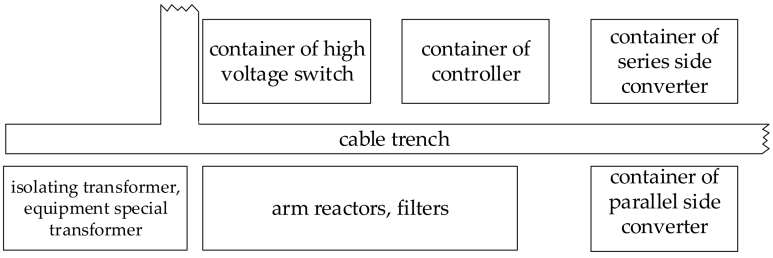


Figure 14. Layout of the UPQC prototype equipment.

Figure 15. Scene picture of the UPQC devices.

At present, only preliminary functional experiments have been completed, which means that open loop experiments have been carried out. Figures 16 and 17 are parallel side function experiments, and the experimental waveform has been recorded by the power quality analyzer Elspec G4500. Figure 15 shows the value of the reactive power, the RMS value of the output current of the parallel side, and the current waveform of the parallel side. The main test was conducted on the parallel side reactive power output (step 0 to 100%) to see the response time, which was less than 10 ms from the waveform. Figure 16 shows a comprehensive compensation function for testing the reactive, harmonic, and negative sequence current of the parallel side (10% of the rated reactive current, the 5 harmonic 5% rated current, the negative sequence current, and the 5% rated current combination of experimental output).

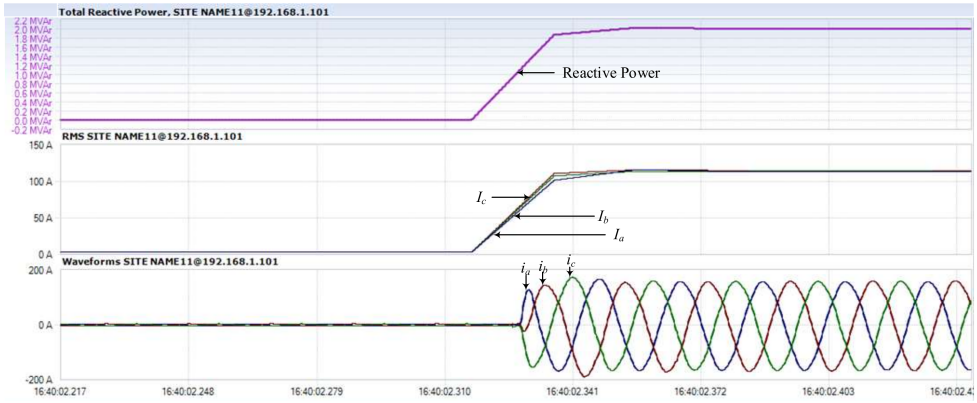


Figure 16. Reactive step response on the parallel side of the UPQC.

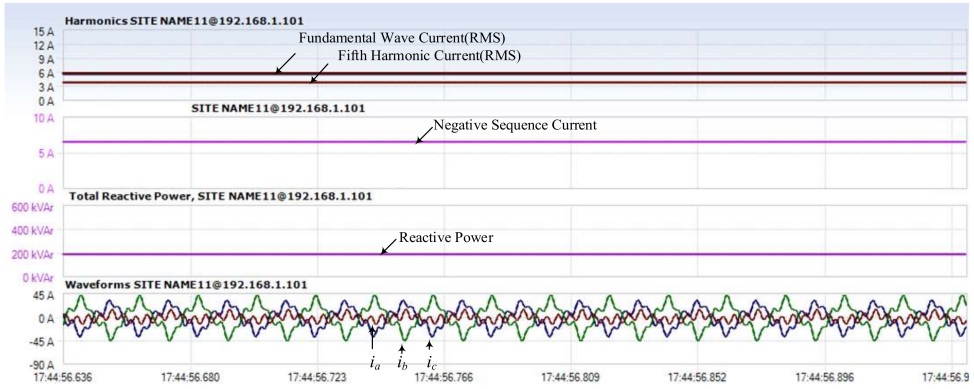


Figure 17. Combined function output on parallel side in UPQC.

Figure 18 shows the series side function experiment, and the experimental waveform is recorded by the oscilloscope Tektronix TDS2024. It also depicts the voltage sag compensation (manual output voltage of 5% instructions) and the response time, which was less than 5 ms, as seen from the waveform, which essentially achieved the functional requirements. The u_s in Figure 18 is the grid voltage, and the u_c is the reverse phase 5% voltage output from the UPQC series side MMC converter (with the purpose of testing its ability for voltage sags), and the u_{load} is the voltage of the load side value of 95%.

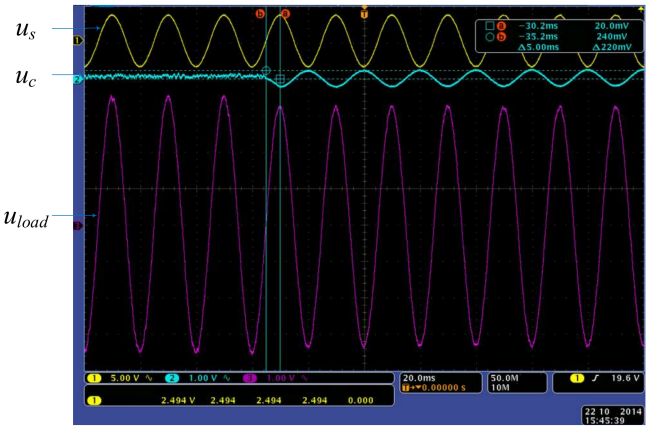


Figure 18. Compensation response upon series side voltage sag of the UPQC.

In the follow-up, we would further carry out various functional performance experiments to fully verify the performance of the industrial prototype.

5. Conclusions

This paper presented the UPQC based on the MMC. Due to the modular topology of the MMC and the characteristics of distributed energy storage, it is very suitable for the voltage sags compensation of the UPQC. Based on the analysis of the energy–flow relationship between the UPQC parallel converter and the series converter, this paper reveals the essence of the energy release of voltage sag compensation, and puts forward the corresponding UPQC series and parallel coordination control method using the MMC structure. Then, the performance index of voltage sag compensation was determined through energy storage theory calculations, and the range and support time of the UPQC sags compensation was defined. This laid the foundation for determining the operation mode of voltage sag compensation of the UPQC by utilizing the characteristics of the MMC dispersed energy storage. The simulation experiment of voltage sags compensation characteristics of the UPQC was carried out under PSCAD/EMTDC, the correctness of the theoretical calculation was verified, and finally, the UPQC industrial prototype of 10 kV based on the MMC was developed, and the basic functional experiment was carried out. However, this paper is only an analysis of the MMC based on the UPQC for power quality sags compensation. Future research should investigate other aspects of power quality, such as voltage fluctuation and flicker, unbalance, harmonics, mutual coupling, and other aspects of the in-depth analysis of the power quality indices that are not the same. The design of the UPQC parameters based on the MMC control of the UPQC is of great significance; in addition, since the number of SMs in the MMC is greater in the simulation of PSCAD/EMTDC, a detailed MMC electromagnetic transient model was used, and the speed of simulation was very slow, which greatly affected the efficiency of off-line simulation analysis. The switch function model of the MMC that has been proposed in literature [28] is a fairly good idea to accelerate the speed of simulation, and in the following study, we will adopt such a model to enhance the efficiency of simulation analysis. Lastly, the experiment of the UPQC industrial prototype based on the MMC structure was further carried out, and the control characteristics of the MMC were revealed more deeply from the physical experiment.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations and Nomenclature

MMC	modular multilevel converter
UPQC	unified power quality controller
APF	active power filter
SVC	static var compensator
SM	sub module
VSC	voltage source converter
NLM	nearest level modulation
PLL	phase locked loop
UCC	unit capacitance constant
PWM	pulse width modulation
SVPWM	space vector pulse width modulation
PI	proportional integral
FFT	fast Fourier transformation
RMS	root meam square
ITIC	Information Technology Industry Council

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