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A Novel Three-Level Voltage Source Converter for AC–DC–AC Conversion

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Abstract: This paper presents a novel three-level voltage source converter for AC–DC–AC conversion. The proposed converter based on H-bridge structure is studied in detail. The control method with traditional double-closed-loop control strategy and voltage balancing algorithm is applied to the rectifier side. Correspondingly, a simplified modulation algorithm is applied to the inverter side, and the voltage balancing of inverter side is realized through the optimal selection of switching combination. Then, the application of the proposed topology is assessed in general and ideal operation conditions. Furthermore, the proposed topology with a variable voltage variable frequency (VVVF) is verified in experimental conditions. The performance of the proposed converter and control strategy is evaluated by experimental and simulation results.

Keywords: three-level converter; simplified PWM strategy; redundant switching combination; voltage balance control

1. Introduction

With the development of the multilevel converter (MC), it has become a cost-effective solution of medium-voltage AC drives [1]. Due to its merits compared with a conventional two-level voltage source converter—such as lower voltage stress on switches, improved output waveforms, reduced common mode voltage, and high voltage capability—MC has been applied to more emerging fields [2–4]. The areas of applications include renewable energy generation, electric vehicle traction [5], high-power energy storage system [6], micro-grids [7], high-voltage ac or dc transmission [8–10], and some newly-developing fields.

In general, there are two conventional types of AC–DC–AC multilevel converters in view of whether it has common dc-links. The diode-clamped MC (DCMC) [11] and fly-capacitor MC (FCMC) [12] are widespread adopted structures with common dc-links, which can operate in four quadrants and be supplied by single rectifier. Besides, there are some other topologies, such as five-level active neutral-point-clamped MC (5L-ANPC) [13], modular MC (MMC) [9,10], and some newly-developed MC [14–16]. However, these kinds of MCs, except MMC, are hard to extend towards higher output voltage levels and power grades because of the complicated structures. The other drawback of these types is the poor ability to deal with some special systems which have different voltage grades, e.g., connection of two grids with different voltage grades [16–18]. Separated dc-links are the features of the other types of MCs, including cascaded H-bridge MC (CHBMC) [17], five-level H-bridge NPC (5L-HNPC) [18], and some hybrid and asymmetrical cascaded H-bridge MCs with

different sub-modules [19] or dc-link voltages [20]. It has the advantage of flexible extending of the output levels and power rating. However, the bulky and expensive phase-shifting transformers for isolated dc sources make it hard to increase the power density. A back-to-back CHB converter without any isolating device [21] can avoid these problems. However, short-circuits caused by the hardware topology are difficult to solve and the proposed topology cannot be expanded to a three phase system.

In this paper, a new three-level voltage source converter for AC–DC–AC conversion is proposed. It can be used in three-phase system and more easily to extend to higher voltage level than a back-to-back NPC converter. Compared to the back-to-back CHB converter proposed in [21], a half H-bridge cell used in the new topology provides more redundant vectors and makes it overcome the short-circuit problem, which simplifies the control method. In addition, the proposed topology utilizes fewer switches at the cost of increasing the number of dc-link capacitors, the separated dc links will decrease the total dc voltage of the system, which is beneficial for the insulation design in many fields [22].

The rest of the paper is organized as follows. In Section 2, the circuit configuration, characteristics and working principles of the proposed topology are studied in detail. The overall control strategy and pulse-width modulation strategy considering the voltage balance control is given in Section 3. In Section 4, two operation conditions are analyzed, and the simulation and experimental results demonstrate the effectiveness of the proposed control strategies. Section 5 concludes the paper.

2. Circuit Configuration of Proposed Three-Level Voltage Source Converter

2.1. Circuit Configuration

The proposed three-level converter is presented in Figure 1. It includes two basic submodules, power unit I and power unit II. Port 2 of power unit II in the three-phase topology is connected together, forming the neutral point N of the converter.

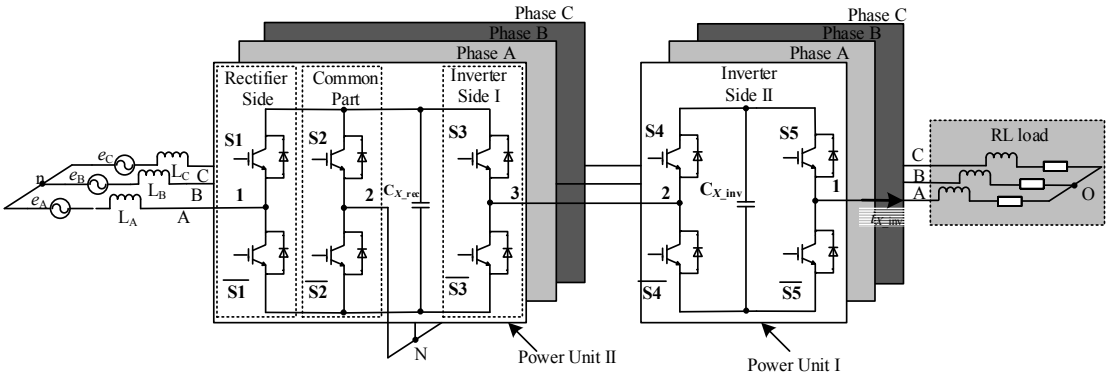

Figure 1. Circuit configuration of the proposed three-level voltage source converter.

For convenience, the rectifier side, common part, inverter side I, and inverter side II can be defined as shown in Figure 1. The rectifier side connects in series with three-phase inductors and the grid through three phase electrical terminals A, B, and C. The three electrical terminals A, B, and C of inverter side connect with the three-phase load.

2.2. Working Principle of Rectifier Side

All the dc-link voltage values are assumed to be equal to U_{dc}. Obviously, the output voltage levels relative to neutral point N are determined by S1/$\overline{S1}$ and S2/$\overline{S2}$. u_{X_rec} (X = A, B, C) is defined as the output voltage of rectifier side, which can be obtained as Equation (1).

$$u_{X\_rec} = (S1 - S2)U_{dc} \quad (1)$$

2.3. Working Principle of Inverter Side I

Combined with the common parts shown in Figure 1, inverter side I can produce three level voltages similar to u_{X_rec}. u_{X_inv} referenced to N is obtained as Equation (2).

$$u_{X\_inv} = (S3 - S2)U_{dc} \tag{2}$$

2.4. Master–Slave Control Principle

Combining with common part, there will be no problem obviously when rectifier side or inverter side I works independently. Due to the special structure, the operation principle of each side cannot be analyzed independently when they work together. In other words, there is a coupling relationship between two sides. Since any side can be chosen as the master control side, the rectifier side is chosen as an example. Hence the switching command of S2 is decided by rectifier side. Output voltage levels of u_{X_inv} will be limited in some switching combinations. For example, if rectifier side is P, S2 should be 0. However, if the inverter side I needs to be N, S2 should be 1. Consequently, a contradiction appears.

In order to reduce the coupling relationship, a submodule power unit I is added on the right of power unit II, which is defined as inverter side II, as shown in Figure 1. According to the switching states, the switching commands of S3S4S5 can be decided after switching commands of S1S2 are generated as shown in Table 1. The output voltage of inverter side, u_{X_inv} can be rewritten as Equation (3).

$$u_{X\_inv} = (S3 - S2)U_{dc} + (S5 - S4)U_{dc} \tag{3}$$

Table 1. Switching states of rectifier side and inverter side.

Rectifier State	S1 S2	Inverter State	S3 S4 S5
P	S1S2 = 10	P	S3 = 1, S4 = S5 or S3 = 0, S4 = 0, S5 = 1
		O	S3 = 0, S4 = S5 or S3 = 1, S4 = 1, S5 = 0
		N	S3 = 0, S4 = 1, S5 = 0
O	S1 = S2	P	S3 = S2, S4 = 0, S5 = 1 or S2 = 0, S3 = 1, S4 = S5
		O	S2 = S3, S4 = S5 or S2 = 1, S3 = 0,S4 = 0, S5 = 1 or S2 = 0, S3 = 1, S4 = 1, S5 = 0
		N	S2 = S3, S4 = 1, S5 = 0 or S2 = 1, S3 = 0, S4 = S5
N	S1S2 = 01	P	S3 = 1, S4 = 0, S5 = 1
		O	S3 = 1, S4 = S5 or S3 = 0, S4 = 0, S5 = 1
		N	S3 = 1, S4 = 1, S5 = 0 or S3 = 0, S4 = S5

2.5. Comparison with Classic Multilevel Topologies

For better understanding of the proposed technology, it is necessary to make a comparison over classic multilevel converter topologies. In order to achieve four-quadrant AC–DC–AC conversion, NPC, FC, and CHB are arranged in a back-to-back (B2B) scheme [23]. As a matter of convenience, the proposed topology is abbreviated as CMC. The state-of-the-art 4.5 kV, 450 A and 3.3 kV, 450 A IGBTs are applied in aforementioned three level and five level topologies, respectively, with the output line-to-line voltage V_{ll_rms} = 3 kV and power rating of 600 kW. It is assumed that the voltage rating of each clamping diode and flying capacitor is equal to the main switch device voltage rating. A comprehensive list of the requested components number of each converter topology is shown in Table 2 [24,25]. Obviously, the counts of active devices of these types are equal except the CMC, which needs two extra switches in each phase. A total of 36 diodes are requested in a five level B2B NPC converter, and the count will increase dramatically with the number of levels. Capacitors contain dc-link capacitors and flying capacitors, so the number of capacitors—as an example—for 5L B2B FC topology is 4 + 18. These large numbers of capacitors increase size and cost of the converter and reduce the reliability. Through the total component amount, CHB topology is extremely advantageous in

quantity in the Table, but it must be equipped with a transformer and PWM rectifier for four-quadrant applications. In the rest of the topologies, CMC topology, without clamping diodes and capacitors, has a lower number of components than other topologies with the improvement of voltage level.

Table 2. Comparison of different topologies (V_{ll_rms} = 3 kV, I_{ph_rms} = 115.5 A, P = 600 kW).

Level	**3L**				**5L**			
Topology	NPC	FC	CHB	CMC	NPC	FC	CHB	CMC
Rated device voltage (IGBT)	4.5 kV	4.5 kV	4.5 kV	4.5 kV	3.3 kV	3.3 kV	3.3 kV	3.3 kV
Rated device current (IGBT)	450 A	450 A	450 A	450 A	450 A	450 A	450 A	450 A
IGBTs	24	24	24	30	48	48	48	54
Diodes	12	---	---	---	36	---	---	---
Capacitors	2 + 0	2 + 6	3 + 0	6 + 0	4 + 0	4 + 18	6 + 0	12 + 0
Total Components	38	32	23	36	88	70	54	66

To compare with the B2B 3L-NPC, the switching losses for both topologies are calculated and normalized according to the method proposed in [26] and the datasheet of IGBT. The result is shown in Figure 2 where the modulation index of the inverter side ranges from 0.5 to 1.15 and the power factor of the load ranges from 0.7 to 1.

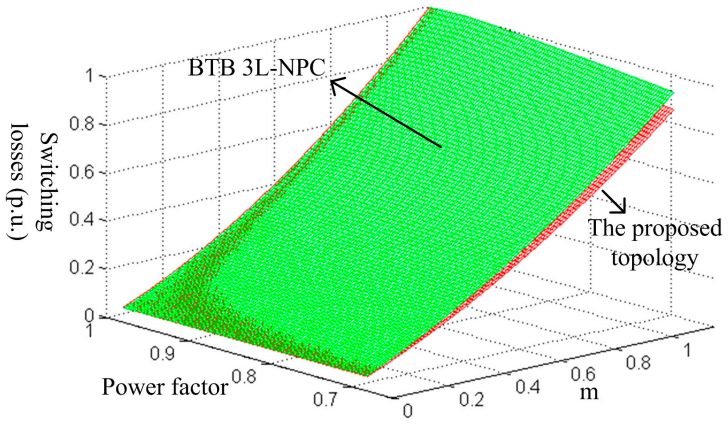

Figure 2. Switching losses comparison.

3. Control Method of the Proposed Three-Level Voltage Source Converter

3.1. Control Method

Since this work focuses on testing the proposed three-level converter topology, a common control method should be used. So dual close loop control structure in d–q synchronous reference frame is adopted in rectifier side [20]. The voltage loop contains a conventional proportional-integral (PI) controller to regulate the average value of capacitor voltage of C_{X_rec}, $U_{dc\_ave\_rec}$ to reference value U_{dcref_rec} (=U_{dc}). The reference current of the q-axis (i^*_q) is set to a certain value to adjust input power factor of the whole converter. Then, the inner current loops generate the reference voltage of rectifier side, $u^*_{X\_rec}$. Subsequently, the zero sequence voltage u_{z_rec} generated by the voltage balancing algorithm is injected to $u^*_{X\_rec}$ to control voltage values of C_{X_rec}. Then a simplified modulation algorithm in [27] is adopted to calculate the duration time of switching states, P/O/N, in the rectifier side and inverter side.

Due to the coupling relationship, proper switching commands of S2/S3/S4/S5 should be chosen to achieve voltage balancing of the capacitors C_{X_inv}. The optimal selection of switching combination (OSSC) is introduced later to generate the converter switching commands of S1~S5. The whole control block diagram of the proposed three-level converter is shown in Figure 3.

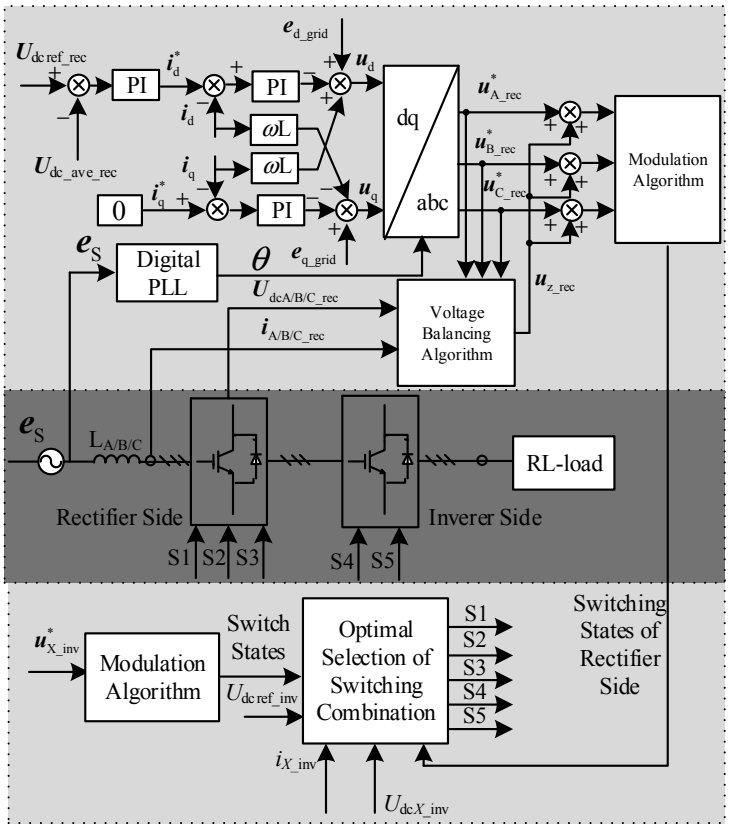

Figure 3. Control block diagram of the proposed multilevel converter.

3.2. Modulation Algorithm

A simplified PWM strategy [27] which is easier and more flexible to realize different targets was used as modulation algorithm. Taking inverter side as an example and assuming that $U_{\mathrm{dcref\_inv}} = U_{\mathrm{dc}}$, $u_{X\_\mathrm{inv}}(t)$ consists of U_{dc} and 0 when the reference voltage $u^*_{X\_\mathrm{inv}} > 0$; otherwise, $u_{X\_\mathrm{inv}}(t)$ consists of $-U_{\mathrm{dc}}$ and 0. This divides the space vector diagram into six sectors, as denoted by S in Figure 4.

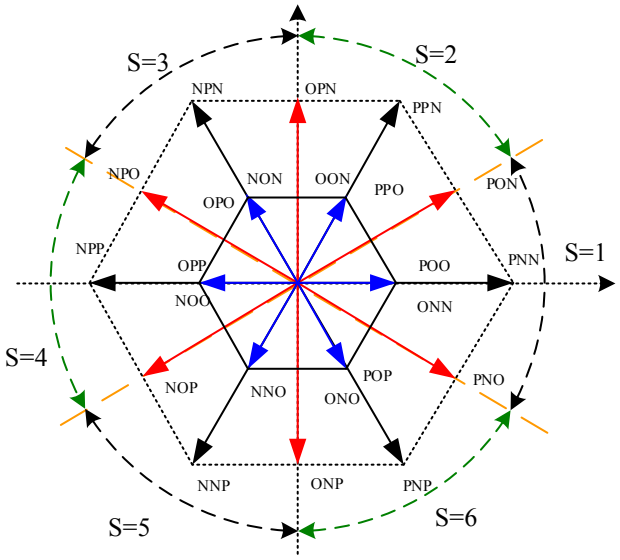

Figure 4. Sectors for the proposed three-level converter with the simplified PWM.

When S = 1, the voltage-second balancing principle can be represented by Equation (4), where u_z represents the equivalent zero-sequence voltage. The general solutions of (4) can be obtained as Equation (5).

$$\begin{cases} u^*_{\mathrm{A\_inv}} \cdot T_\mathrm{s} = \int_0^{T_\mathrm{s}} u_\mathrm{AN}(t)dt + \int_0^{T_\mathrm{s}} u_\mathrm{z}(t)dt \\ u^*_{\mathrm{B\_inv}} \cdot T_\mathrm{s} = \int_0^{T_\mathrm{s}} u_\mathrm{BN}(t)dt + \int_0^{T_\mathrm{s}} u_\mathrm{z}(t)dt \\ u^*_{\mathrm{C\_inv}} \cdot T_\mathrm{s} = \int_0^{T_\mathrm{s}} u_\mathrm{CN}(t)dt + \int_0^{T_\mathrm{s}} u_\mathrm{z}(t)dt \end{cases}, \tag{4}$$

$$\begin{cases} T_{\mathrm{A\_inv}} = (u^*_{\mathrm{A\_inv}} - u_\mathrm{z}) \cdot T_\mathrm{s}/U_{\mathrm{dcA\_inv}} \\ T_{\mathrm{B\_inv}} = T_\mathrm{s} + (u^*_{\mathrm{B\_inv}} - u_\mathrm{z}) \cdot T_\mathrm{s}/U_{\mathrm{dcB\_inv}} \\ T_{C\_inv} = T_\mathrm{s} + (u^*_{\mathrm{C\_inv}} - u_\mathrm{z}) \cdot T_\mathrm{s}/U_{\mathrm{dcC\_inv}} \end{cases}, \tag{5}$$

T_{X_inv} stands for the duration time of switching state P when ($u^*{}_{\mathrm{X\_inv}} - u_\mathrm{z} > 0$) otherwise stands for the duration time of O.

3.3. Voltage Balancing Algorithm of Rectifier Side

There is only one capacitor in each phase. It only needs to consider the voltage balancing of $\mathrm{C}_{\mathrm{X\_rec}}$ between three-phase. Assuming that $u_{\mathrm{z\_rec}}$ is the zero sequence voltage injected into $u^*{}_{\mathrm{X\_rec}}$, which is used to realize the targets of voltage balancing of $\mathrm{C}_{\mathrm{X\_rec}}$. The voltage-second balancing principle can be represented by Equation (6).

$$\begin{cases} T_{\mathrm{A\_rec}} = (u^*_{\mathrm{A\_rec}} - u_{\mathrm{z\_rec}}) \cdot \mathrm{T_s}/U_{\mathrm{dcA\_rec}} \\ T_{\mathrm{B\_rec}} = T_\mathrm{s} + (u^*_{\mathrm{B\_rec}} - u_{\mathrm{z\_rec}}) \cdot \mathrm{T_s}/U_{\mathrm{dcB\_rec}} \\ T_{\mathrm{C\_rec}} = T_\mathrm{s} + (u^*_{\mathrm{C\_rec}} - u_{\mathrm{z\_rec}}) \cdot \mathrm{T_s}/U_{\mathrm{dcC\_rec}} \end{cases}, \tag{6}$$

If $U_{\mathrm{dcX\_rec}}$ is imbalanced, $u_{\mathrm{z\_rec}}$ should be calculated to adjust the reference voltage $u^*{}_{\mathrm{X\_rec}}$. As an example, if voltage values of $\mathrm{C}_{\mathrm{X\_rec}}$ satisfy $U_{\mathrm{dcA\_rec}} > U_{\mathrm{dcB\_rec}} > U_{\mathrm{dcC\_rec}}$, it means that the magnitude of charge change within T_s should be $Q_\mathrm{A} < Q_\mathrm{B} < Q_\mathrm{C}$. $u_{\mathrm{z\_rec}}$ can be changed to adjust Q_X. Calculation of $u_{\mathrm{z\_rec}}$ is as follows:

1. Q_X, $u^*{}_{\mathrm{X\_rec}}$, and $i_{\mathrm{X\_rec}}$ are sorted according to $U_{\mathrm{dcX\_rec}}$. In order to realize the voltage balancing, Q_X should satisfy Equation (7).

$$Q_\mathrm{max} < Q_\mathrm{mid} < Q_\mathrm{min}, \tag{7}$$

Q_X is defined as Equation (8).

$$Q_X = i_{\mathrm{X\_rec}} \cdot \frac{u^*_{\mathrm{X\_rec}} - u_{\mathrm{z\_rec}}}{U_{\mathrm{dcX\_rec}}} \cdot T_\mathrm{s}, \tag{8}$$

If $i_{\mathrm{X\_rec}} > 0$ and ($u^*{}_{\mathrm{X\_rec}} - u_{\mathrm{z\_rec}}$) > 0, $u_{\mathrm{X\_rec}}$ consists of P/O. The current paths of S1S2 are shown in Figure 5. Obviously, $Q_X > 0$ and $\mathrm{C}_{\mathrm{X\_rec}}$ is charged in this case. $\mathrm{C}_{\mathrm{X\_rec}}$ is discharged within T_s when $i_{\mathrm{X\_rec}} < 0$ and ($u^*{}_{\mathrm{X\_rec}} - u_{\mathrm{z\_rec}}$) > 0.

2. Substituting (8) into (7) gives (9).

$$i_{\mathrm{max\_rec}} \cdot \frac{u^*_{\mathrm{max\_rec}} - u_{\mathrm{z\_rec}}}{U_{\mathrm{dcmax\_rec}}} \cdot T_\mathrm{s} < i_{mid\_\mathrm{rec}} \cdot \frac{u^*_{\mathrm{mid\_rec}} - u_{\mathrm{z\_rec}}}{U_{\mathrm{dcmid\_rec}}} \cdot T_\mathrm{s} < i_{\mathrm{min\_rec}} \cdot \frac{u^*_{\mathrm{min\_rec}} - u_{\mathrm{z\_rec}}}{U_{\mathrm{dcmin\_rec}}} \cdot T_\mathrm{s}, \tag{9}$$

$$\begin{cases} a1 = i_{\mathrm{max\_rec}} \cdot U_{\mathrm{dcmid\_rec}} - i_{mid\_\mathrm{rec}} \cdot U_{\mathrm{dcmax\_rec}} \\ b1 = i_{\mathrm{max\_rec}} \cdot u^*_{\mathrm{mid\_rec}} \cdot U_{\mathrm{dcmid\_rec}} - i_{mid\_\mathrm{rec}} \cdot u^*_{\mathrm{mid\_rec}} \cdot U_{\mathrm{dcmax\_rec}} \\ a2 = i_{\mathrm{mid\_rec}} \cdot U_{\mathrm{dcmin\_rec}} - i_{min\_\mathrm{rec}} \cdot U_{\mathrm{dcmid\_rec}} \\ b2 = i_{\mathrm{mid\_rec}} \cdot u^*_{\mathrm{mid\_rec}} \cdot U_{\mathrm{dcmin\_rec}} - i_{min\_\mathrm{rec}} \cdot u^*_{\mathrm{min\_rec}} \cdot U_{\mathrm{dcmid\_rec}} \end{cases}, \tag{10}$$

$$u_{\mathrm{temp1}} = b1/a1, \text{ and } u_{\mathrm{temp2}} = b2/a2.$$

3. The range of u_{z_rec} can be obtained from Equation (9), and u_{z_rec} can take any value within the range. However, it should satisfy Equation (11) to acquire a linear modulation.

$$\begin{cases} -U_{dcmax\_rec} \le u^*_{max\_rec} - u_{z\_rec} \le U_{dcmax\_rec} \\ -U_{dcmid\_rec} \le u^*_{mid\_rec} - u_{z\_rec} \le U_{dcmid\_rec} \\ -U_{dcmin\_rec} \le u^*_{min\_rec} - u_{z\_rec} \le U_{dcmin\_rec} \end{cases}, \tag{11}$$

4. Calculating the limit value of u_{z_rec}: the corresponding limitations of the injected zero-sequence voltages are given in (12).

$$\begin{cases} u_{zmax} = \max(u^*_{max\_rec} - U_{dcmax\_rec}, u^*_{mid\_rec} - U_{dcmid\_rec}, \\ u^*_{min\_rec} - U_{dcmin\_rec}) \\ u_{zmin} = \min(u^*_{max\_rec} + U_{dcmax\_rec}, u^*_{mid\_rec} + U_{dcmid\_rec}, \\ u^*_{min\_rec} + U_{dcmin\_rec}) \end{cases}, \tag{12}$$

Finally, u_{z_rec} can be obtained to realize the targets of voltage balancing as shown in Table 3. The voltage balancing algorithm is shown in Figure 6 in detail.

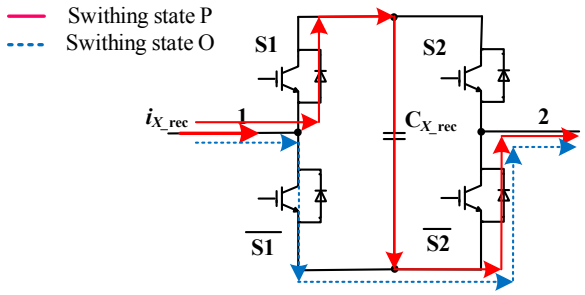

Figure 5. Voltage balancing algorithm of C_{X_rec}.

Table 3. Value of u_{z_rec}.

*a*1	*a*2	u_{temp1}, u_{temp2}	u_{z_rec}
>0	>0	$u_{temp1} > u_{temp2}$	u_{temp1}
		$u_{temp1} \le u_{temp2}$	u_{temp2}
	<0	$u_{temp1} > u_{temp2}$	0
		$u_{temp1} \le u_{temp2}$	$(u_{temp1} + u_{temp2})/2$
<0	>0	$u_{temp1} > u_{temp2}$	$(u_{temp1} + u_{temp2})/2$
		$u_{temp1} \le u_{temp2}$	0
	<0	$u_{temp1} > u_{temp2}$	u_{temp2}
		$u_{temp1} \le u_{temp2}$	u_{temp1}

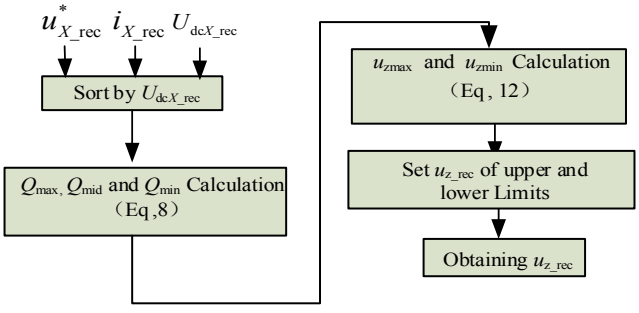

Figure 6. Current paths of S1S2 when $i_{X\_rec} > 0$ and $(u^*_{X\_rec} - u_{z\_rec}) > 0$.

3.4. Voltage Balancing Method of Inverter Side

Maintaining voltage balancing of the flying-capacitors in the inverter side is the main aim of this section. As introduced before, the coupling relationship shown in Table 1 can provide considerable number of redundant switching combinations. These combinations can provide a charging or discharging current paths for each flying-capacitors. The voltage balance control can be realized by selecting a proper combination. The optimal selection of switching combination can be generated as follows.

3.4.1. Effect of the Switching States on the Capacitors Voltages

According to Equation (3), the switching states of the inverter side P/O/N can be generated by inverter side I or II. However, only the switching states produced by inverter side II (S4S5) have an effect on the capacitors voltages U_{dcX_inv}. Which inverter side is selected to generate the required switching states is decided by the inverter state, the direction of i_{X_inv}, and switching commands of S2 as listed in Table 4.

For example, when the inverter state is P, $i_{X\_inv} > 0$, and S2 = 0, the switching state can be generated as marked in the Table 4. The discharging and keeping paths of capacitor C_{X_inv} have been shown in Figure 7, respectively.

Table 4. Switching states of rectifier side and inverter side.

Inverter State	i_{X_inv}	S2	Inverter Side I	Inverter Side II	Switch Combinations	Charge State
P	>0	1	O	P	S3S4S5 = 101	D
		0	O	P	S3S4S5 = 001	D
			P	O	S3 = 1, S4 = S5	K
	≤0	1	O	P	S3S4S5 = 101	C
		0	P	O	S3 = 1, S4 = S5	K
			O	P	S3S4S5 = 001	C
O	>0	1	N	P	S3S4S5 = 001	D
			O	O	S3 = 1, S4 = S5	K
		0	O	O	S3 = 0, S4 = S5	K
			P	N	S3S4S5 = 110	C
	≤0	1	O	O	S3 = 1, S4 = S5	K
			N	P	S3S4S5 = 001	C
		0	P	N	S3S4S5 = 110	D
			O	O	S3 = 0, S4 = S5	K
N	>0	1	N	O	S3 = 0, S4 = S5	K
			O	N	S3S4S5 = 110	C
		0	O	N	S3S4S5 = 010	C
		1	O	N	S3S4S5 = 110	D
			N	O	S3 = 0, S4 = S5	K
		0	O	N	S3S4S5 = 010	D

C: Charging; D: Discharge; K: Keeping.

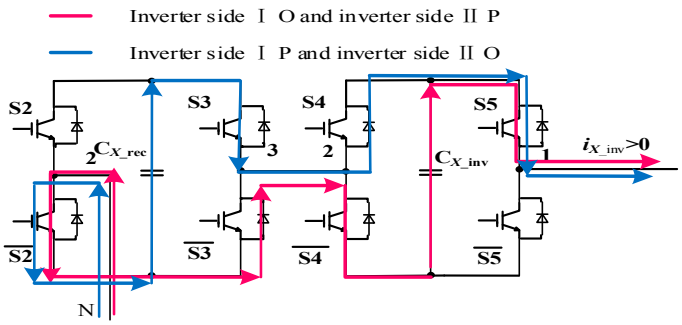

Figure 7. The discharging and keeping paths of capacitor C_{X_inv}.

3.4.2. Optimal Selection of Switching Combination (OSSC)

To balance the voltage of C_{X_inv}, OSSC is set to select proper switching combinations after the previous step (1). Before selecting the switching combination, the duration of switching state (T_{X_rec}/T_{X_inv}) is calculated through the simplified modulation algorithm in [27], thus the inverter state and rectifier state are determined. The switching commands of S2 should be a certain state 0(1) if the rectifier side is P(N). While it cannot be decided when rectifier side is O. Based on the actual situation, i_{X_inv} can be measured. To analyze the working principle of OSSC, the two examples are listed.

$$\begin{array}{c}(u^*_{A\_rec} - u_{z\_rec}) < 0,\ (u^*_{A\_inv} - u_z) > \\ U_{dcA\_inv} > U_{dcref\_inv}\end{array} \begin{cases} \text{Condition I}: & i_{X\_inv} > 0 \\ \text{Condition II}: & i_{X\_inv} > 0 \end{cases}, \quad (13)$$

Condition I: U_{dcA_inv} should be decreased with a proper switching combination. Referring to Table 4, when the switching state of the rectifier and inverter sides are N (S2 = 1) and O, respectively, there are two switching combinations to choose from the Table 4. It is obvious that the combination S2S3S4S5 = 1001 is the optimal one to decrease the voltage deviation in condition I. In this way, the combination of switch can be selected out at different switching states as shown in Figure 8a.

Condition II: Due to $i_{X\_inv} < 0$, the P state should be generated by the inverter side I as much as possible. Similarly, the combination of switching can be acquired referring the Table 4. When the calculation result of duration satisfied the inequality $T_{A\_rec} < T_{A\_inv}$, the situation that the switching state of rectifier and inverter side are N (S2 = 1) and P will exist as shaded areas depicted in Figure 8b. In this situation, no discharge switching combination can be found except a charge combination in Table 4. Therefore, the deviation of C_{X_inv} is uncontrollable. Those situations, defined as 'uncontrollable switching combination' (USC), restrict the operation range of the converter.

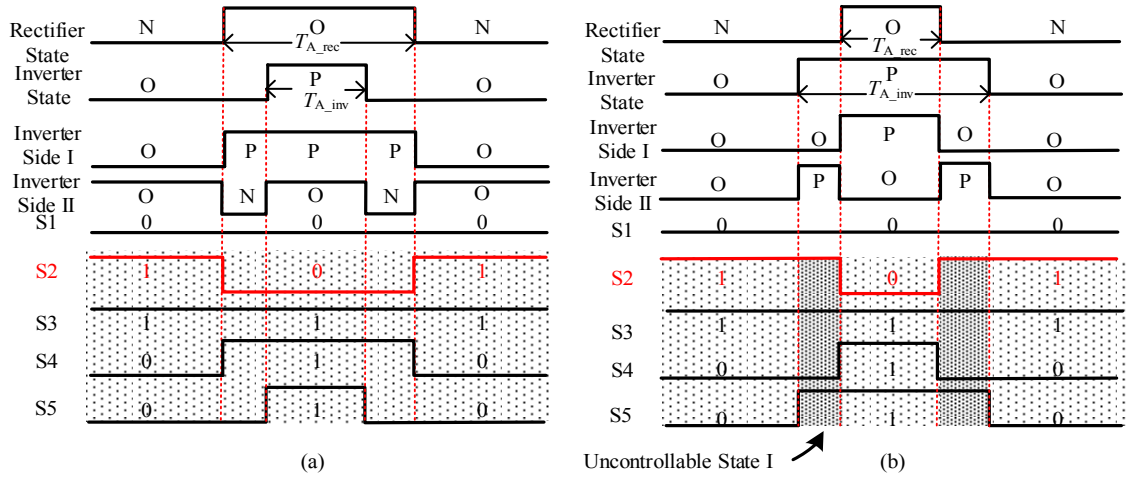

Figure 8. Converter state and switching commands. (**a**) $(u^*_{A\_rec} - u_{z\_rec}) < 0$, $(u^*_{A\_inv} - u_z) > 0$, and $U_{dcA\_inv} > U_{dcref\_inv}$; $i_{X\_inv} > 0$, $T_{A\_rec} > T_{A\_inv}$; (**b**) $(u^*_{A\_rec} - u_{z\_rec}) < 0$, $(u^*_{A\_inv} - u_z) > 0$, and $U_{dcA\_inv} > U_{dcref\_inv}$; $i_{X\_inv} < 0$, $T_{A\_rec} < T_{A\_inv}$.

3.5. Calculation of Duration Time of Each Arm

Based on the above analysis, the optimal selection of switching combination can be acquired. Then the duration time of S1~S5 in the proposed three-level converter can be calculated easily in each case as shown in Table 5. It should be noted that the high or low of S2 should be transformed as shown in Figure 8b. Then the trigger signals of each switch can be generated easily according to Table 5 in the proposed three-level converter.

Table 5. Switching states of rectifier side and inverter side.

$u^*_{A\_rec} - u_{z\_rec}$	$u^*_{A\_inv} - u_z$	U_{dcA_inv}	i_{A_inv}	t_{S1}	t_{S2}	t_{S3}	t_{S4}	t_{S5}
>0	>0	$U_{dcA\_inv} > U_{dcref\_inv}$	>0	T_{A_rec}	0	0	0	T_{A_inv}
			≤0	T_{A_rec}	0	T_s	T_s	T_{A_inv}
		$U_{dcA\_inv} \leq U_{dcref\_inv}$	>0					
			≤0	T_{A_rec}	0	0	0	T_{A_inv}
	≤0	$U_{dcA\_inv} > U_{dcref\_inv}$	>0	T_s	T_{A_rec}	0	T_{A_rec}	T_{A_inv}
			≤0	T_{A_rec}	0	T_{A_inv}	T_s	0
		$U_{dcA\_inv} \leq U_{dcref\_inv}$	>0					
			≤0	T_s	T_{A_rec}	0	T_{A_rec}	T_{A_inv}
≤0	>0	$U_{dcA\_inv} > U_{dcref\_inv}$	>0	T_{A_rec}	T_s	T_{A_inv}	0	T_s
			≤0	0	T_{A_rec}	T_s	T_{A_rec}	T_{A_inv}
		$U_{dcA\_inv} \leq U_{dcref\_inv}$	>0					
			≤0	T_{A_rec}	T_s	T_{A_inv}	0	T_s
	≤0	$U_{dcA\_inv} > U_{dcref\_inv}$	>0	T_{A_rec}	T_s	0	0	T_{A_inv}
			≤0	T_{A_rec}	T_s	T_s	T_s	T_{A_inv}
		$U_{dcA\_inv} \leq U_{dcref\_inv}$	>0					
			≤0	T_{A_rec}	T_s	0	0	T_{A_inv}

$t_{S1\sim S5}$ is the duration time of each switch, S1~S5.

4. Simulation and Experimental Analysis

4.1. Operation of the Proposed Three-Level Voltage Source Converter

4.1.1. Ideal Operation Condition

The ideal operation condition of the proposed converter is that the sign of output voltages are synchronized to the input voltages, if Equation (14) is satisfied

$$\mathrm{Sgn}(u^*_{X\_rec} - u_{z\_rec}) = \mathrm{Sgn}(u^*_{X\_inv} - u_z), \tag{14}$$

there will be no uncontrollable cases based on the above analyses in this operation condition. That is, the voltage deviation of C_{X_inv} will be kept under control completely. Although this condition can balance the capacitor voltages well, the use of this structure is restricted in some applications such as power electronic transformers and AC regulators.

4.1.2. General Operation Condition

In this condition, there is no connection between $\mathrm{Sgn}(u^*_{X\_rec} - u_{z\_rec})$ and $\mathrm{Sgn}(u^*_{X\ \_inv} - u_z)$, the reference voltage of inverter side

$(u^*_{X\_inv} - u_z)$ can operate at the frequency and magnitude different with $(u^*_{X\_rec} - u_{z\_rec})$. Figure 9a has been drawn to illustrate the extreme case when $U_{dcX\_inv} < U_{dcref\_inv}$, $\mathrm{Sgn}(u^*_{X\_rec} - u_{z\_rec}) = -\mathrm{Sgn}(u^*_{X\_inv} - u_z)$. Based on Table 5, voltage deviation of C_{A_inv} is enlarged in most areas. However, the shadow areas can be removed under the condition that the modulation index of the rectifier side and inverter side satisfy Equation (15). Then, voltage deviation can be controlled in this extreme case.

$$m_{inv} \leq 1 - m_{rec} = 1 - \frac{\mathrm{magnitude}(u^*_{X\_rec} - u_{z\_rec})}{U_{dc}}, \tag{15}$$

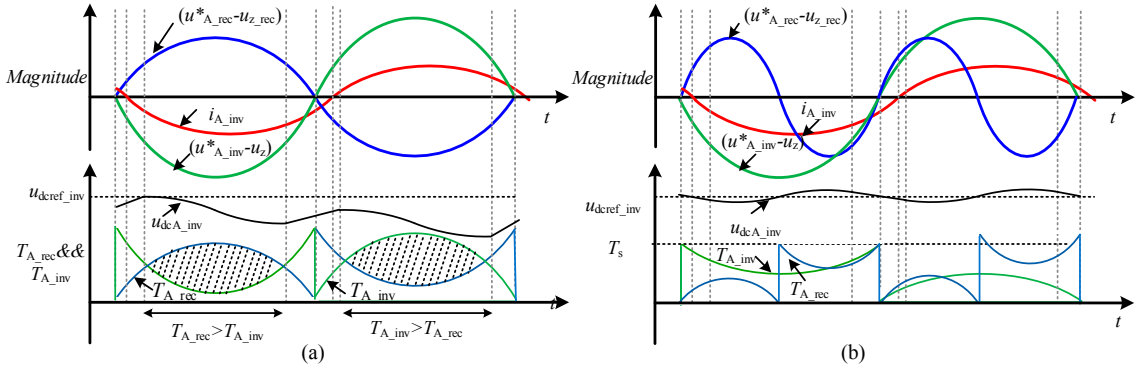

Figure 9. Analysis of voltage deviation with C_{A_inv}. (**a**) When $\mathrm{Sgn}|(u^*_{A\_rec} - u_{z\_rec})| = -\mathrm{Sgn}|(u^*_{A\_inv} - u_z)|$; (**b**) when $m_{inv} < 1 - m_{rec}$.

Including this special case, the uncontrollable states can be eliminated absolutely when $\mathrm{Sgn}(u^*_{X\_rec} - u_{z\_rec}) \neq \mathrm{Sgn}(u^*_{X\_inv} - u_z)$ and $m_{inv} \leq 1 - m_{rec}$ as shown in Figure 9b. Although the time of uncontrollable state can be quantified as shown in Figure 9b when $m_{inv} \geq 1 - m_{rec}$, the voltage deviation of C_{X_inv} still cannot be improved without efficient measures. Hence, the magnitude of output voltage will be limited. DC voltage deviation and low-frequency fluctuation will exist in the whole system.

4.2. Experimental Results

A low power prototype has been developed in lab conditions to verify the performance of the proposed three-level converter, as depicted in Figure 10. The three-level converter was built by using power IGBTs (TOSHIBA, Tokyo, Japan). The control method was implemented in a 150-MIPS float-point 32-bit TMS320F28335 board, and XC3S500E-4PQ208C of XILINX Company (San Jose, CA, USA) has been used to generate switching commands. The experimental parameter settings are shown in Table 6. In order to observe necessary signals, two scopes were used to monitor the signals after DA conversion. U_{AB_inv} was measured by voltage probes directly.

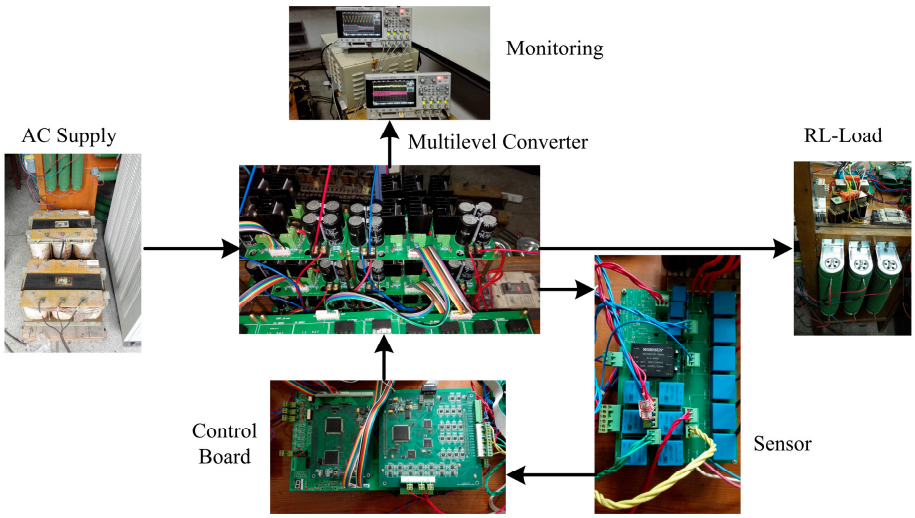

Figure 10. Experimental setup for the proposed multilevel converter.

Table 6. Parameter settings for simulation and experiment.

Parameter	Value
Source voltage, e_{X_rec}	55 V
DC-link voltage	100 V
DC-link capacitor	1200 μF
Filter-inductive	2.2 mH
Resistive-inductive load	20 Ω, 2.2 mH
Switching frequency	5 kHz

The experimental results obtained in Figure 11 show the voltage–current waveforms of the rectifier side and inverter side at different modulation indexes m_{inv} and switching frequency f during the whole working process. Figure 11a,c shows that the three-phase current i_{X_rec} rectifier side and i_{X_inv} inverter side increase with the increase of modulation index and frequency. In Figure 11c, the waveforms of line-to-line voltage u_{AB_inv} have three-levels when f = 20 Hz, m_{inv} = 0.4 and f = 30 Hz, m_{inv} = 0.6, while it changes to five-levels when f = 40 Hz, m_{inv} = 0.8 and f = 50 Hz, m_{inv} = 0.9. $U_{\text{dcX\_rec}}$ and $U_{\text{dcX\_inv}}$ are shown in Figure 11b,d are the waveforms of three-phase capacity of C_{X_rec} and C_{X_inv}. It can be seen that $U_{\text{dcX\_rec}}$ and $U_{\text{dcX\_inv}}$ do not change with the modulation index and frequency after the system is working. Capacitor voltages can be balanced well, and better performance of the proposed multilevel converter is verified in this process. Figure 12 shows the performance of the converter in transient-state condition with the modulation index m_{inv} changing from 0.4 to 0.6 and output frequency f changing from 20 Hz to 30 Hz. Figure 12a,b shows the input voltage–current waveforms and voltage waveforms of C_{X_rec}. Figure 12c show the waveforms of line-to-line voltage u_{AB_inv} and three-phase currents i_{X_inv}. The capacitor voltages of C_{X_inv}, $U_{\text{dcX\_rec}}$ are shown in Figure 12d.

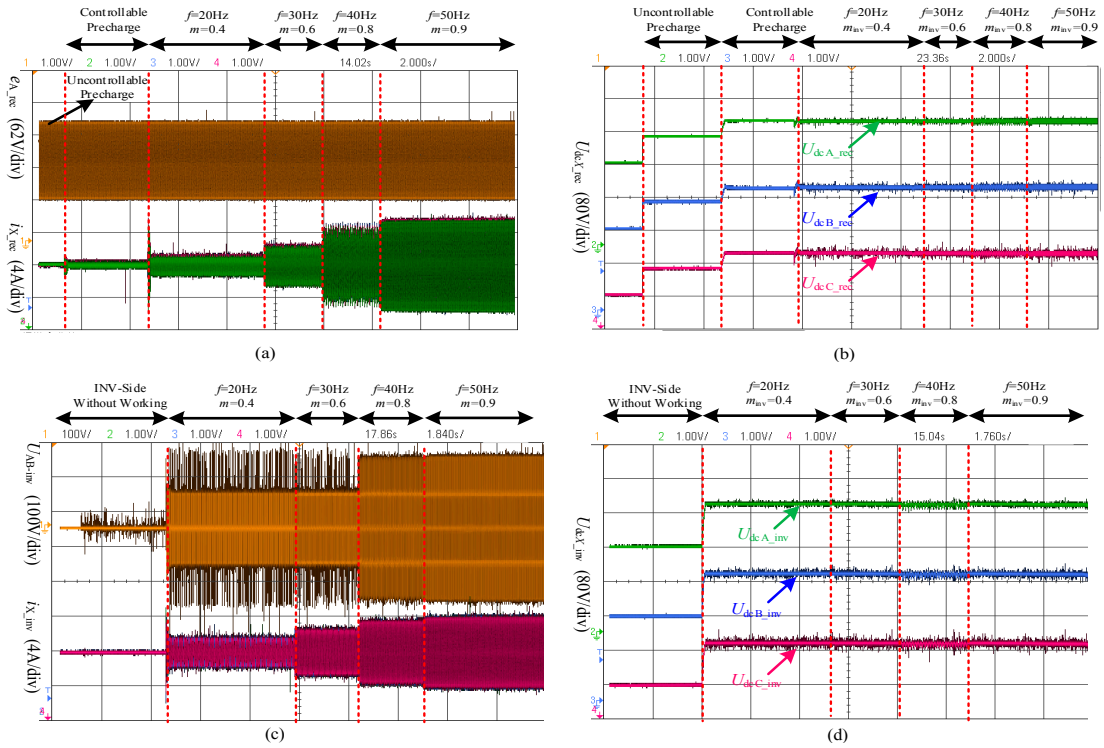

Figure 11. Experimental results of the whole working-process in transient-state condition; (**a**) Input voltage–current waveforms, e_{A_rec} and i_{X_rec}; (**b**) voltages of C_{X_rec}; (**c**) output voltage–current waveforms, u_{AB_inv} and i_{X_inv}; (**d**) voltages of C_{X_inv}.

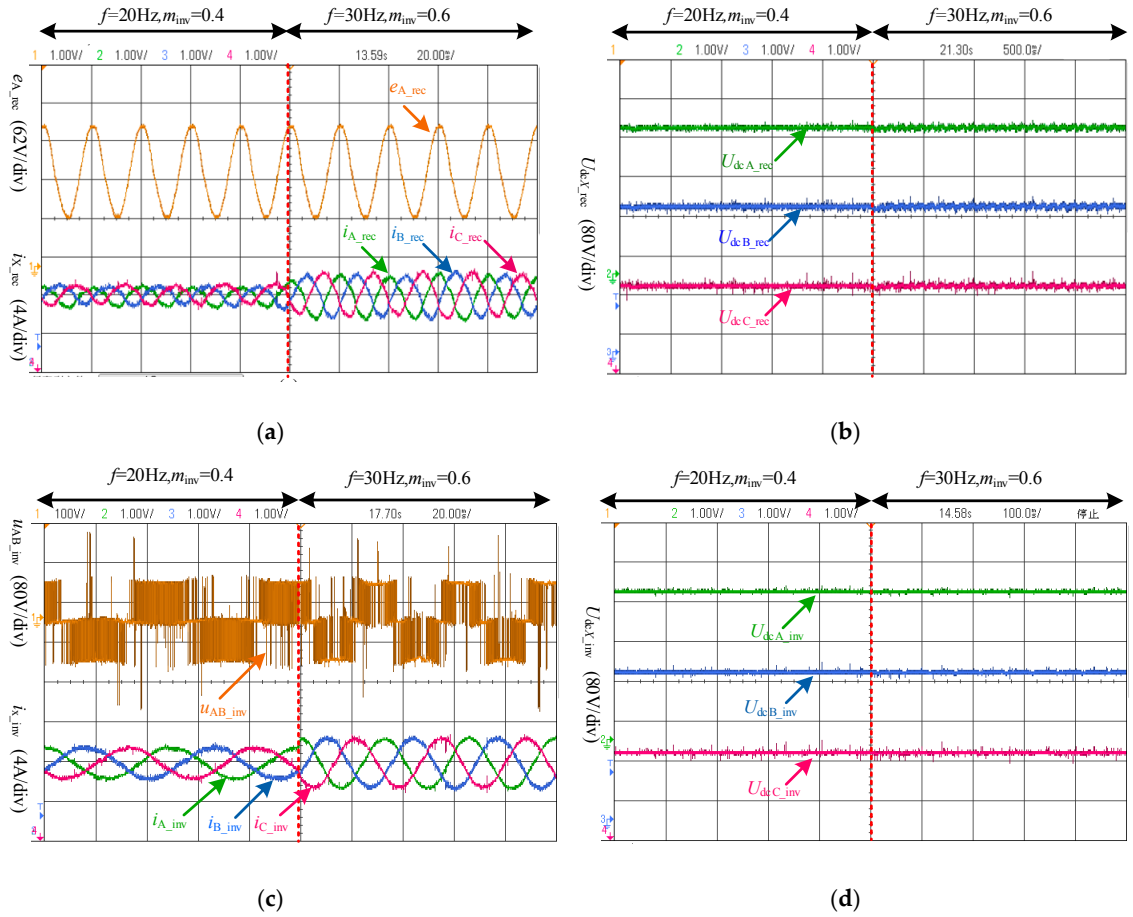

Figure 12. Experimental results of the whole working process in transient-state conditions; (**a**) Input voltage–current waveforms, e_{A_rec} and i_{X_rec}; (**b**) voltages of C_{X_rec}; (**c**) output voltage–current waveforms, u_{AB_inv} and i_{X_inv}; (**d**) voltages of C_{X_inv}.

As can be seen from Figure 11a, when the output frequency f and modulation index m_{inv} are 20 Hz and 0.4, the peak value of three-phases on the rectifier side current i_{X_rec} has low-frequency fluctuations, and the sine effect is not ideal; when switching to f = 20Hz and m_{inv} = 0.4, the three-phase current i_{X_rec} stabilizes rapidly after about 25 ms, the sine is good, and the amplitude is basically the same. In the process of switching, the entire control system can achieve a balanced three-phase current and unity power factor control, and show good robust performance. U_{dcX_rec} and U_{dcX_inv} shown in Figure 11b,d have almost no change when the frequency and modulation index switching. They are constantly maintained at a fixed value, showing strong anti-interference performance. As shown in Figure 11c, after switching, the inverter side line-to-line voltage u_{AB_inv} and three-phase currents i_{X_inv} are rapidly stabilized, and the three-phase current change trend remains the same.

Obviously, the inverter side of the converter performs well in this case. Figure 13 shows the experimental results in transient-state conditions with the modulation index set at 0.8 and 0.9 and the output frequency f set from 40 Hz to 50 Hz. Figure 13a,c shows the same results as Figure 12 and will not be repeated here. According to Figure 13b,d, voltages of rectifier side and inverter side are maintained at their given values. At the same time, it becomes more stable after switching. Thus, the effectiveness of the proposed three-level converter to capacitor voltage equalization control is verified.

4.3. Simulation Results

Figure 14 shows the curves of the voltage weight total harmonic distortion WTHD with different modulation indexes m_{inv} and switching frequency f_{switch} based on MATLAB/Simulink.

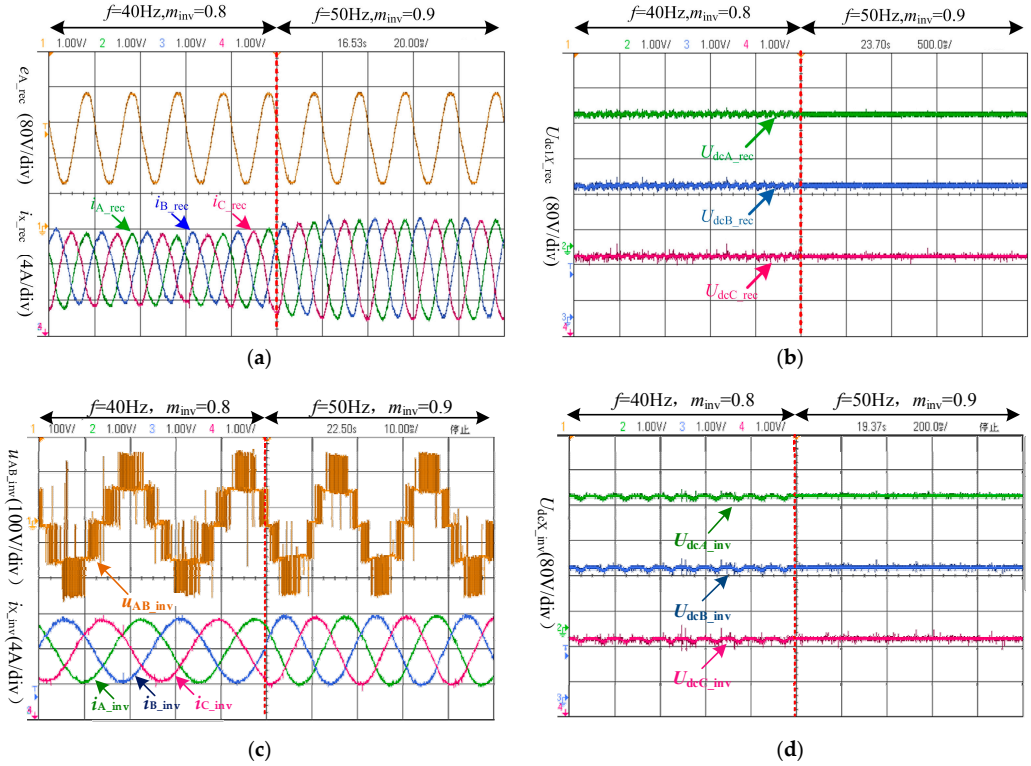

Figure 13. Experimental results of the multilevel converter in transient-state conditions; m_{inv} changes from 0.8 to 0.9; (**a**) Input voltage-current waveforms, $e_{\mathrm{A\_rec}}$ and $i_{\mathrm{X\_rec}}$; (**b**) voltages of $\mathrm{C_{X\_rec}}$; (**c**) output voltage–current waveforms, $u_{\mathrm{AB\_inv}}$ and $i_{\mathrm{X\_inv}}$; (**d**) voltages of $\mathrm{C_{X\_inv}}$.

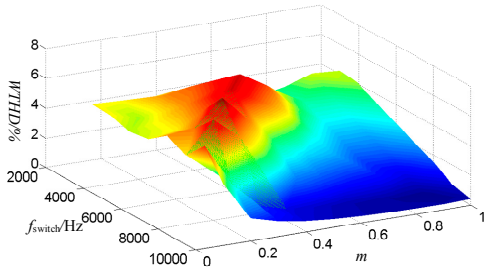

Figure 14. Harmonic characteristic results of WTHD curves of $u_{\mathrm{AB\_inv}}$ with f_{switch} and m_{inv}.

WTHD is defined in Equation (16), where V_1 and V_n mean the fundamental and n order harmonic components in line-to-line voltage respectively. As shown in Figure 14, WTHD of $u_{\mathrm{AB\_inv}}$ increases with the decrease of switching frequency f_{switch} and modulation index m_{inv}. It shows better performance when $m_{\mathrm{inv}} > 0.4$, while WTHD becomes taller when $m_{\mathrm{inv}} < 0.4$ in some areas. In general, the performance of the proposed converter can operate well.

$$\mathrm{WTHD} = \sqrt{\sum_{n=2}^{\infty} \frac{V_n^2}{n^2}} / V_1 \quad , \tag{16}$$

4.4. Simulation Analysis of 5/3 Level Voltage Source Converter

This new topology can be expanded asymmetrically, which means the rectifier side and inverter side can work with different nominal voltages. It is possible to the proposed topology to connect the asynchronous multi-scale power network. On the basis of the proposed three level voltage source converter, the voltage level in rectifier side has been expended to five level. The circuit configuration

of 5/3 level converter has shown in Figure 15. Due to the similar structure, the control methods of 5/3 level voltage source converter are as same as the aforementioned methods of the three-level converter.

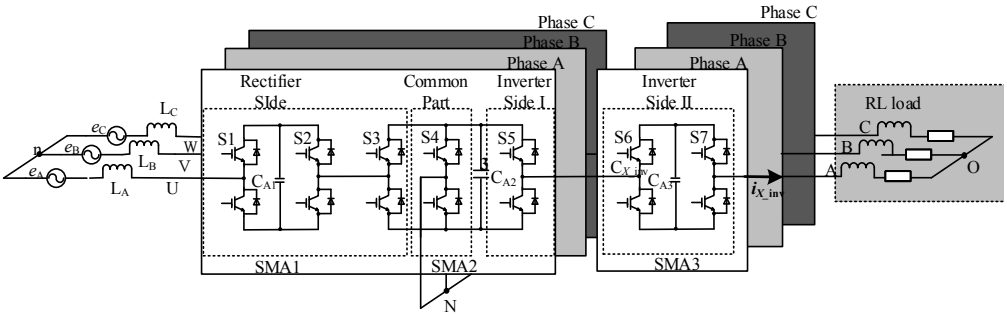

Figure 15. Circuit configuration of 5/3 level voltage source converter.

The simulation result is shown in Figure 16. The whole working process shown in Figure 16a, is divided into three sections: uncontrollable precharge, controllable precharge, and inverter side working. In the uncontrollable precharge section, uncontrollable full wave rectification is achieved only by diodes with anti-parallel device. Then the rectifier side starts in Power Unit II, and the voltages of modules SMX1 and SMX2 are selected as 50 V and 100 V, respectively. Figure 16b,c shows line-to-line voltages and three-phase currents of the rectifier side under the modulation index set at 1. Obviously, the voltage reaches nine levels and the currents are undistorted sinusoidal waveforms.

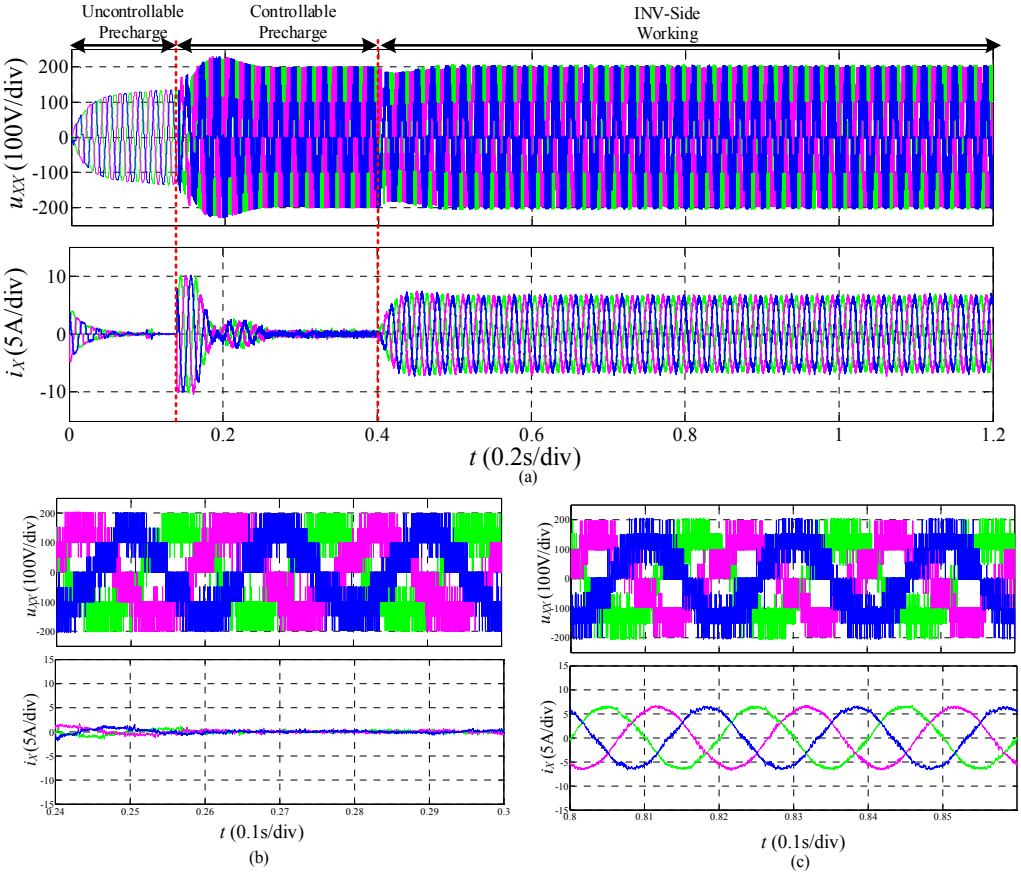

Figure 16. Simulation results of the whole working process; (**a**) Output voltage–current waveforms, u_{xx} and i_X; (**b**) Output voltage–current waveforms, u_{xx} and i_X ; time from 0.24s to 0.3s;(**c**) Output voltage–current waveforms, u_{xx} and i_X; time from 0.8 s to 0.86 s.

5. Conclusions

In order to balance the voltage of flying-capacitors, a novel three-level voltage source converter for AC–DC–AC conversion was proposed in this paper. The circuit configuration and work principle of the proposed three-level voltage source converter were studied in detail. The dual double-closed-loop control strategy and voltage balancing algorithm, especially the method of inverter capacitors with OSSC, were introduced to elaborate the control method of a three-level converter. Then, two operation conditions were analyzed to assess the operating characteristics of the proposed converter. Finally, the balanced control capabilities of this new topology to the three-phase suspension capacitor voltage of the rectifier side and inverter side was verified by simulations and experiments.

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