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A Modularized Discharge-Type Balancing Topology for Series-Connected Super Capacitor String

Shaogui Fan [1], Li Sun [1], Jiandong Duan [1,*] and Dong Zhang [2]

[1] School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China; 15b306002@hit.edu.cn (S.F.); sunli1960168@163.com (L.S.)

[2] State Grid Heilongjiang Electric Power Company Limited, Qiqihar Power Supply Company Power Dispatching Center, Qiqihar 161005, China; 18945053506@163.com

* Correspondence: duanjiandong1985@126.com; Tel.: +86-158-0451-0569

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Abstract: This paper proposed a modularized discharge-type topology for the voltage balance of series-connected super capacitor (SC) string. The proposed topology consists of cascaded converter modules and a boost converter. The cascaded converter modules discharge the higher voltage SCs directly with the ideal output current to realize a fast balancing speed and the boost converter feedbacks the extra energy from the higher voltage SCs to the super capacitor energy storage system (SCESS). The modular design of the cascaded converter modules makes the balancing system suitable for different voltage levels of SCESS. Unlike the charge-type topologies which discharge the higher voltage SCs indirectly, the proposed topology discharges the higher voltage SCs directly with a big current, and the over voltage phenomenon of SCs is then avoided, which means the reliability of the SCESS can be improved. The voltage stress of the switches inside the cascaded converter modules is low, which is different from the existing modularized discharge-type balancing topology. What is more, the control of cascaded converter modules and the boost converter can be implemented by analog devices which will simplify the control of the whole system. The control degree of freedom is high and the voltage of each cell can be controlled. An in-depth comparison analysis with the charge-type balancing topology is performed from the perspective of balancing speed and round-trip energy efficiency. The proposed topology and the balancing performance are confirmed by experimental results.

Keywords: super capacitor balancing topology; cascaded converter; maximum power discharge; fast balancing speed; high round-trip energy efficiency

1. Introduction

The super capacitor energy storage system (SCESS) with the advantages of a high-power density, long life, and widely operating temperature, is widely used in industrial applications. The super capacitors (SCs) are low voltage devices, the rated voltage of which with organic electrolytes is <3.0 V per cell, whereas with aqueous electrolytes, it is <1.23 V per cell [1]. However, the SCESS is often used with a high voltage, such as the SCESS used in the metro regenerative braking energy absorption system [2] and wind farms or photovoltaic plants [3]. The high voltage SCESS is composed of a large number of SCs connected in series. Because of the limitation of the manufacturing process and inconsistent parameters attenuation during use, the parameters such as capacitance, internal resistance, and leakage are inconsistent, which will cause voltage inconsistency, and the overvoltage phenomena of SCs even appear, which will reduce the life of SCs [4,5]. A fast voltage equalizer is needed for high voltage SCESS to avoid the SCs' overvoltage phenomena and ensure the security of the SCESS.

During use, the voltage of SC is usually from 0.5 times U_N to U_N (the rated voltage). A voltage lower than $0.5U_N$ but higher than zero will be harmless to SC, which is different from batteries, because a low voltage can damage the batteries. Once the voltage is higher than U_N, it will cause irreversible damage to SCs and results in life reduction [5]. The focus of the equalizer for SCESS should be discharging the higher voltage SCs with high speed. The SCESS usually works with instantaneous high-power, while the balancing current of the equalizer is relatively small, so the effects of the equalizer can be ignored during the working of SCESS. In most high-power applications, the SCESS works with a high current for a short time and is then left to stand for a time t_s to prepare next power rush [6]. When the SCESS is charged from $0.5U_N$ to U_N, the SC with the minimum capacitance C_{min} will have the highest voltage V_{SCmax}. The equalizer should discharge the highest voltage SC and make the voltage drop to the average voltage V_{SCav} within the time t_s. Then, the desired balancing speed for SCESS can be described as (1), where i_{dis} is the value of discharging current which represents the desired balancing speed and ΔQ is the charge to be discharged. Different applications have different standing times t_s, so the desired balancing speed will also be different; in any case, the faster the better.

$$i_{dis} \geq \frac{\Delta Q}{t_s} = \frac{C_{min}(V_{SCmax} - V_{SCav})}{t_s} \quad (1)$$

Numerous balancing topologies have been developed by scholars and engineers. According to the ways in which energy can be transferred, the voltage balancing system can be divided into ideal balancing topologies, charge-type balancing topologies, and discharge-type balancing topologies, which are shown in Figure 1.

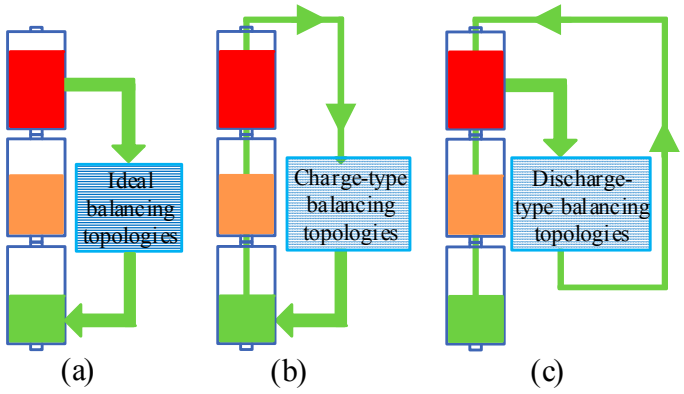

Figure 1. Classification of balancing system based on the ways that energy can be transferred. (**a**) With ideal balancing topologies; (**b**) With charge-type balancing topologies; (**c**) With discharge-type balancing topologies.

As shown in Figure 1a, the technical characteristics of ideal balancing topology are: the energy from the higher voltage SCs is transferred to the lower voltage SCs directly and simultaneously. In the literature [7,8], the ideal balancing topology is realized by using switches connecting each SC to the transformer windings. These windings with the same turn ratio share the same transformer core. When the switches are turned on simultaneously, the energy from the higher voltage SCs is transferred to the lower voltage SCs directly by the transformer core. However, with these balancing topologies, the turn ratio of windings should be strictly consistent. Furthermore, it is difficult to use in the high voltage SCESS, because the number of windings which share the same core are limited. The modularization technique can be used to make the multi-winding transformer balancing topology suitable for the high voltage energy storage system (ESS) [7,9,10]. These voltage equalizers with a high efficiency and small balancing current between modules are very suitable for the battery energy storage system (BESS). However, they are not suitable for SCESS, which needs a faster balancing speed. Because

the SCESS will be repeatedly charged and discharged with an instantaneous high current and the terminal voltage will be changed frequently, the fast voltage equalizers are needed to avoid the SCs' overvoltage phenomena.

The isolation bi-directional DC/DC converters with the properties of being easily cascaded and low-cost are one of the perfect candidates for the realization of an ideal balancing topology. In [11], the bidirectional DC/DC converter balancing topologies are used to realize the ideal balancing topology; however, the cost of the bidirectional DC/DC converters is high. Quasi ideal balancing topologies are easier to implement, including the buck/boost converter balancing topologies [12,13], the switched capacitor balancing topologies [14,15], and so on. These balancing topologies can discharge the higher voltage SCs and charge the lower voltage SCs, but not directly and simultaneously, so the balancing speed is slower than the ideal balancing topology. Beside the ideal balancing topologies, the charge-type topologies and discharge-type topologies are widely researched and used.

As shown in Figure 1b, the technical characteristics of the charge-type balancing topologies are: the lower voltage SCs are charged with the energy from the SCESS directly. The higher voltage SCs are discharged indirectly with a small current. Many charge-type balancing topologies are researched, such as the topology based on the voltage multiplier [16,17], based on the fly-back circuit [18,19], based on the forward circuit [20,21], and so on. These topologies are not aimed at the discharging of the higher voltage SCs, but the charging of the lower voltage SCs and the discharging speed of the higher voltage SCs is slow. Once the voltage of an SC is much higher than the average voltage, it will take a long time to discharge it, so the overvoltage phenomena may then occur. So, the charging-type topologies can do little to protect the overvoltage SCs, which are not the absolute security topologies.

The discharge-type balancing topologies are security topologies, shown in Figure 1c, and the technical characteristics are: the higher voltage SCs are discharged directly, and the extra energy from the higher voltage SCs is fed back to the SCESS. The discharge-type topologies discharge the higher voltage SCs directly and the overvoltage phenomena of SCs will not occur. The passive balancing topologies belong to discharge-type topologies, but with zero efficiency [22]. This is because the extra energy of the higher voltage SCs is dissipated in the form of heat by resistance, Zener diodes, and so on. In the literature [23], the higher voltage SCs are discharged by the fly-back converters and the extra energy is fed back to the SCESS by making the output voltage of the fly-back converters higher than the voltage of SCESS, the high step-up ratio fly-back converters are needed, which are difficult to implement in a small size, and high voltage stress of switches will cause a power loss increase. Furthermore, if the output current passes through lots of diodes then the efficiency is reduced.

In some applications, the ESS can work without the additional equalizer and voltage balancing is achieved by the control of a cascaded multilevel converter (CMC) or modular multilevel converter (MMC). The cells or cell units are connected in series by means of a half-bridge or full-bridge multilevel converter to form MMC or CMC, and the voltage balancing is realized by the control of MMC or CMC [24–28]. It is easy to achieve voltage balancing of SCESS with MMC or CMC and each cell can be removed from the current path without interrupting the operation of the system. However, there are some drawbacks that limit the wide use of MMC or CMC. First, the control strategy of MMC or CMC is usually complex. Furthermore, the MMC or CMC is high-cost and has a poor efficiency with high current applications. Because the high load current passes through each half-bridge or full-bridge converter, the high-current level switches are costly and the high current will cause high on-resistance of switches, which can reduce the efficiency of the system. Besides, large numbers of switches working with a high current will give rise to hidden faults, which will reduce the reliability of the system.

To achieve a fast and security balancing topology for series-connected super capacitor string, a novel modularized discharge-type equalizer for a series-connected SC string is proposed in this paper. With the proposed topology, the higher voltage SCs are discharged by the cascaded converter modules with a big current, so the overvoltage phenomena of the SCs can be avoided. The energy from the higher voltage SCs is transferred to the cascaded converter modules and will be fed back to the SCESS by a boost converter. The critical characteristics of the proposed balancing topology are:

(a) Modularized converter makes the balancing system suitable for different voltage levels SCESS; (b) it belongs to discharge-type balancing topology and has an excellent discharge performance which can avoid the over voltage phenomenon of SCs and increase the security of the system; (c) it is suitable for series-connected SC string due to the excellent isolation performance; (d) the voltage stress of the switches inside the cascaded converter modules is low, which is different from the existing modularized discharge-type balancing topology [23]; and (e) the control of the cascaded converter modules and boost converter can be implemented by analog devices which will simplify the control of the system. The next part of this paper is organized as follows: In the second section, the working principle of the proposed balancing topology is discussed. In the third section, the control strategy of the proposed topology is discussed and an in-depth comparative analysis with the charge-type balancing topology is made from the perspectives of balancing speed and round-trip energy efficiency. In the fourth section, the experiment is implemented to verify the proposed topology. Following this, a conclusion to this paper is presented.

2. Working Principle of the Propose Balancing Topology

The proposed discharge-type modularized equalizer is shown in Figure 2, which is composed of n (the number of series-connected SCs) cascaded converter modules, a boost converter. The boost converter consists of a filter inductor L, a diode D_R, and a switch S. Each SC corresponds to a cascaded converter module, and the outputs of the cascaded converter modules are connected in series to form a cascaded converter. The cascaded converter module consists of a fly-back converter and a switch S_{Si} paralleled with the output capacitor C_{oi}.

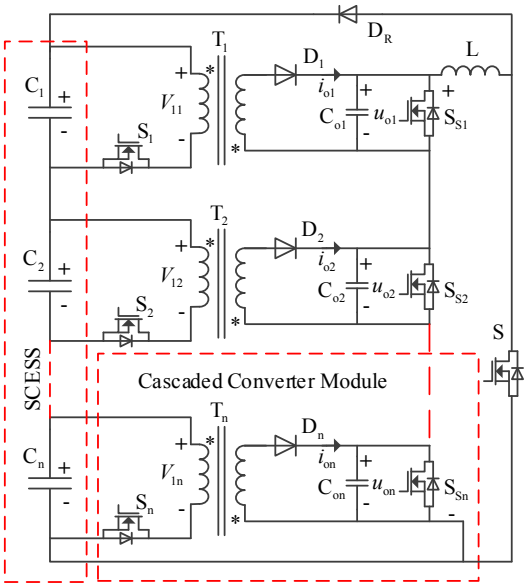

Figure 2. The proposed modularized discharge-type equalizer.

In order to better illustrate the working principles of the proposed balancing topology, an SCESS that consists of three SCs is analyzed in detail. Assume that the SCs named C_1, C_2, C_3 and the voltage satisfy $u_{SC1} > u_{SC3} > u_{average} > u_{SC2}$. The higher voltage SCs C_1 and C_3 should be discharged and the extra energy is transferred to the filter capacitors C_{o1} and C_{o3}, while the lower voltage SC C_2 should not be discharged, and the corresponding cascaded converter module acts as wires. The block diagram of the balancing principle is shown in Figure 3. The outputs of the cascaded converter modules are connected in series to form a cascaded converter and the cascaded output voltage is $u_{o1} + u_{o3}$. The boost converter feedbacks the energy stored in the filter capacitors C_{o1} and C_{o3} to the SCESS.

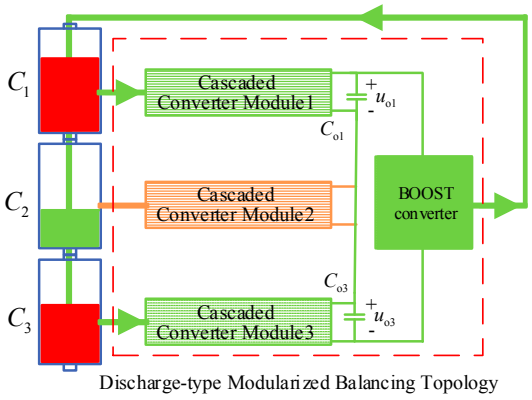

Figure 3. The balancing principle block diagram of the proposed topology.

The cascaded converter modules are controlled by the control signal CS_i, which is generated by the balancing controller. For the higher voltage SCs, the control signal is $CS_i = 1$, while for the lower voltage SCs, it is $CS_i = 0$. When $CS_i = 1$, the fly-back converter of the ith cascaded converter module starts working to discharge the higher voltage SC and transfer the excess energy to the filter capacitor C_{oi}. When $CS_i = 0$, the fly-back converter does not work, and the switch S_{si} is turned on, so that the output of the cascaded converter module acts as wires. The drives of the cascaded converter modules and the main waveforms of the boost converter are shown in Figure 4, and the currents of the boost converter are shown in Figure 5.

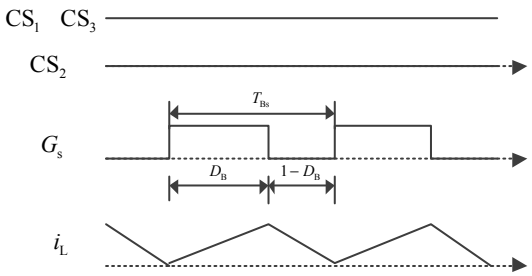

Figure 4. The drive of the cascaded converter modules and the main waveforms of the boost converter.

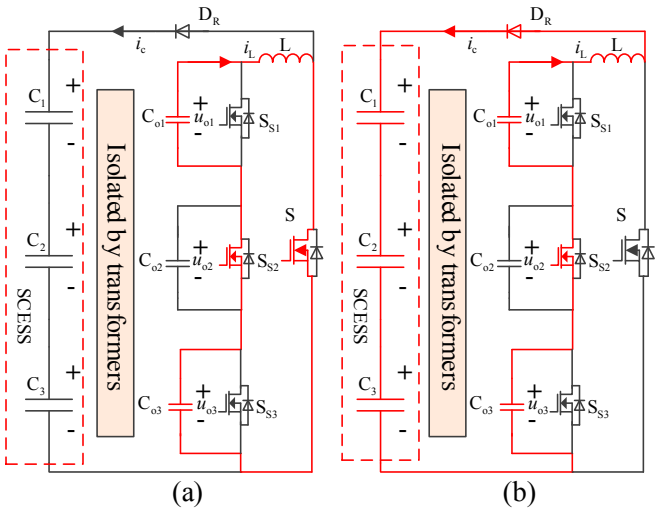

Figure 5. The currents of the boost converter. (**a**) The switch S is turned on; (**b**) The switch S is turned off.

As shown in Figure 4, the control signals $CS_1 = 1$ and $CS_3 = 1$, while $CS_2 = 0$. The output of the cascaded converter is equal to $u_{o1} + u_{o3}$. The boost converter is driven by the PWM signal G_s, and the current is shown in Figure 5. As shown in Figure 5a, when the PWM is high, the inductor current i_L increases. As shown in Figure 5b, when the PWM is low, the inductor current decreases and the energy is fed back to the SCESS.

The energy transferred process of the proposed balancing topology is divided into two parts: one is the cascaded converter modules, which discharge the higher voltage SCs and transfer the extra energy to the filter capacitors; and the other is the boost converter, which transfers the energy stored in the filter capacitors to the SCESS. The energy transferred process works simultaneously with an independent control sequence. Next, the working principle of the cascaded converter module is discussed in detail.

The topology of the cascaded converter module is shown in Figure 6, which consists of a fly-back converter and a switch S_{Si} paralleled with the output capacitor C_{oi}. The fly-back converter has the function of isolation and discharge. Compared to the forward converter, the fly-back converter has the advantages of avoiding the use of output filter inductance, a freewheeling diode, and a specialized transformer reset circuit, which will make the converter small in size. The switch S_{Si} is used to make a short circuit of the output capacitor C_{oi} to make the cascaded converter module act as wires.

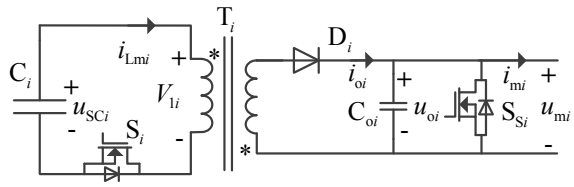

Figure 6. The cascaded converter module.

The drive of the cascaded converter module is shown as Figure 7, where the control signal CS_i is used to control the working of the fly-back converter. The switch S_{Si} is driven by the complementary signals of CS_i. If the voltage of ith SC is higher than the average voltage, $CS_i = 1$, the corresponding cascaded converter module starts discharging the SC. If the voltage of ith SC is lower than the average voltage, the CS_i is low, the fly-back converter does not work and the short circuit switch S_{Si} is on, and the cascaded converter module acts as wires.

Figure 7. The drives of the cascaded converter module.

To improve the discharging power of the modularized converter module, the fly-back converters are operated in continuous current mode (CCM) [29]. The switch S_i is driven by high frequency PWM G_{si}. In the time interval $0 \sim DT_s$, the switch S_i is on, and the current i_{Lmi} increases linearly, which can be expressed as (2). In the time interval $DT_s \sim T_s$, the switch S_i is off, and the energy stored in the magnetizing inductance is transferred to the filter capacitor. The peak current control strategy with the peak current i_p is used to control the fly-back converter. The discharging power of the fly-back converter can be expressed as (3).

$$i_{\mathrm{Lmi}}(t) = i_{\mathrm{Lm0}} + \frac{u_{\mathrm{SC}i}}{L_m} t \quad t \in [0 - DT_s] \tag{2}$$

$$\begin{aligned} P_{fi} &= \tfrac{1}{2}Du_{\mathrm{SCi}}(i_{\mathrm{p}} + i_{\mathrm{p}} - \Delta i) \\ &= \tfrac{1}{2}Du_{\mathrm{SCi}}(2i_{\mathrm{p}} - \tfrac{Du_{\mathrm{SCi}}T_{\mathrm{s}}}{L_{\mathrm{m}}}) \end{aligned} \tag{3}$$

where i_{Lm0} is affected by the load current; L_{m} is the magnetizing inductance; $\triangle i$ is the increment of current i_{Lm} during the time interval 0~DT_{s}; D is the duty cycle of the PWM and T_{s} is the period; and $u_{\mathrm{sc}i}$ is the voltage of ith SC.

The output voltage of the cascaded converter module is controlled by the control signal CS_i. When $\mathrm{CS}_i = 1$, $G_{\mathrm{SS}i} = 0$, the output of the cascaded converter module is $u_{\mathrm{o}i}$. When $\mathrm{CS}_i = 0$, $G_{\mathrm{SS}i} = 1$, the output of the cascaded converter module is zero. Thus, the output voltage of the cascaded converter module $u_{\mathrm{m}i}$ can be expressed as (4). The outputs of the cascaded converter modules are connected in series to form a cascaded converter, thus, the cascaded output voltage U_{e} can be expressed as (5).

$$\begin{cases} u_{\mathrm{m}i} = u_{\mathrm{o}i} & \mathrm{CS}_i = 1 \\ u_{\mathrm{m}i} = 0 & \mathrm{CS}_i = 0 \end{cases} \tag{4}$$

$$U_{\mathrm{e}} = \sum_{i=1}^{n} \mathrm{CS}_i u_{\mathrm{o}i} \tag{5}$$

where n is the number of series-connected SCs; CS_i is the control signal of ith SC; and $u_{\mathrm{o}i}$ is the voltage of ith filter capacitor $C_{\mathrm{o}i}$, which will be calculated in the next part.

The boost converter can be simplified as shown in Figure 8, where the input voltage of the boost converter is U_{e} and the output voltage is the voltage of SCESS U_{SCESS}. The working principle of the boost converter is very classic and familiar, and control of the boost converter will be discussed in the next part.

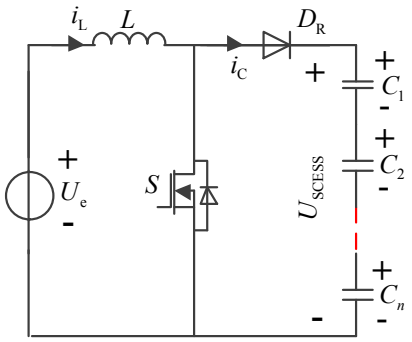

Figure 8. The simplified boost converter.

Through the above analysis, the voltage stress of switches can be ascertained. The voltage of SC is u_{sc}, and the turn ratio of transformer is n. Then, the voltage stress of switch S_i is $(u_{\mathrm{sc}} + u_{\mathrm{o}i}/n)$, and the voltage stress of switch Ss_i is $u_{\mathrm{o}i}$. Because the values of u_{sc} and $u_{\mathrm{o}i}$ are small, the voltage stress of switches inside the cascaded converter modules is low. The voltage stress of switch S in the boost converter is U_{SCESS}, which is high. However, only one switch S is used in one balancing system and the current stress of switch S is low, so the price of switch S is acceptable.

3. Control and Analysis of The Proposed Balancing Topologies

3.1. Control and Analysis of the Cascaded Converter Module

The cascaded converter module is controlled by the control signal CS. The peak current control strategy with a 50% maximum duty cycle is used to control the fly-back converter, which can guarantee the stability of the fly-back converter without the need of current ramp compensation [30]. The control circuit of the cascaded converter module is shown in Figure 9.

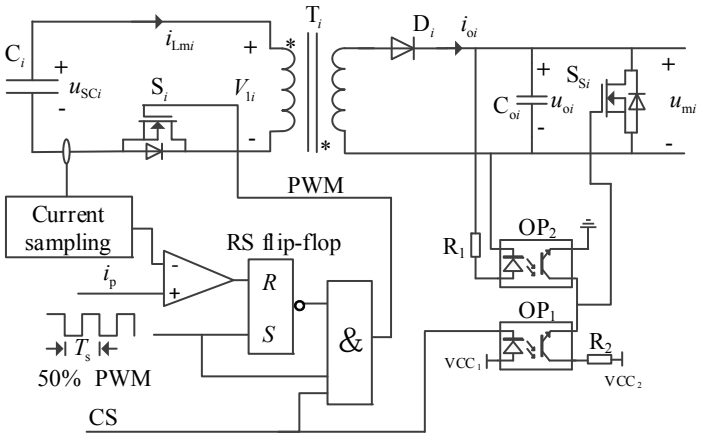

Figure 9. Control circuit of the cascaded converter module.

The drive of the fly-back converter is the result of logical operations of control signal CS AND 50% duty cycle PWM AND the output of the RS flip-flop. The control signal CS is used to control the cascaded converter in terms of whether it works or not. The 50% duty cycle PWM is used to limit the max duty cycle of the PWM to ensure the stability of the converter. The output of the RS flip-flop is used to limit the peak current to i_P to prevent over current. Figure 10 shows the main waveforms of the cascaded converter module. Figure 10a a is the waveforms with a small load current, where the PWM duty cycle is limited to 50% and the current i_{Lm} does not reach the peak current i_P. Figure 10b is the waveforms with a big load current, where the current i_{Lm} reaches the peak value i_P, the PWM is forced to low-level until the next cycle, and the converter is in cycle-by-cycle peak current limit mode. The turning on of the short circuit switch S_{Si} is decided by optocouplers OP_1 and OP_2. Optocoupler OP_1 is controlled by CS. If CS = 0, one condition to turn on S_{Si} is ready. Optocoupler OP_2 is used to monitor the output capacitor voltage u_{oi} to avoid the high voltage before the output capacitor C_{oi} is short circuited. The short circuit switch S_{Si} will not turn on until CS = 0 and the output capacitor voltage u_{oi} reaches a reasonably low value.

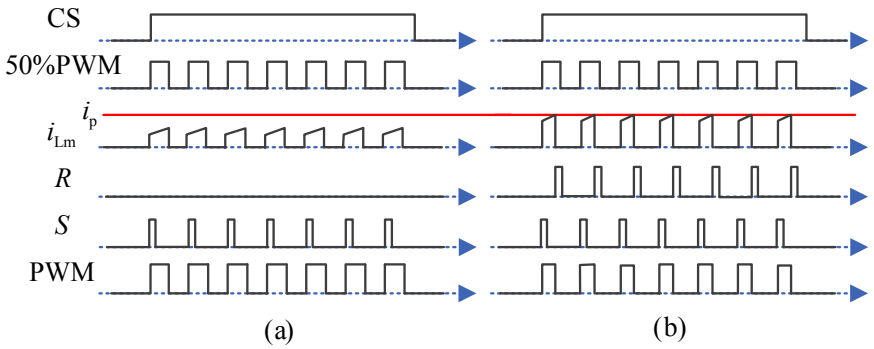

Figure 10. Main waveforms of the cascaded converter module. (**a**) With a small load current. (**b**) With a big load current.

To ensure that the discharging power is greater than the designed value P_0, the magnetizing inductance L_m should be bound. The discharging power of the fly-back converter can be expressed as (3), and the maximum discharging power can be expressed as (6). Let P_{omax} be bigger than P_o, which results in (7).

$$P_{omax} = \frac{1}{2} D_{max} u_{SCmax} \left(2 i_p - \frac{D_{max} u_{SCmax} T_s}{L_m}\right) \quad (6)$$

$$L_{\mathrm{m}} > \frac{T_{\mathrm{s}} D_{\max}^2 u_{\mathrm{SCmax}}^2}{2(i_{\mathrm{p}} D_{\max} u_{\mathrm{SCmax}} - P_{\mathrm{o}})} \tag{7}$$

where $D_{\max} = 0.5$, u_{SCmax} is the maximum voltage of SC, i_{p} is the peak current, and T_{s} is the period.

Next, the relationships between the output current and discharging power of the cascaded converter module will be discussed. During the time interval $0 \sim DT_{\mathrm{s}}$, the rise rate of i_{Lm} can be expressed as (8) and the current i_{Lm} changing with time is shown in Figure 11. The current i_{Lm} is limited to a rectangle which is made of ranges of time $D_{\max} T_{\mathrm{s}}$ and peak current i_{p}. The average value of the current i_{Lm} can be expressed as (9).

$$m = \frac{u_{sc}}{L_{\mathrm{m}}} \tag{8}$$

$$\bar{i}_{\mathrm{Lm}} = i_{\mathrm{Lm0}} + \frac{1}{2} m D^2 T_s \tag{9}$$

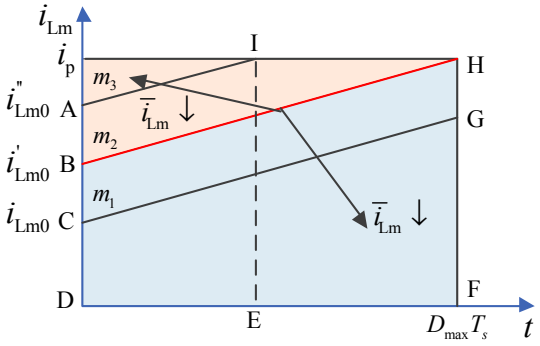

Figure 11. The current i_{Lm} changing with time.

The initial current i_{Lm0} and duty cycle D vary with load current. Line segments CG, BH, and AI represent the i_{Lm} at a small load current, ideal load current, and large load current, respectively, and the line segments have the same rise rate m. When the current i_{Lm} reaches the line segment BH, the average current of i_{Lm} reaches the maximum value, which can be expressed as (10). When the average discharging current $\bar{i}_{\mathrm{Lm}}$ is the maximum, the discharging power reaches the maximum, and the corresponding average output current can be calculated as (11).

$$\bar{i}_{\mathrm{Lmmax}} = \frac{1}{2} D_{\mathrm{Bmax}} (2 i_p - m D_{\mathrm{Bmax}} T_{\mathrm{B}}) \tag{10}$$

$$\bar{i}_{\mathrm{oideal}} = \frac{n(1 - D_{\mathrm{Bmax}})(2 i_p - m D_{\mathrm{Bmax}} T_{\mathrm{B}})}{2} \tag{11}$$

where n is the transformer ratio.

Define the average output current calculated as (11) as the ideal output current, and at this load current, the discharging power of the cascaded converter module reaches the maximum. Due to the implementation of the cascaded converter module being based on the analog devices, the magnetizing inductance L_{m} and the switching period T_{s} will change in a small range near the designed value, and the ideal output current varies with u_{SC}, T_{s}, and L_{m}. The three-dimensional graph of the ideal output current with parameters $D_{\max} = 0.5$, $n = 1/3$, $i_{\mathrm{p}} = 20$ A, $u_{\mathrm{SC}} = 1.5 \sim 3$ V, $T_{\mathrm{s}} = 15 \times 10^{-6} \sim 20 \times 10^{-6}$ s, $L_{\mathrm{m}} = 15 \times 10^{-6} \sim 25 \times 10^{-6}$ H is shown as Figure 12.

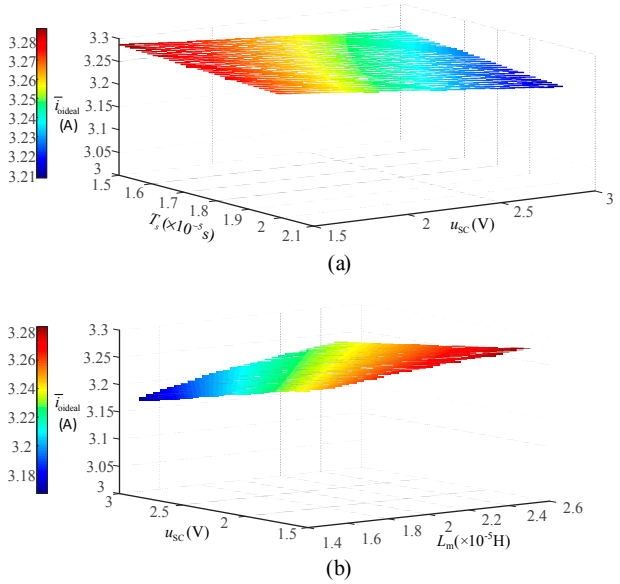

Figure 12. Ideal output current varies with u_{SC}, T_s, and L_m. (**a**) Ideal output current varies with u_{SC} and T_s. (**b**) Ideal output current varies with u_{SC} and L_m.

As shown in Figure 12, the ideal output current decreases with the increase of u_{SC} and T_s, and increases with the increase of L_m, but the range of the changes is small. When u_{SC} = 3 V, $T_s = 20 \times 10^{-6}$ s, and $L_m = 15 \times 10^{-6}$ H, the ideal output current reaches the minimum value of 3.17 A; when $u_{SC} = 1.5$ V, $T_s = 15 \times 10^{-6}$ s, and $L_m = 25 \times 10^{-6}$ H, the ideal output current reaches the maximum value of 3.29 A. Trying to make the parameters of each cascaded converter module consistent can further reduce the change. So, it can be assumed that the ideal output current remains constant throughout the range of u_{SC}.

3.2. The Control Strategy of the Boost Converter

The cascaded converter modules should output the ideal output current to discharge the higher voltage SCs with the maximum discharging power to achieve a fast balancing speed. The ideal output current of cascaded converter modules is realized by control of the boost converter. The inductance current i_L is difficult to regulate due to the wide range of the input voltage U_e. So, the hysteresis current control strategy which has self-stabilization characteristics [31,32] is used to control the boost converter and the control circuit diagram, as shown in Figure 13.

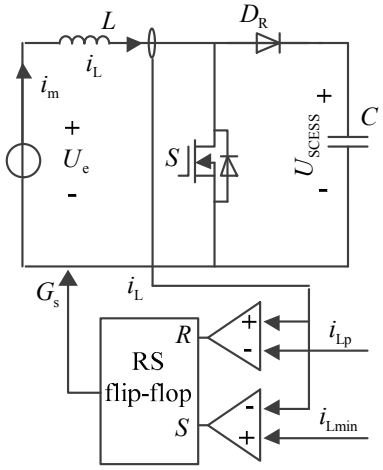

Figure 13. Control circuit diagram of the boost converter with hysteresis current control strategy.

As shown in Figure 13, the hysteresis current control strategy is realized by an RS Flip Flop and comparators, and the main waveforms of the boost converter are shown as Figure 14. The given minimum inductance current i_{Lmin} and maximum inductance current i_{Lp} are set by potentiometers. When $i_L < i_{Lmin}$, the Flip Flop is set, and the switch is turned on, so i_L begins to increase. When $i_L > i_{Lp}$, the Flip Flop is reset, the switch is turned off, and i_L begins to decrease. The average input current of the boost converter which is in hysteresis current control mode can be expressed as (12). In order to make the cascaded converter output the ideal output current, Equation (13) should be satisfied. According to Equation (12) and Equation (13), (14) is obtained. When $i_{Lmin} \approx 0$ and i_{Lp} satisfy Equation (14), the ideal output current of the cascaded converter is realized.

$$\bar{i}_L = 0.5 i_{Lmin} + 0.5 i_{Lp} \tag{12}$$

$$\bar{i}_L = \bar{i}_{oideal} \tag{13}$$

$$i_{Lp} = 2\bar{i}_{oideal} - i_{Lmin} \tag{14}$$

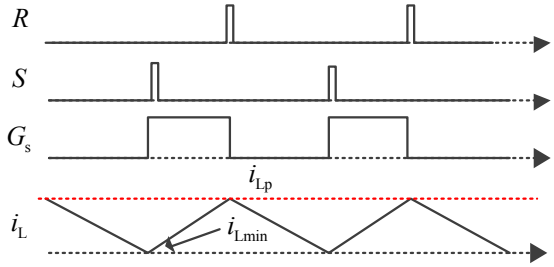

Figure 14. The main waveforms of the boost converter.

The PWM frequency of the boost converter changes with U_e and the maximum frequency should be limited. The PWM frequency can be expressed as (15). When $U_e = 0.5U_{SCESS}$, the PWM frequency f_B reaches the maximum, and the maximum value can be expressed as (16). If the maximum PWM frequency of the boost converter is limited to f_{Bmax}(f_{Bmax}), then the filter inductance L shall satisfy (17).

$$f_B = \frac{U_e}{L(i_{Lp} - i_{Lmin})}\left(1 - \frac{U_e}{U_{SCESS}}\right) \tag{15}$$

$$f_{Bmax} = \frac{U_{SCESS}}{4L(i_{Lp} - i_{Lmin})} \tag{16}$$

$$L > \frac{U_{SCESS}}{4f_{Bmax}(i_{Lp} - i_{Lmin})} \tag{17}$$

where U_e is the output voltage of the cascaded converter, U_{SCESS} is the voltage of the SCESS, and $U_e < U_{SCESS}$.

A too small or too large U_e value will lead to a too low frequency, which will cause failure of the control system. The low frequency caused by a too small and too large U_e value will be discussed, respectively.

When U_e is small, the extreme case is that only one higher voltage SC needs to be discharged, and the cascaded output voltage is equal to the output voltage of one cascaded converter module. When the switch S is turned on, the inductance L of the boost converter is connected in parallel with the output capacitance C_o to form a resonant circuit. When the PWM frequency is less than two times that of the resonant frequency of L and C_o, the output voltage of the cascaded converter module will reach zero (ignoring the line resistance). This will cause a short circuit of the cascaded converter module, the inductance current i_L cannot increase, and the peak current value i_{Lp} will not be reached.

The switch S of the boost converter will maintain the on state and the cascaded converter module maintains the short circuit state. Figure 15 illustrates the waveforms of the output voltage u_o of the cascaded converter module and the inductor current i_L of the boost converter, with the PWM frequency slightly higher than two times that of the resonant frequency of L and C_o.

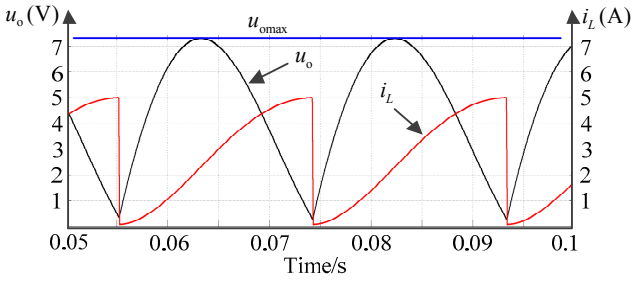

Figure 15. Waveform of u_o and i_L with the PWM frequency slightly higher than two times of the resonant frequency of L and C_o.

As shown in Figure 15, the voltage u_o is near zero at the end of each PWM cycle, so once the voltage reaches zero, the cascaded converter module will lead to a short circuit. The discharging power will reach the minimum and the extra energy cannot be fed back to the SCESS. To ensure the normal operation of the balancing system, the resonant frequency of L and C_o should satisfy (18).

$$\frac{2}{2\pi\sqrt{LC_o}} \le f_B = \frac{\overline{U}_e}{L(i_{Lp} - i_{Lmin})}\left(1 - \frac{\overline{U}_e}{U_{SCESS}}\right) \tag{18}$$

where $\overline{U}_e$ is the average output voltage of the cascaded converter.

The output voltage of the cascaded converter voltage U_e can be assumed to be invariant when the PWM frequency is high; however, U_e changes with the inductor current i_L when the PWM frequency is low. So, the average voltage $\overline{U}_e$ is used to replace U_e to calculate the frequency in Equation (18). Assume that the average voltage $\overline{U}_e = u_{omax}/\sqrt{2}$, u_{omax} is the maximum output voltage of the cascaded converter. The inductance current i_L increases from zero, and the output voltage and discharging power increase with the increase of i_L. When the discharging power reaches the maximum, the output voltage reaches the peak voltage u_{omax}, and the output current is equal to the ideal output current, so the peak voltage u_{omax} can be calculated as (19). Combining (18) and (19) produces (20).

$$u_{omax} = \frac{\eta P_{omax}}{\bar{i}_{oideal}} \tag{19}$$

$$L \le \frac{\pi^2\eta^2 P_{omax}^2}{2\bar{i}_{oideal}^2(i_{Lp} - i_{Lmin})^2}C_o \tag{20}$$

where η is the efficiency of the modularized converter module; P_{omax} is the maximum discharge power, which can be calculated as (6); and $\bar{i}_{oideal}$ is the ideal output current, which can be calculated as (11).

Once $U_e > U_{SCESS}$, the inductance current i_L cannot decrease to the minimum value i_{Lmin}, and the switch S will remain in the off state. The diode D_R is turned on and the voltage U_e is clamped to U_{SCESS}. In this case, the output current of the cascaded converter is uncontrollable, and the ideal output current cannot be guaranteed. So, the voltage U_e should be limited by (21). Combining (19) and (21) gets the maximum number of discharged higher voltage SCs and the maximum number is calculated as (22). Suppose N SCs' voltage exceed the average voltage and need to be discharged. If N > m_{max}, the SCs need to be sorted according to the order of the voltage from big to small in real-time, and the SCs at the top m_{max} are allowed to be discharged. If N < m_{max}, N SCs are all allowed to be discharged.

$$U_e = mu_{omax} < U_{SCESS} \tag{21}$$

$$m_{\max} < \frac{\bar{i}_{\text{oideal}} U_{\text{SCESS}}}{\eta P_{o\max}} \tag{22}$$

where m is the number of discharged higher voltage SCs.

The summary of the boost converter control strategy: The hysteresis current control strategy is used to control the input current of the boost converter, and the average input current is equal to the ideal output current of the cascaded converter module. To make the hysteresis current control strategy work normally, the filter inductance L is bound by (17) and (20) and the maximum number of discharged SCs is calculated as (22).

3.3. Compared with Charge-Type Balancing Topology from the Aspect of Balancing Time

Assume that the average charging current and efficiency of the charge-type topology is equal to discharge-type topology. The average current is i_{cd} and the efficiency is η. The capacitance values of SCs are distributed uniformly in the center of C_{N}, and the maximum deviation is $\triangle C_{\max}$, so the minimum capacitance value is $C_{\text{N}} - \triangle C_{\max}$. Assume that the SCESS is in a balanced state with the initial charges Q and the average voltage of each SC is Q/C_{N}. After charging with $\triangle$Q, the voltages of SCs appear inconsistent, and the highest voltage of SCs can be expressed as (23). When the balanced state is reached again, the average voltage value of the SCs can be expressed as (24). The highest voltage of SC reaches the average voltage, and the system reaches a balanced state. The charges that need to be discharged from the highest voltage of SC can be expressed as (25). The charge-type balancing topology discharges the higher voltage SCs indirectly. When a lower voltage SC is charged, the indirect discharging current of the higher voltage SCs can be expressed as (26).

$$u_{\max} = \frac{Q}{C_{\text{N}}} + \frac{\Delta Q}{C_{\text{N}} - \Delta C_{\max}} \tag{23}$$

$$u_a \approx \frac{Q + \Delta Q}{C_{\text{N}}} \tag{24}$$

$$\begin{aligned} \Delta Q_d &= (C_{\text{N}} - \Delta C_{\max})(u_{\max} - u_a) \\ &= \Delta C_{\max} \Delta Q / C_{\text{N}} \end{aligned} \tag{25}$$

$$i_{\text{ed}} = \frac{u_i i_{\text{cd}}}{U_{\text{SCESS}} \eta} \tag{26}$$

where u_i is the voltage of the lower voltage SC, i_{cd} is the charging current, U_{SCESS} is the voltage of SCESS, and η is the efficiency.

The indirect discharging current with m_1N ($1/\text{N} \leq m_1 \leq 0.5$) lower voltage SCs being charged can be expressed as (27). Assuming that $\sum_{i=1}^{m_1 \text{N}} u_i = m_1 U_{\text{SCESS}}$, the indirect discharging current can be rewritten as (28). The balancing time of SCESS can be expressed as (29).

$$i_{\text{edm}} = \frac{\sum_{i=1}^{m_1 \text{N}} u_i i_{\text{cd}}}{U_{\text{SCESS}} \eta} \tag{27}$$

$$i_{\text{edm}} = \frac{m_1 i_{\text{cd}}}{\eta} \tag{28}$$

$$t_c = \frac{\Delta Q_d}{i_{\text{edm}}} = \frac{\eta \Delta C_{\max} \Delta Q}{C_{\text{N}} m_1 i_{\text{cd}}} = \frac{\eta}{m_1} t_{cd} \tag{29}$$

where $t_{cd} = \frac{\Delta C_{\max} \Delta Q}{C_{\text{N}} i_{\text{cd}}}$.

The discharge-type topology discharges the higher voltage SCs directly and feeds the extra energy back to the SCESS with the current i_{ec}. When a higher voltage SC is discharged, the feedback current

i_{ec} can be expressed as (30). The feedback current with m_2N ($1/\mathrm{N} \leq m_2 \leq 0.5$) higher voltage SCs being discharged can be expressed as (31). The balancing time of SCESS can be expressed as (32).

$$i_{ec} = \frac{\eta u_j i_{cd}}{U_{SCESS}} \tag{30}$$

$$i_{ecm} = \eta m_2 i_{cd} \tag{31}$$

$$t_d = \frac{\Delta Q_d}{i_{cd} - i_{ecm}} = \frac{\Delta C_{max} \Delta Q}{C_N i_{cd}(1 - \eta m_2)} = \frac{t_{cd}}{(1 - \eta m_2)} \tag{32}$$

where u_j is the voltage of the higher voltage SC, i_{cd} is the discharge current, and U_{SCESS} is the voltage of SCESS.

The balancing time of charge-type topology and discharge-type topology changing with m_1, η and m_2, η are shown as Figures 16 and 17, respectively.

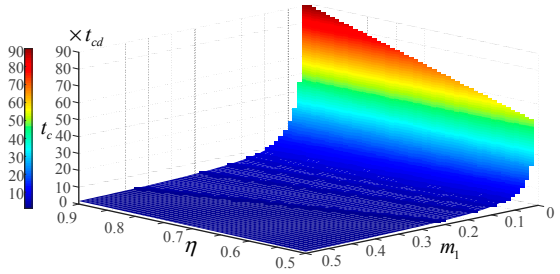

Figure 16. The balancing time of charge-type topology t_c changing with m_1, η.

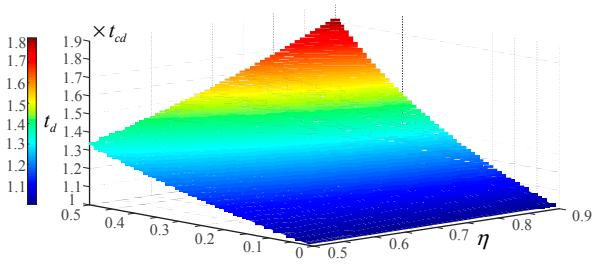

Figure 17. The balancing time of discharge-type topology t_d changing with m_2, η.

As shown in Figures 16 and 17, the balancing time increases with the increase of efficiency, but the effect is little. Figure 16 shows the balancing time of charge-type topology. The balancing time is less when the number of being charged SCs is large and increases significantly when the number of being charged SCs decreases. During the balancing process of SCESS, the number of being charged SCs is large at the beginning but decreases as the balancing continues. So, the balancing speed is fast at the beginning, but decreases significantly as the balancing progresses. Figure 17 shows the balancing time of discharge-type topology. The balancing time decreases with the decrease of the number of SCs being discharged. So, the balancing speed of discharge-type topology will be faster and faster as the balancing continues. Figure 18 shows the balancing time of the discharge-type and charge-type topology changing with the number of SCs being discharged (charged). It can be seen that when the number of SCs being discharged (charged) is large, the balancing time of discharge-type topology is approximately equal to the charge-type topology. But, the balancing time of discharge-type topology is far outweighed by the charge-type topology when the number of SCs being discharged (charged) is few. The number of SCs being discharged (charged) gradually decreases as the balancing continues. So, during the whole balancing process, the balancing time of charge-type topology will be longer than

the discharge-type topology, that is to say, the balancing speed of the discharge-type topology is faster than the charge-type topology.

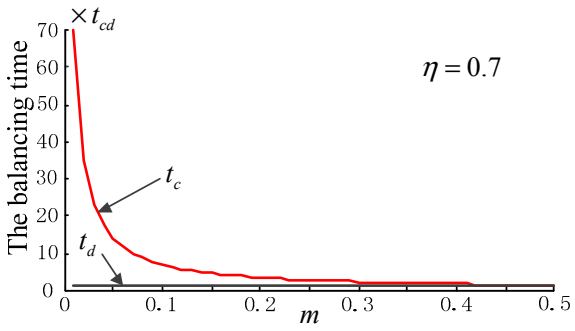

Figure 18. The balancing time $t_c(t_d)$ change with charge (discharge) number m.

3.4. Analysis of the Round-Trip Energy Efficiency

Under the normal working condition, the voltage of SC is usually from 0.5 V_{CN} to V_{CN} (the rated voltage). The voltage lower than 0.5 V_{CN} but higher than zero will be harmless to the SC, which is different from batteries, because a low voltage can damage the batteries. The focus of the balancing topology for SCESS should be discharging the higher voltage SCs. Assuming that the average voltage $u_{average}$ of SCESS remain unchanged, the energy to be transferred during one balancing process can be calculated as (33). The total power losses in one balancing process can be calculated as (34). Then, the round-trip energy efficiency of balancing system can be expressed as (35).

$$W_{\text{to\_be\_transfered}} = \frac{1}{2}\sum_{j=1}^{n} C_j(u_j^2 - u_{\text{average}}^2) \tag{33}$$

$$W_{\text{total\_losses}} = \frac{1}{2}\sum_{i=1}^{N} C_i(u_i^2 - u_{\text{end}i}^2) \tag{34}$$

$$\eta = 1 - \frac{W_{\text{total\_losses}}}{W_{\text{to\_be\_transfered}}} (\text{if } \eta < 0,\ \eta = 0) \tag{35}$$

where n is the number of higher voltage cells, u_j is the voltage of jth higher voltage SC before balancing, N is the total number of series-connected SCs, u_i is the voltage of ith SC before balancing, and $u_{\text{end}i}$ is the voltage after balancing. u_j, u_i, and $u_{\text{end}i}$ can be measured before and after the balancing process, respectively.

In order to simplify the calculation, assume that only one SC's voltage u_h is higher than the average voltage u_a and the capacitance of SCs is equal to C. The energy to be transferred is calculated as (36). The round-trip energy efficiency of different balancing topologies is analyzed.

$$W_{\text{to\_be\_transfered}} = \frac{1}{2}C(u_h^2 - u_a^2) \tag{36}$$

(1) Switch resistance balancing topology

The extra energy from the higher voltage SC is dissipated by resistance, so the total power losses is slightly higher than $W_{\text{to\_be\_transfered}}$, and the round-trip energy efficiency is $\eta = 0$.

(2) Charge-type balancing topology

Assume that the charging current of charge-type topology is i_c, the efficiency is η_c, and the voltage of SCESS is U_{SCESS}. The discharge current of the higher voltage SC is $u_a i_c / U_{SCESS} / \eta_c$. The balancing

time can be calculated as (37). Then, the total power losses can be calculated as (38). The round-trip energy efficiency is expressed as (39).

$$t_{\mathrm{c}} = \eta_{\mathrm{c}} C U_{\mathrm{SCESS}} (u_{\mathrm{h}} - u_{\mathrm{a}}) / u_a i_{\mathrm{c}} \tag{37}$$

$$W_{\mathrm{total\_losses}} = (u_{\mathrm{a}} i_c / \eta_{\mathrm{c}} - u_{\mathrm{a}} i_c) t_{\mathrm{c}} = (1 - \eta_{\mathrm{c}}) C U_{\mathrm{SCESS}} (u_{\mathrm{h}} - u_{\mathrm{a}}) \tag{38}$$

$$\eta = 1 - \frac{W_{\mathrm{total\_losses}}}{W_{\mathrm{to\_be\_transfered}}} = 1 - \frac{2(1 - \eta_{\mathrm{c}}) U_{\mathrm{SCESS}}}{u_{\mathrm{h}} + u_{\mathrm{a}}} \tag{39}$$

(3) Proposed dischage-type balancing topology

Assume that the current of discharge-type topology is i_{d} and the efficiency is η_{d}. The discharging current of the higher voltage SC is i_{d}-$i_{\mathrm{d}} u_{\mathrm{h}} \eta_{\mathrm{d}} / U_{\mathrm{SCESS}}$. The balancing time can be calculated as (40). Then, the total power losses can be calculated as (41). The round-trip energy efficiency is expressed as (42).

$$t_{\mathrm{d}} = \frac{C U_{\mathrm{SCESS}} (u_{\mathrm{h}} - u_{\mathrm{a}})}{(U_{\mathrm{SCESS}} - u_{\mathrm{h}} \eta_{\mathrm{d}}) i_{\mathrm{d}}} \tag{40}$$

$$W_{\mathrm{total\_losses}} = (u_{\mathrm{h}} i_{\mathrm{d}} - u_{\mathrm{h}} i_{\mathrm{d}} \eta_{\mathrm{d}}) t_{\mathrm{d}} = \frac{(1 - \eta_{\mathrm{d}}) C u_{\mathrm{h}} (u_{\mathrm{h}} - u_{\mathrm{a}})}{1 - u_{\mathrm{h}} \eta_{\mathrm{d}} / U_{\mathrm{SCESS}}} \tag{41}$$

$$\eta = 1 - \frac{W_{\mathrm{total\_losses}}}{W_{\mathrm{to\_be\_transfered}}} = 1 - \frac{2(1 - \eta_{\mathrm{d}}) u_{\mathrm{h}}}{(1 - u_{\mathrm{h}} \eta_{\mathrm{d}} / U_{\mathrm{SCESS}})(u_{\mathrm{h}} + u_{\mathrm{a}})} \tag{42}$$

From the above analysis, we can see that the round-trip energy efficiency increases with the increase of efficiency of balancing topology. The round-trip energy efficiency of switched resistance balancing topology is zero. The round-trip energy efficiency of charge-type balancing topology can even be less than zero, that is to say, the charge-type balancing topology can dissipate more energy than the switched resistance balancing topology in a particular condition. That is because the energy will be consumed when passing through the charge-type balancing topology and the longer the balancing time is, the more energy will be expenditure. The round-trip energy efficiency of proposed discharge-type topology is slightly lower than the efficiency of the cascaded converter module. It is a pity that many hypotheses are assumed and some power losses (for example, the power losses of equivalent internal resistance) are ignored in mathematical analysis, so the calculated results of round-trip energy efficiency are not very accurate. Fortunately, we can obtain accurate round-trip energy efficiency by experiments, and the experimental results can be processed as (33)–(35).

4. Experiment and Results

The 7500 F, 2.7 V organic electrolyte carbon electrode SCs manufactured by china railway rolling stock corporation are used in this experiment and the SCESS consists of three SCs. The input of the cascaded converter module can be selected as 1.5–3 V. The peak current of the fly-back converter is i_{p} = 20 A and the frequency is f_s = 50 KHz. The UC3844 ICs are used to control the fly-back converters which have the cycle-by-cycle peak current limit function with a 50% maximum duty cycle. The comparator LM319 and the flip-flop HEF4027B (NXP Semiconductors, Washington, WA, USA) are used to achieve hysteresis current control of the boost converter. An STM32F407 control board (ST Microelectronics, Geneva, Switzerland) is used to control the whole system, including the voltage sampling, generating the control signal CS. Other experiment conditions are summarized in Table 1 and the photograph of the experiment platform is shown in Figure 19.

Table 1. The experiment conditions.

cascaded converter module	Switches	IRLR7843TRPBF
	Transformer ratio n	1:3
	Magnetizing inductances L_m	20 μH
	Filter capacitor C_o	2200 μF/16 V
	Peak current i_p	20 A
	Current transformer ratio	100:1
Boost converter	The switch S	IRFR4620
	Filter inductance L	10 μH
	The diode D_R	VBT4045BP

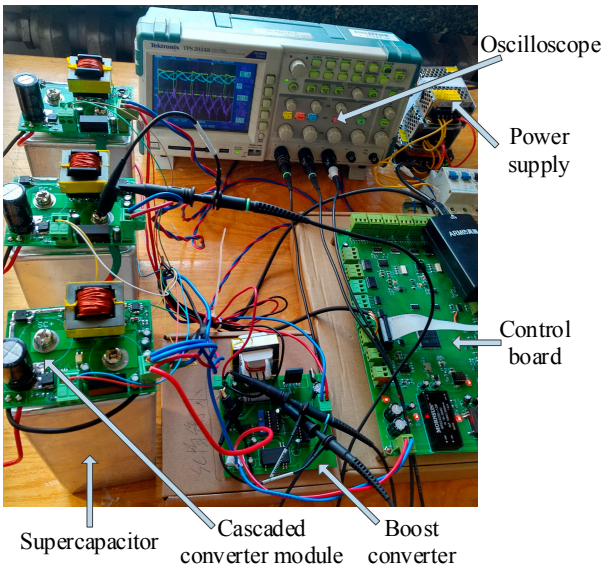

Figure 19. The photograph of the experiment platform.

The waveforms of the output current i_o, current i_{Lm}, and PWM of the cascaded converter module are shown as Figure 20. As shown in Figure 20a, the output current i_o = 1 A, the PWM duty cycle is 50%, and the peak current of i_{Lm} is 6 A which does not reach the designed 20 A peak current. As shown in Figure 20b, the output current i_o = 3.1 A, the PWM duty cycle is 50%, and the peak current of i_{Lm} is 20 A. As shown in Figure 20c, the output current i_o = 4 A, the PWM duty cycle is 35%, and the peak current of i_{Lm} is 20 A. The ideal output current $\bar{i}_{oideal}$ is 3.2 A, which is calculated as (11). When $i_o < \bar{i}_{oideal}$, the discharge current i_{Lm} increases with the increase of output current i_o, while i_{Lm} decreases with the increase of i_o when $i_o > \bar{i}_{oideal}$. The discharging power and efficiency change with output current i_o are shown as Figure 21. The discharging power first increases and then decreases with the increase of output current i_o. When i_o = 3.2 A, the discharging power reaches the maximum, which is consistent with the calculated ideal output current. The ideal output current hardly changes with the changing of u_{SC} and the discharging power increases with the increase of u_{SC}. The efficiency of the cascaded converter module decreases with the increase of the output current and the efficiency is 80% at the ideal output current. The drive of short circuit switch S_S is decided by the control signal CS and the voltage of the output capacitor u_{oi}. As shown in Figure 22, CS is the control signal, u_o is the voltage of the output capacitor, and G_{SS} is the drive of the short circuit switch S_S. The short circuit switch S_S will not turn on until CS = 0 and the voltage u_o reaches an acceptable low value.

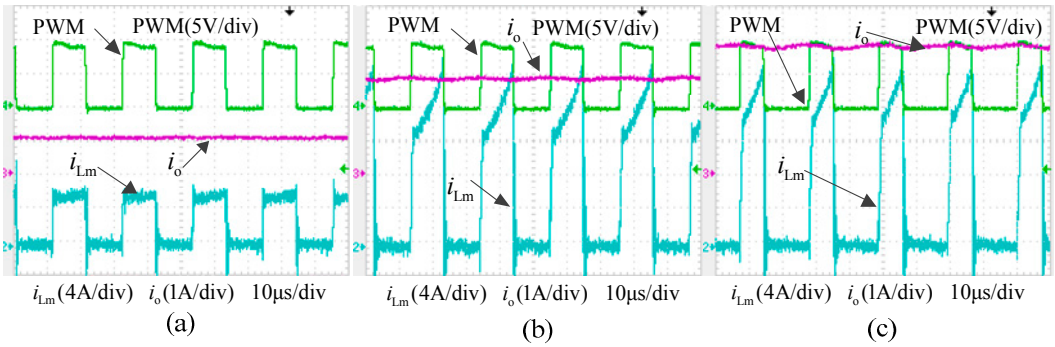

Figure 20. Main waveforms of the modularized converter module. (**a**) With output current i_o = 1 A. (**b**) With output current i_o = 3.1 A. (**c**) With output current i_o = 4 A.

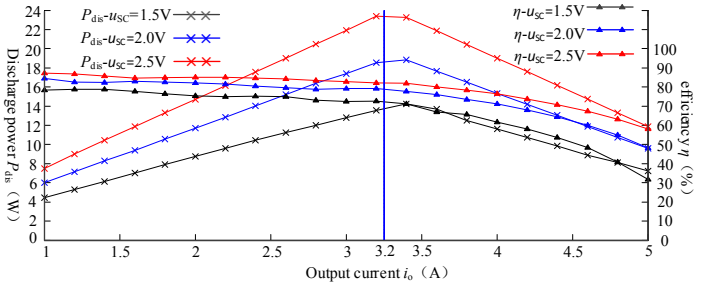

Figure 21. The discharging power and efficiency change with output current.

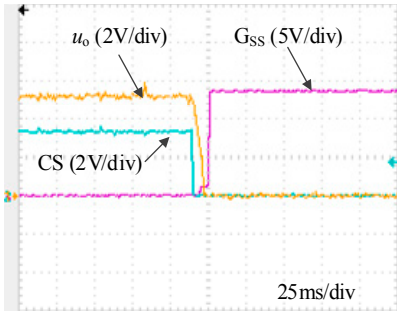

Figure 22. The drive of short circuit switch S_S.

The voltages of the SCs are u_{SC1} = 2.6 V, u_{SC2} = 2.4 V, and u_{SC3} = 2.2 V. The main waveforms of the boost converter and balancing time are shown as Figure 23. As shown in Figure 23, i_L is the inductor current of the boost converter which is controlled with the hysteresis current control strategy, and the average value can be calculated as Equation (12). U_e is the input voltage of the boost converter, and is also the output voltage of the cascaded converter. The periodic fluctuation of U_e is caused by the periodic variation of i_L, and the average value of U_e remains unchanged at a certain i_L value. i_{fb} is the output current of the boost converter which feeds back the extra energy to the SCESS, and i_{fb} increases with the increasing of the discharging power of the cascaded converter. The PWM waveform is the drive of the boost converter and the duty cycle of the PWM increases with the increase of i_L, while the frequency decreases with the increase of i_L. The initial voltages of the SCs are u_{SC1} = 2.6 V, u_{SC2} = 2.4 V, and u_{SC3} = 2.2 V, and E_{sci} (i = 1,2,3) represents the errors between the voltages of SCs and the average voltage. When the SCESS reaches the balanced state, E_{sci} =0 (i = 1,2,3). As shown in Figure 23d, the balancing time is 300 s with the average inductor current $\bar{i}_L$ = 2A. As shown in Figure 23e, the balancing time is 220 s with the average inductor current $\bar{i}_L$ = 3.1A. As shown in

Figure 23f, the balancing time is 320 s with the average inductor current $\bar{i}_L = 3.6A$. The maximum balancing speed is reached near the ideal output current of the cascaded converter; if the output current is too large or too small, it will reduce the balancing speed. So, the control strategy based on the maximum discharging power of the boost converter will achieve the maximum balancing speed of the proposed topology.

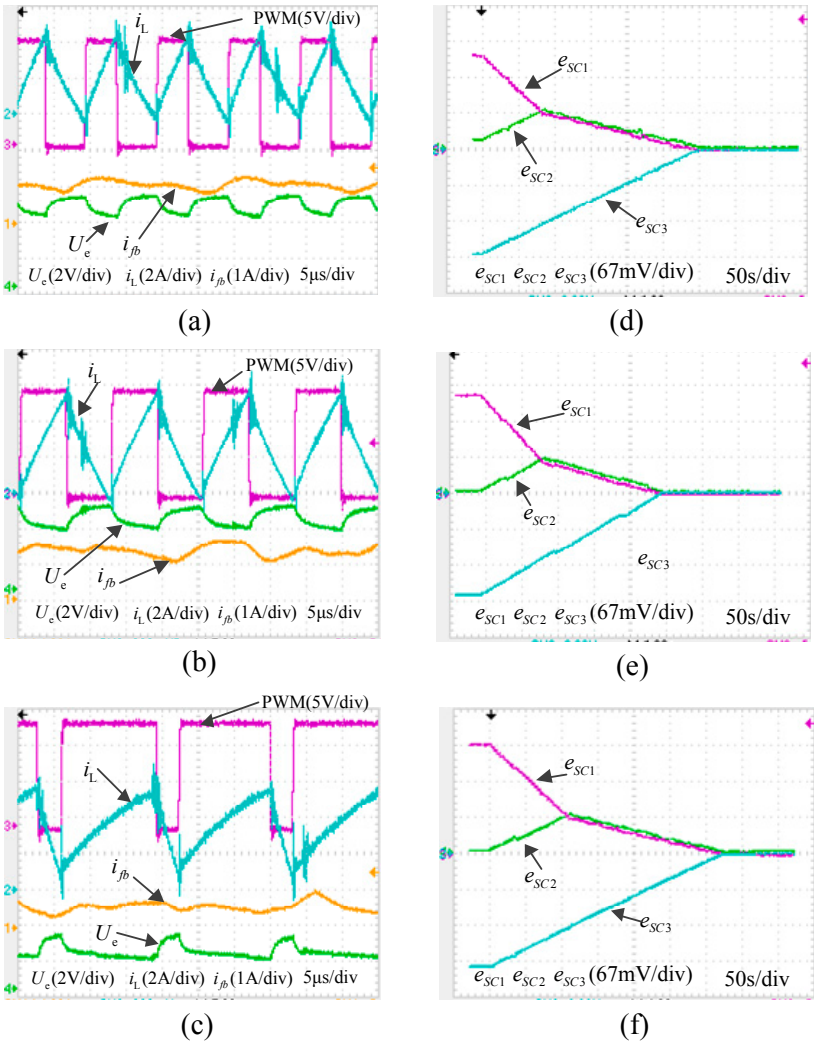

Figure 23. The main waveforms of the boost converter and the balancing time. (**a**)–(**c**) are the main waveforms of the boost converter with 2 A, 3.1 A, and 3.6 A average input current, respectively. (**d**)–(**f**) are the corresponding balancing time.

A comparative experiment is conducted to compare the balancing speed and round-trip energy efficiency. As shown in Figure 24a [18], the fly-back converters which are powered by the SCESS with 10 A output current to charge the lower voltage SCs are used as the charge-type balancing topology. As shown in Figure 24b [22], the 0.25 Ω 50 W resistor is used to discharge the higher voltage SC in the switched resistance balancing topology. The SCESS consists of three SCs with the voltages u_{SC1} = 2.6 V, u_{SC2} = 2.3 V, and u_{SC3} = 2.3 V. The balancing time is shown in Figure 25 and the experimental results are shown in Table 2.

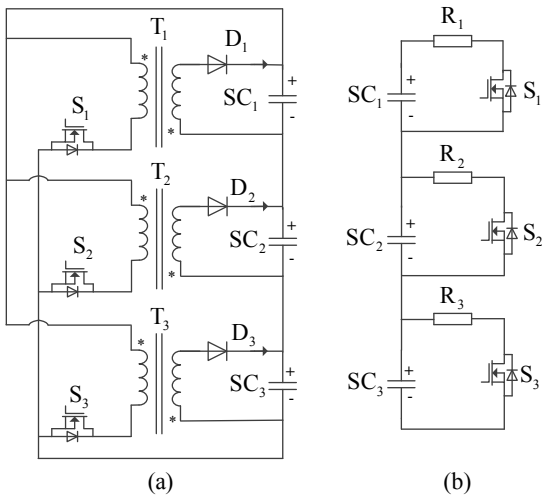

Figure 24. Charge and discharge type balancing topology used in the comparative experiment. (**a**) Charge type in [18]. (**b**) Discharge type in [22].

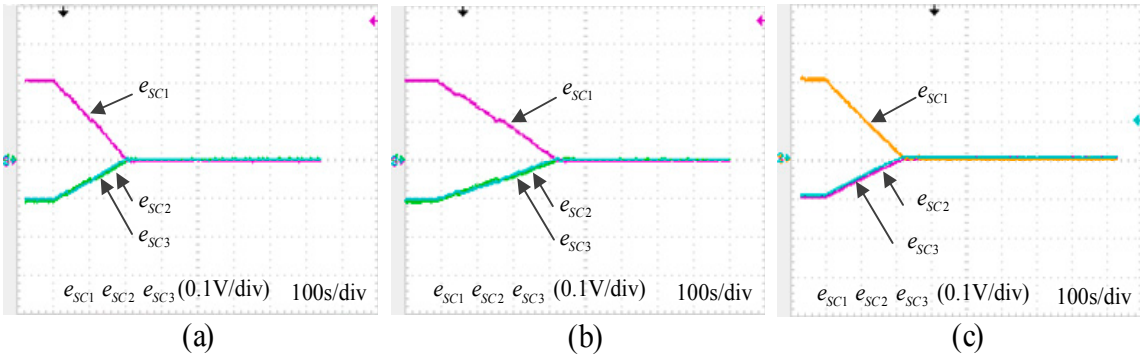

Figure 25. The balancing time of the comparative experiment. (**a**) Proposed modularized discharge-type topology. (**b**) Charge-type balancing topology. (**c**) Switched resistor method.

Table 2. The experiment results.

Methods	Voltage after Balancing u_{end}	Balancing Time t_b	Round-Trip Energy Efficiency η
Proposed method	2.38 V	200 s	68.15%
Charge-type method	2.36 V	340 s	39.12%
Switched resistor method	2.30 V	220 s	0

The experiment results are shown in Table 2. The balancing time of charge-type topology is 340 s, while the balancing time is 200 s of the proposed topology and 220 s of the switched resistor method. The proposed modularized discharge-type topology has the fastest balancing speed and the balancing speed of the switched resistor method is close to the proposed topology. However, the 0.25 Ω 50 W resistor has a big size and the round-trip energy efficiency is zero because the extra energy is dissipated in the form of heat. The round-trip energy efficiency of the charge-type method is higher than the switched resistor method but lower than the proposed topology. This experiment proved that the proposed modularized discharge-type topology has an excellent discharging performance. The balancing speed is faster and the round-trip energy efficiency is higher than the charge-type balancing topology and the switched resistor method when the voltage of an SC is much higher than the average voltage.

There are many other excellent balancing topologies; however, most of them are designed for the BESS with a small balancing current. Few papers discussed the round-trip energy efficiency of

the equalizer for BESS, because the round-trip energy efficiency for BESS is difficult to calculate or measure. Fortunately, the efficiency of many topologies is given. It will be interesting to compare the proposed balancing topology with the conventional ones and the comparison results are summed as Table 3. In Table 3, five index parameters are employed to evaluate the balancing performances, which are the discharging current (P_1), average efficiency of converter (P_2), voltage stress (P_3), number of circuit components (P_4), and control degree of freedom (P_5). The discharging current (P_1) refers to the balancing speed and the desired balancing speed of SCESS is described in (1). The average efficiency of the converter (P_2) reflects the round-trip energy efficiency; generally, high efficiency of a converter will result in a high round-trip energy efficiency. The voltage stress (P_3) refers to the voltage stress of the switches or diodes which have the largest number in the balancing system. The number of circuit components (P_4) represents the hardware cost. The control degree of freedom (P_5) refers to the control ability of SC's voltage or state of charge (SOC), which is evaluated by "high (refer to each SC's voltage can be controlled)" and "low (refer to the voltages of SCs are automatic balanced which can't be controlled)".

Table 3. Comparison of the proposed balancing topology with the conventional ones.

Topologies	Type	P_1	P_2	P_3	P_4	P_5
Bidirectional DC/DC converters [11]	Ideal	0.9 A	η	24 V	≥4N + 1	high
Multi-winding transformer [7]	Quasi ideal	0.5 A	η	10.8 V	N + 2x	low
Multi-winding transformer [9]		<0.5 A	95.6%	14.4 V	N + x + 1	low
Buck/boost converter [13]		<4 A	82.5%	5.4 V	>3N + 1	high
Switched capacitor [14]		<0.5 A	η	2.7(N − 1)	4N + 3x	low
Switched capacitor [15]		<0.5 A	90.5%	2.7(N − 1)/2	3N	low
Voltage multiplier [16]	Charge	<2 A	86%	8.2 V	3N + 2	low
Fly-back circuit [19]		<1 A	80%	80 V	3N + 2x	high
Forward circuit [20]		<0.5 A	89%	>40 V	N + 2	low
Passive discharge [22]	Discharge	0.27 A	0	2.7 V	2N	high
Fly-back converter [23]		10 A	η	3.4N − 0.7	5N + 2	high
Proposed		10 A	80%	8.1 V	5N + 3	high

① η represents the converter efficiency that is not mentioned or found in the paper; ② N is the number of cells in the battery string, x is the number of SC modules in the SCESS; ③ The voltage of the SC cell is assumed to be 2.7 V.

In Table 3, some discharging currents are represented by inequality < i_{peak} A, which means that the discharging current is a triangular current with a peak value i_{peak} and the average current changing with duty cycle D. The voltage stress of diodes in [16] is $V_B/2$ (V_B is the voltage of battery or battery module). However, the charging current flows through two diodes and the voltage drop of diodes is big. The voltage V_B should be much larger than the voltage drop, otherwise the efficiency will be low. Thus, in the experiment in [16], V_B = 16.4 V, and the voltage stress is 8.2 V in Table 3. In [20], the voltage stress is not mentioned; however, it can be calculated from the experimental data. In [23], the voltage stress is 3.4N − 0.7 = 2.7 N + 0.7(N − 1), where 0.7 is the diode forward voltage.

As shown in Table 3, each conventional balancing topology has its own advantages. For example, the topology in [11] has a high control degree of freedom, has a high converter efficiency in [9], has a small number of circuit components in [20], and has a low voltage stress in [22]. However, most of them are designed for BESS, not for SCESS, which needs a large discharge current. Although the topology in [23] has a large discharge current, the voltage stress is high and the efficiency is low. The proposed balancing topology has a large discharge current which can avoid the SCs' overvoltage phenomena and ensure the security of the SCESS. The efficiency is acceptable at a large discharge current. If the voltage stress is lower than 10 V, then the 20 V voltage level MOSFET can be used as switches. The drawback of the proposed balancing topology is the number of circuit components, which is slightly large. However, this will result in a high control degree of freedom. Thus, each SC's

voltage can be controlled and an advanced voltage balancing strategy can be used to enhance the lifetime of energy storage systems [22].

5. Conclusions

A novel modularized discharge-type topology for the voltage balance of SC string is proposed in this paper, which consists of cascaded converter modules and a boost converter. The modularized converter module is controlled in peak current mode with a 50% maximum duty cycle and the boost converter is controlled with the hysteresis current control strategy. The output of the cascaded converter modules is connected in series to form a cascaded converter and the average output current of the cascaded converter is equal to the ideal output current to achieve the maximum discharging power. The proposed modularized discharge-type voltage balancing topology has an excellent discharge performance, thus, the higher voltage SCs will be discharged with high current, and the overvoltage phenomena of SCs are avoided. The performance of the proposed topology under different output currents of the cascaded converter is verified by experiments, and the proposed topology has the fastest balancing speed with the ideal output current of the cascaded converter modules. The proposed topology has a faster balancing speed in discharging the higher voltage SCs and has a higher round-trip energy efficiency than the charge-type balancing topology and switched resistor method, which is proved by theoretical analysis and experimental results. The proposed topology can be realized by analog devices which will simplify the control of the system. What is more, the control degree of freedom is high; thus, an advanced voltage balancing strategy can be used to enhance the lifetime of energy storage systems. The proposed topology has the advantages of being secure, fast, and easy to control, which make it very suitable for high voltage SCESS applications.

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