energies

MDPI

Article

Large-Signal Stabilization of Three-Phase VSR with Constant Power Load

Bo Liu *, Hongqi Ben and Xiaobing Zhang

School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China; benhq@hit.edu.cn (H.B.); hitdqzxb@sina.com (X.Z.)

* Correspondence: hiteelb@hotmail.com; Tel.: +86-156-5762-0553

Received: 18 May 2018; Accepted: 27 June 2018; Published: 1 July 2018

Abstract: As an important interface converter, the three-phase voltage-source rectifier (VSR) connects the grid to DC-input converters. The constant power load (CPL) characteristic of the converter-load often causes large-signal stability problems. In order to solve this problem, the stability boundary of the VSR with CPL is analyzed based on the mixed potential theory, and the stability condition under large-signal disturbance is obtained; thus, the jump range of the load power can be estimated. To improve the stability of the system, a voltage loop control scheme based on ADRC is proposed. A theoretical analysis based on the mixed potential theory shows the proposed scheme expands the power jump range of the VSR with CPL effectively, and improves its disturbance rejection performance. Finally, experimental results prove the effectiveness of the proposed control scheme.

Keywords: voltage source rectifier (VSR); constant power load (CPL); large-signal stability; mixed potential theory; active disturbance rejection control (ADRC); power jump range

1. Introduction

In order to achieve the goal of multi-functionality, low-cost and high reliability, modularization has become an important trend in power electronics [1–3]. In the process of modularizing power electronic devices, the situation of converters as loads becomes more and more common, and has attracted wide attention [4,5]. As important interface converters, three-phase voltage-source rectifiers (VSRs) connect the grid to DC-input converters, and are widely used in the fields of electric vehicle charging [6], DC micro-grid [7], more electric aircrafts (MEAs) [8], and photovoltaic generation [9].

Many academic papers have focused on stability issues related to three-phase VSRs (or voltage-source inverters, VSIs). In [10], bifurcation and large-signal stability of VSR are analyzed under grid voltage dips, and the stable operating region is identified. Mehrasa M. and Pouresmaeil E. use direct Lyapunov method to discuss a series of stability issues of VSRs applied in different power sectors such as modular multilevel converters (MMCs) [3,11], shunt active power filters [12], and distributed generation [13,14]. A dynamic model in d-q frame with six independent dynamical state variables is obtained, and global asymptotical stability is achieved by the use of direct Lyapunov method [11]. Furthermore, a multi-loop control strategy is proposed to provide stable operation under both MMC's arm inductance and resistance parameters variations, and also loads changes [3].

However, the above studies do not focus on the effect of load characteristics on the stability of VSR. Figure 1 shows the schematic of a three-phase VSR cascaded with a DC-input converter. In this situation, for VSR, the load is no longer a resistance, but a converter with a constant power load (CPL) characteristic because of its closed-loop control. The CPL causes stability problems easily [15–17]; moreover, the problems are more significant when the DC-bus capacitance is a small-capacity film capacitor to improve the system life and reliability. Some scholars have discussed this problem and put forward some solutions based on small signal stability theory, such as the passive damping

method [18,19], sliding mode control method [17], virtual impedance (active damping) method [20–22], and so on. However, when the cascaded system suffers from a large-signal disturbance such as load power jump or grid voltage drop, the small signal stability theory is no longer applicable, because the theory only studies the stability problems near the operating point.

The problems of large-signal stability in converters with CPLs were analyzed in some literature in recent years [16,23,24]. In [23], the large-signal stability region of a DC/DC converter is estimated by a small signal loop. The norm inequalities are used to get the sufficient conditions for converter stability in order to estimate the stable region of the system. Furthermore, the effect of the small signal loop gain on the large-signal stability region is revealed. In [24], the Hamiltonian function method is used to discuss the influence of pulse load on the stability of the system, and some details of the transient response are shown. It indicates that pulse load has special effect on the stability of cascaded systems. For example, the system is in an unstable state when the load is connected, however it may attenuate to a stable state during the load disconnection. In general, it was called a metastable state. In [16], the influence of the negative impedance characteristic of CPLs on the stability of the converter is studied based on the mixed potential theory. In addition, a method to improve the large-signal stability in the cascade system is proposed with multistage LC filters. However, this method requires additional passive components, which increases the volume of the device.

On the premise of no additional circuits, some meaningful work on control methods has been undertaken to improve the large-signal stability of converters with CPLs [25–28]. The sliding mode control method to improve the stability of VSR is proposed in [25]. In this method, the voltage loop is controlled by sliding mode, and the state observer of the real-time power of the system is designed to observe the power. Furthermore, the parameters of the state observer are derived from the Lyapunov stability theorem. However, for different systems, there is no uniform method to establish the Lyapunov function, so the realization process of the control algorithm is relatively complicated. Moreover, due to the boundary of the current and grid voltage, the range of attraction area for large-signal disturbance is limited, which limits its practicality. In [26], a "stabilizing agent" is implemented on each CPL to reduce the negative impedance characteristic to solve the DC micro-grid stability problem. Thanks to the improved fault tolerance of the solution, the method permits us to consider several fault scenarios, such as the electrical reconfiguration, or the failure of an agent. In [27], multiple linear controllers are designed at different operating points of a three-phase VSR and switched according to certain rules. When the load changes, the drop and overshoot of DC bus voltage are both significantly reduced. The stability of the control method is proved by the general Lyapunov functions. To improve the dynamic performance of three-phase VSR with large-signal disturbance, a direct voltage control method based on feedback linearization is proposed in [28]. The scheme breaks through the conventional double closed-loops control mode, and directly controls input variables by voltage error, so as to stabilize the bus voltage rapidly. However, this scheme relies on an accurate mathematical model of the circuits. Some abnormal operating conditions, such as the imbalance of the grid voltage, would lead to poor control performance.

Active disturbance rejection control (ADRC) has been widely studied because of its excellent immunity against disturbance sources [29–31], and has been applied to motion control [30], power electronics, and so on [31]. However, the stability of converters with ADRC has not been adequately analyzed, especially for large-signal stability problems.

In this paper, the authors are discussing the large-signal stability of three-phase VSRs with CPL. The main contributions are triple:

(1) Obtaining a large-signal model of three-phase VSR with CPL based on mixed potential theory, whose stable boundary is derived when load power jumps.
(2) Proposing a voltage control scheme to improve the large-signal stability based on ADRC, and whose control stability is proven.
(3) Deriving the stable boundary of VSR with CPL based on ADRC, which proves that the proposed control scheme expands the load power jump range effectively.

The rest of this paper is organized into four sections. Following the introduction, a large-signal stability analysis based on mixed potential theory under PI control is provided in Section 2. The proposed control scheme based on ADRC and the stability analysis of it is presented in Section 3. Moreover, the effectiveness of the control scheme is verified by experiments in Section 4. Finally, some conclusions are drawn in Section 5, and an Appendix A is given after that.

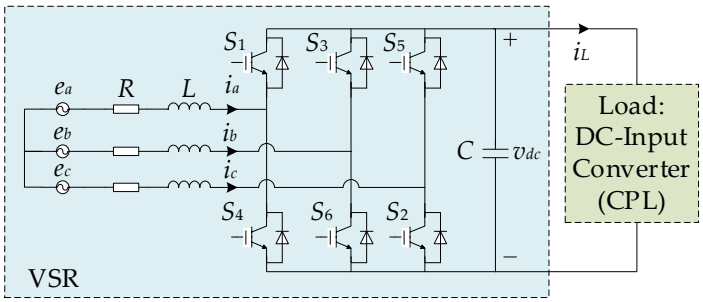

Figure 1. Schematic of three-phase VSR cascaded with a DC-input converter.

2. Large-Signal Stability Analysis Based on Mixed Potential Theory under PI Control

2.1. Introduction to the Mixed Potential Theory

The mixed potential theory is a method to study the stability of nonlinear circuits by constructing Lyapunov functions, especially for circuits with CPLs [32,33]. The mixed potential functions are functions related to energy, which are composed of current potential functions and voltage potential functions. The core content of the theory is to establish mixed potential functions to satisfy certain stability theorems, and finally, to obtain the ranges of the system parameters to ensure stability.

The mixed potential function P consists of resistance, capacitance, and inductance in a nonlinear network. Assume $i_1, \ldots, i_r$ represents inductor currents, and $v_{r+1}, \ldots, v_{r+s}$ are capacitor voltages. P is defined as:

$$P = \int \sum_{\mu > r+s} v_\mu di_\mu + \sum_{\sigma=r+1}^{r+s} i_\sigma v_\sigma \tag{1}$$

In Equation (1), the first item on the right is the current potential of all the non-storage elements; the second is the sum of energy in capacitors. If v_μ can not be represented by i_μ, the current potential can be written by voltage potential and Equation (2):

$$\int v_\mu di_\mu = v_\mu i_\mu - \int i_\mu dv_\mu \tag{2}$$

The relationship between P and the system state equation can be described as:

$$\begin{cases} L\frac{di_\rho}{dt} = \frac{\partial P}{\partial i_\rho} \\ -C\frac{dv_\sigma}{dt} = \frac{\partial P}{\partial v_\sigma} \end{cases} \tag{3}$$

where L and C are inductance and capacitance respectively in the circuit.

Equation (3) gives the criterion to verify the validity of the mixed potential functions. Generally speaking, the unified form of P is:

$$P(i, v) = -A(i) + B(v) + (i, \gamma v - \alpha) \tag{4}$$

where $A(i)$ and $B(v)$ represents the current potential and voltage potential of the non-storage elements in the circuit respectively, $(i, \gamma v - \alpha)$ represents the energy of capacitors and parts of non-storage

elements in the circuits, where γ is a constant matrix not necessarily associated with circuit topology with elements ± 1, 0, and α is constant vector.

2.2. Stability Problems of the Three-Phase VSR with CPL

Because VSRs are often used as grid interface converters, their loads are usually not resistors, but power electronic converters. Power electronic converters are usually controlled by closed loops; therefore, they are regarded as CPLs. Taking the DC/DC converter as an example of the load, when the input current suddenly rises, the input voltage will decrease in order to maintain the output constant. The characteristic of maintaining constant power is called the CPL characteristic. This characteristic is bad for the stability, which will be explained below.

Take the voltage source in series with CPL as an example, as shown in Figure 2. When the CPL is disturbed to cause the input current i_{CPL} to rise, in order to maintain its output constant, the input voltage v_{CPL} of the CPL will decrease. However, this will lead to an increase in the voltage on the resistance Rs to make the current i_{CPL} rise again. This response, similar to positive feedback, takes the circuit away from the operating point, and causes it to lose stability. The larger the disturbance, the more significant stability problems caused by CPL will be.

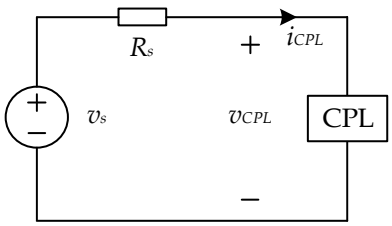

Figure 2. The circuit of voltage source in series with CPL.

2.3. Analysis of Power Jump Range of Three-Phase VSR with CPL

The average model equivalent circuit of three-phase VSR with CPL in dq coordinates system is shown in Figure 3. Neglecting the power loss, Equation (5) can be obtained based on the power balance.

$$i_o = \frac{v_d i_d + v_q i_q}{v_{dc}} \tag{5}$$

where $v_{d,q}$ are the control voltage in the dq coordinates respectively, $i_{d,q}$ are the grid current in the dq coordinates respectively, i_o is the output current of the equivalent current source on the DC side, and v_{dc} is the output voltage of the VSR.

According to the mixed potential theory, the current potential function of non-storage elements in the circuit is:

$$\begin{aligned} \int \sum_{\mu > r+s} v_\mu di_\mu \quad &= \int_0^{i_d} e_d di_d - \int_0^{i_d} Ri_d di_d - \int_0^{i_d} v_d di_d + \int_0^{i_d} 3\omega L i_q di_d + \int_0^{i_q} e_q di_q \\ &- \int_0^{i_q} Ri_q di_q - \int_0^{i_q} v_q di_q - \int_0^{i_q} 3\omega L i_d di_q + \int_0^{i_o} v_{dc} di_o - \int_0^{i_L} v_{dc} di_L \end{aligned} \tag{6}$$

where $v_{d,q}$ are the control voltage in the dq coordinates respectively, R is the equivalent series resistance of the grid side, i_L is the load current of the VSR.

The potential energy stored in the capacitor in the circuit is:

$$\sum_{\delta=r=1}^{r+s} i_\delta v_\delta = -i_o v_{dc} + P_{CPL} \tag{7}$$

where P_{CPL} is the power of the CPL.

From Equations (6) and (7), the mixed potential function of the system can be obtained as:

$$P(v,i) = \int \sum_{\mu>r+s} v_\mu di_\mu + \sum_{\delta=r=1}^{r+s} i_\delta v_\delta = \begin{array}{l} e_d i_d + e_q i_q - \frac{1}{2}Ri_d^2 - \frac{1}{2}Ri_q^2 - \int_0^{i_d} v_d di_d - \int_0^{i_q} v_q di_q \\ + \int_0^{i_d} 3\omega L i_q di_d - \int_0^{i_q} 3\omega L i_d di_q - \int_0^{v_{dc}} i_o dv_{dc} + \int_0^{v_{dc}} \frac{P_{CPL}}{v_{dc}} dv_{dc} \end{array} \quad (8)$$

According to Equation (3), the relationship between P and the state equations of the circuit can be used to verify the correctness of the function:

$$\begin{cases} \frac{\partial P}{\partial i_d} = e_d - Ri_d - v_d + 3\omega L i_q = L\frac{di_d}{dt} \\ \frac{\partial P}{\partial i_q} = e_q - Ri_q - v_q - 3\omega L i_d = L\frac{di_q}{dt} \\ \frac{\partial P}{\partial v_{dc}} = -i_o + \frac{P_{cpl}}{v_{dc}} = -C\frac{dv_{dc}}{dt} \end{cases} \quad (9)$$

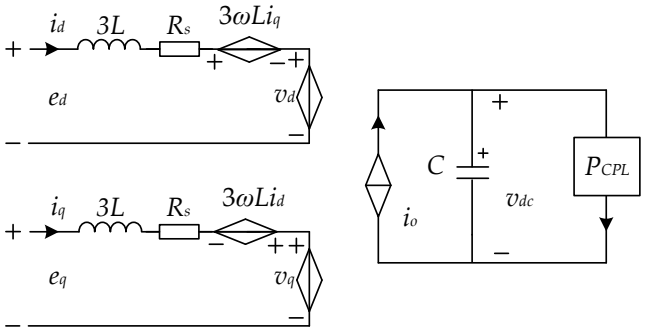

Figure 3. The equivalent circuit of three-phase VSR with CPL in dq coordinates.

This indicates that Equation (9) satisfies the form Equation (3), which proves that the mixed potential function P is correct.

The proportional integral (PI) regulators are commonly used to control voltage and current of the three-phase VSR, as shown in Figure 4. The control loop equations are:

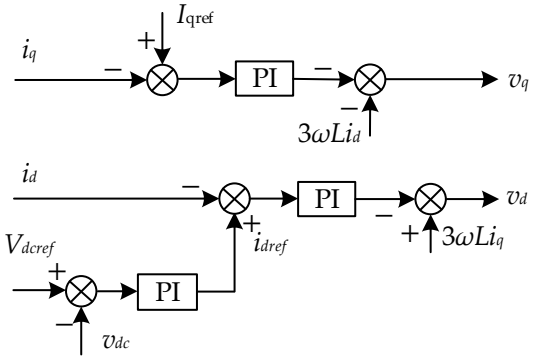

Figure 4. Control block diagram of the three-phase VSR with conventional PI control.

$$\begin{cases} v_d = -\left(K_{ip}\left(i_{dref} - i_d\right) + K_{ii}\int\left(i_{dref} - i_d\right)dt\right) + 3\omega L i_q & (10a) \\ v_q = -\left(K_{ip}\left(I_{qref} - i_q\right) + K_{ii}\int\left(I_{qref} - i_q\right)dt\right) - 3\omega L i_d & (10b) \\ i_{dref} = K_{vp}\left(V_{dcref} - v_{dc}\right) + K_{vi}\int\left(V_{dcref} - v_{dc}\right)dt & (10c) \end{cases}$$

where V_{dcref} is the output voltage reference of the VSR, I_{qref} is the current reference of the q axis, ω is the frequency of the grid, K_{ip} and K_{ii} are the proportion and integral coefficients of PI regulator of d

axis current and q axis current respectively, K_{vp}, K_{vi} are the proportion and integral coefficients of PI regulator in voltage loop, respectively.

According to Appendix A, the current potential function of the circuit is a second order matrix:

$$\boldsymbol{A}(i) = \begin{bmatrix} -e_d i_d + \frac{1}{2}Ri_d^2 + \int_0^{i_d} v_d di_d + \int_0^{i_d} 3\omega L i_q di_d & 0 \\ 0 & -e_q i_q + \frac{1}{2}Ri_q^2 + \int_0^{i_q} v_q di_q - \int_0^{i_q} 3\omega L i_d di_q \end{bmatrix} \tag{11}$$

and the voltage potential function is a first order matrix:

$$\boldsymbol{B}(v) = -\int_0^{v_{dc}} i_o dv_{dc} + \int_0^{v_{dc}} \frac{P_{CPL}}{v_{dc}} dv_{dc} \tag{12}$$

In order to analyze the stability, the second order partial derivatives of $\boldsymbol{A}(i)$ and $\boldsymbol{B}(v)$ are solved as:

$$\boldsymbol{A_{ii\_PI}}(i) = \frac{\partial^2 \boldsymbol{A}(i)}{\partial i^2} = \begin{bmatrix} R + K_{ip} & 0 \\ 0 & R + K_{ip} \end{bmatrix} \tag{13}$$

$$\boldsymbol{B_{vv\_PI}}(v) = \frac{\partial^2 \boldsymbol{B}(v)}{\partial v^2} = \frac{K_{vi}K_{ip}i_d C\left(V_{dcref} - v_{dc}\right)}{e_d i_d - P_{CPL}} - \frac{K_{vp}K_{ip}i_d}{v_{dc}} + \frac{v_d i_d - P_{CPL}}{v_{dc}^2} \tag{14}$$

According to the mixed potential stability theorem in the Appendix A, the sufficient condition for the stability of the three-phase VSR with CPL under large-signal perturbation is:

$$P_{CPL\_PI} < \frac{C(R + K_{ip})}{3L} v_{dc}^2 - K_{vp}K_{ip}v_{dc}i_d + v_d i_d + \underbrace{\frac{K_{vi}K_{ip}Cv_{dc}}{e_d i_d - P_{CPL\_PI}}\left(V_{dcref} - v_{dc}\right)}_{M} \tag{15}$$

By Equation (15), the maximum power jump range of the three-phase VSR with CPL can be estimated. This result is used on the one hand to measure the performance of the VSR, and on the other hand, as a technical requirement to improve the parameter design. It is worth noting that because this result is a sufficient condition for large-signal stability, it is somewhat conservative.

3. Control Scheme and Stability Analysis Based on ADRC

In the case of disturbance, the principle of PI regulators is to compensate for errors which occur in the integrator. However, when the disturbance is large, the delay effect of the integrator makes the regulator unable to quickly and accurately obtain the disturbance information and compensate, which easily leads to instability. Therefore, a control scheme based on ADRC with excellent immunity is proposed to enhance the stability of VSR with CPL under large-signal disturbance.

The general structure of ADRC is shown in Figure 5. It includes the expanded state observer (ESO), the state error feedback (SEF), the transient profile generation (TPG) and the rejection. ADRC is not dependent on the mathematical model of the controlled plant. All the uncertain disturbances acting on the controlled plant are considered as "uncertain disturbances", and the input and output signals are used to estimate and compensate for them. Thanks to the ESO and rejection, ADRC has omitted the integral part compared with the conventional PI regulator. This characteristic coincided with the need to improve the stability under large-signal disturbance. In this paper, a linear ADRC is proposed and the parameters can be simplified by ESO bandwidth and system bandwidth, which makes it easy to set.

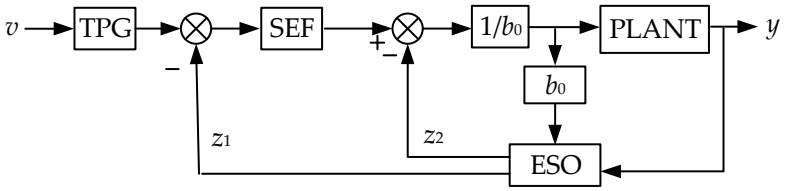

Figure 5. General structure of ADRC.

3.1. Voltage Loop Control Scheme Based on the First Order ADRC

The control block of the voltage loop of three-phase VSR based on ADRC is shown in Figure 6. For the three-phase VSR with CPL, the DC side voltage equation is:

$$C\frac{dv_{dc}}{dt} = \frac{e_d i_d - Ri_d^2}{v_{dc}} - \frac{P_{CPL}}{v_{dc}} \tag{16}$$

Ignoring the equivalent series resistance R and matching the form of ADRC plant, Equation (16) is rewritten as a first order differential equation:

$$\dot{y} = w + bu \tag{17}$$

where $w = -2P_{CPL}/C$ is the external disturbance, $u = i_{dref}$ is the reference of d-axis current, $b = 2e_d/C$ is the control gain, and $y = v_{dc}^2$ is the input of ADRC.

Assume $b_0 \approx b$ is the estimation of control gain. Let $x_1 = y$, uncertain disturbance (including external disturbance and internal disturbance) $f(y, \dot{y}, u) = w + (b - b_0)u$. Then, extending the uncertain disturbance to the state variable $x_2 = f(y, \dot{y}, u)$, the state equations of voltage loop are:

$$\begin{cases} \dot{x}_1 = x_2 + b_0 u \\ \dot{x}_2 = h \\ y = x_1 \end{cases} \tag{18}$$

where x_1, x_2 is the state variables, and $h = \dot{f}(y, \dot{y}, u)$.

A liner ESO can be established from Equation (18) as:

$$\begin{cases} \dot{z}_1 = z_2 + \beta_1(x_1 - z_1) + b_0 u \\ \dot{z}_2 = \beta_2(x_1 - z_1) \end{cases} \tag{19}$$

Suitable gains β_1 and β_2 make z_1 and z_2 in ESO achieve good tracking effect on x_1 and x_2. Ignore the estimation error of ESO, that is, $z_1 \to x_1$ and $z_2 \to x_2$. Meanwhile, if we let

$$u = \frac{-z_2 + u_0}{b_0} \tag{20}$$

Equation (17) can be simplified as:

$$\dot{y} = (f(y, \dot{y}, u) - z_2) + b_0 u = u_0 \tag{21}$$

The SEF of ADRC is designed as a proportional term:

$$u_0 = K_p(v - z_1) \tag{22}$$

where $v = V_{dcref}^2$.

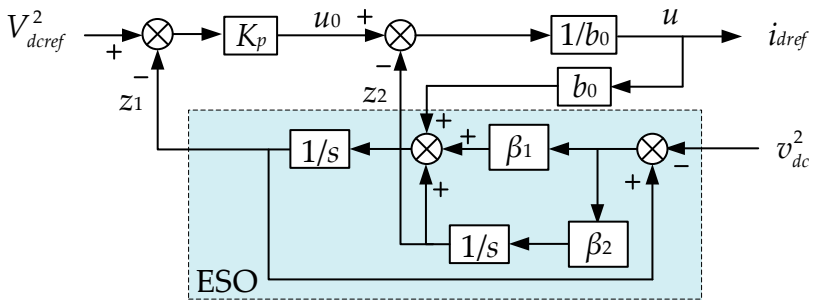

Figure 6. Control block of the voltage loop of three-phase VSR based on ADRC.

3.2. Parameters Simplification and Stability Proof

First, the key parameters of ESO and SEF in ADRC are designed. For the ESO as Equation (19), the characteristic polynomial is given by:

$$\lambda(s) = s^2 + \beta_1 s + \beta_2 \tag{23}$$

Setting the pole of the characteristic equation as ESO bandwidth ω_0, which results in:

$$\beta_1 = 2\omega_0,\ \beta_2 = \omega_0^2 \tag{24}$$

Let the proportional gain

$$K_p = \omega_c \tag{25}$$

where ω_c is the system bandwidth.

Therefore, the parameters design of the ADRC is simplified as the design of system bandwidth and ESO bandwidth. In this paper, taking ω_c = 100. According to engineering experience, ω_0 is generally five to ten times ω_c, and is set as ω_0 = 800 here.

In order to prove the VSR based on ADRC stable, the convergence of ESO should be proven first. From Equations (19) and (24), the transfer functions of the variables z_1 and z_2 of ESO in the frequency domain are given by:

$$z_1 = \frac{\beta_1 s + \beta_2}{s^2 + \beta_1 s + \beta_2} y + \frac{b_0 s}{s^2 + \beta_1 s + \beta_2} u = \frac{2\omega_0 s + \omega_0^2}{s^2 + 2\omega_0 s + \omega_0^2} y + \frac{b_0 s}{s^2 + 2\omega_0 s + \omega_0^2} u \tag{26}$$

$$z_2 = \frac{\beta_2 s}{s^2 + \beta_1 s + \beta_2} y - \frac{b_0 \beta_2}{s^2 + \beta_1 s + \beta_2} u = \frac{\omega_0^2 s}{s^2 + 2\omega_0 s + \omega_0^2} y - \frac{b_0 \omega_0^2}{s^2 + 2\omega_0 s + \omega_0^2} u \tag{27}$$

Let the tracking error $e_1 = z_1 - y$ and $e_2 = z_2 - f(y, \dot{y}, u)$, then

$$e_1 = -\frac{s^2}{s^2 + 2\omega_0 s + \omega_0^2 s} y + \frac{b_0 s}{s^2 + 2\omega_0 s + \omega_0^2 s} u \tag{28}$$

$$e_2 = -\left(1 - \frac{\omega_0^2}{s^2 + 2\omega_0 s + \omega_0^2}\right) ys + \left(1 - \frac{\omega_0^2}{s^2 + 2\omega_0 s + \omega_0^2}\right) b_0 u \tag{29}$$

Without loss of generality, y and u are all set as step signals of magnitude K, that is, $y = K/s$ and $u = K/s$. Then the steady-state errors are:

$$\begin{cases} e_{1s} = \lim\limits_{s \to 0} s e_1 = 0 \\ e_{2s} = \lim\limits_{s \to 0} s e_2 = 0 \end{cases} \tag{30}$$

This indicates that the ESO has good convergence and estimation. On this basis and from Equations (17)–(22), the voltage closed loop transfer function of VSR based on ADRC is given by:

$$G(s) = \frac{K_p}{s + K_p} \tag{31}$$

Obviously, if only $K_p > 0$, the three-phase VSR based on ADRC is stable.

3.3. Large Sigal Stability Analysis of Three-Phase VSR with CPL Based on ADRC

The power jump range is still analyzed by mixed potential theory in this section to discuss the stability of three-phase VSR with CPL based on ADRC. Assume $z_1 = v_{dc}^2$ and $b_0 = b$, then

$$z_2 = f(y, \dot{y}, u) = -2P_{CPL}/C \tag{32}$$

The control function of voltage loop is given by:

$$i_{dref} = \frac{u_0 - z_2}{b_0} = \frac{CK_p(V_{dcref}^2 - v_{dc}^2) + 2P_{CPL}}{2e_d} \tag{33}$$

The control loop equations of a three-phase VSR based on ADRC are constructed by Equations (10a), (10b) and (33). The current potential function and the voltage potential function are still Equations (11) and (12) respectively. In the same way as in Section 2.3, the stability is analyzed by the theorem in the Appendix A. According to the control loop Equations (10a), (10b) and (33), the second order partial derivatives of $\boldsymbol{A}(i)$ and $\boldsymbol{B}(v)$ are solved as:

$$\boldsymbol{A_{ii\_ADRC}}(i) = \begin{bmatrix} R + K_{ip} & 0 \\ 0 & R + K_{ip} \end{bmatrix} \tag{34}$$

$$\boldsymbol{B_{vv\_ADRC}}(v) = -\frac{K_p K_{ip} C i_d}{e_d} + \frac{v_d i_d - P_{CPL}}{v_{dc}^2} \tag{35}$$

According to the mixed potential stability theorem in the Appendix A, the sufficient condition for the stability of the three-phase VSR with CPL based on ADRC under large-signal perturbation is:

$$P_{CPL\_ADRC} < \frac{C(R + K_{ip})}{3L} v_{dc}^2 - \frac{K_p K_{ip} C v_{dc}^2 i_d}{e_d} + v_d i_d \tag{36}$$

Compared with the Equation (15), it can be seen that the power jump range under large-signal disturbance is different from that of PI control. Specifically, on the premise that the two methods have the same gain (i.e., $K_p = K_{vp}$), the difference between Equations (15) and (36) is determined by item M in Equation (15). The instability leads by large-signal disturbance mainly refers to the shock and divergence of the bus voltage when the CPL power increases. Therefore, under the premise of restoring stability, the minimum bus voltage must appear at the first oscillatory trough after the disturbance, as shown in Figure 7. In the process, the bus voltage reduces from V_{dcref} to the minimum value V_{dcmin}, energy in the capacitor is continuously extracted to meet the power requirement of the CPL, so $e_d i_d - P_{CPL\_PI} < 0$, or $M < 0$. It can be concluded that when there is a large-signal disturbance, the power jump range of VSR based on ADRC is larger than PI control. In other words, the stability is better.

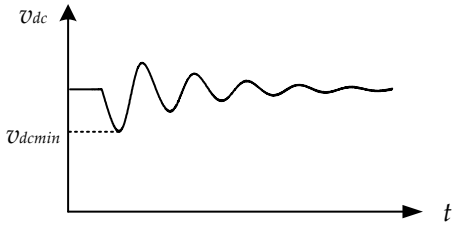

Figure 7. Bus voltage under large-signal disturbance (power sudden increase).

4. Experiments

To verify the proposed control methods, a prototype of the three-phase VSR with CPL as shown in Figure 8 is built and tested. The system configuration is shown in Figure 1. Detailed parameters of the three-phase VSR are listed in Table 1, and the control circuit is based on the digital signal processor (TMS320F28335). The CPL is a full bridge DC/DC converter, of which the input voltage is 650 V, the output voltage v_{CPL_o} is 300 V, and switching frequency is 20 kHz.

Figure 9a shows the main operating waveforms of the VSR with conventional PI control. At the beginning, the load power of VSR was 2 kW, and the system operated under light load. When the load power suddenly increased to 10 kW, the bus voltage v_{dc} and grid current i_a, i_b, and i_c begin to oscillate until the protection was triggered and the system shut down. This indicates that this large-signal disturbance (load power suddenly increases by five times) caused the system to lose stability, and that the conventional PI control failed.

Figure 9b shows the main operating waveforms of the VSR with proposed ADRC. The other experimental conditions are the same as PI control. When the load power suddenly increased from 2 kW to 10 kW, the bus voltage v_{dc} was quickly regulated back to the reference 650 V. In this case, the cascade system composed of VSR and CPL ran well, and the steady performance was good. The THD of grid currents was 3.5%, 3.9%, and 4% respectively. Compared with Figure 9a, the power jump range of the VSR with CPL had been effectively expanded and stability had been improved.

Figure 10 shows the main operating waveforms of the CPL when load power is changed from 2 kW to 10 kW. It can be seen that after the load power jumped, the closed-loop control of CPL makes the output voltage v_{CPL_o} quickly back to 300 V, and the oscillation is very small. The CPL output current i_{CPL_o} and output power P_{CPL} also quickly reached the target value, which satisfies the CPL characteristic. This shows that the results of Figure 9 is meaningful and sufficient.

Table 1. Circuit Parameters of the Three-phase VSR.

Symbol	Quantity	Value
E_{abc}	Grid phase voltage	220 V
f_g	Grid frequency	50 Hz
f_s	PWM frequency	16 kHz
L	Input inductance	3.2 mH
V_{dcref}	Bus voltage	650 V
R	Equivalent resistance	0.2 Ω
C	Bus capacitance	100 μF
K_{ip}	Proportional gain of the current PI regulator	5
K_{ii}	Integral gain of the current PI regulator	100
K_{vp}	Proportional gain of the voltage PI regulator	0.2
K_{vi}	Integral gain of the voltage PI regulator	80

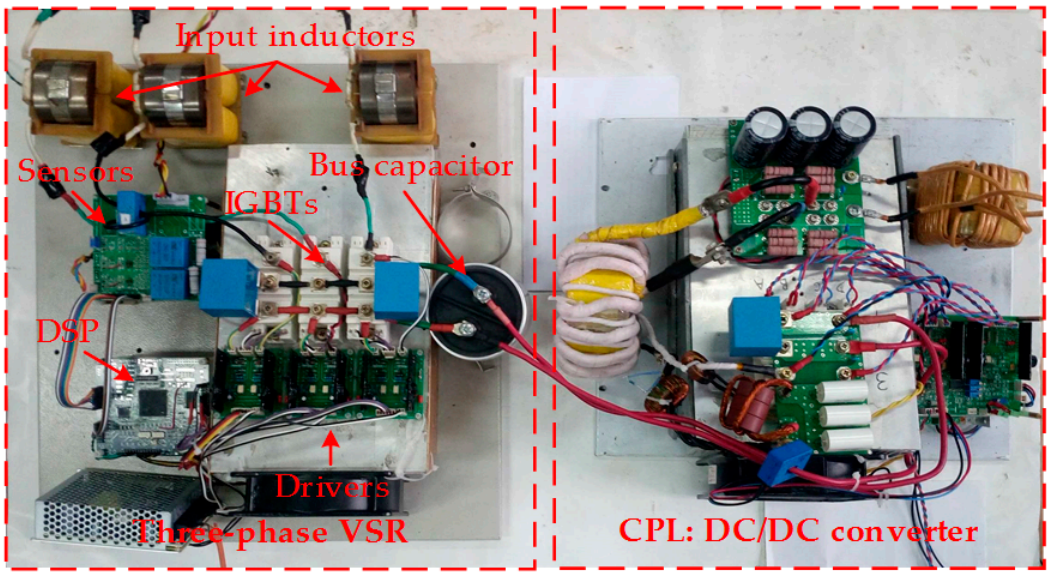

Figure 8. Prototype of the three-phase VSR with CPL.

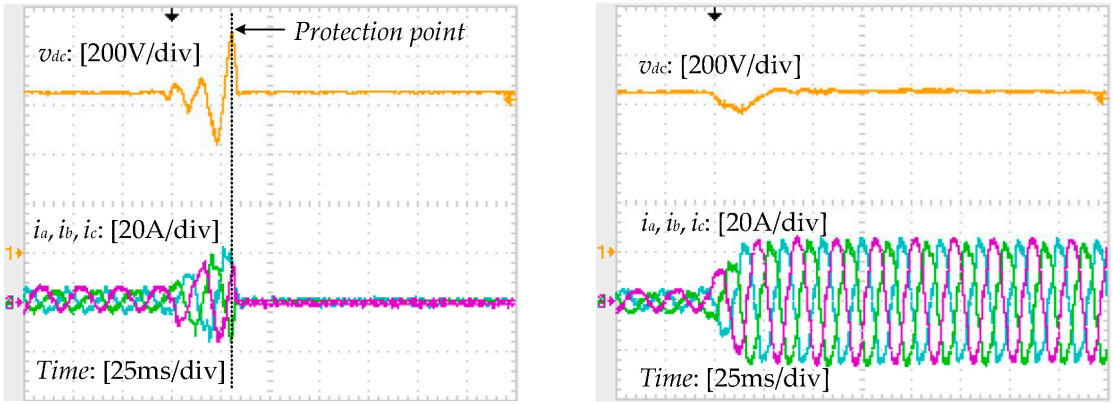

Figure 9. Main operating waveforms of the VSR when load power is changed from 2 kW to 10 kW. (**a**) with conventional PI control; (**b**) with the proposed ADRC.

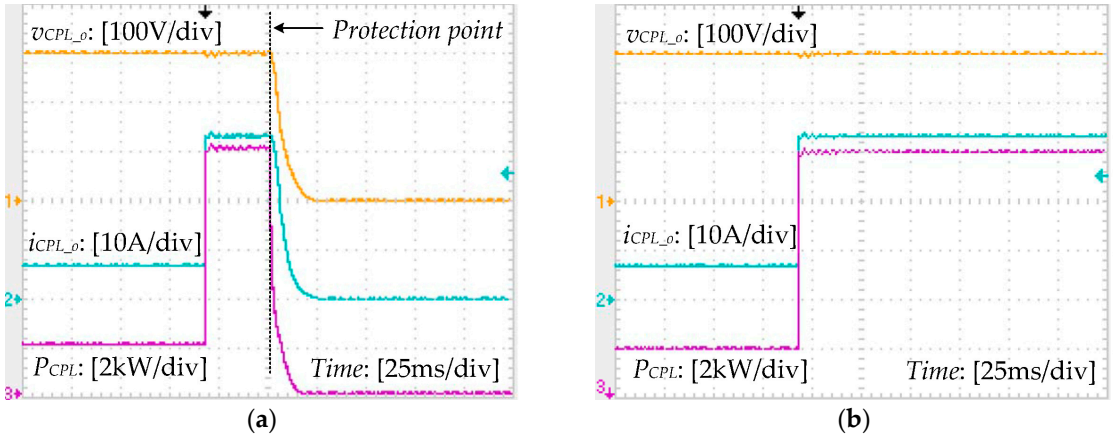

Figure 10. Main operating waveforms of the CPL when load power is changed from 2 kW to 10 kW. (**a**) with conventional PI control; (**b**) with the proposed ADRC.

5. Conclusions

In this paper, the problem that three-phase VSRs with CPL are unstable under large-signal disturbance is discussed first. Then, based on the mixed potential theory, the stability boundary of VSR with CPL when load power jumps (a typical large-signal disturbance) is analyzed. In order to improve the large-signal stability of the system, a voltage loop control scheme based on ADRC is proposed. It was shown that the scheme expands the power jump range of the VSR effectively, and improves the disturbance rejection performance, so that it is more suitable for applications with heavy load frequently switching. Finally, the validity of the control scheme is demonstrated by experiments.

Author Contributions: B.L. analyzed the method, designed the experiments and wrote the paper. H.B. proposed the main idea. X.Z. was responsible for the theoretical derivation.

Funding: This study was supported by the National Natural Science Foundation of China (NSFC) (grants 51377036).

Acknowledgments: The authors would like to thank Yuxuan Zhu for her support and suggestions.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix Mixed Potential Theory Stability Theorem 3

Define $\boldsymbol{i} = \begin{bmatrix} i_{L1} \\ i_{L2} \end{bmatrix}^T$, $\boldsymbol{v} = \begin{bmatrix} v_{C1} \\ v_{C2} \end{bmatrix}^T$, $\boldsymbol{A_{ii}}(i) = \frac{\partial^2 \boldsymbol{A}(i)}{\partial i^2}$, $\boldsymbol{B_{vv}}(v) = \frac{\partial^2 \boldsymbol{B}(v)}{\partial v^2}$, $\boldsymbol{P_v} = \frac{\partial P(i,v)}{\partial v}$, $\boldsymbol{P_i} = \frac{\partial P(i,v)}{\partial i}$, $\boldsymbol{L} = \begin{bmatrix} L_1 & 0 \\ 0 & L_2 \end{bmatrix}$ and $\boldsymbol{C} = \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix}$. Define μ_1 is the minimum eigenvalue of matrix $\boldsymbol{L}^{-1/2}\boldsymbol{A_{ii}}(i)\boldsymbol{L}^{-1/2}$, μ_2 is the minimum eigenvalue of matrix $\boldsymbol{C}^{-1/2}\boldsymbol{B_{vv}}(v)\boldsymbol{C}^{-1/2}$. If all the i and v in the circuits meet

$$\mu_1 + \mu_2 > 0 \tag{A1}$$

and when $|v| + |i| \to \infty$, there is

$$P(i,v) = \frac{\mu_1 - \mu_2}{2} P(i,v) + \frac{1}{2} P_i^T \left(L^{-1} P_i \right) + \frac{1}{2} P_v^T \left(C^{-1} P_v \right) \to \infty \tag{A2}$$

Then when $t \to \infty$, all variables of the circuit will approach the operating point, that is, no matter how the voltage and current change, the system will eventually become stable.

References

1. Ramirez-Hernandez, J.; Araujo-Vargas, I.; Rivera, M.; Ramirez-Hernandez, J.; Araujo-Vargas, I.; Rivera, M. A Modular AC-DC Power Converter with Zero Voltage Transition for Electric Vehicles. *Energies* **2017**, *10*, 1386. [CrossRef]
2. Nami, A.; Liang, J.; Dijkhuizen, F.; Demetriades, G.D. Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities. *IEEE Trans. Power Electron.* **2015**, *30*, 18–36. [CrossRef]
3. Mehrasa, M.; Pouresmaeil, E.; Zabihi, S.; Vechiu, I.; Catalao, J.P.S. A multi-loop control technique for the stable operation of modular multilevel converters in HVDC transmission systems. *Int. J. Electr. Power Energy Syst.* **2018**, *96*, 194–207. [CrossRef]
4. Zhang, X.; Zhong, Q.C.; Ming, W.L. Stabilization of a Cascaded DC Converter System via Adding a Virtual Adaptive Parallel Impedance to the Input of the Load Converter. *IEEE Trans. Power Electron.* **2015**, *31*, 1826–1832. [CrossRef]
5. Du, W.; Zhang, J.; Zhang, Y.; Qian, Z. Stability Criterion for Cascaded System with Constant Power Load. *IEEE Trans. Power Electr.* **2013**, *28*, 1843–1851. [CrossRef]
6. Mishima, T.; Akamatsu, K.; Nakaoka, M. A High Frequency-Link Secondary-Side Phase-Shifted Full-Range Soft-Switching PWM DC–DC Converter with ZCS Active Rectifier for EV Battery Chargers. *IEEE Trans. Power Electr.* **2013**, *28*, 5758–5773. [CrossRef]

7. Shin, S.C.; Lee, H.J.; Kim, Y.H.; Lee, J.H.; Won, C.Y. Transient Response Improvement at Startup of a Three-Phase AC/DC Converter for a DC Distribution System in Commercial Facilities. *IEEE Trans. Power Electron.* **2014**, *29*, 6742–6753. [CrossRef]
8. Cao, W.; Mecrow, B.C.; Atkinson, G.J.; Bennett, J.W.; Atkinson, D.J. Overview of Electric Motor Technologies Used for More Electric Aircraft (MEA). *IEEE Trans. Ind. Electron.* **2012**, *59*, 3523–3531. [CrossRef]
9. Verma, A.K.; Jain, C.; Singh, B.; Shahani, D.T. Adaptive noise cancellation based harmonic elimination in grid integrated photovoltaic system. *IET Renew. Power Gener.* **2016**, *10*, 1096–1104. [CrossRef]
10. Huang, M.; Peng, Y.; Chi, K.T.; Liu, Y.; Sun, J.; Zha, X. Bifurcation and large-signal stability analysis of three-phase voltage source converter under grid voltage dips. *IEEE Trans. Power Electron.* **2017**, *32*, 8868–8879. [CrossRef]
11. Mehrasa, M.; Pouresmaeil, E.; Zabihi, S.; Catalao, J.P.S. Dynamic model, control and stability analysis of MMC in HVDC transmission systems. *IEEE Trans. Power Deliv.* **2016**, *32*, 1471–1482. [CrossRef]
12. Mehrasa, M.; Pouresmaeil, E.; Zabihi, S.; Rodrigues, E.M.G.; Catalão, J.P.S. A control strategy for the stable operation of shunt active power filters in power grids. *Energy* **2016**, *96*, 325–334. [CrossRef]
13. Pouresmaeil, E.; Shaker, H.R.; Mehrasa, M.; Shokridehaki, M.A.; Rodrigues, E.M.G. Stability analysis for operation of DG units in smart grids. In Proceedings of the IEEE International Conference on Power Engineering, Energy and Electrical Drives, Riga, Latvia, 11–13 May 2015; pp. 447–452.
14. Pouresmaeil, E.; Bo, N.; Mehrasa, M.; Erdinc, O.; Catalao, J.P.S. A control algorithm for the stable operation of interfaced converters in microgrid systems. In Proceedings of the Innovative Smart Grid Technologies Conference Europe, Istanbul, Turkey, 12–15 October 2014; pp. 1–6.
15. Rahimi, A.M.; Emadi, A. Active Damping in DC/DC Power Electronic Converters: A Novel Method to Overcome the Problems of Constant Power Loads. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1428–1439. [CrossRef]
16. Liu, X.; Zhou, Y.; Zhang, W.; Ma, S. Stability Criteria for Constant Power Loads with Multistage LC Filters. *IEEE Trans. Veh. Technol.* **2011**, *60*, 2042–2049. [CrossRef]
17. Zhang, M.; Li, Y.; Liu, F.; Luo, L.; Cao, Y.; Shahidehpour, M. Voltage Stability Analysis and Sliding Mode Control Method for Rectifier in DC Systems with Constant Power Loads. *IEEE J. Emerg. Sel. Top. Power Electr.* **2017**, *5*, 1621–1630. [CrossRef]
18. Mitchell, D.M. Damped EMI Filters for Switching Regulators. *IEEE Trans. Electromagn. Compat.* **1978**, *EMC-20*, 457–463. [CrossRef]
19. Cespedes, M.; Xing, L.; Sun, J. Constant-Power Load System Stabilization by Passive Damping. *IEEE Trans. Power Electr.* **2011**, *26*, 1832–1836. [CrossRef]
20. Liu, B.; Ben, H.; Zhang, X.; Meng, T.; Wang, X. Stabilization of a cascaded AC/DC system based on small signal analysis, in Book Stabilization of a cascaded AC/DC system based on small signal analysis. In Proceedings of the International Conference on Electrical Machines and Systems, Sydney, Australia, 11–14 August 2017; pp. 1–6.
21. Hatua, K.; Jain, A.K.; Banerjee, D.; Ranganathan, V.T. Active Damping of Output LC Filter Resonance for Vector-Controlled VSI-Fed AC Motor Drives. *IEEE Trans. Ind. Electron.* **2012**, *59*, 334–342. [CrossRef]
22. Dannehl, J.; Liserre, M.; Fuchs, F.W. Filter-Based Active Damping of Voltage Source Converters with LCL Filter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 3623–3633. [CrossRef]
23. Liu, S.; Zhou, L.; Lu, W. Simple analytical approach to predict large-signal stability region of a closed-loop boost DC–DC converter. *IET Power Electron.* **2013**, *6*, 488–494. [CrossRef]
24. Weaver, W.W.; Iii, R.D.R.; Wilson, D.G.; Matthews, R.C. Metastability of Pulse Power Loads Using the Hamiltonian Surface Shaping Method. *IEEE Trans. Energy Convers.* **2017**, *32*, 820–828. [CrossRef]
25. Zhang, X.N.; Vilathgamuwa, D.M.; Foo, G.; Tseng, K.J.; Kandasamy, K.; Gupta, A.K.; Chandana, G. Cascaded sliding mode control for global stability of three phase AC/DC PWM rectifier with rapidly varying power electronic loads. In Proceedings of the 39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–14 November 2013; pp. 4580–4587.
26. Magne, P.; Nahid-Mobarakeh, B.; Pierfederici, S. Dynamic Consideration of DC Microgrids with Constant Power Loads and Active Damping System—A Design Method for Fault-Tolerant Stabilizing System. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *2*, 562–570. [CrossRef]
27. Zhang, W.; Hou, Y.; Liu, X.; Zhou, Y. Switched Control of Three-Phase Voltage Source PWM Rectifier Under a Wide-Range Rapidly Varying Active Load. *IEEE Trans. Power Electr.* **2012**, *27*, 881–890. [CrossRef]

28. Zhang, P.H.; Yang, G.J.; Tie-Cai, L.I. Direct Voltage Control of Three-phase PWM Rectifier Based on Feedback Linearization. *Proc. CSEE* **2010**, *30*, 39–46. [CrossRef]
29. Han, J. From PID to Active Disturbance Rejection Control. *IEEE Trans. Ind. Electron.* **2009**, *56*, 900–906. [CrossRef]
30. Tian, J.; Zhang, S.; Zhang, Y.; Li, T. Active disturbance rejection control based robust output feedback autopilot design for airbreathing hypersonic vehicles. *ISA Trans.* **2018**, *74*, 45–59. [CrossRef] [PubMed]
31. Xiao, Y.; Hong, Y.; Chen, X.; Huo, W. Switching control of wind turbine sub-controllers based on an active disturbance rejection technique. *Energies* **2016**, *9*, 793. [CrossRef]
32. Brayton, R.K.; Moser, J.K. A theory of nonlinear networks. I. *Q. Appl. Math.* **1964**, *2*, 1–33. [CrossRef]
33. Jeltsema, D.; Scherpen, J.M.A. On Brayton and Moser's missing stability theorem. *IEEE Trans. Circuits Syst. II Express Briefs* **2005**, *52*, 550–552. [CrossRef]