energies

MDPI

Article

Design of Current Programmed Switching Converters Using Sliding-Mode Control Theory

Javier Calvente, Abdelali El Aroudi *, Roberto Giral, Angel Cid-Pastor, Enric Vidal-Idiarte and Luis Martínez-Salamero

Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, 43007 Tarragona, Spain; javier.calvente@urv.cat (J.C.); roberto.giral@urv.cat (R.G.); angel.cid@urv.cat (A.C.-P.); enric.vidal@urv.cat (E.V.-I.); luis.martinez@urv.cat (L.M.-S.)
* Correspondence: abdelali.elaroudi@urv.cat; Tel.: +34-977-558-522

Received: 19 June 2018; Accepted: 24 July 2018; Published: 6 August 2018

Abstract: This paper presents a comprehensive approach to analyze and design the voltage and current loops of switching DC-DC converters by using sliding-mode control theory. The approach is interchangeably applied to switching converters under current-programmed control with both fixed and variable frequency modulation. An ideal sliding-mode dynamics model is then obtained together with its circuit schematic representation that can be used for designing the output voltage compensator, as well as to predict the large signal behavior such as during start-up and under large disturbances. Simulations and experimental measurements illustrate the theoretical approach for two different examples of switching converters.

Keywords: switching converters; sliding-mode control; current-mode control; hysteresis control

1. Introduction

Switched mode power converters are widely used for power processing in different applications such as in portable devices, solid-state lighting drivers and technologies for renewable energy production. With the aim of either regulating an output variable to a desired reference or balancing the values of different variables, a control strategy is needed [1–3].

One of the key factors affecting the response of these systems is the control mode used. Conventional Voltage Mode Control (VMC) is a simple single feedback loop with only the output voltage as a control variable. However, its first generation version features poor response against load changes [2]. Current Mode Control (CMC), also known in the literature as current-programmed control [4], utilizes the inductor current as an additional control variable, which improves the transient response [2] at the expense of extra cost and more complex controller design. CMC of power converters is nowadays an extensive design practice due to its intrinsic advantages and the existence of an important number of dedicated commercial chips that facilitate its implementation. CMC offers superior performances over conventional VMC in both parallel operation of power converters [5] and voltage regulation of non-minimum phase switching conversion structures [6]. In the first case, current sharing among the different converters of the parallel ensemble is a relatively simple task for both static and dynamic sharing [5], while in the second case, CMC is the best solution for an indirect output voltage regulation [7].

A usual way of controlling switching converters consist of imposing the duration during which a switch is maintained closed or open. In CMC, the control strategy must impose switching instants for the switches by comparing the inductor current with a desired reference. Under fixed switching frequency operation, there are three main types of CMC strategies, namely peak CMC, valley CMC and average CMC. The peak and valley cases are dual, i.e., the internal control loop forces respectively

the maximum and the minimum value of the current to track the reference given by the voltage control loop. Average control, in turn, uses the current average value in a switching cycle to track the reference supplied by the outer loop. Although most commercial ICs of CMC are based on the peak-current control principle due to its simplicity of implementation, the existence of sub-harmonic oscillations for duty cycles bigger than 50% makes necessary the use of a compensating ramp, which constitutes the main drawback of this technique.

From the seminal paper of Deisch [8] until now, more than three decades have elapsed during which a great number of researchers have contributed to building a solid representation of the dynamic behavior of the internal loop by means of either continuous or discrete-time models, or a combination of both. Dozens of papers were reported on this topic during the 1980s, the most representative being [4,9]. Some important contributions to this topic were published in the early 1990s [10–12] until the subject reached enough maturity to be treated as a chapter in some recent text books [2].

In the last decade, a renewed interest has emerged in variable frequency CMC strategies such as constant ON-time CMC [13], which, at the expense of a variable switching frequency operation, offers high efficiency under light load operation and precludes the existence of sub-harmonic oscillations in most cases. A detailed analysis of the dynamic behavior of this control technique can be found in [14], where the main difference with respect to peak CMC is investigated in the buck converter by means of an equivalent circuit consisting of the output load and the LC output filter, which is supplied by two current sources with a resistor and a capacitor in parallel.

Variable switching frequency would also result from the insertion of a hysteretic comparator instead of the Pulse Width Modulator (PWM) with constant switching frequency in the case of current programming, or instead of the PWM with constant ON-time duration in the case of constant ON-time CMC.

The voltage regulation of DC-DC switching converters using hysteretic control, also called free running or bang-bang controlled converters, goes back in time to the early years of modern power electronics when conditions for stable limit cycles in a buck switching regulator were first established [15,16].

Recently, hysteretic controllers were used in Voltage Regulator Module (VRM) applications that require current control with fast response [17–19], and some commercial chips are already available [20].

Traditionally, hysteresis-based control systems have been analyzed by means of frequency domain techniques like the descriptive function or Tsypkin's method [21–23].

On the other hand, Sliding-Mode Control (SMC) theory is a time-domain analytical technique that predicts with high precision the dynamic behavior of a Variable Structure System (VSS) [24,25]. Power converters can be classified as VSSs, and SMC is the natural way to regulate their outputs and deal with their dynamical behavior because the generation of chattering, which is intrinsic to the use of SMC, is also inherent to the nature of power converters operation. In other words, the sliding chattering becomes converter ripple, which is a physical manifestation of the way a converter absorbs energy from the input source, storing it usually in an inductor and then transferring it to an output load.

There are two main results in the SMC theory applicable to switching converters. The first one is the fact that for single input systems, a suitable Lyapunov function $V(x) = \frac{1}{2}\sigma^2(x)$ exists, where $\sigma(x)$ is the switching function. If the switching feedback gains are chosen so that $\dot{V} = \sigma\dot{\sigma} < 0$ in the domain of attraction, then the state trajectory converges to the surface $\sigma = 0$ and is restricted to it for all subsequent time. The second one provides the ideal sliding-mode dynamics on the switching surface. In this case, Filippov's method [26] and the equivalent control approach yield identical sliding equations when applied to systems that are linear with respect to the control input [27].

These techniques have been used in [28] considering feedback switching conditions of the form $\sigma = x_j - K = 0$, expressed in terms of a suitable state variable x_j that is desired to be regulated at a suitable level K. They have been employed in output voltage regulation of DC-DC switching converters in early works such as in [29–33] and also in some recent contributions to this field such

as [34–38]. In [39], SMC theory has been applied to control paralleled inverters of the buck type and in [40,41]. In [42,43], it has been used in the analysis of interleaved boost converters with hysteretic control in a ring configuration. In [44], sliding mode control theory was used to synthesize canonical elements for power processing such as in impedance matching in PV systems and in power factor correction. These techniques were also combined with other robust control methods such as fuzzy logic [45] and H_∞ [46] for designing these systems.

In the field of switching converters, two different kinds of studies using SMC theory exist in the literature. The one that uses this theory to design the switching decision and to analyze the ideal sliding dynamics and that ultimately uses a hysteretic loop to limit the switching frequency [7]. Other works use this theory to derive the equivalent control, and this is used finally to implement a PWM control [32,33]. Actually, with this strategy, all the advantages of SMC are not maintained. Small-signal analysis of sliding mode-controlled switching converters, based on hysteresis modulation, were reported in [47], where Bode plot and root locus analysis were used to reveal the effect of the parameters on the system behavior.

In this paper, on the basis of the equivalent control method, a procedure to design the control loop of DC-DC power converters operating in CMC with both variable and fixed frequency modulation strategies is proposed. The controller employs one switching function of the form $\sigma = i_r - i_L$, where i_L is a converter current and i_r is the output of an outer compensating network that processes the output voltage error. The paper comprehensively explains the dynamics of switching converters regardless of their modulation strategies. In particular, it will be demonstrated that under sliding mode conditions, the behavior of the switching converters under all the control strategies tend to the same dynamics known as the ideal sliding mode dynamics when the switching period tends to zero. The advantages, limitations and drawbacks of each strategy in a practical implementation are also discussed. It is worth noting that in this paper, it is not pretended to control switching converters using sliding mode control that ultimately end-up in a variable frequency implementation of the modulator, but the dynamics of these systems under both constant and variable frequency modulation schemes are explained by using sliding mode control theory, while providing circuit equivalent models that can be used for designing these systems by utilizing conventional frequency-domain methods.

The rest of the paper is organized as follows. The description of the behavior of current-programmed DC-DC converters is presented in Section 2 in the light of sliding mode control theory. A small-signal model is used to design the voltage loop by means of linear techniques in the frequency domain, as well as simulation results on two practical examples of switching converters in Section 3. The examples consist of a boost converter under fixed and variable frequency operation and a buck converter with current-mode hysteretic control and high bandwidth voltage regulation. An experimental validation of the results corresponding to the buck converter is given in Section 4. The application of the approach to single-loop ripple-based voltage mode control is discussed in Section 5. Finally, the conclusions of this work are summarized in Section 6.

2. Sliding-Mode Control of Switching Converters Based on Two-Loop Current Mode Control

In CCM operation, a switching converter is described by a piecewise linear state-space model that can be written in the following form:

$$\dot{x}(t) = \begin{cases} A_1 x(t) + B_1 w(t) & u = 1 \\ A_2 x(t) + B_2 w(t) & u = 0 \end{cases} \tag{1}$$

where u is a binary signal that can take the values of zero or one. It is assumed that the switching is instantaneous. $x(t)$ is the vector of state variables, and $w(t)$ is the vector of independent sources. Equation (1) can be expressed as follows:

$$\dot{x}(t) = [A_1 x(t) + B_1 w(t)]u + [A_2 x(t) + B_2 w(t)](1 - u). \tag{2}$$

Conventionally, the output variable y is a linear combination of the state variables. However, the approach is also applicable to the case with a nonlinear switching surface as in high-order boundary control schemes [48]. Hereinafter, let the linear combination of state variables $y(t) = c^\intercal x(t)$ be the output to be controlled, where c is a suitable vector to select the output $y(t)$ from the state variables $x(t)$. The derivative of the controlled output $y(t)$ is of the form:

$$\dot{y} = (m_1(x,t) + m_2(x,t))u - m_2(x,t) \tag{3}$$

where $m_1(x,t)$ and $m_2(x,t)$ are the rising and falling slopes of the signal $y(t)$ that can be expressed as follows:

$$m_1(x,t) = \quad c^\intercal[A_1 x(t) + B_1 w(t)] \tag{4}$$
$$m_2(x,t) = \quad -c^\intercal[A_2 x(t) + B_2 w(t)]. \tag{5}$$

Our interest is in situations where y can be controlled in sliding mode, so that it follows the reference smooth function $r(t)$ (continuous and differentiable). The switching function can be expressed as follows:

$$\sigma(x,t) = r(t) - y \tag{6}$$

along with the following control law (Figure 1):

$$u = \begin{cases} 1 & \text{if} \quad \sigma > 0 \\ 0 & \text{if} \quad \sigma < 0. \end{cases} \tag{7}$$

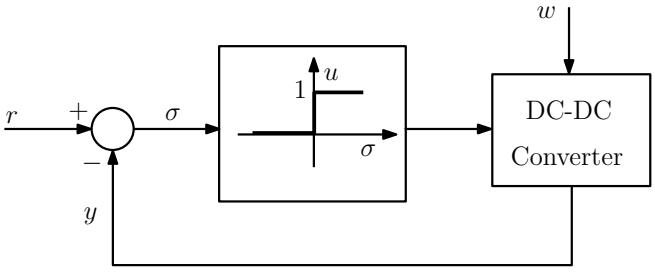

Figure 1. Simplified diagram of a DC-DC converter under Current Mode Control (CMC).

For the existence of a sliding regime on the time-variant surface Σ defined by $\{x|\sigma(x,t) = 0\}$, the sliding condition $\sigma\dot{\sigma} < 0$ must be fulfilled, which is equivalent to:

$$\dot{\sigma}_{\sigma>0} < 0 \tag{8}$$
$$\dot{\sigma}_{\sigma<0} > 0. \tag{9}$$

According to (3), the derivative $\dot{\sigma}$ of the switching function σ can be expressed as follows:

$$\dot{\sigma}(x,t) = \dot{r}(t) - ((m_1(x,t) + m_2(x,t))u - m_2(x,t)). \tag{10}$$

By using (7), the sliding conditions (8) and (9) are:

$$\dot{\sigma}_{\sigma>0} = \dot{r}(t) - m_1(x,t) < 0 \tag{11}$$
$$\dot{\sigma}_{\sigma<0} = \dot{r}(t) + m_2(x,t) > 0 \tag{12}$$

or in compact form:

$$-m_2(x,t) < \dot{r}(t) < m_1(x,t) \tag{13}$$

Equation (13) implies that the rate of change of the signal r must be lower than the absolute values of the slopes $m_1(x,t)$ and $m_2(x,t)$ of the control signal y. This is easily met if the bandwidth of the outer loop is much lower than the switching frequency, as is the case in any practical design. Therefore, under this condition, the trajectory of the system (2) with the control decision (7) will reach the sliding surface Σ in finite time and stay on it in sliding mode [27].

To maintain the trajectory in this regime, it is necessary to switch continuously at infinite frequency in the ideal case. This is not an acceptable behavior for DC-DC switching converters, which are designed to operate in a specific switching frequency range. Operating at higher frequencies, the converter efficiency decreases, and the instantaneous switching model (2) is no longer valid. This problem is solved by introducing a boundary layer around Σ and replacing the switching decision (7) by:

$$u = \begin{cases} 1 & \text{if} \quad \sigma > +\Delta \\ 0 & \text{if} \quad \sigma < -\Delta \end{cases} \tag{14}$$

where $\Delta > 0$. With this control law, the switching frequency in sliding-mode will be finite. In turn, the sliding motion will not occur strictly on the surface Σ, but in a neighborhood that meets the condition $|\sigma| \leq \Delta$. This means that a certain switching ripple will exist in the output to be controlled and other state variables as a penalty of a bounded switching frequency. This is a natural way of exchanging the energy between the reactive components of the converter.

The ideal sliding-mode dynamics is the behavior of the system (2) in the sliding regime with a control of the form (14) and in the limit case when Δ tends to zero. In order to find the ideal sliding-mode equations, the equivalent control method [27] is used. A necessary condition for the existence of an equivalent control u_{eq} and therefore to apply this method is that u appears explicitly on the right side of (10), i.e.,

$$m_1(x,t) + m_2(x,t) \neq 0. \tag{15}$$

Remark 1. *The previous condition is largely related to the fact that the relative degree of the converter u-to-σ loop is equal to one. The fast response characterizing CMC is due to this fact. The relative degree of a switched system is the number of differentiations one needs to perform on the switching function σ to make the input explicitly appear in its derivative, i.e., the minimum n that satisfies the following equation:*

$$\frac{\partial}{\partial u}\frac{\mathrm{d}^n \sigma(x,t)}{\mathrm{d}t^n} \neq 0 \tag{16}$$

Remark 2. *At high frequencies, if the relative degree is one, the system behaves as an integrator, which converts the square-wave signal u to a triangular signal σ.*

Remark 3. *It should be noted that apart from the widely-used hysteresis comparison, any other strategy to limit the switching frequency can be used without invading the sliding motion. Other possible strategies to limit the switching frequency are time delays, filtering and clocked switching.*

In all the cases, if (15) is accomplished, the equation $\dot{\sigma} = 0$ can be solved with respect to u to obtain the equivalent leading to the following expression:

$$u_{eq}(x,t) = \frac{\dot{r}(t) + m_2(x,t)}{m_1(x,t) + m_2(x,t)}. \tag{17}$$

The equivalent control caused by any modulation scheme such as the variable frequency hysteretic modulation and constant switching-frequency peak/valley control methods are the same since the equivalent control corresponds to the ideal sliding dynamics with theoretically infinite switching frequency or to the averaged dynamics of the converter under the switching constraints' imposed previous modulation strategies. The order of the averaged dynamics or the ideal sliding dynamics

is reduced due to the relationship imposed between the state variables by the switching constraint. From (17), if $m_1(x,t) + m_2(x,t) \neq 0$, the equivalent control u_{eq} will exist, and according to (13), its value will be comprised between zero and one. The ideal sliding-mode dynamics is obtained by substituting u in (2) by u_{eq} given by (17) and introducing the order reduction due to the constraint $\sigma = 0$. In DC-DC converters, the ideal sliding-mode dynamics should have an asymptotically-stable equilibrium point.

Note that u is undetermined when $|\sigma| \leq \Delta$; therefore, there is a plurality of controls compatible with (14) [49]. For example, in the hysteretic control (Figure 2a), from the moment that the condition $|\sigma| < \Delta$ is fulfilled, a switching occurs whenever $|\sigma| = \Delta$. Other examples are constant-switching-frequency controls [50], such as peak (Figure 2b) and valley (Figure 2c) current, in which time-driven switching occurs periodically, while event-driven switching occurs whenever $|\sigma| = \Delta$. DC-DC switching converters typically have a periodic behavior in steady-state with two switchings per period. In the limit as Δ tends to zero, the periodic solution tends to the equilibrium point of the ideal sliding-mode dynamics.

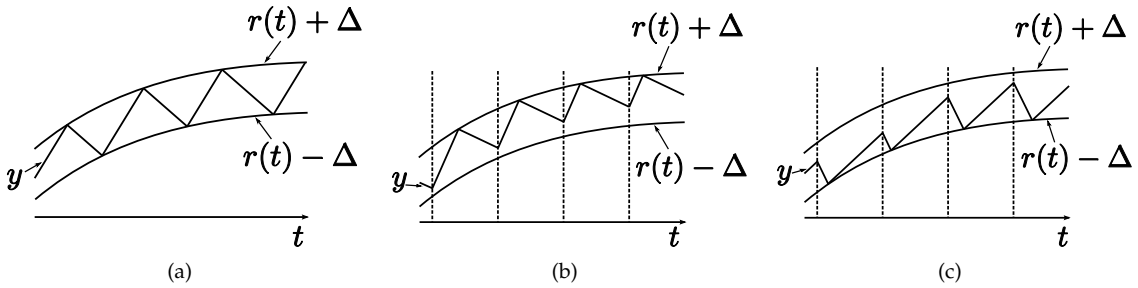

Figure 2. Evolution of the controlled output and its reference in sliding-mode for three types of control implementing (14). (**a**) Hysteresis control. (**b**) Peak control at constant switching frequency. (**c**) Valley control at constant switching frequency.

The DC-DC converter with sliding-mode current control is a system, the control input of which is the current reference $r(t)$. To regulate the output voltage of the converter, a second slower control loop that dictates $r(t)$ from the voltage error must be added. The examples considered in the next section show how to design such a controller using the ideal sliding-mode dynamics model.

3. Practical Examples

3.1. Example 1: A Boost Converter under Fixed and Variable Frequency CMC

Let us consider the boost converter depicted in Figure 3a. The state variables are the inductor current i_L and the capacitor voltage v_o. The independent sources correspond to the input voltage $v_g(t)$ and the current $i_d(t)$, which models load variations. For this example, (2) becomes as follows:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_g(t)}{L} - \frac{v_o(1-u)}{L} \tag{18}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_L(1-u)}{C} - \frac{v_o}{RC} + \frac{i_d(t)}{C}. \tag{19}$$

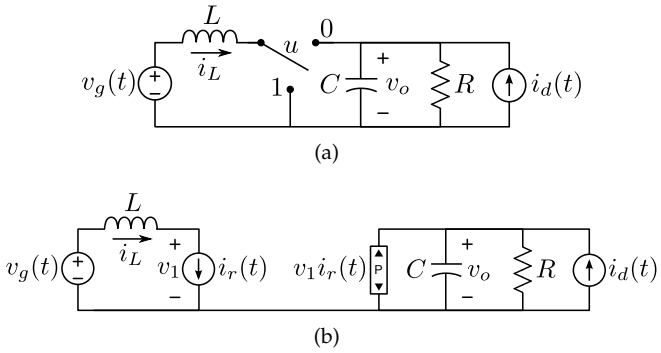

Figure 3. Schematic circuit diagram of (**a**) a Boost converter and (**b**) its ideal sliding-mode dynamics model under CMC.

Let $i_r(t)$ be the current reference. Using the switching function $\sigma = i_r(t) - i_L$ together with the control law (7), the sliding condition (13) leads to the following inequality:

$$\frac{v_g(t) - v_o}{L} < \frac{\mathrm{d}i_r(t)}{\mathrm{d}t} < \frac{v_g(t)}{L}. \tag{20}$$

When $i_r(t)$ is constant, (20) becomes $0 < v_g(t) < v_o$. In this case, starting from zero initial conditions, as soon as v_o reaches $v_g(t)$, the sliding condition is fulfilled, and after a finite time, the system trajectory is constrained in the sliding manifold defined by the constraint $i_r - i_L = 0$. When $i_r(t)$ is time varying or state-dependent, according to (17), the equivalent control for this example becomes as follows:

$$u_{eq} = \frac{L\frac{\mathrm{d}i_r(t)}{\mathrm{d}t} + v_o - v_g(t)}{v_o}. \tag{21}$$

After substituting u by u_{eq} in (18) and (19) and using $\sigma = 0$ ($i_L = i_r(t)$), the system order is reduced, and the following ideal sliding-mode dynamics is obtained:

$$i_L = i_r(t) \tag{22}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_r(t)\left[v_g(t) - L\frac{\mathrm{d}i_r(t)}{\mathrm{d}t}\right]}{Cv_o} - \frac{v_o}{RC} + \frac{i_d(t)}{C}. \tag{23}$$

Expression (23) also establishes a power balance between the input port and the output port of the boost converter provided that $i_L = i_r$. These equations can be represented by means of an equivalent circuit using a power source [51] to model the nonlinear term (Figure 3b). The ideal sliding-mode dynamics (23), with the following constant inputs:

$$i_r(t) = I_r, \;\; v_g(t) = V_g, \;\; i_d(t) = 0, \tag{24}$$

has the following equilibrium point:

$$v_o{}^* = V_r = \sqrt{I_r R V_g} \tag{25}$$

which is asymptotically stable, as can be demonstrated by means of the Lyapunov function $V(v_o) = (1/2)(v_o - V_r)^2$ [52].

Note that $v_o{}^*$ depends on both the line voltage and the supplied load resistance. That is why a regulation of the voltage v_o is needed when disturbances in $i_d(t)$ and $v_g(t)$ take place. The regulation can be accomplished by adding another external voltage loop and making the current reference i_r be the output of this loop.

Figure 4 shows a double-loop control scheme, which is proposed for output voltage regulation. The voltage controller consists of three cascaded stages. Namely, a Proportional-Integral (PI) block to process the error, a limiter to avoid the current reference overpassing an admissible level and a low-pass filter to ensure the smoothness of $i_r(t)$. The current controller is of the type (14) with $\Delta = I_\Delta$. The transfer function of the voltage controller in the linear region has the following form:

$$G_c(s) = K_p \left(1 + \frac{\omega_I}{s}\right) \frac{1}{1 + s/\omega_h}. \tag{26}$$

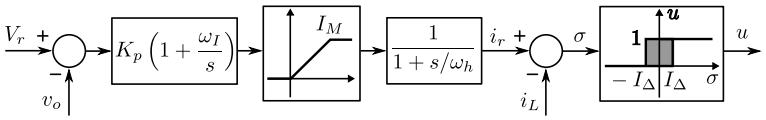

Figure 4. Control scheme with a double loop voltage regulation.

To design $G_c(s)$, a small-signal model of the ideal sliding-mode dynamics will be used. Linearizing (23) around (24) and (25) leads to the following equation for the small-signal variables represented by a "hat" (^) over the letter:

$$\frac{\mathrm{d}\hat{v}_o}{\mathrm{d}t} = -\frac{2}{CR}\hat{v}_o + \frac{V_g}{CV_r}\hat{i}_r(t) - \frac{LV_r}{CRV_g}\frac{\mathrm{d}\hat{i}_r(t)}{\mathrm{d}t} + \frac{V_r}{CRV_g}\hat{v}_g(t) + \frac{1}{C}\hat{i}_d(t). \tag{27}$$

Applying the Laplace transform to (27) yields the following model in terms of transfer functions:

$$\hat{V}_o(s) = G_{vir}(s)\hat{I}_r(s) + G_{vvg}(s)\hat{V}_g(s) + G_{vid}(s)\hat{I}_d(s) \tag{28}$$

where:

$$G_{vir}(s) = \frac{\hat{V}(s)}{\hat{I}_r(s)} = \frac{RV_g}{2V_r}\frac{1 - s/\omega_z}{1 + s/\omega_p} \tag{29}$$

$$G_{vvg}(s) = \frac{\hat{V}V(s)}{\hat{V}_g V(s)} = \frac{V_r}{2V_g}\frac{1}{1 + s/\omega_p} \tag{30}$$

$$G_{vid}(s) = \frac{\hat{V}V(s)}{\hat{I}_d V(s)} = \frac{R}{2}\frac{1}{1 + s/\omega_p} \tag{31}$$

$$\omega_z = \frac{RV_g{}^2}{LV_r{}^2};\ \omega_p = \frac{2}{RC}. \tag{32}$$

The loop gain is $T(s) = G_c(s)G_{vir}(s)$, and the closed-loop output impedance is given by $Z_o(s) = G_{vid}(s)/(1 + T(s))$. Besides, the closed-loop input to output transfer function is expressed as $G_{vvg}(s)/(1 + T(s))$. The coefficients of $G_c(s)$ are chosen to ensure that the frequency response of the total loop gain exhibits a high value of the modulus and a sufficient stability margin. The higher the value of $|T(j\omega)|$, the better will be the disturbance rejection, but for a poor relative stability, there can be a range of frequencies very sensitive to disturbances. In the boost converter, the right half-plane zero of $G_{vir}(s)$ (29) imposes an upper bound on the achievable bandwidth [53].

Let us consider an example of a boost converter with the following set of parameter values: $L = 30\,\mu\mathrm{H}$, $C = 100\,\mu\mathrm{F}$, $R = 10\,\Omega$, $V_g = 10\,\mathrm{V}$ and $V_r = 30\,\mathrm{V}$. Two cases of CMC will be considered, i.e., valley CMC at constant switching frequency (Figure 2c) with $I_\Delta = 2.5\,\mathrm{A}$ and $f_s = 50\,\mathrm{kHz}$ and hysteresis CMC (Figure 2a) with $I_\Delta = 2.22\,\mathrm{A}$, which in the steady-state exhibits the same switching frequency of 50 kHz. In Figure 5, the frequency response from the theoretical expression of $G_{vir}(j\omega)$ is compared to the simulated corresponding frequency response of the two mentioned CMC controllers. The simulated frequency response was obtained using the power electronics simulator software

PSIM©, which has a specific feature to get different types of frequency responses, basically input, output and closed loop gains. The AC sweep module manages the frequency sweep (amplitude, initial frequency, final frequency, number of points) as in a frequency response analyzer.

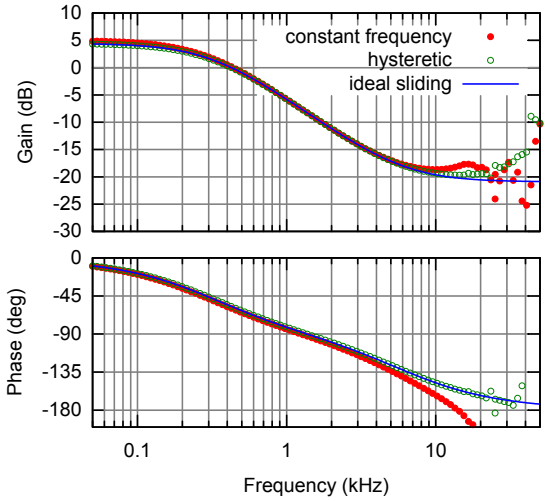

Figure 5. Theoretical and simulated frequency responses from the current reference to output voltage in a boost converter.

A good agreement among the three frequency responses can be clearly observed at low frequencies until approximately 5 kHz ($f_s/10$). The right half-plane zero is located at 6 kHz. Therefore, the control bandwidth will be placed within the region wherein the three responses almost coincide, and the design based on the ideal sliding-mode dynamics model will be valid for the other two cases.

It can be verified in a Bode diagram of $T(j\omega)$ that choosing $\omega_h = \omega_z = 37\,\text{krad/s}$, $\omega_I = 1.2\,\text{krad/s}$ and $K_p = 3.7\,\text{A/V}$, the crossover frequency at 0 dB is $f_c = 2\,\text{kHz}$, the phase margin is 57° and the gain margin is 10 dB at 6 kHz. The Bode diagrams obtained by simulation for the two cases with finite switching frequency show similar results to the ideal case, not only in the loop gain (Figure 6), but also in the output impedance (Figure 7). The closed-loop converter response to a step change in $i_d(t)$ is shown in Figure 8, where the simulated ideal sliding-mode dynamics based on the circuit of Figure 3b is compared to the two previous cases of finite switching frequency. The concordance of the three responses is in agreement with the frequency results depicted in Figure 7.

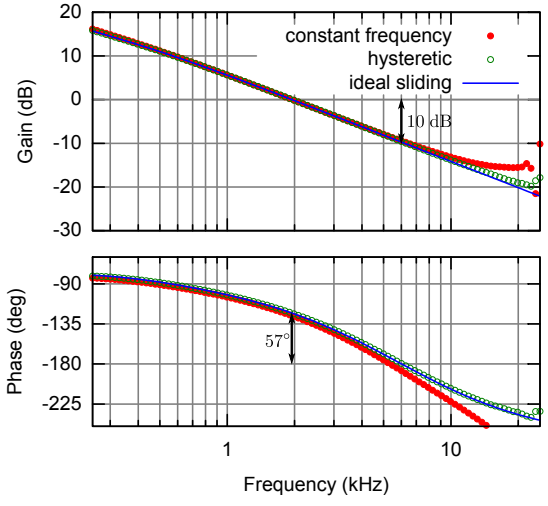

Figure 6. Theoretical and simulated loop gain Bode plots in a boost converter.

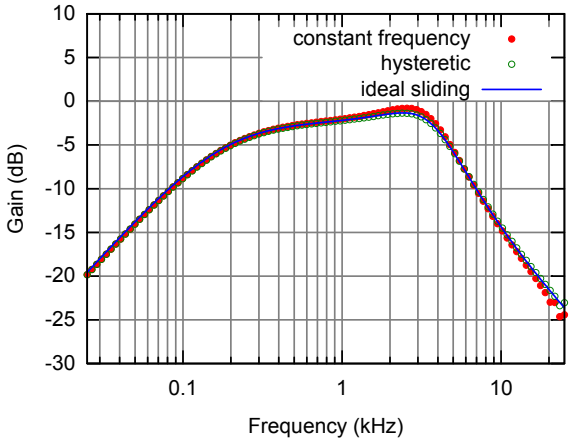

Figure 7. Theoretical and simulated closed-loop output impedance in a boost converter.

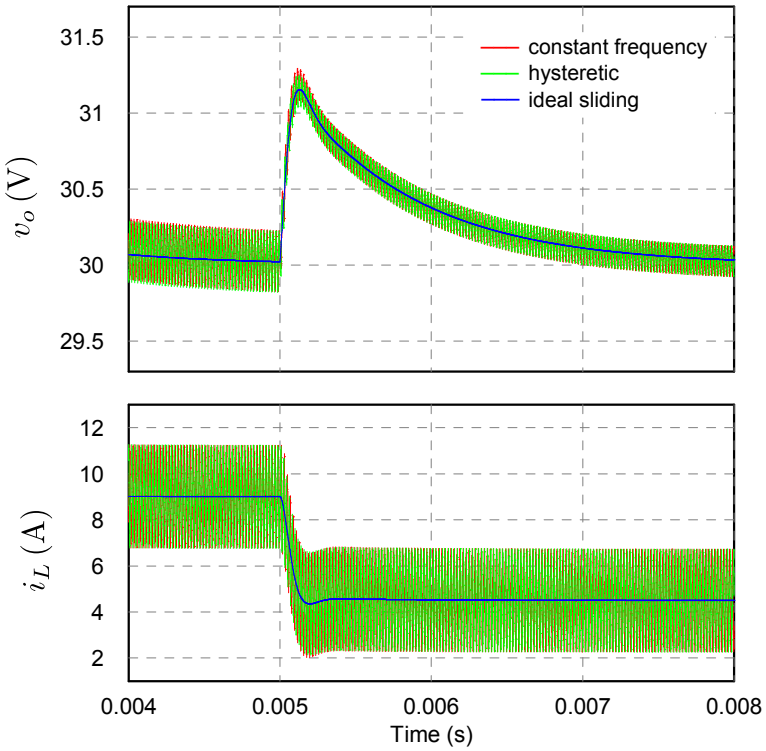

Figure 8. Response of the state variables v_o and i_L of the boost converter in closed-loop to a step change of 1.5 A in $i_d(t)$. Comparison of the ideal sliding-mode dynamics with that corresponding to two different types of control methods at finite switching frequency.

Let us analyze now the time-domain closed-loop converter response from zero initial conditions and without the presence of any disturbance. Figure 9 depicts the case of valley CMC at constant switching frequency. The case of hysteresis control is very similar. It is worth mentioning that the inductor current must be limited in the transient-state. The current control ensures that the inequality $|i_r(t) - i_L| \leq I_\Delta$ is satisfied in sliding mode. The limiter of the voltage controller guarantees that $i_r(t) < I_M$, so that, in the sliding regime, the inductor current satisfies at any instant the inequality $i_L < I_{max}$ where $I_{max} = I_M + I_\Delta$. In this example, the inductor current must reach at least the value ${V_r}^2/(RV_g) = 9$ A, which corresponds to the equilibrium point. The maximum current was fixed to $I_{max} = 15$ A, so that $I_M = 12.78$ A in the case of hysteresis CMC and $I_M = 12.5$ A in the case of valley

CMC. In both cases, the same regions in the response can be observed. Initially $v_o = 0$ V, so that the sliding condition (20) is not accomplished, and the trajectory goes away from the switching manifold defined by $\sigma = 0$ while i_L is increasing. Since the voltage error is positive, $i_r(t)$ also increases until its saturation. This ensures that in some instant, the inequality $i_L > i_r(t) + I_\Delta$ will be satisfied so that $u = 0$ and v_o will be also increasing. When v_o overpasses V_g, the sliding condition is fulfilled, the trajectory alters course and later enters in sliding mode as predicted by the theory. In this regime and with $i_r(t)$ saturated, v_o tends asymptotically towards an equilibrium point in which $v_o{}^* > V_r$. Once v_o surpasses V_r, the voltage controller enters in the linear region, and the trajectory tends towards the desired equilibrium point. An anti-windup system in the integrator can improve this start-up transient by reducing the voltage overshooting, although in this example, it has not been included. Moreover, the converter structure can be modified to avoid the initial current peak [7].

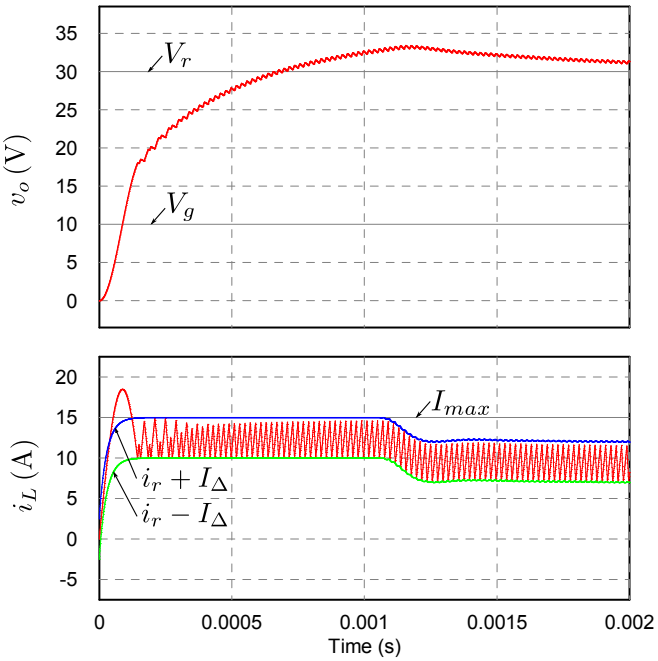

Figure 9. Boost converter response from zero initial conditions using a valley current control at constant switching frequency and voltage regulation.

3.2. Example 2: Buck Converter under Fixed and Variable Frequency CMC

Let us consider the buck converter depicted in Figure 10a, the state equations of which are:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_g(t)u - v_o}{L} \tag{33}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_L}{C} - \frac{v_o}{RC} + \frac{i_d(t)}{C} \tag{34}$$

$$i_g = i_L u \tag{35}$$

$$i_o = \frac{v_o}{R} - i_d(t). \tag{36}$$

Using the switching function $\sigma = i_r(t) - i_L$ and the control law (7), the sliding condition (13) for this converter becomes:

$$-\frac{v_o}{L} < \frac{\mathrm{d}i_r(t)}{\mathrm{d}t} < \frac{v_g(t) - v_o}{L}. \tag{37}$$

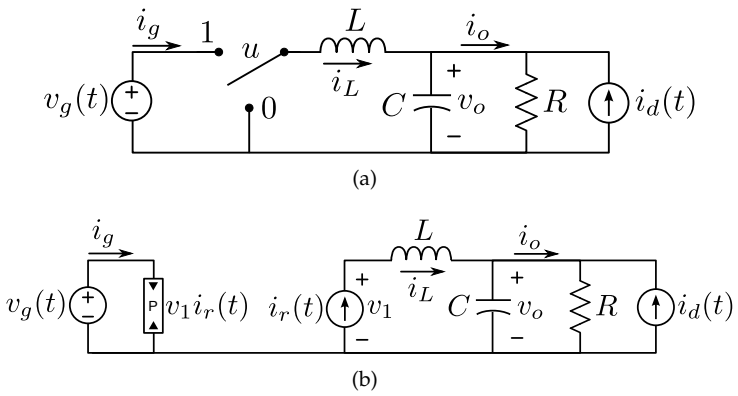

Figure 10. Schematic circuit diagram of (**a**) a Buck converter and (**b**) its ideal sliding-mode dynamics model under CMC.

Inequalities (37) are fulfilled for $i_r(t)$ constant provided that $0 < v_o < v_g(t)$, which are the normal operating conditions of a buck converter. For this converter, the sliding motion is guaranteed from the start-up even with zero initial conditions. The ideal sliding-mode dynamics, obtained by means of the equivalent control method, is the following:

$$i_L = i_r(t) \tag{38}$$

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{i_r(t)}{C} - \frac{v_o}{RC} + \frac{i_d(t)}{C} \tag{39}$$

$$i_g = \frac{i_r(t)\left[v_o + L\frac{\mathrm{d}i_r(t)}{\mathrm{d}t}\right]}{v_g(t)} \tag{40}$$

$$i_o = \frac{v_o}{R} - i_d(t) \tag{41}$$

and it can be represented by the circuit illustrated in Figure 10b. The equilibrium point for constant inputs (24), ${v_o}^* = V_r = I_r R$ is asymptotically stable. Linearizing the ideal sliding-mode dynamics around the equilibrium point yields a small-signal model, which is used to design the voltage controller or to analyze the system stability when an input filter is added.

The voltage loop consists of the current reference $\hat{I}_r(s)$ to the output voltage $\hat{V}_o(s)$ transfer function, $G_{vir}(s)$, i.e.,

$$G_{vir}(s) = \frac{R}{1 + sRC}, \tag{42}$$

and the same controller (26) employed in the previous example. In this converter, $G_{vir}(s)$ is a minimum phase transfer function. In the ideal case, the loop gain and the control bandwidth can be made boundlessly high without affecting the system stability. For instance, if a particular value of ω_c is chosen and the coefficients of $G_c(s)$ are calculated according to the following criteria:

$$\omega_c \gg 1/(RC); \;\; K_p = C\omega_c; \;\; \omega_I = \omega_c/4; \;\; \omega_h = 4\omega_c, \tag{43}$$

then ω_c will be the crossover frequency at 0 dB of the loop gain, the phase margin will be higher than 60° and the gain margin will be infinite.

However, the sliding condition (37) is a constraint that must be respected. For example, let us assume that the system is in equilibrium and that a step disturbance of amplitude I_d in current $i_d(t)$ is applied at $t = 0$. If the controller has been designed according to (43), the slope of $i_r(t)$ during the transient-state will be maximal at $t = 0.55/\omega_c$ approximately, reaching a value of:

$$\left.\frac{\mathrm{d}i_r(t)}{\mathrm{d}t}\right|_{t=0.55/\omega_c} \approx -0.8\,\omega_c I_d \tag{44}$$

and therefore, the conditions to keep the sliding mode with this disturbance are:

$$-V_r < -0.8\,\omega_c I_d L < V_g - V_r. \tag{45}$$

Hence, if the bandwidth is too large, small disturbances could provoke very fast variations of $i_r(t)$, violating (37). Moreover, in the case of finite switching frequency, the distortion of the frequency response near the switching frequency degrades the phase margin and limits in turn the control bandwidth. As was observed in Figure 5, the phase decrease is higher in the case of constant switching frequency than in the case of hysteresis, and therefore, a larger bandwidth can be achieved by means of the hysteretic control.

4. Experimental Results

A prototype of the buck converter with hysteretic CMC has been constructed for the set of parameter values $L = 3.3\,\mu\text{H}$, $C = 350\,\mu\text{F}$, $R = 1\,\Omega$, $V_g = 15\,\text{V}$ and $V_r = 5\,\text{V}$. The switching frequency has been tuned to 100 kHz in the equilibrium point. The gain of the current sensor was $R_s = 44\,\text{mV/A}$, and the coefficients of the voltage controller have been calculated according to (43) with $\omega_c = 2\pi \cdot 40\,\text{krad/s}$. A picture of the the experimental setup is shown in Figure 11, and the schematic diagram is depicted in Figure 12. While in the numerical simulations, we used the scheme depicted in Figure 4 in which the saturation block is inserted between the PI compensator and the low-pass filter, our experimental measurements were obtained from a system under the control scheme of Figure 12 in which the saturation block acted after the low-pass filter. From an implementation point of view, it is much simpler to use Figure 12 rather than Figure 4. It is clear that if no saturation takes place, both schemes are equivalent, and this is the case of all the small signal responses (time and frequency domains) presented in the paper. A small difference may arise however under large signal responses such as for instance during the transient. Moreover, it is worth noting that this saturation block was added to limit the current reference during start-up, and this can be accomplished by the scheme of Figure 4, as well as by the one shown at the bottom of Figure 12.

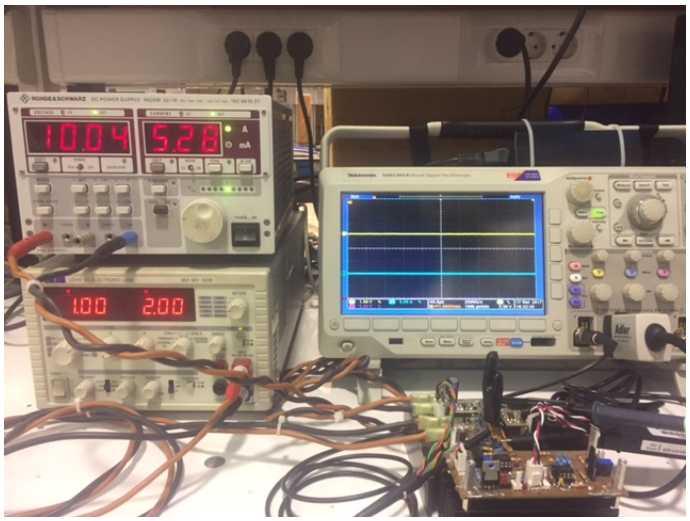

Figure 11. The experimental setup used to validate the theoretical and the simulation results corresponding to the buck converter under two-loop hysteretic CMC.

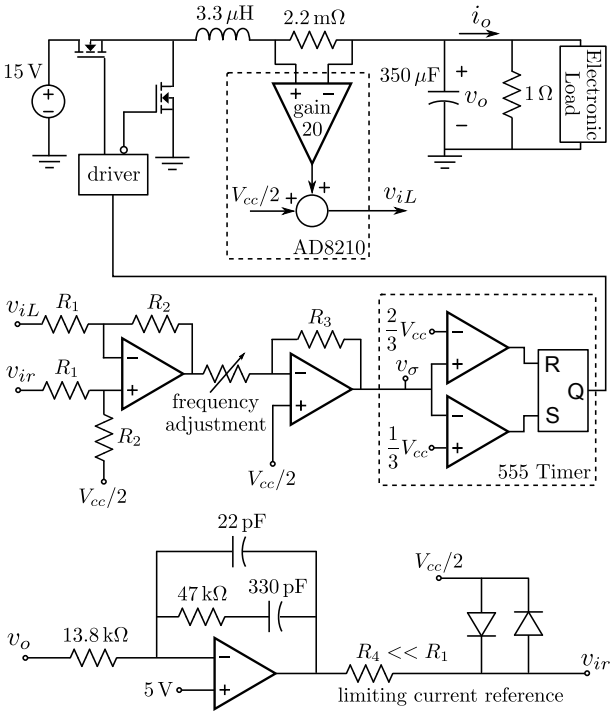

Figure 12. Schematic circuit diagram of the buck converter with hysteretic CMC and output voltage regulation.

The frequency response of the system being the input $\hat{v}_{ir}$ and the output $\hat{v}_o$, in the case of an open voltage loop, has been obtained experimentally, and it is depicted in Figure 13 with the Bode diagram of $G_{vir}(s)/R_s$. The experimental frequency response in Figure 13 was obtained by using the Venable 3120 FRA. In this particular case, the analog control circuit is the one in Figure 12; with the voltage loop opened, the FRA provides the voltage reference v_{ir}, which is composed of a sinusoidal variable frequency reference and a DC component to polarize the system around the desired steady-state operating point. Closed loop gains in Figure 14 were obtained in closed loop using also the Venable 3120 FRA; in this case, a wideband medium frequency injection transformer model Bode Box 200-002 and two probes to obtain differential measurements are connected to the R4-100 Ω resistor.

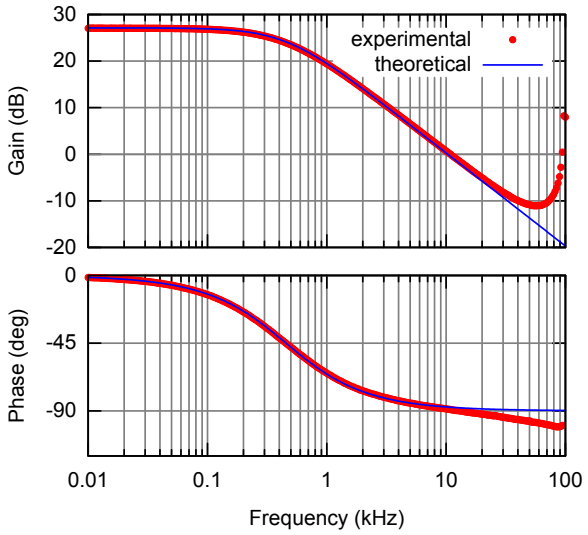

Figure 13. Theoretical and experimental frequency responses from current reference $\hat{v}_{ir}$ to output voltage $\hat{v}_o$ in the buck converter of Figure 12.

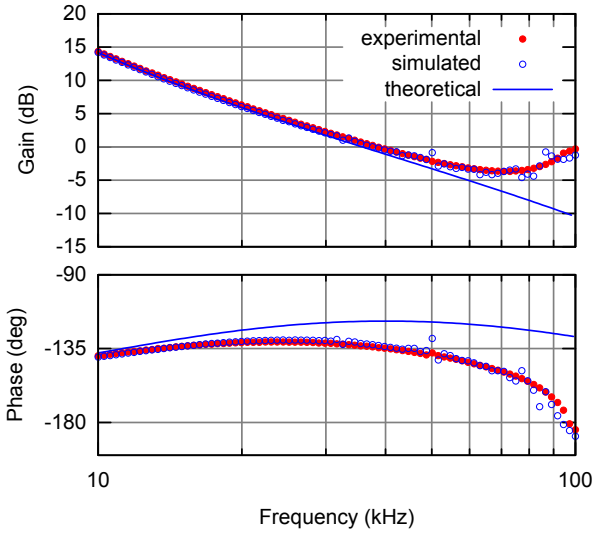

Figure 14. Theoretical, simulated and experimental Bode diagrams of the voltage loop gain in the buck converter.

It can be observed that the model based on the ideal sliding-mode dynamics is valid up to almost one half of the switching frequency. The loop gain has been also measured, and it is shown in Figure 14 with the Bode diagram of $G_c(s)G_{vir}(s)/R_s$ and with the frequency response obtained by numerical simulation of the switched model. It can be observed that the experimental closed-loop bandwidth (ω_c) hardly deviated from the theoretical one, but the phase margin was reduced from 60°–45° due to non-ideal high frequency effects. To match the simulation with the experimental results at high frequency, it was necessary to include in the simulation a dynamic model of the current sensor (a low-pass second-order filter with a cutoff frequency of 450 kHz and a damping ratio of 0.7) and pure delays for both control logic circuits and switching elements (300 ns in total). Figures 15 and 16 show respectively the experimental and simulated response of the converter to a load variation of step type that satisfies the condition (45) by including these non-ideal effects. Note that signal v_σ representing the switching function is not totally within the hysteresis band due to propagation delays and to the dynamics of the current sensor.

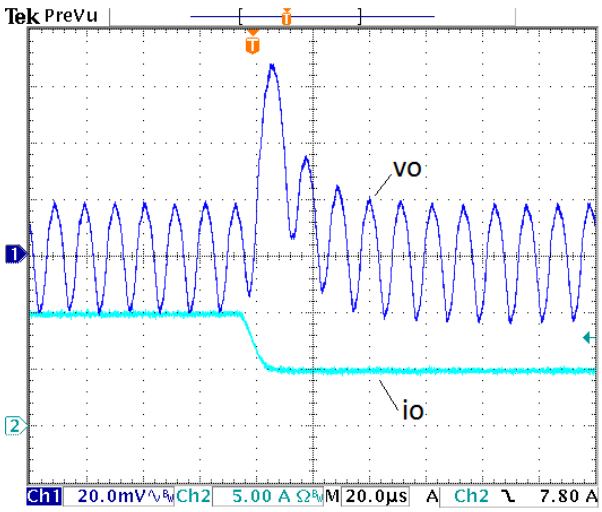

Figure 15. Experimental output voltage response to a load current step in the buck converter from 10 A–5 A.

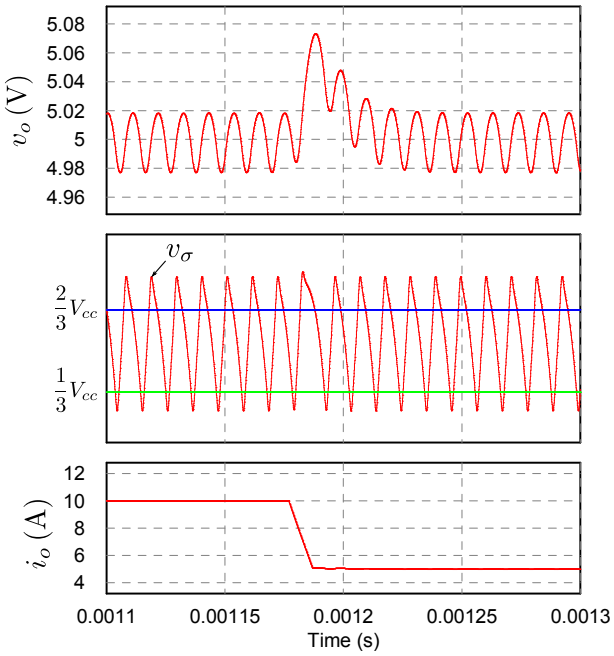

Figure 16. Simulated response to a load current step in the buck converter from 10 A–5 A corresponding to Figure 15.

Remark 4. *The analysis of the same converter with fixed frequency V^2 control and enhanced V^2I_L control [54–56], the V^2I_C [57] and the V^1 control concept [58] can be done following the same procedures with a little effort.*

5. Discussion: Extension to Single-Loop Ripple-Based VMC Strategies

Although the CMC of power converters is nowadays an extensive design practice due to its intrinsic advantages and the existence of an important number of dedicated commercial chips that facilitate its implementation, different ripple-based VMC schemes, that use the parasitic output voltage ripple instead of the inductor current as an additional feedback signal have been also proposed to improve the load transient response of switching converters. For instance, conventional hysteretic voltage mode controllers use the output voltage ripple as the control signal, and a hysteretic comparator is used to generate the square wave for the switch drivers. This is the case of hysteretic voltage regulator modules [59], the V^2 and the enhanced V^2I_L control strategies [54–56] and also the case of the V^2I_C [57] and its equivalent scheme known as the V^1 control concept [58]. Except the V^2I_L control scheme, in all these control strategies, the inductor current is used indirectly in the feedback, and the system works as desired only with a non-ideal output capacitor characterized by a high Equivalent Series Resistance (ESR). Although it is conventionally claimed that hysteretic controllers show faster response than traditional fixed frequency PWM controllers, this happens only with relatively large ESR, and similar responses can be obtained with both modulations if a similar ESR is used. In fact, this ESR introduces indirectly inductor current feedback, and this is the main reason for making the response faster. The enhanced V^2I_L ripple-based control [56] and the I^2 control [60] directly introduce this current feedback. Other approaches for introducing current feedback indirectly in the controller are the so-called raster control surfaces in [61], the use of the capacitor current as in [62] and the introduction of the derivative term of the error signal as in [63].

Although the interest for hysteretic controllers seems a recent practice, due to its immediate application in Voltage Regulation Modules (VRMs) [17,19] and the existence of some commercial chips [20], its use in the voltage regulation of DC-DC switching converters goes back in time to the early years of modern power electronics when conditions for stable limit cycles in a buck switching

regulator were first established [15,16]. Other control schemes that can be placed into the same category are boundary control [48,64] and synergetic control [65] strategies.

All the previous strategies can be implemented either with the variable frequency modulation strategy or a fixed frequency modulation scheme. Variable frequency would result from the use of a hysteretic comparator. It would be also the case for constant ON-time and constant OFF-time strategies. Fixed frequency operation will result from peak CMC (or VMC), valley CMC (or VMC) and average CMC (or VMC) using a latch and a clock signal in the modulator. The same theory can be applied interchangeably to all the previous strategies.

6. Conclusions

A two-loop control design technique for DC-DC switching converters has been presented. The double loop consists of an inner current loop in sliding-mode and an outer voltage regulation loop that includes a limiter of the current reference.

When the sliding condition is accomplished, the converter enters in sliding mode after a finite time, and the current tracks its reference. The ideal sliding-mode dynamics describes the system behavior, and a small-signal model around the equilibrium point is used to design the voltage regulation loop by means of the frequency response method.

It has to be pointed out that sliding-mode control theory does not specify the nature of the switching law when $|\sigma| < \Delta$. Hence, hysteresis control and constant switching frequency control have been compared for a boost converter. The frequency response in both cases almost coincides with the theoretical prediction of the ideal sliding-mode dynamics at low frequencies, the hysteresis control response being much more similar to the ideal case near the switching frequency region. However, in the example reported here for the boost converter, the most limiting factor in the regulation bandwidth is the right half-plane zero, and for that reason, the closed-loop response in both cases is very similar to the ideal one.

In the example of the buck converter, an expression of the sliding condition in terms of both voltage regulation bandwidth and load disturbance amplitude has been derived. A bandwidth of the voltage loop near one half the switching frequency has been obtained using a hysteretic current mode controller. In the same example, it has been found that the actual dynamic behavior of the current sensor and the delay of both switching and control logic circuits can have an appreciable influence upon the phase margin of the voltage loop.

Author Contributions: Conceptualization, J.C., A.E.A. and L.M.-S; All the authors contributed equally to the other parts of the work.

Funding: This work has been sponsored by the Spanish Agencia Estatal de Investigación (AEI) and the Fondo Europeo de Desarrollo Regional (FEDER) under Grants DPI2017-84572-C2-1-R and DPI2016-80491-R (AEI/FEDER, UE).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. El Fadil, H.; Giri, F. Robust nonlinear adaptive control of multiphase synchronous buck power converters. *Control Eng. Pract.* **2009**, *17*, 1245–1254. [CrossRef]
2. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*; Kluwer: Alphen aan den Rijn, The Netherlands, 2001.
3. Yfoulis, C.; Giaouris, D.; Stergiopoulos, F.; Ziogou, C.; Voutetakis, S.; Papadopoulou, S. Robust constrained stabilization of boost DC-DC converters through bifurcation analysis. *Control Eng. Pract.* **2015**, *35*, 67–82. [CrossRef]
4. Middlebrook, R. Topics in multiple-loop regulators and current-mode programming. *IEEE Trans. Power Electron.* **1987**, *PE-2*, 109–124. [CrossRef]
5. Ramos, R.; Biel, D.; Fossas, E.; Gri, R. Sliding mode controlled multiphase buck converter with interleaving and current equalization. *Control Eng. Pract.* **2013**, *21*, 737–746. [CrossRef]

6. Liu, Y.-F.; Sen, P.C. Large-signal modeling of hysteretic current-programmed converters. *IEEE Trans. Power Electron.* **1996**, *11*, 423–430.
7. Martinez-Salamero, L.; Garcia, G.; Orellana, M.; Lahore, C.; Estibals, B. Start-up control and voltage regulation in a boost converter under sliding-mode operation. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4637–4646. [CrossRef]
8. Deisch, C.W. Simple switching control method changes power converter into a current source. In Proceedings of the PESC'78, Power Electronics Specialists Conference, Syracuse, NY, USA, 13–15 June 1978; pp. 300–306.
9. Redl, R.; Sokal, N. Current-mode control, five different types, used with the three basic classes of power converters-small-signal ac and large-signal dc characterization, stability requirements, and implementation of practical circuits. In Proceedings of the PESC'85 Record, 16th Annual IEEE, Toulouse, France, 24–28 June 1985; pp. 771–785.
10. Perreault, D.; Verghese, G.C. Time-varying effects and averaging issues in models for current-mode control. *IEEE Trans. Power Electron.* **1997**, *12*, 453–461. [CrossRef]
11. Ridley, R. A new, continuous-time model for current-mode contro. *IEEE Trans. Power Electron.* **1991**, *6*, 271–280. [CrossRef]
12. Tan, F.; Middlebrook, R. A unified model for current-programmed converters. *IEEE Trans. Power Electron.* **1995**, *10*, 397–408. [CrossRef]
13. Yan, Y.; Lee, F.; Mattavelli, P. Comparison of small signal characteristics in current mode control schemes for point-of-load buck converter applications. *IEEE Trans. Power Electron.* **2013**, *28*, 3405–3414. [CrossRef]
14. Li, J.; Lee, F. New modeling approach and equivalent circuit representation for current-mode control. *IEEE Trans. Power Electron.* **2010**, *25*, 1218–1230.
15. Babaa, I.; Wilson, T.; Yu, Y. Analytic solutions of limit cycles in a feedback-regulated converter system with hysteresis. *IEEE Trans. Autom. Control* **1968**, *13*, 524–531. [CrossRef]
16. Schweitzer, B.P.; Rosenstein, A.B. Free Running-Switching Mode Power Regulator: Analysis and Design. *IEEE Trans. Aerosp.* **1964**, *2*, 1171–1180. [CrossRef]
17. Huerta, S.; Soto, A.; Alou, P.; Oliver, J.; Garcia, O.; Cobos, J. Advanced control for very fast DC-DC converters based on hysteresis of the C_{out} current. *IEEE Trans. Circuits Syst. I Regular Pap.* **2013**, *60*, 1052–1061. [CrossRef]
18. Ki, W.-H.; Lai, K.-M.; Zhan, C. Charge balance analysis and state transition analysis of hysteretic voltage mode switching converters. *IEEE Trans. Circuits Power Syst.* **2011**, *58*, 1142–1152. [CrossRef]
19. Wen, Y.; Trescases, O. Analysis and comparison of frequency stabilization loops in self-oscillating current mode dc-dc converters. *IEEE Trans. Power Electron.* **2013**, *28*, 4753–4766. [CrossRef]
20. Castilla, M.; Guerrero, J.; Matas, J.; Miret, J.; Sosa, J. Comparative study of hysteretic controllers for single-phase voltage regulators. *IET Power Electron.* **2008**, *1*, 132–143. [CrossRef]
21. Atre, S.R.; Lele, V.P. Analytic application of Tsypkin's method relay with hysteresis and dead zone. *Proc. Inst. Electr. Eng.* **1977**, *124*, 1241–1242. [CrossRef]
22. Barrado, J.A.; El Aroudi, A.; Valderrama-Blavi, H.; Calvente, J.; Martinez-Salamero, L. Analysis of a self-oscillating bidirectional DC-DC converter in battery energy storage applications. *IEEE Trans. Power Deliv.* **2012**, *27*, 1292–1300. [CrossRef]
23. Tsypkin, Y.Z. *Relay Control Systems*; Cambridge Univ. Press: Cambridge, UK, 1984.
24. Boiko, I. Variable-structure PID controller for level process. *Control Eng. Pract.* **2013**, *21*, 700–707. [CrossRef]
25. Utkin, V.; Guldner, J.; Shi, J. *Sliding Mode Control in Electro-Mechanical Systems, (Automation and Control Engineering)*; CRC Press: Boca Raton, FL, USA, 2009.
26. Filippov, A.F. Differential equations with discontinuous right-hand side. *Am. Math. Soc. Transl.* **1964**, *42*, 199–231.
27. Utkin, V.I. *Sliding Modes in Control and Optimization*; Springer-Verlag: Berlin, Germany, 1992.
28. Sira-Ramirez, H. Sliding motions in bilinear switched networks. *IEEE Trans. Circuits Syst.* **1987**, *34*, 919–933. [CrossRef]
29. Bilalovic, F.; Music, O.; Sabanovic, A. Buck converter regulator operating in the sliding mode. In Proceedings of the 7th Internatinal PCI Conference, Orlando, FL, USA, 19–21 April 1983; pp. 331–340.
30. Malesani, L.; Rossetto, L.; Spiazzi, G.; Tenti, P. Performance optimization of Cuk converters by sliding-mode control. *IEEE Trans. Power Electron.* **1995**, *10*, 302–309. [CrossRef]

31. Spiazzi, G.; Mattavelli, P. Sliding-mode control of switched-mode power supplies. In *The Power Electronics Handbook*; Chapter 8; Lappeenranta University of Technology: Lappeenranta, Finland, 2002.
32. Tan, S.-C.; Lai, Y.; Cheung, M.; Tse, C. On the practical design of a sliding mode voltage controlled buck converter. *IEEE Trans. Power Electron.* **2005**, *20*, 425–437. [CrossRef]
33. Tan, S.-C.; Lai, Y.; Tse, C.; Cheung, M. Adaptive feedforward and feedback control schemes for sliding mode controlled power converters. *IEEE Trans. Power Electron.* **2006**, *21*, 182–192.
34. Chen, Z.; Gao, W.; Hu, J.; Ye, X. Closed-loop analysis and cascade control of a nonminimum phase boost converter. *IEEE Trans. Power Electron.* **2011**, *26*, 1237–1252. [CrossRef]
35. Chen, Z. PI and sliding mode control of a Ćuk converter. *IEEE Trans. Power Electron.* **2012**, *27*, 3695–3703. [CrossRef]
36. Komurcugil, H. Non-singular terminal sliding-mode control of DC-DC buck converters. *Control Eng. Pract.* **2013**, *21*, 321–332. [CrossRef]
37. Singh, P.; Hote, Y.; Garg, M. Comments on PI and sliding mode control of a Cuk converter. *IEEE Trans. Power Electron.* **2014**, *29*, 1551–1552. [CrossRef]
38. Sira-Ramirez, H.; Luviano-Juarez, A.; Romero, J.C. Robust input-output sliding mode control of the buck converter. *Control Eng. Pract.* **2013**, *21*, 671–678. [CrossRef]
39. Ramos, R.; Biel, D.; Fossas, E.; Guinjoan, F. Interleaving quasi-sliding-mode control of parallel-connected buck-based inverters. *IEEE Trans. Ind. Electron.* **2008**, *55*, 3865–3873. [CrossRef]
40. Cid-Pastor, A.; Martinez-Salamero, L.; Alonso, C.; Estibals, B.; Alzieu, J.; Schweitz, G.; Shmilovitz, D. Analysis and design of power gyrators in sliding-mode operation. *IEE Proc. Electr. Power Appl.* **2005**, *152*, 821–826. [CrossRef]
41. Haroun, R.; Cid-Pastor, A.; El Aroudi, A.; Martinez-Salamero, L. Synthesis of canonical elements for power processing in dc distribution systems using cascaded converters and sliding-mode control. *IEEE Trans. Power Electron.* **2014**, *29*, 1366–1381. [CrossRef]
42. Cid-Pastor, A.; Giral, R.; Calvente, J.; Utkin, V.; Martinez-Salamero, L. Interleaved converters based on sliding-mode control in a ring configuration. *IEEE Trans. Circuits Syst. I Regular Pap.* **2011**, *58*, 2566–2577. [CrossRef]
43. Utkin, V. Sliding mode control of dc/dc converters. *J. Frank. Inst.* **2013**, *350*, 2146–2165. [CrossRef]
44. Cid-Pastor, A.; Martinez-Salamero, L.; El Aroudi, A.; Giral, R.; Calvente, J.; Leyva, R. Synthesis of loss-free resistors based on sliding-mode control and its applications in power processing. *Control Eng. Pract.* **2013**, *21*, 689–699. [CrossRef]
45. Vidal-Idiarte, E.; Martinez-Salamero, L.; Guinjoan, F.; Calvente, J.; Gomariz, S. Sliding and fuzzy control of a boost converter using an 8-bit microcontroller. *IET Electr. Power Appl.* **2004**, *151*, 5–11. [CrossRef]
46. Vidal-Idiarte, E.; Martínez-Salamero, L.; Calvente, J.; Romero, A. An H_∞ control strategy for switching converters in sliding-mode current control. *IEEE Trans. Power Electron.* **2006**, *21*, 553–556. [CrossRef]
47. Mattavelli, P.; Rossetto, L.; Spiazzi, G. Small-signal analysis of DC-DC converters with sliding mode control. *IEEE Trans. Power Electron.* **1997**, *12*, 96–102. [CrossRef]
48. Chan, M.P.; Mok, P.K.T. A monolithic 2nd-order boundary controller for buck converter with fast transient response. In Proceedings of the 2010 IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia, 6–9 December 2010.
49. Biel, D.; Fossas, E. SMC applications in power electronics. *Var. Struct. Syst. Princ. Implementation* **2004**, *66*, 265–293.
50. Silva, J.; Paulo, S. Fixed frequency sliding mode modulator for current mode PWM inverters. In Proceedings of the 24th Annual IEEE Power Electronics Specialist Conference—PESC '93, Seattle, WA, USA, 20–24 June 1993; pp. 623–629.
51. Singer, S.; Erickson, R. Power-source element and its properties. *IEE Proc. Circuits Devices Syst.* **1994**, *141*, 220–226. [CrossRef]
52. Sira-Ramirez, H.; Silva-Ortigoza, R. *Control Design Techniques in Power Electronics Devices, Power Systems Series*; Springer: London, UK, 2006.
53. Doyle, J.; Francis, B.; Tannenbaum, A. *Feedback Control Theory*; Macmillan Publishing Co.: Basingstoke, UK, 1990.
54. Goder, D.; Pelletier, W.R. *V2 Architecture Provides Ultra-Fast Transient Response in Switch Power Supplies*; Intertect International: Las Vegas, NV, USA, 1996; pp. 19–23.

55. Redl, R.; Sun, J. Ripple-based control of switching regulators: an overview. *IEEE Trans. Power Electron.* **2009**, *24*, 2669–2680. [CrossRef]
56. Sun, J. Characterization and performance comparison of ripple-based control for voltage regulator modules. *IEEE Trans. Power Electron.* **2006**, *21*, 346–353.
57. Del Viejo, M.; Alou, P.; Oliver, J.A.; García, O.; Cobos, J.A. V^2IC control: A novel control technique with very fast response under load and voltage steps. In Proceedings of the 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011.
58. Cortes, J.; Svikovic, V.; Alou, P.; Oliver, J.; Cobos, J.A. V^1 concept: Designing a voltage mode control as current mode with near time-optimal response for Buck-type converters. *IEEE Trans. Power Electron.* **2015**, *30*, 5829–5841. [CrossRef]
59. Chen, M.; Zhao, M.; Wu, X. A fixed-frequency fast transient response DC-DC controller for VRMs. *J. Semiconduct.* **2013**, *34*, 125002. [CrossRef]
60. Yan, Y.; Lee, F.C.; Mattavelli, P.; Liu, P.H. I^2 average current mode control for switching converters. *IEEE Trans. Power Electron.* **2014**, *29*, 2027–2036. [CrossRef]
61. Pitel, G.E.; Krein, P.T. Minimum-time transient recovery for DC-DC converters using raster control surfaces. *IEEE Trans. Power Electron.* **2009**, *12*, 2692–2703. [CrossRef]
62. Kapat, S.; Krein, P.T. Improved time optimal control of a buck converter based on capacitor current. *IEEE Trans. Power Electron.* **2012**, *27*, 1444–1454. [CrossRef]
63. Kapat, S.; Krein, P.T. Formulation of PID control for DC-DC converters based on capacitor current: A geometric context. *IEEE Trans. Power Electron.* **2012**, *27*, 1424–1432. [CrossRef]
64. Onwuchekwa, C.N.; Kwasinski, A. Analysis of boundary control for buck converters with instantaneous constant-power loads. *IEEE Trans. Power Electron.* **2010**, *2*, 2018–2032. [CrossRef]
65. Santi, E.; Monti, A.; Li, D.; Proddutur, K.; Dougal, R.A. Synergetic control for DC-DC boost converter: Implementation options. *IEEE Trans. Ind. Appl.* **2003**, *39*, 1803–1813. [CrossRef]