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Power and Voltage Control for Single-Phase Cascaded H-Bridge Multilevel Converters under Unbalanced Loads

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Abstract: The conventional control method for a single-phase cascaded H-bridge (CHB) multilevel converter is vector (dq) control; however, dq control requires complicated calculations and additional time delays. This paper presents a novel power control strategy for the CHB multilevel converter. A power-based dc-link voltage balance control is also proposed for unbalanced load conditions. The new control method is designed in a virtual $\alpha\beta$ stationary reference frame without coordinate transformation or phase-locked loop (PLL) to avoid the potential issues related to computational complexity. Because only imaginary voltage construction is needed in the proposed control method, the time delay from conventional imaginary current construction can be eliminated. The proposed method can obtain a sinusoidal grid current waveform with unity power factor. Compared with the conventional dq control method, the power control strategy possesses the advantage of a fast dynamic response. The stability of the closed-loop system with the dc-link voltage balance controller is evaluated. Simulation and experimental results are presented to verify the accuracy of the proposed power and voltage control method.

Keywords: cascaded H-bridge (CHB); dc-link voltage balance control; multilevel converter; power control; single-phase system

1. Introduction

Multilevel converters have gained increasing attention as of late. Commonly used multilevel converters include cascaded H-bridge (CHB), flying capacitor, and neutral-point-clamped converters [1]. Among these, the CHB converter has advantages of simple implementation, high reliability, and low harmonics [2], hence, it has been widely researched in academia and industry, particularly in relation to static synchronous compensators [3], solid-state transformers [4], and active power filters [5].

Many control schemes have been proposed to enable the pulse width modulation (PWM) converter to achieve a high power factor and near-sinusoidal grid current [6]. These strategies can be broadly classified into two categories: direct power control (DPC) and direct current control (DCC).

DPC was originally proposed by Ohnishi [7], whose method directly controls the active and reactive power of the PWM converter using three-phase instantaneous power theory. Compared with DCC, DPC has advantages of simple structure, fast dynamic response, high efficiency, and wide applicability [8]. Currently, many advanced DPC strategies have been proposed, such as predictive DPC (P-DPC) [9], deadbeat DPC [10], and slide-mode DPC [11]. In the single-phase PWM converter

system, instantaneous power estimation is more complicated than in the three-phase system, which limits the development of DPC schemes in single-phase systems [12].

DCC methods have been frequently used with the PWM converter. The most commonly used DCC method utilizes vector control theory (*dq* control) [13–16]. Coordination transformation is needed in *dq* control to change the ac signals into dc signals [17]. The grid voltage phase angle is essential in the coordinate transformation; therefore, a phase-locked loop (PLL) is employed to synchronize the output voltage with the grid voltage vector [18]. To accurately obtain the information on the grid voltage including the amplitude and phase angle, some advanced PLLs have been proposed, such as hybrid filtering technique-based PLL [19], grid sequence separator PLL [20], frequency-fixed SOGI-based PLL [21], and repetitive learning-based PLL [22]. However, the computational complexity of coordinate transformation and PLL increases the calculation burden of the embedded processor like the digital signal processor (DSP) [23]. Therefore, the development of a convenient control method without PLL or coordination transformation is appealing. Recently proposed control methods of the CHB converter are based on model-predictive control (MPC) [24,25]. However, three major problems arise in the MPC scheme used for the CHB converter. First, the calculation burden persists in the MPC method because the number of switching states increases exponentially as more H-bridges are added [26]. The second one is the MPC system sensitiveness problem like sensitive to the parameter [27]. The third problem is that under unbalanced load conditions, the MPC strategy cannot provide a proper control function [28].

It is exceedingly difficult to implement the *dq* control scheme in the single-phase CHB converter system; imaginary orthogonal current and voltage signals must be created for coordinate transformation ($\alpha\beta$ to dq) because only one physical axis is accessible [29]. In *dq* control, the imaginary orthogonal current signal is essential in acquiring the dc current signals i_d and i_q for the inner current loop [30]. Thus, an imaginary current construction module is required to produce the imaginary orthogonal current signal [31]. Although the performance of conventional imaginary current construction under the steady state is mostly acceptable, the time delay tends to slow down the system dynamic response and result in further distortion [32,33].

The control scheme performance of the CHB converter in the single-phase system depends on two key factors: sinusoidal grid current waveform with unity power factor and balanced dc-link voltages [34,35]. Therefore, the CHB multilevel converters need a control method to balance the dc-link voltages, especially when the dc-side loads are unbalanced. In [36,37], the dc-link voltages were controlled using individual capacitor voltage controllers. In [38], the presented voltage balance control method uses a weighting factor to adjust the dc-link voltages. In [39], two voltage-balancing techniques were presented, allowing for much more efficient regulation of dc-link voltages. However, these voltage balanced control methods are all based on ac voltage reference duty cycle regulation; a power-based dc-link voltage balance controller has not been analyzed in detail.

In the conventional *dq* control strategy, the current calculation is complicated and additional time delay is required. For optimization purposes, a power control method without coordinate transformation, PLL or conventional imaginary current construction is introduced and applied to control the single-phase CHB multilevel converter system. Moreover, a power-based dc-link voltage balance control scheme is presented to make the proposed power control strategy available under unbalanced load conditions. This power and voltage control method can achieve a sinusoidal grid current waveform and balanced dc-link voltages. Several experimental tests were conducted to compare dynamic responses of the presented control scheme with those of the classical *dq* control method. The proposed voltage balance controller is verified as well.

The remainder of this paper is organized as follows: in Section 2, principles of the proposed control scheme and dc-link voltage balance controller are discussed, and the stability of the closed-loop system with the dc-link voltage balance controller is evaluated. Section 3 presents the simulation results. Experimental results are addressed in Section 4. The proposed control method is discussed in Section 5. Finally, relevant conclusions are drawn in Section 6.

2. Control Method Principles

2.1. Model of the Cascaded H-Bridge Multilevel Converter

Figure 1 presents the topology of a two-cell CHB system in which u_s is the grid voltage, i_{sa} is the grid current, u_c is the ac side voltage, L and R_L denote the filter inductor and line resistance, respectively,. u_{dc1} and u_{dc2} represent the dc-link voltages of the first and second H-bridge, and u_{dc_sum} is the total dc-link voltage ($u_{dc1} + u_{dc2}$). R_1 and R_2 are the resistive loads connected to the dc side of each H-bridge.

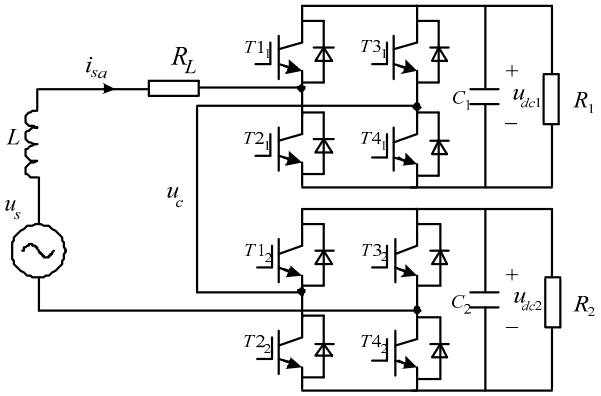

Figure 1. Two-cell single-phase CHB converter.

The mathematical model of the CHB converter is as follows:

$$\begin{cases} L\frac{di_{sa}}{dt} = u_s - u_c - R_L i_{sa} \\ u_{dc\_sum} = u_{dc1} + u_{dc2} \end{cases} \quad (1)$$

To simplify analysis of system stability, according to Equation (1), a small-signal model of the stationary reference frame ($\alpha\beta$ frame) was built, as illustrated in Figure 2. Here, $u_{s\alpha}$ equals u_s, and $u_{s\beta}$ is the orthogonal signal of u_s; $\tilde{u}_{s\alpha}$ and $\tilde{u}_{s\beta}$ represent the small-signal ac variation of $u_{s\alpha}$ and $u_{s\beta}$; $\tilde{u}_{dc1}$ and $\tilde{u}_{dc2}$ denote the small-signal ac variation of u_{dc1} and u_{dc2}; $i_{s\alpha}$ equals i_{sa}, and $i_{s\beta}$ is the orthogonal signal of i_{sa}; $\tilde{i}_{s\alpha}$ and $\tilde{i}_{s\beta}$ represent the small-signal ac variation of $i_{s\alpha}$ and $i_{s\beta}$; $I_{s\alpha}$ and $I_{s\beta}$ stand for the quiescent operating point of $i_{s\alpha}$ and $i_{s\beta}$; $D_{\alpha1}$, $D_{\alpha2}$, $D_{\beta1}$, and $D_{\beta2}$ are the duty cycles of the first and second H-bridge; and $\tilde{d}_{\alpha1}$, $\tilde{d}_{\alpha2}$, $\tilde{d}_{\beta1}$, and $\tilde{d}_{\beta2}$ represent the small-signal ac variation of $D_{\alpha2}$, $D_{\beta1}$, and $D_{\beta2}$.

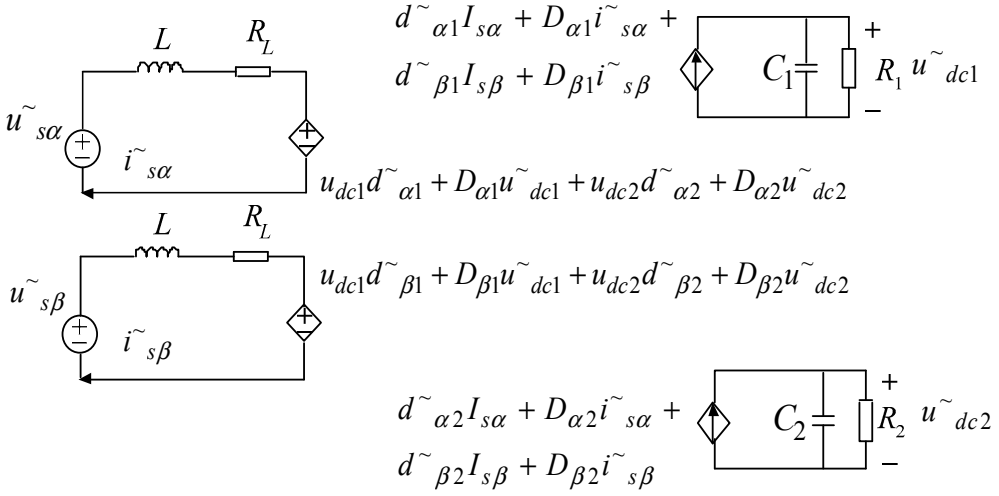

Figure 2. Small-signal model of two-cell single-phase CHB converter in $\alpha\beta$ frame coordination.

2.2. Principle of the Proposed Power Control Method

The main function of CHB multilevel converter is to obtain active power and reactive power from the grid to satisfy load needs. For the CHB converter, the essence of controlling the grid current as well as the dc-link voltage is control of the input and output power. By rapidly and effectively controlling the active and reactive power, the converter can achieve strong dynamic and static characteristics.

In the three-phase CHB converter system, the active power p and reactive power q can be described as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ u^*_{s\alpha} & u^*_{s\beta} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{2}$$

where $u^*_{s\alpha} = u_{s\beta}$, $u^*_{s\beta} = -u_{s\alpha}$.

Only one phase physical variable is available in the single-phase CHB converter system; a second-order generalized integrator (SOGI) block is needed to introduce the imaginary signal. The virtual $\alpha\beta$ stationary reference frame is depicted in Figure 3, the α-axis coincides with the a-axis, and the β-axis is orthogonal to the α-axis.

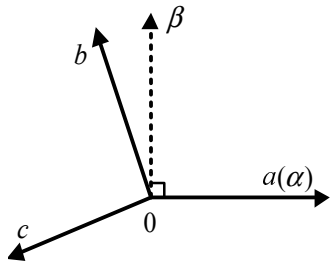

Figure 3. Schematic diagram of virtual $\alpha\beta$ coordinate axis.

In the single-phase CHB converter system, p and q can be described as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \frac{1}{3}\begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ u^*_{s\alpha} & u^*_{s\beta} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{3}$$

p^* and q^* are defined as the active power and reactive power reference, respectively; $i^*_{s\alpha}$ and $i^*_{s\beta}$ represent the current reference.

Equations (4) and (5) are shown as follows according to Equation (3), and the coefficient calculation of the proposed power control is shown in Equation (6):

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \frac{3}{u_{s\alpha} * u^*_{s\beta} - u^*_{s\alpha} * u_{s\beta}} \begin{bmatrix} u^*_{s\beta} & -u_{s\beta} \\ -u^*_{s\alpha} & u_{s\alpha} \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \begin{bmatrix} \frac{3u^*_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} p^* + \frac{-3u_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} q^* \\ \frac{-3u^*_{s\alpha}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} p^* + \frac{3u_{s\alpha}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} q^* \end{bmatrix} \tag{5}$$

$$\begin{cases} k_1 = \frac{3u^*_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} \\ k_2 = \frac{-3u_{s\beta}}{u_{s\alpha}*u^*_{s\beta}-u^*_{s\alpha}*u_{s\beta}} \end{cases} \tag{6}$$

If the grid voltage is sinusoidal, then the result of $u_{s\alpha} * u^*_{s\beta} + u^*_{s\alpha} * u^*_{s\beta}$ is constant; p^* is controlled by the outer power loop; q^* is constant because it is given directly; therefore the frequency and phase of the current references $i_{s\alpha}$ and $i_{s\beta}$ are consistent with the instantaneous grid voltage, and the real-time tracking can be achieved. Notably, only $i^*_{s\alpha}$ is used as the current reference, because the CHB multilevel converter is used on a single-phase system.

2.3. Presentation of Proposed Dc-Link Balance Controller

Figure 4 presents the conventional dc-link voltage balance controller. In this approach, the duty cycles of each ac voltage reference u^*_{a1} and u^*_{a2} are modified separately to keep the voltages balanced, and the scheme is suitable for the *dq* method. A power-based dc-link voltage balance controller adjusting the ac current reference duty cycle is introduced in this paper to regulate the individual H-bridge dc-link voltage.

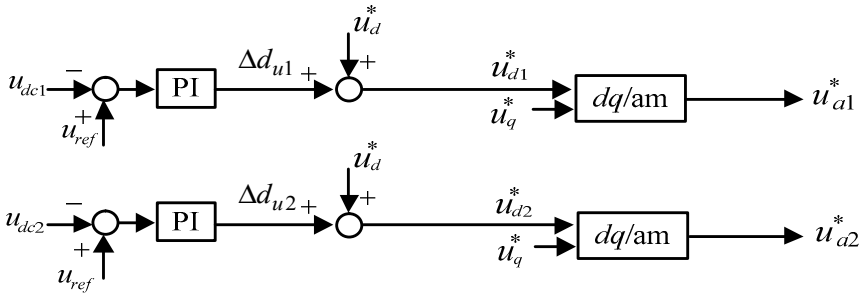

Figure 4. Conventional voltage balance controller [37].

If the dc-link voltage of each H-bridge is unbalanced (mainly via load imbalance), then the power of these H-bridges becomes uneven. To keep the dc-link voltage balanced, the uneven power should be extracted from the grid. Δd_{p1} and Δd_{p2} are used as the compensation values to eliminate uneven power. Δd_{p1} and Δd_{p2} are calculated by the voltage balance controller:

$$\begin{cases} \Delta d_{p1} = (K_p + \frac{K_i}{s})(u_{ref} - u_{dc1}) \cdot u_{dc1} \\ \Delta d_{p2} = (K_p + \frac{K_i}{s})(u_{ref} - u_{dc2}) \cdot u_{dc2} \end{cases} \tag{7}$$

where K_p and K_i represent the proportional and integral coefficient of the proportional-integral (PI) controller, respectively, and u_{ref} is the voltage reference of every H-bridge cell.

The presented voltage balance controller is shown in Figure 5, which modifies the duty cycles of each ac current reference i^*_{sa1} and i^*_{sa2} individually to reduce the dc voltage imbalance. The current reference for each H-bridge can be calculated according to Equations (8)–(10):

$$\begin{cases} i^*_{s\alpha 1} = \Delta d_{i^*sa1} + i^*_{s\alpha} \\ i^*_{s\alpha 2} = \Delta d_{i^*sa2} + i^*_{s\alpha} \end{cases} \tag{8}$$

$$\begin{cases} i^*_{s\alpha 1} = \Delta d_{p1}(k_1 + k_2) + p^*k_1 + q^*k_2 \\ i^*_{s\alpha 2} = \Delta d_{p2}(k_1 + k_2) + p^*k_1 + q^*k_2 \end{cases} \tag{9}$$

$$\begin{cases} i^*_{s\alpha 1} = k_1(\Delta d_{p1} + p^*) + k_2(\Delta d_{p1} + q^*) \\ i^*_{s\alpha 2} = k_1(\Delta d_{p2} + p^*) + k_2(\Delta d_{p2} + q^*) \end{cases} \tag{10}$$

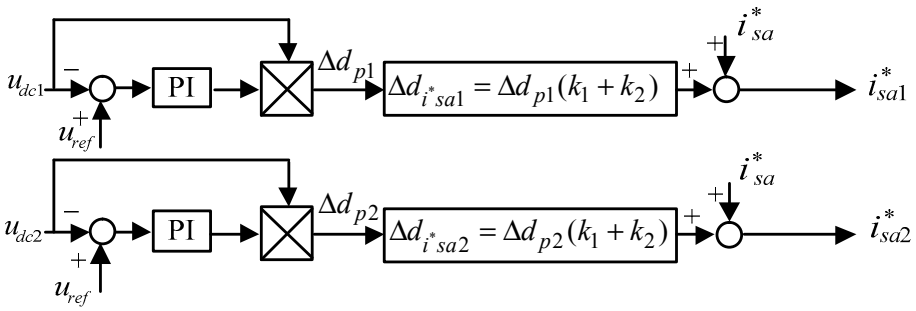

Figure 5. Proposed voltage balance controller.

2.4. Proposed Power Control of the Cascaded H-Bridge Multilevel Converter

The overall control topology of the proposed control method is depicted in Figure 6. The main idea of the proposed control is to obtain command signals in the orthogonal $\alpha\beta$ frame; as such, the dc-link voltages can be balanced.

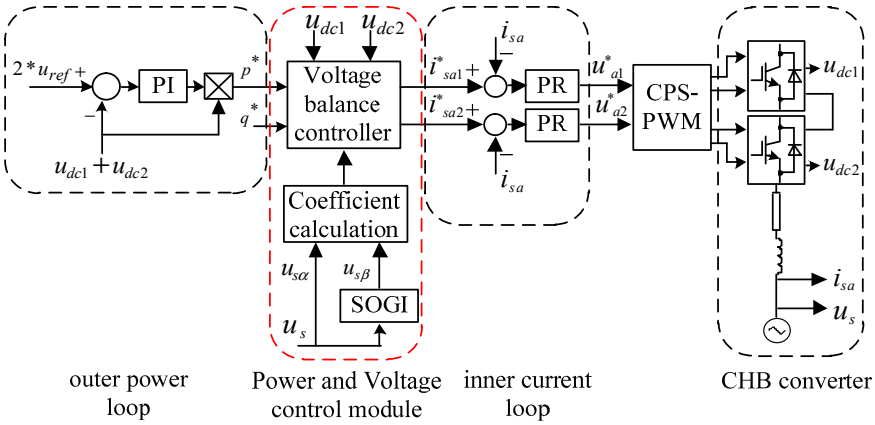

Figure 6. Proposed power and voltage control of CHB converter.

The control system is formed as a double closed-loop control structure using the inner current loop and the outer power loop.

The inner current loop is implemented in the orthogonal $\alpha\beta$ frame. Compared with classical single-phase dq schemes, the current calculation of the proposed control method is simpler because no coordinate transformation, PLL, or conventional imaginary current construction is needed. However, the current references i^*_{sa1} and i^*_{sa2} are ac variables. To track the current references with zero error in the stationary frame and achieve high tracking accuracy when the grid frequency fluctuates, rather than relying on conventional PI controllers or a repetitive controller [40], proportional-plus-resonant (PR) controllers are utilized in the current loop.

As for the outer power loop, a PI controller is used to adjust the total dc-link voltage u_{dc_sum} (u_{dc1} + u_{dc2}). The active power p^* is generated by multiplying the output of the PI controller by the total dc-link voltage u_{dc_sum}. Reactive power reference q^* is given directly.

The detailed control topology of the power and voltage control module is shown in Figure 7. Current reference i^*_{sa1} of the first H-bridge and i^*_{sa2} of the second H-bridge are acquired through the dc-link voltage balance control block; these current references are controlled independently. Deviation values between the grid current i_{sa} and the current references are input into the PR regulators separately, and the modulation voltage signals u^*_{a1} and u^*_{a2} are generated for the first and second H-bridge. Carrier phase-shifted PWM (CPS-PWM) technology is adopted to generate five-level voltage, achieving multi-level modulation. Furthermore, if the reactive power reference q^* is set to zero, then a unity power factor can be achieved.

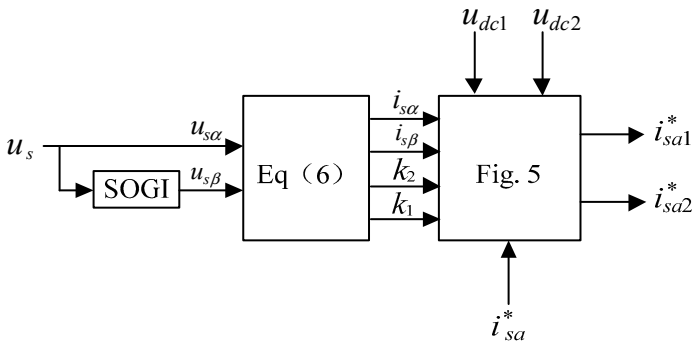

Figure 7. Power and voltage control module.

2.5. Stability Analysis of the Power and Voltage Control Scheme

Assume that the parameters of the H-bridges are identical, such that the dc-link voltage $u_{dc1} = u_{dc2} = u_{dc}$. The double-loop control diagram presented in Figure 6 can thus be transformed as illustrated in Figure 8. In Figure 8, G_V is the voltage gain of CHB, G_{PIV} is the voltage PI regulator, K is the conversion coefficient between p^* and i^*_{sa}, G_{qPR} is the current PR regulator, G_{TPWM} is the transfer function of the PWM modulator, G_{IV} is the transfer function of the voltage to output current i^*_{sa}, and G_{VI} is the transfer function of the current to output voltage u_{dc}. G_{IV} and G_{VI} can be deduced from the small-signal model shown in Figure 2.

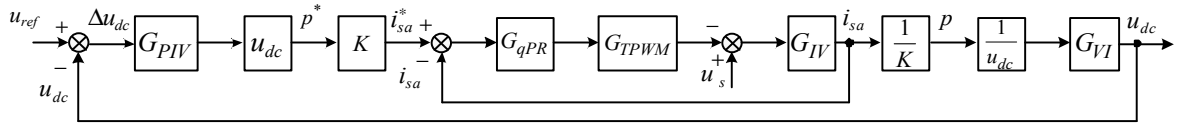

Figure 8. Basic double-loop controller structure diagram of the proposed power control.

The closed-loop transfer function can be expressed as follows:

$$G_V = \frac{G_{PIV}G_{qPR}G_{TPWM}G_{IV}G_{VI}}{1 + G_{PIV}G_{qPR}G_{TPWM}G_{IV}G_{VI}} \tag{11}$$

One bridge of the CHB converter can be simplified according to Figure 9 per Thevenin law. However, the dc-link voltage unbalance problem in CHB remains under the unbalanced load condition; therefore the voltage balance control module should be added. Figure 10 shows the Thevenin equivalent circuit with the dc-link voltage balance module, where Z_1 is the load impedance, Z_{io} is the impedance between the input and output of CHB, M is the gain of the voltage balance control module, G_1 is the conversion coefficient of power to voltage, and i_{out} is the output current. In this case $G_1 = 1/(G_{PIV} * u_{dc})$.

Taking the first H-bridge as an example:

$$G_1[p^* + (u_{ref} - u_{dc1})M]G_V = Z_{io}\frac{u_{dc1}}{Z_1} + u_{dc1} \tag{12}$$

$$u_{dc1} = \frac{G_V G_1}{Z_{io}/Z_1 + 1 + G_V G_1 M}p^* + \frac{G_V G_1 M}{Z_{io}/Z_1 + 1 + G_V G_1 M}u_{ref} \tag{13}$$

Because $Z_1 >> Z_{io}$, GG_1M represents the gain in the basic double-loop controller with the dc-link voltage balance module from Equation (13); the Bode plot is shown in Figure 11. The amplitude margin is 12.7 dB, the cut-off frequency is 272 Hz, the phase margin is 105°, and the cross-over frequency is 78 Hz. All roots of $(Z_{io}/Z_1 + 1 + GG_1M)$ are on the left half-complex plane, ensuring stability of the system with the voltage balance control module.

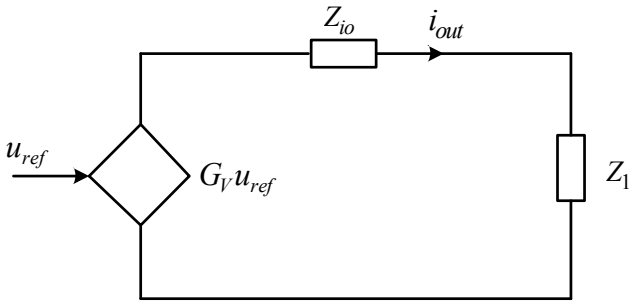

Figure 9. Thevenin equivalent circuit of the basic double-loop.

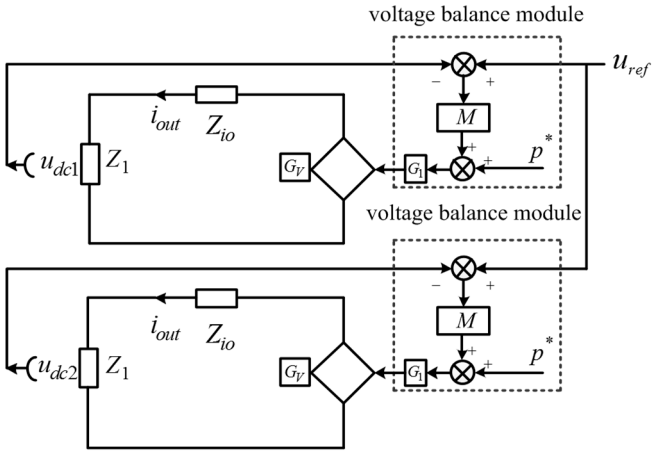

Figure 10. Thevenin equivalent circuit with the voltage balance module controller.

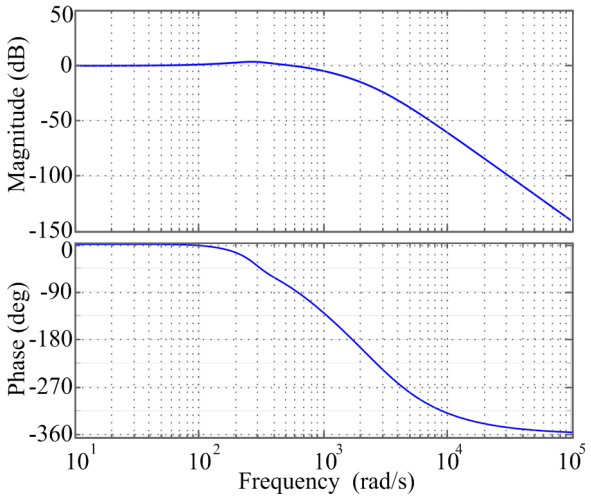

Figure 11. Bode plot of the basic double-loop controller with the dc-link voltage balance module.

3. Simulation Results

The CHB converter system shown in Figure 1 was modelled in the MATLAB/Simulink R2015a (MATLAB/Simulink R2015a, MathWorks, Natick, MA, USA) software environment to verify the power and voltage control scheme. The main system parameters used for simulation are shown in Table 1.

Table 1. Parameters Used For Simulation.

Parameter	Symbol	Simulation Value
Grid voltage *rms* value	u_s	220 V
Grid frequency	f_g	50 Hz
Input inductance	L	3.0 mH
dc-link total voltage	U_{dc}	400 V
dc-link capacitance	C_1, C_2	4700 μF
dc-link load resistance	R_1, R_2	10 Ω, 15 Ω
Switching frequency	f_{sw}	10 kHz
Inner current loop control parameters	P, R, w_c	0.5, 100, 6.28
Outer power loop control parameters	P, I	0.1, 8

3.1. Proposed Power Control Scheme Simulation

Figures 12–14 show the simulation results with unbalanced loads, where R_1 = 10 Ω and R_2 = 15 Ω. Figure 12a displays the grid voltage and grid current waveform in the steady state, revealing that the unity power factor was achieved.

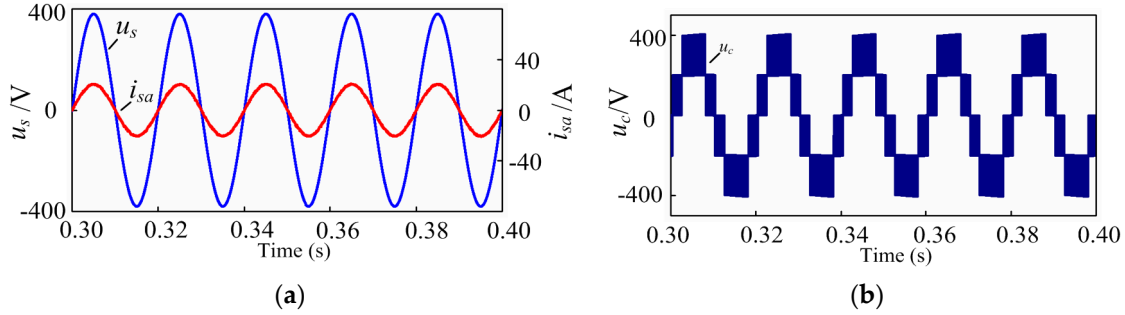

Figure 12. Simulation waveforms of CHB converter in steady state: (**a**) Grid voltage and grid current; (**b**) Five-level voltage staircase waveform.

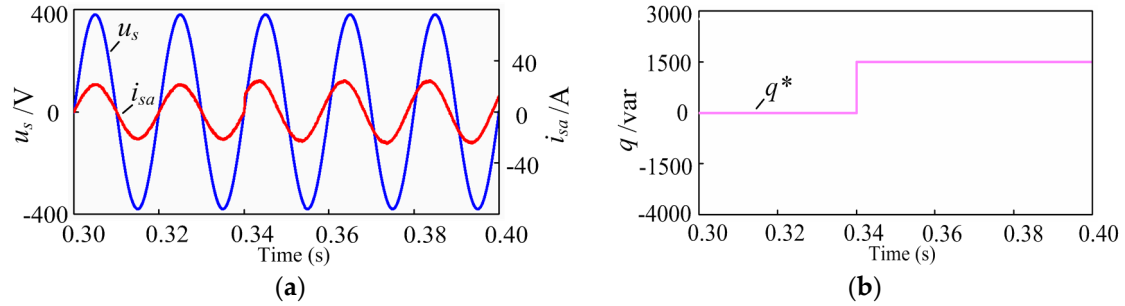

Figure 13. q^* changed from 0 var to 1500 var: (**a**) Dynamic response of the grid current; (**b**) Dynamic response of the reactive power.

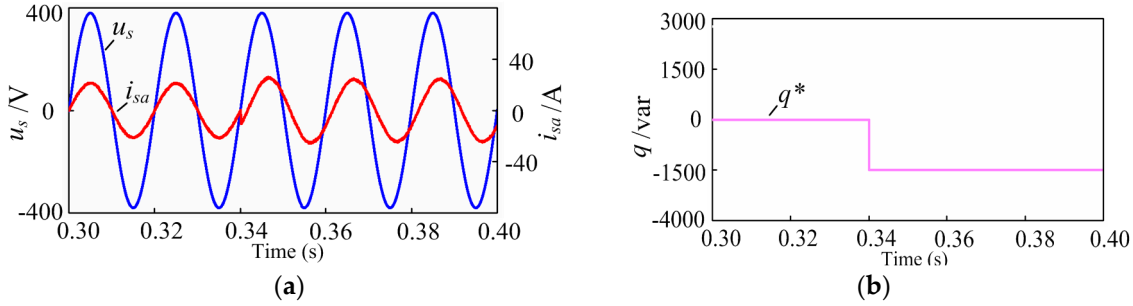

Figure 14. q^* changed from 0 var to −1500 var: (**a**) Dynamic response of the grid current; (**b**) Dynamic response of the reactive power.

Figure 12b shows the ac side five-level staircase voltage. Dynamic responses of the proposed method under sudden reactive power change conditions are shown in Figures 13 and 14. In these, the active power reference p^* is governed by the outer power loop, and the reactive power reference q^* is changed from 0 to −1500 var and 0 to 1500 var at 0.34 s.

3.2. Power-Based Voltage Balance Control Simulation

In this simulation, the initial loads of two H-bridges were 15 Ω resistors. At 1.0 s, the resistor of the first H-bridge declined to 10 Ω. Two distinct cases were considered. In Figure 15a, the voltage balance control module was not utilized, and the dc-link voltages became different after the load change. The second H-bridge, whose resistor was unchanged, demonstrated higher dc-link voltage

than the first H-bridge. Figure 15b shows the dc-link voltages with the voltage balance control method. Using the proposed voltage balance control module, the dc-link voltages returned to the initial value (200 V).

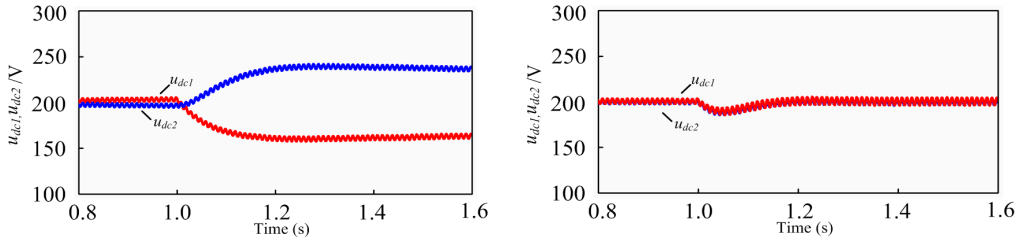

Figure 15. Simulated response of dc-link voltages when load changed: (**a**) Without voltage balance control; (**b**) With voltage balance control.

4. Experimental Results

4.1. Experimental Prototype

A single-phase five-level CHB converter experimental platform was adopted to validate the presented power and voltage control scheme, as shown in Figure 16.

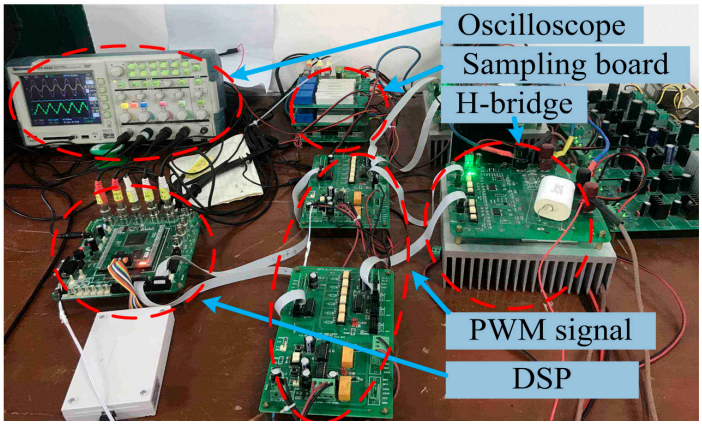

Figure 16. Platform of the experiments.

Two H-bridge converters with serially connected inputs formed the ac side of the experimental setup. The dc output of each converter fed the loads. The converter was interfaced to the grid through a coupling transformer and a voltage regulator to ensure safety during the experiments. The secondary-side voltage of the regulator was set to 80 V (rms), while the dc-link voltage references u_{dc1} and u_{dc2} were set to 50 V. The grid voltage, grid current, ac side voltage, and dc-link voltages were measured using the outer high-performance hall sensors. A TMS320F28377D DSP processor board was utilized to implement the control algorithm. Measured voltage and current signals were fed back to the DSP processor board employing a built-in, 16-bit analog-digital conversion module. The power factor and total harmonic distortion (THD) of the grid current were measured via a Fluke 435 power quality analyzer.

4.2. Steady State

Figure 17 depicts the experimental waveforms of the grid voltage u_s (200 V/division), the grid current i_{sa} (20 A/division), the dc-link voltage of the first H-bridge u_{dc1} (20 V/division), and the ac side voltage u_c (100 V/division) for the proposed scheme in the steady state, where loads R_1 and R_2 in Figure 1 are 10 Ω and 15 Ω, separately. When the reactive power reference q^* was set to zero, the grid

current was in phase with the grid voltage, so the unity power factor was achieved. The THD of the grid current in the steady state was 4.3%, indicated in Figure 18. Moreover, this method was found to compensate for the reactive power: CHB converters can generate or absorb reactive power to the power grid when the reactive power reference is positive or negative. In Figure 19, the grid current was leading the grid voltage; thus, the CHB converter was generating reactive power to the system. In Figure 20, the grid current was lagging the voltage, and the CHB converter was absorbing reactive power from the system.

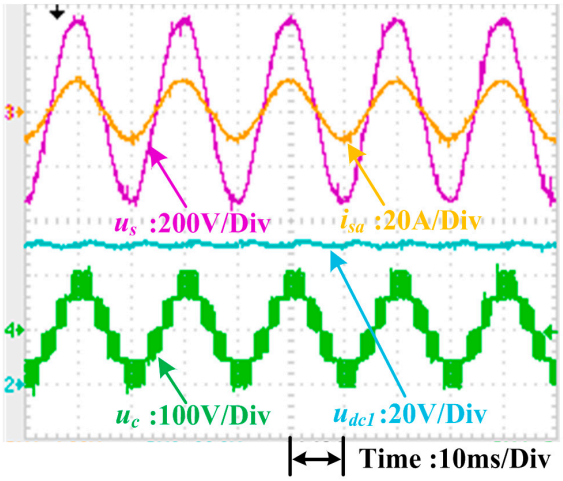

Figure 17. Experimental waveforms of CHB converter in steady state.

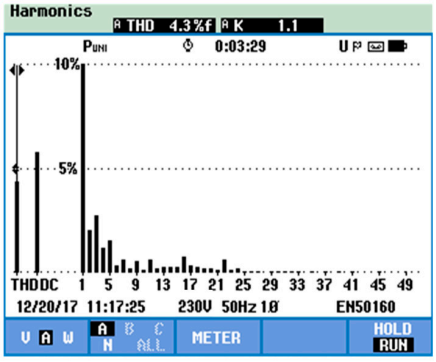

Figure 18. THD of grid current in steady state.

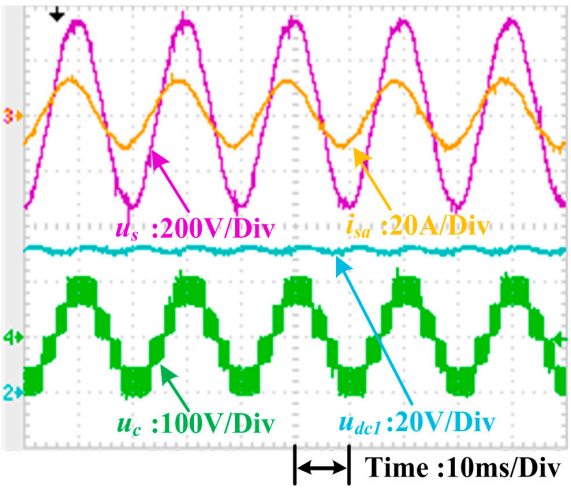

Figure 19. Experimental grid currents of CHB capacitive mode.

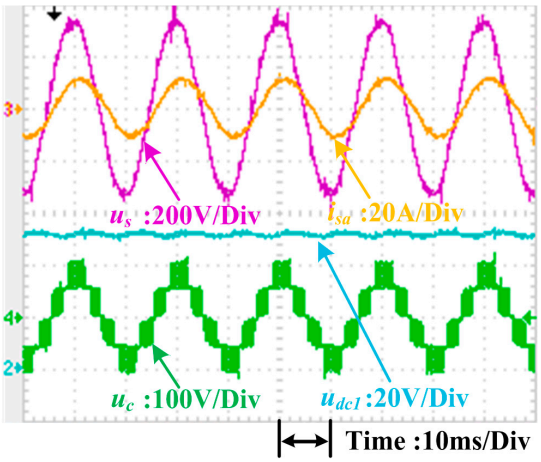

Figure 20. Experimental grid currents of CHB inductive mode.

4.3. Dynamic Response Compared with dq Control

Currently, the most popular control method for the single-phase CHB converter is *dq* control. Several experiments were carried out to compare conventional *dq* control with the proposed control method. These experiments tested the dynamic responses of the systems under sudden power change conditions. In these tests, the total dc-link voltage u_{dc_sum} was kept at 100 V, and the system was connected to two resistive loads where R_1 is 10 Ω and R_2 is 15 Ω, respectively. The dynamic of the d-axis current i^*_d in the *dq* control was managed by the outer voltage loop, and active power p^* in the proposed scheme was controlled by the outer power loop. Therefore, only step changes in the reactive current reference i^*_q in the *dq* control and reactive power reference q^* in the proposed control were applied to evaluate the dynamic control performance of each. Differences in the dynamic performance of the *dq* control scheme and the proposed control method are illustrated in Figures 21–28.

The total dc-link voltage u_{dc_sum} is 100 V; i^*_q and q^* are given directly in each control method. Reactive power reference q^* equals u_{dc_sum} * i^*_q (100 * i^*_q). For instance, when the step change of i^*_q is 5 A, the step change of q^* equals 100 * i^*_q (500 var); when the step change of i^*_q is −5 A, the step change of q^* equals 100 * i^*_q (−500 var).

As shown, the transient responses of the proposed power control method (less than 1 ms) were faster than the *dq* control method (more than 5 ms). In the *dq* control method, a time delay of 1/4 in the fundamental period arose from classical imaginary current construction.

Grid current and five-level staircase voltage continuous distortions also appeared in the *dq* control method due to conventional imaginary current construction.

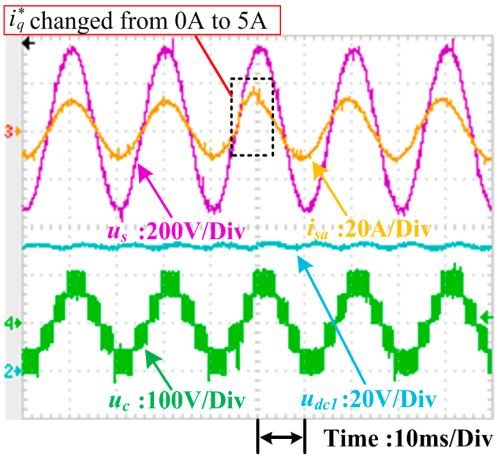

Figure 21. i^*_q changed from 0 A to 5 A (*dq* control method).

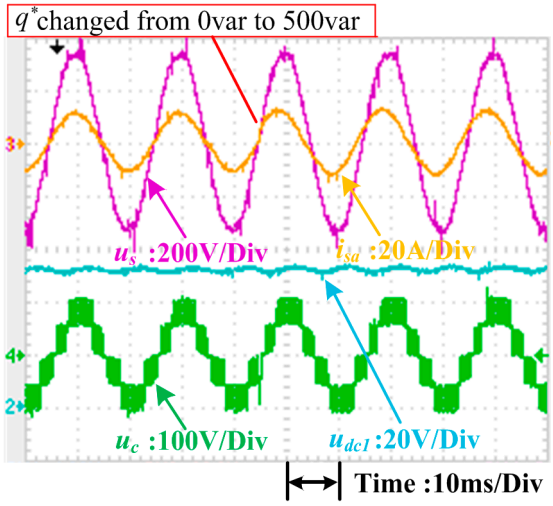

Figure 22. q^* changed from 0 var to 500 var (proposed control method).

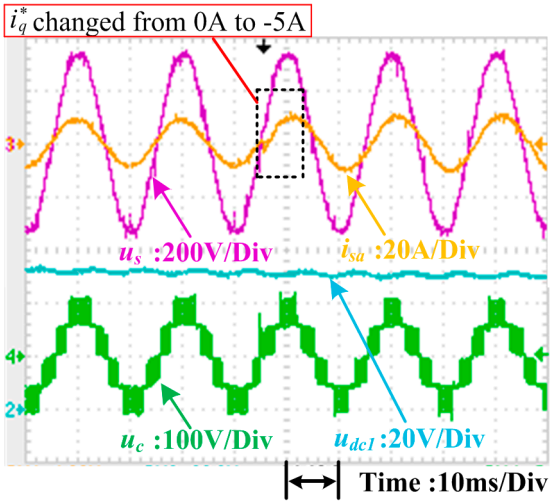

Figure 23. i^*_q changed from 0 A to −5 A (dq control method).

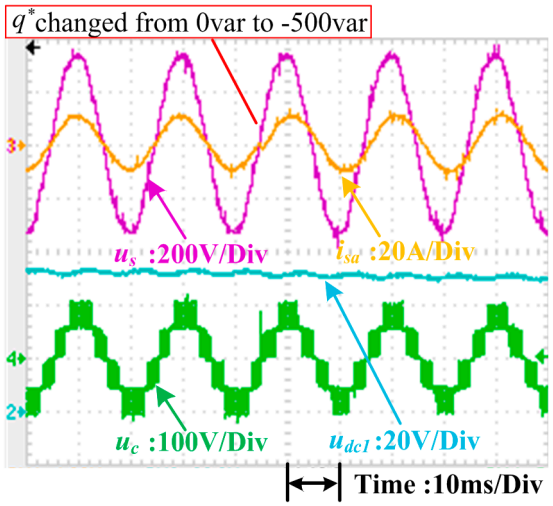

Figure 24. q^* changed from 0 var to −500 var (proposed control method).

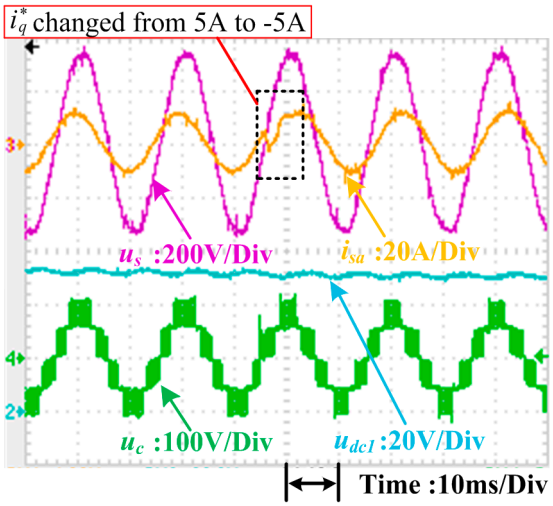

Figure 25. i^*_q changed from 5 A to −5 A (*dq* control method).

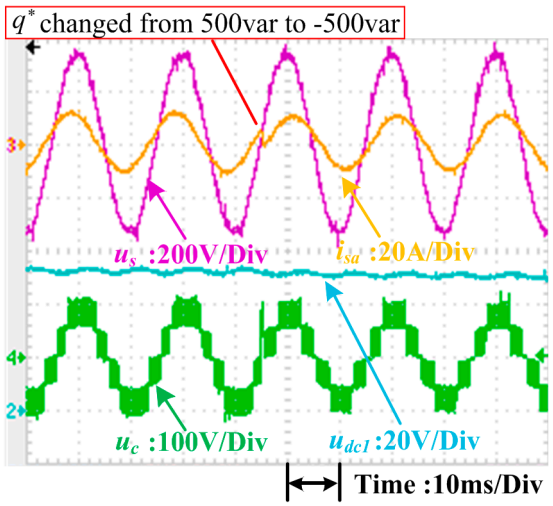

Figure 26. q^* changed from 500 var to −500 var (proposed control method).

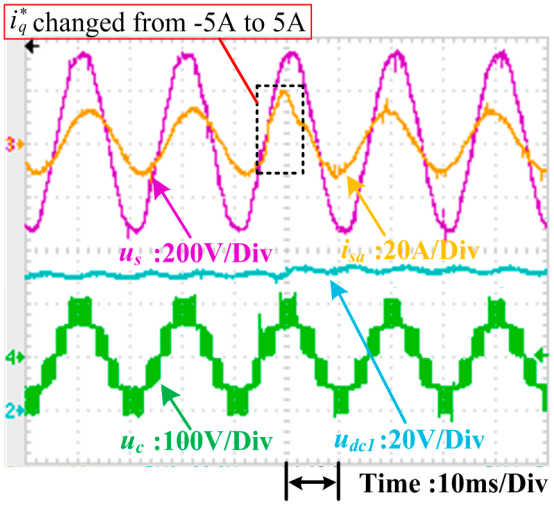

Figure 27. i^*_q changed from −5 A to 5 A (*dq* control method).

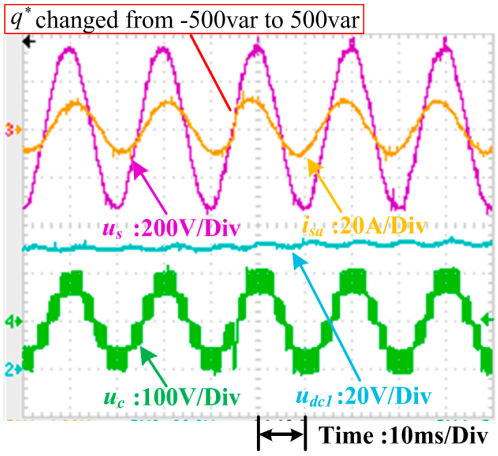

Figure 28. q^* changed from −500 var to 500 var (proposed control method).

4.4. Voltage Balance Control

Besides grid current control, balance control of the dc-link voltages is another important issue. A dc-link voltage balance control method based on power was adopted to render the proposed power control strategy applicable to the CHB converter under unbalanced load conditions.

Unbalanced load experimental tests were conducted to verify the voltage-balancing performance of the presented scheme. In these experiments, the load resistor of the first H-bridge R_1 was stepped from 15 Ω to 10 Ω whereas that of the second H-bridge R_2 was maintained at 15 Ω. In Figure 29a, when the load resistors were changed, the dc-link voltage of the first H-bridge u_{dc1} (10 V/division) declined from 50 V to 45 V, and that of the second H-bridge u_{dc2} (10 V/division) increased from 50 V to 55 V. Figure 29b shows that when the voltage balance controller was adopted, the dc-link voltages could be controlled to 50 V when the load resistors were changed. Thus, the accuracy of the presented dc-link voltage balance control method was confirmed.

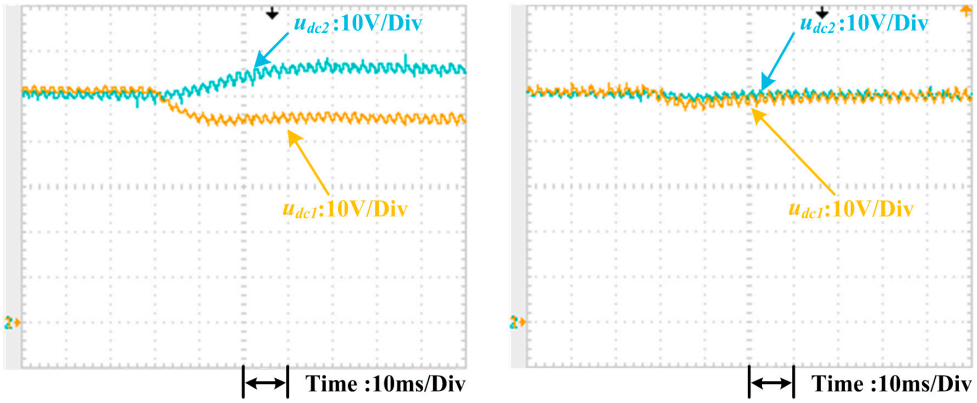

Figure 29. Experimental response of dc-link voltages when load changed: (**a**) Without voltage balance controller, (**b**) With voltage balance controller.

5. Discussion

The proposed power and voltage control method offers many advantages including no coordinate transformation, PLL, or conventional imaginary current construction. Moreover, it was found to exhibit faster transient responses and lower distortions compared with the conventional *dq* control method, as illustrated in Figures 21–28.

The natural frame control scheme presented in [23] also shows the advantages of no coordinate transformation, PLL, or conventional imaginary current construction. Differ from the natural frame

control scheme, the proposed scheme connects power control with current control through the instantaneous power theory. Besides, the proposed voltage balance control module is based on power, in which the power compensation values are used to eliminate the uneven power in active power p and reactive power q.

Even so, this control strategy has some limitations: First, although classical imaginary current construction is not necessary, the creation of an imaginary voltage component cannot be avoided. Therefore, an algorithm can be developed to reduce the time delay caused by imaginary voltage construction. Second, only the steady grid voltage condition was considered here, although abnormal operating states (e.g., grid voltage distortion) exist; thus, the control method should be optimized to make it applicable to such states.

6. Conclusions

A power control method is introduced for the single-phase CHB multilevel converter in this paper. A power-based dc-link voltage balance control module is also presented to eliminate the different dc-link voltages caused by the unbalanced loads.

The proposed power and voltage control method is designed in a virtual $\alpha\beta$ stationary reference frame without coordinate transformation or phase-locked loop. So, the complicated calculation issue can be avoided. What is more, conventional imaginary current construction is not necessary. Problems like time delay can also be avoided. The inner loop current calculation is simplified compared with the conventional dq control scheme. Stability of the proposed control scheme can be guaranteed through the analysis based on small-signal model.

Simulation and experimental results were presented to verify the effectiveness of the proposed control method. In the steady state, the proposed method can obtain the sinusoidal grid current and unity power factor under unbalanced load conditions. Upon comparing the dynamic response of the presented control strategy with that of the dq control scheme, the conducted experiments indicate that the salient feature of the proposed scheme is as follows: the proposed scheme maintains a fast dynamic response advantage over the conventional dq control method. This approach has been shown to be useful for the single-phase CHB multilevel converter system. The proposed control scheme can also be utilized with other multilevel converter systems.

Author Contributions: The individual contribution of each co-author with regards to the reported research and writing of the paper is as follows. D.Y. conceived the idea, L.Y. carried out the experiments and analyzed the data, and all authors wrote the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

CHB	Cascaded H-bridge
PWM	Pulse Width Modulation
DPC	Direct Power Control
DCC	Direct Current Control
P-DPC	Predictive DPC
PLL	Phase-Locked Loop
DSP	Digital Signal Processor
MPC	Model-Predictive Control
SOGI	Second-Order Generalized Integrator
PI	Proportional-Integral
PR	Proportional-plus-Resonant
CPS-PWM	Carrier, Phase-Shifted PWM
THD	Total Harmonic Distortion

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