energies

MDPI

Article

A Modified Step-Up DC-DC Flyback Converter with Active Snubber for Improved Efficiency

Cristian Pesce [1,*], Javier Riedemann [2], Ruben Pena [3], Werner Jara [2], Camilo Maury [1] and Rodrigo Villalobos [1]

[1] Department of Electrical Engineering, Universidad de La Frontera, Temuco 4811230, Chile; c.maury01@ufromail.cl (C.M.); rodrigo.villalobos@ufrontera.cl (R.V.)
[2] Department of Electrical Engineering, Pontificia Universidad Católica de Valparaíso, Valparaíso 2362804, Chile; javier.riedemann@pucv.cl (J.R.); werner.jara@pucv.cl (W.J.)
[3] Department of Electrical Engineering, Universidad de Concepción, Concepción 4030000, Chile; rupena@udec.cl
* Correspondence: cristian.pesce@ufrontera.cl

Received: 10 April 2019; Accepted: 28 May 2019; Published: 30 May 2019

Abstract: The research on DC-DC power converters has been a matter of interest for years since this type of converter can be used in a wide range of applications. The main research is focused on increasing the converter voltage gain while obtaining a good efficiency and reliability. Among the different DC-DC converters, the flyback topology is well-known and widely used. In this paper, a novel high efficiency modified step-up DC-DC flyback converter is presented. The converter is based on a *N*-stages flyback converter with parallel connected inputs and series-connected outputs. The use of a single main diode and output capacitor reduces the number of passive elements and allows for a more economical implementation compared with interleaved flyback topologies. High efficiency is obtained by including an active snubber circuit, which returns the energy stored in the leakage inductance of the flyback transformers back to the input power supply. A 4.7 kW laboratory prototype is implemented considering four flyback stages with an input voltage of 96 V and an output voltage of 590 V, obtaining an efficiency of 95%. The converter operates in discontinuous current mode then facilitating the output voltage controller design. Experimental results are presented and discussed.

Keywords: DC-DC power converters; DC power supply; snubber

1. Introduction

The flyback converter topology is a well-known and widely-used DC-DC power converter whose applications cover a broad spectrum including DC motor drives [1,2], switching power supplies [3,4], photovoltaic generation [5,6], electric cars [7,8] and fuel cell-based generation systems [9,10], among others [11,12]. For the standard flyback converter topology [13], different modifications have been proposed in the literature. In reference [14] a converter consisting of the integration of basic zeta and flyback converter topologies is presented. This zeta-flyback converter combines the main features of both topologies such as low output voltage and current ripple of the zeta converter with the galvanic isolation provided by the flyback converter configuration. In reference [8], a topology based on a bidirectional flyback converter is proposed. The converter is capable of handling multiple power sources and is intended to manage the energy stored in the batteries of a hybrid vehicle.

Another type of configuration extensively presented in the technical literature consists of splitting a full converter into several standard flyback cells, each managing a part of the converter overall power. These modular converters can be classified into four architectures depending on the connection form of the individual cells, namely input-parallel output-parallel (IPOP), input-parallel output-series (IPOS),

input-series output-parallel (ISOP), and input-series output-series (ISOS). Figure 1 shows schemes of the mentioned architectures.

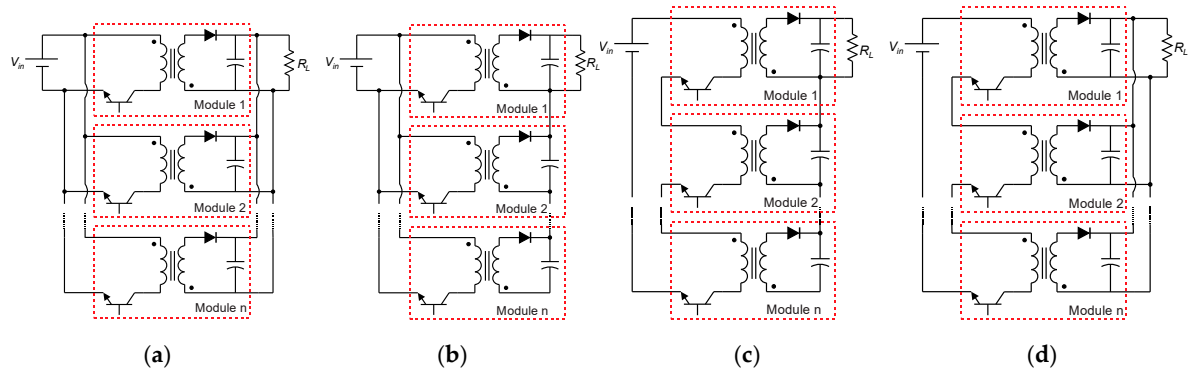

Figure 1. Architectures of modular flyback converters: (**a**) IPOP, (**b**) IPOS, (**c**) ISOS, (**d**) ISOP.

In general, these modular converters are known as flyback interleaved [15–19] and have become the most widely used circuit configuration arisen from the basic flyback topology. Their goal is to increase the effective output switching frequency and to reduce the peak-to-peak voltage ripple.

However, most of the interleaved topologies consider a full standard flyback converter as a basic module; therefore, in a converter built with N cells, the number of every circuit element will be multiplied by N. This will considerably increase the cost and volume of the modular converter compared to the standard topology. Moreover, as the interleaving requires to shift the triggering pulses of the power switches, the control system must produce N independent transistors gate pulses, then increasing the complexity of the control scheme.

On the other hand, in reference [20] a novel N-stages flyback converter with parallel inputs and series outputs is presented. The main feature of this converter is that it considers the series connection of the secondary winding transformers instead of connecting in series the output capacitors of the individual stages, as in the interleaved ISOP topology. Therefore, only one output diode and capacitor are necessary. Furthermore, this converter does not require shifting the transistors triggering pulses, and because of this, the control circuit should produce only one gate pulse for all the power switches, reducing its complexity.

Nevertheless, a drawback of the flyback converter is within the transformer leakage inductances. As the transformers' secondary windings should manage the overall output current, and the converter must allow or block the current circulation in a short period of time, there could be high voltage peaks in the transformer (Ldi/dt voltages due to leakage inductance). To reduce this effect, a passive snubber network could be used to suppress the voltage transients dissipating the associated energy as heat in a resistor (RCD snubber circuit).

Another type of snubber network uses an auxiliary switch connected in series with a capacitor. This configuration allows to reduce the voltage peaks while the energy stored in the capacitor can be returned to the power supply, thus increasing the operating efficiency of the converter. In this work, a modified flyback converter based on the topology shown in reference [20] is presented. To reduce the voltage transient problems and increase the converter efficiency, active snubber networks are incorporated in every flyback converter transformer. Although simpler and cheaper circuits could be proposed instead of an active snubber (e.g., an auxiliary winding with a diode [21]), the advantage of the active snubber network is that the peak collector-emitter voltage of the switches can be controlled by adjusting the duty cycle of the snubber switch. On the other hand, when using passive snubber networks, the peak voltages in a semiconductor can be damped but this damping is not controllable. Moreover, with active snubbers the recovery of energy is greater than with passive snubbers and the converter efficiency increases [21].

In this sense, the inclusion of active snubber networks is highlighted as an important contribution of this article. The topology proposed is depicted in Figure 2.

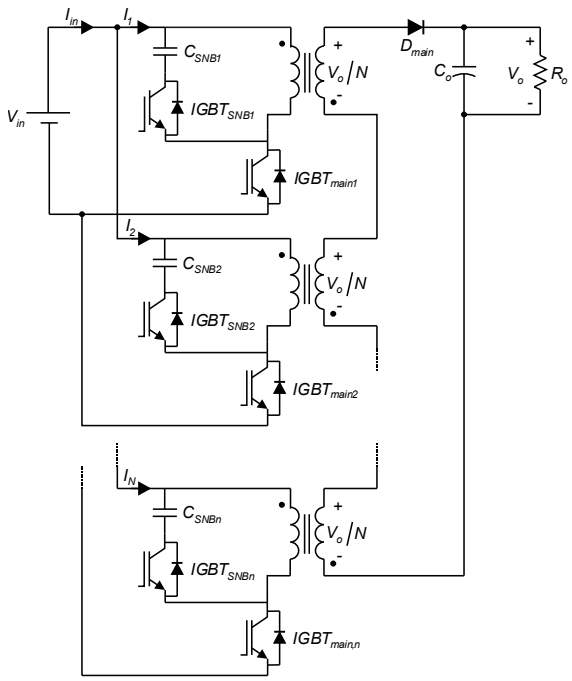

Figure 2. Proposed topology.

The different operation modes of the converter are presented and discussed. To validate the feasibility of the proposed converter, a laboratory prototype of 4.7 kW has been built and experimental results are presented considering a closed-loop voltage control scheme. Moreover, an efficiency analysis for the topology presented is carried out.

The paper is organized as follows. Section 2 describes the operating principle of the converter including voltage and current equations. Section 3 shows a mathematic derivation of the converter voltage transfer ratio. Section 4 describes the control scheme used for the proposed topology, Section 5 shows the experimental results obtained, and Section 6 presents a brief efficiency analysis of the converter. The conclusions of the work are stated in Section 7.

2. Operating Principle

The different operation modes of the proposed converter are analyzed under the following assumptions:

(1) The output voltage has negligible ripple.
(2) The coupled inductors (so called "flyback transformers") are identical and have unity turns ratio.
(3) The parameters of the flyback transformers are referred to the primary side.
(4) The windings resistances are neglected.
(5) The active snubber circuit returns the energy stored in the leakage inductance back to the supply.
(6) The power semiconductor devices are ideal.
(7) The converter operates in Discontinuous Conduction Mode (DCM).
(8) Main switches and snubber switches cannot be closed at the same time. D_1 is the duty cycle for the main switch, and D_2 is the duty cycle for the snubber switch.

2.1. Operating Mode 1 ($0 \leq t \leq t_{on}$)

In this mode, all the main switches are closed, then the same current circulates in every inductor primary coil and main transistor (Figure 3a). The input voltage is applied to the input magnetizing inductance of every transformer and their leakage inductances store the energy supplied by the source. The diode D_{main} is reverse-biased and the capacitor C_o discharges in the load resistor R_o the energy stored in the last period. It can be shown that the peak current in every main switch S_i with $i = 1 \ldots N$ is given by:

$$I_{N_{max}} = \frac{V_{in}\, D_1}{(L_m + L_l)\; f_s} \tag{1}$$

where V_{in} is the converter supply voltage, D_1 is the duty cycle of the main switches, L_m is the magnetizing inductance of each transformer, L_l is the leakage inductance, and f_s is the switching frequency of the converter. The voltage in the primary and secondary inductors are given by (2) and (3), respectively:

$$V_{p,N} = V_{in} \tag{2}$$

$$V_{s,N} = -\left(\frac{V_{in}}{a}\right) \tag{3}$$

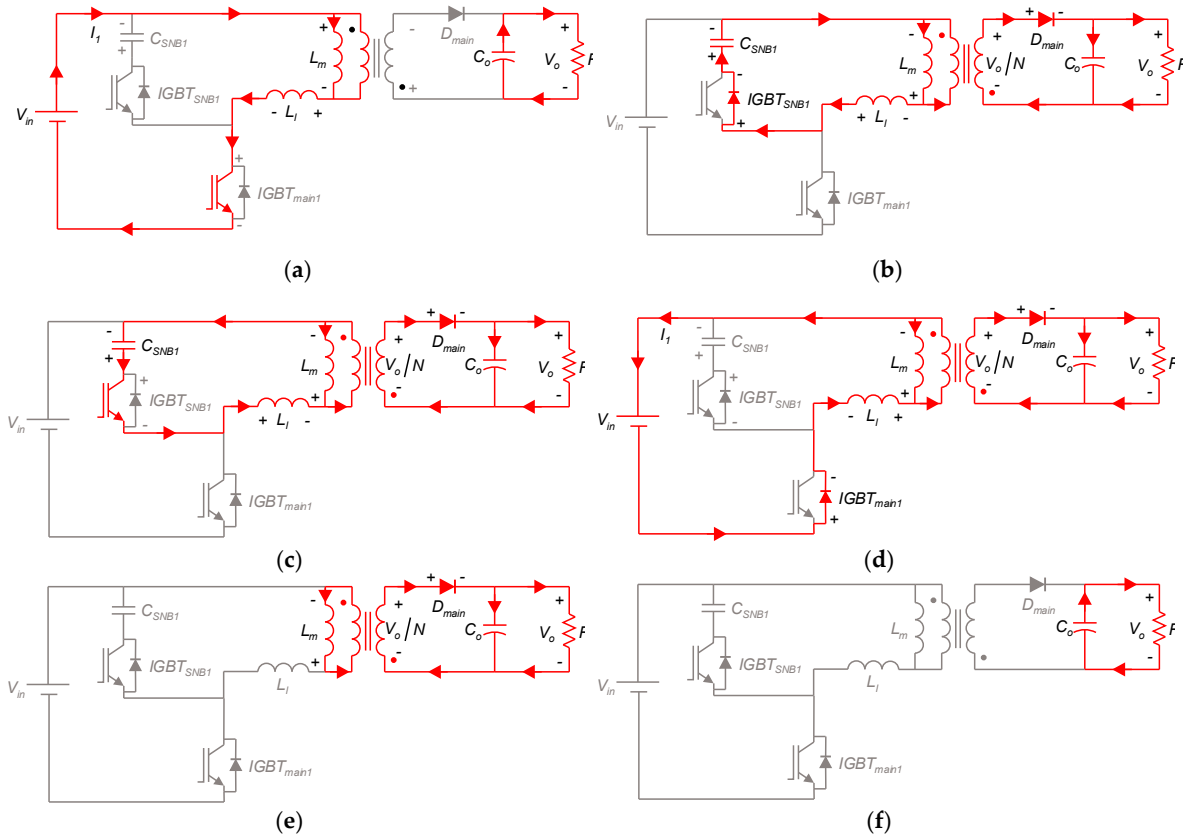

Figure 3. Equivalent circuits for each operating mode: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; (**f**) Mode 6.

The voltage in the main diode is:

$$V_{D_{main}} = -\left(N\frac{V_{in}}{a} + V_o\right) \tag{4}$$

with V_o being the converter output voltage, a is the transformers turns ratio, and N is the number of flyback transformers. The output current is:

$$I_o = \frac{V_o}{R_o} = -I_{C_o} \tag{5}$$

where I_{C_o} is the output capacitor current. On the other hand, the switches of every snubber circuit are opened. However, each snubber capacitor is charged with a voltage $V_{C_{snb}}(0)$ from the previous cycle. This voltage is determined by:

$$V_{C_{snb}}(0) = I_{N_{max}} L_l \frac{1}{\tan\left[\frac{D_2\ T_s}{2\sqrt{L_l\ C_{snb}}}\right]} + V_o \tag{6}$$

where T_s is the switching period, C_{snb} is the snubber capacitor, and $I_{N_{max}}$ is the maximum current in the main switch.

To obtain (6) it is necessary to define the current when the snubber is activated, which is defined by:

$$i_{snb}(t) = \frac{\left(V_o - V_{C_{snb}}(0)\right)}{L_l} \sqrt{L_l C_{snb}}\, \sin(\omega t) + I_{(0)} \cos(\omega t) \tag{7}$$

where $I_{(0)}$ is the initial current (from the previous cycle) and the frequency is $\omega = 1/\sqrt{L_l C_{snb}}$. Then, the voltage $V_{C_{snb}}(0)$ shown in (6) is given by evaluating (7) at $t = (D_2 T_s)/2$ considering that the current $i_{snb}\left(\frac{D_2 T_s}{2}\right) = 0$ and $I_{(0)} = I_{N_{max}}$ (see Figure 4).

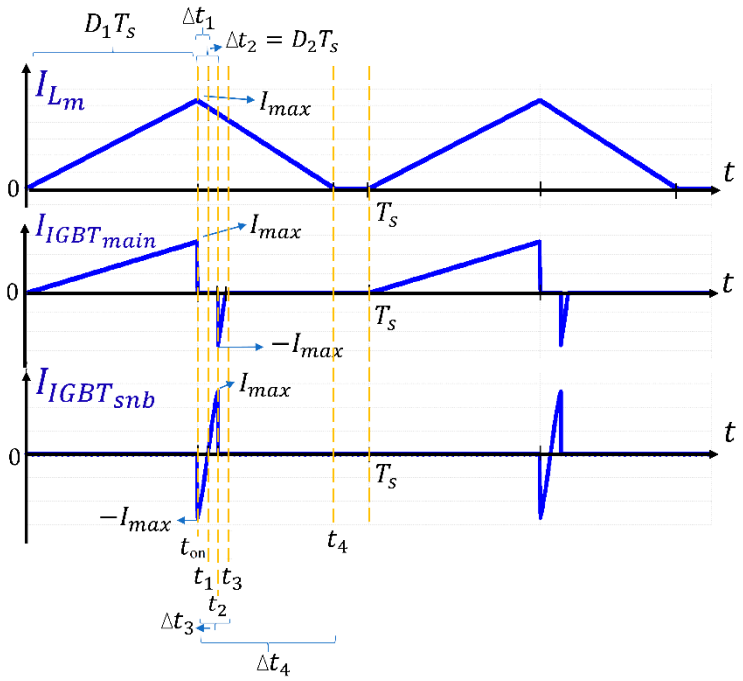

Figure 4. Theoretical waveforms of I_{L_m} (top), $I_{IGBT_{main}}$ (middle) and $I_{IGBT_{snubber}}$.

2.2. Operating Mode 2 ($t_{on} \leq t \leq t_1$)

In this mode, all the main switches are turned off and the snubbers diodes (in parallel with the snubber IGBTs) are conducting current (Figure 3b) from $t = t_{on}$ to $t = t_1$. However, although it will not conduct any current until $t = t_1$, the snubber IGBT is triggered at $t = t_{on}$. This is performed for

simplicity, since it would be very difficult to know precisely the instant $t = t_1$ as it depends on the leakage inductance (which is difficult to measure accurately).

The current in the magnetizing inductance L_m circulates through the primary winding and the leakage inductance (L_l). The current in the main diode is given by:

$$I_{D_{main}} = i_{L_m}(t) - I_{L_l} \tag{8}$$

The magnetizing inductance current i_{L_m} decreases linearly until the stored energy falls to zero in an instant t_{on}. The expression for the magnetizing inductance current is:

$$i_{L_m}(t) = \left(-\frac{I_{L_{m_{max}}} V_o}{V_{in} D_1 T_s} t + I_{L_{m_{max}}}\right) + I_{Ll} \tag{9}$$

The current in the leakage inductance i_{L_l} equals the current in the snubber capacitor and is given by:

$$i_{L_l}(t) = i_{C_{snb}}(t) = \frac{V_o - V_{C_{snb}}(0)}{L_l} \sqrt{L_l C_{snb}} \sin\left(\frac{1}{\sqrt{L_l C_{snb}}} t\right) + I_{L_{m_{max}}} \cos\left(\frac{1}{\sqrt{L_l C_{snb}}} t\right) \tag{10}$$

and the voltage in the leakage inductance (v_{L_l}) is defined by:

$$v_{L_l}(t) = L_l \frac{di_{C_{snb}}(t)}{dt} = V_o/N - V_{C_{snb}}(0) \cos\left(\frac{1}{\sqrt{L_l C_{snb}}} t\right) - I_{L_{m_{max}}} \frac{L_l}{\sqrt{L_l C_{snb}}} \sin\left(\frac{1}{\sqrt{L_l C_{snb}}} t\right) \tag{11}$$

In this state, the voltage in the magnetizing inductance is $V_{L_m} = -V_o$. Then, the snubber capacitor voltage is:

$$v_{C_{Snb}} = V_{L_l} + V_{L_m} \tag{12}$$

At $t = t_1$, the current in the snubber capacitor decreases to zero.

2.3. Operating Mode 3 ($t_1 \leq t \leq t_2$)

In this operating mode (Figure 3c), all the snubbers IGBT switches are turned on. There is an energy balance between the snubber capacitor and the leakage inductance. Therefore, the energy delivered by the inductor to the snubber capacitor is returned to the leakage inductance. Hence, the current in the leakage inductance at $t = t_2$ is maximum of value $I_{L_{m_{max}}}$ but with the opposite direction to operating mode 2.

At the end of this period, the output capacitor recovers its initial charge of operating mode 1. The blocking voltage of the main switches is given by:

$$V_{CE_{off}} = V_{L_l}(t) + V_{L_m} - V_{in} = V_{L_l}(t) - V_o - V_{in} \tag{13}$$

and the current in the main diode is defined by:

$$i_{D_{main}}(t) = i_{L_m}(t) - i_{Ll}(t) \tag{14}$$

2.4. Operating Mode 4 ($t_2 \leq t \leq t_3$)

This operating mode is shown in Figure 3d. In this case, all the main IGBT switches are turned off but their anti-parallel diodes are conducting current. Therefore, the energy stored in the leakage inductance is delivered back to the input voltage source. The leakage inductance current decreases to zero. The main diode current begins to decrease and the voltage in the leakage inductance (V_{L_l}) is defined by:

$$V_{L_l} = V_{in} + V_o/N \tag{15}$$

The instant $t = t_3$ corresponds to the time where the leakage inductance current falls to zero, and can be calculated with:

$$t_3 - t_2 = V_{L_l} \cdot \frac{D_2 T_s}{2\,(V_{in} + V_o/N)} \tag{16}$$

where V_{L_l} is the average voltage in the leakage inductance.

2.5. Operating Mode 5 ($t_3 \leq t \leq t_4$)

In this operating mode (shown in Figure 3e), the energy stored in the leakage inductance is totally delivered to the input supply. The main diode current decreases to zero at $t = t_4$. The period where the main diode is conducting can be calculated as:

$$\Delta t_4 = \frac{V_{in} D_1 T_s}{V_o/N} \tag{17}$$

From $t = t_{on}$ to $t = t_4$, the output capacitor C_o receives the energy stored in the magnetizing inductance, then its charge increases as well as its voltage.

2.6. Operating Mode 6 ($t_4 \leq t \leq T_s$)

In this mode, all the switches are turned-off, as shown in Figure 3f. The energy stored in the output capacitor is delivered to the load resistor. The current in the output capacitor is given by:

$$i_{C_o}(t) = -I_o \tag{18}$$

where the output current I_o is imposed by the load.

The main waveforms obtained from the different operating modes are summarized in Figures 4 and 5. In Figure 4, the magnetizing current I_{L_m} of the transformers (top), the main switches current $I_{IGBT_{main}}$ (middle) and the snubber switches current $I_{IGBT_{snb}}$ (bottom) are shown. Figure 5 shows the voltage in the main switches $V_{CE_{main}}$ (top), the current $I_{D_{main}}$ in the main diode (middle), and the gating signals of main and snubber IGBT switches (bottom).

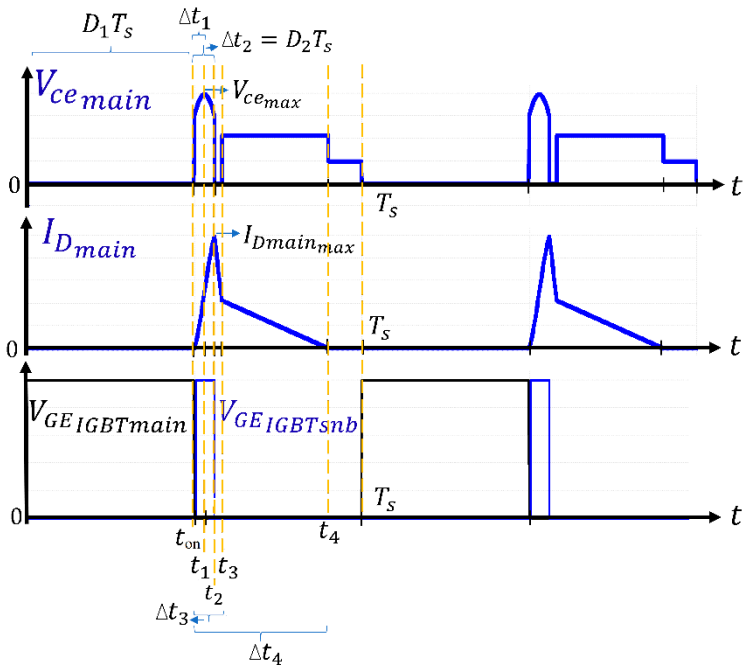

Figure 5. Theoretical waveforms of $V_{CE_{main}}$ (top), $I_{D_{main}}$ (middle) and gating pulses of main and snubber IGBT switches (bottom).

3. Voltage Transfer Ratio

The voltage gain of the power converter is derived assuming equal input and output power $P_{in} = V_{in}I_{in} = V_oI_o = P_o = V_o^2/R_o$ (no losses in the converter). The average current of the snubber switches (in a period) is zero (see Figure 4), and the average current of the main IGBT switches is defined by:

$$I_{IGBT_{main}} = \frac{I_{N_{max}}D_1}{2} - \frac{I_{N_{max}}^2 L_l}{2\,T_s(V_{in} + (V_o/N))} \tag{19}$$

On the other hand, since the expression for $I_{N_{max}}$ is given in (1), the total input average current $I_{in} = NI_{IGBT_{main}}$ is:

$$I_{in} = N\frac{V_{in}D_1^2T_s}{2(L_m + L_l)}\left(1 - \frac{L_l\,V_{in}}{(L_m + L_l)(V_{in} + (V_o/N))}\right) \tag{20}$$

Considering the above equations, it is obtained:

$$\frac{V_o^2}{V_{in}^2} = \frac{ND_1^2R_o\left((L_m + L_l)\left(1 + \frac{V_o}{V_{in}N}\right) - L_l\right)}{2f_s\,(L_m + L_l)^2\left(\frac{V_o}{V_{in}N} + 1\right)} \tag{21}$$

Defining $X = V_o/V_{in}$, Equation (21) can be rewritten as:

$$X^3 + \frac{1}{N}X^2 - \frac{D^2R_oN}{2f_s\,(L_m + L_l)}X - \frac{D^2N^2R_o}{2f_s(L_m + L_l)}\left(\frac{L_l}{L_m + L_l} + 1\right) = 0 \tag{22}$$

This third-order equation is solved using the Cardano method [22], and for the parameters considered in this work, it has two real negative roots and one positive real root. Since the converter does not invert the polarity of the input voltage, only the positive root is valid, therefore the voltage transfer ratio (VTR) of the topology proposed is:

$$\frac{V_o}{V_{in}} = D_1\sqrt{\frac{N\,R_o}{2\,f_s\,(L_m + L_l)}} \tag{23}$$

4. Control Scheme

A voltage control scheme is proposed for the topology. A Proportional+Integral (PI) controller processes the difference between a reference voltage and the output measured voltage. The output of the PI controller is intended to be the duty cycle of the converter D_1 and is limited in the range 0–0.65. The upper limit, so-called critical duty cycle ($D_{1crit} = 0.65$), is set to avoid operation in Continuous Conduction Mode (CCM) as DCM operation offers advantages in term of control simplicity and converter efficiency [17]. For DCM operation, $D_1T_s + \Delta t_4 < T_s$ must be fulfilled. To operate with a safety margin, it is stated that $D_1T_s + \Delta t_4 \leq 0.96T_s$ to ensure DCM. The main duty cycle D_1 is defined by (23) and is dependent on the load (which is constant in this case). On the other hand, Δt_4 is defined by (17) then the critical duty cycle $D_{1_{crit}}$ is given by:

$$D_{1crit} \leq 0.96 - \frac{V_{in}D_1}{(V_o/N)} \tag{24}$$

For controller design purposes, the transfer function $G(s)$ considered (output voltage/main switch duty cycle) is given by:

$$G(s) = \frac{V_o(s)}{D_1(s)} = V_{in}\sqrt{\frac{NR_o}{2(L_m + L_l)f_s}}\left(\frac{1 + sR_{se}C_o}{sR_oC_o + 1}\right) \tag{25}$$

where R_{se} is the series-equivalent resistance of the output capacitor. As can be noted in (25), the transfer function depends on the load resistor R_o. As the output voltage and current are measured, the value of the load resistor can be easily calculated by $R_o = V_o/I_o$. Then the controller parameters are calculated (in a real-time Digital Signal Processor) every sampling period to adapt to the load. For controller design purposes, the closed-loop transfer function of the system is obtained:

$$M(s) = \frac{\frac{A\omega_c\left(K_p s + K_i\right)}{R_o C_o}}{s^3 + s^2\frac{(1+R_oC_o\omega_c)}{R_oC_o} + s\frac{\left(\omega_c + A\omega_c K_p\right)}{R_oC_o} + \frac{A\omega_c K_i}{R_oC_o}} \tag{26}$$

where $A = V_{in}\sqrt{\frac{R_oN}{2f_s(L_m+L_l)}}\cdot(1 + R_{se}C_o)$ (R_{se} is the equivalent series resistor of the output capacitor).

The parameters K_p and K_i of the controller are then calculated by equating the denominator of (26) to the characteristic third-order polynomial $(p(s) = (s+\alpha_o)\left(s^2 + 2\xi\omega_n s + \omega_n^2\right))$. Therefore, the proportional and integral constants of the controller are:

$$K_p = \frac{\left(\frac{2\xi\omega_n\ (1+R_oC_o\omega_c)}{R_o\ C_o} - (2\xi\omega_n)^2 + \omega_n^2\right)R_oC_o - \omega_c}{V_{in}\ \omega_c\ \sqrt{\frac{R_oN}{2\ f_s\ (L_m+L_l)}}(1 + R_{se}C_o)} \tag{27}$$

$$K_i = \frac{\omega_n^2\ R_oC_o\left(\frac{(1+R_oC_o\omega_c)}{R_oC_o} - 2\xi\omega_n\right)}{V_{in}\omega_c\sqrt{\frac{R_oN}{2f_s(L_m+L_l)}}\cdot(1 + R_{se}C_o)} \tag{28}$$

where ω_n is the natural frequency of the control loop, ξ is the damping ratio, and ω_c is the cut-off frequency of a low-pass filter used in the measurement of V_o. The values considered in this work are $\omega_n = 2100$ [rad/s], $\xi = 0.8$ and $\omega_c = 2000\pi$ [rad/s]. In Figure 6, a diagram of the control scheme is shown.

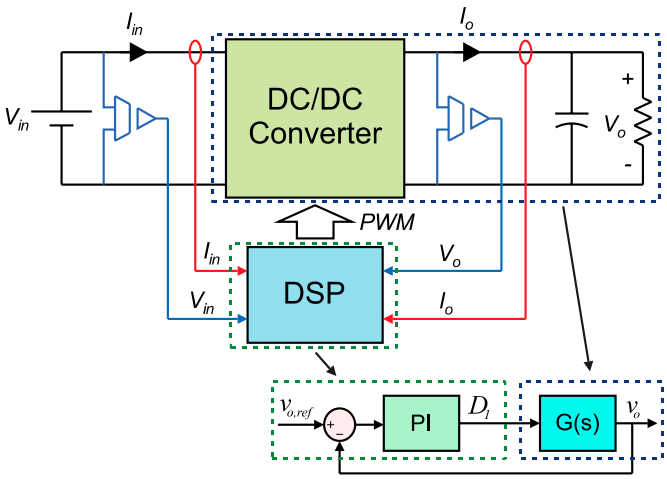

Figure 6. Control scheme.

The Bode diagrams of the system in the open-loop and closed-loop are shown in Figures 7 and 8, respectively:

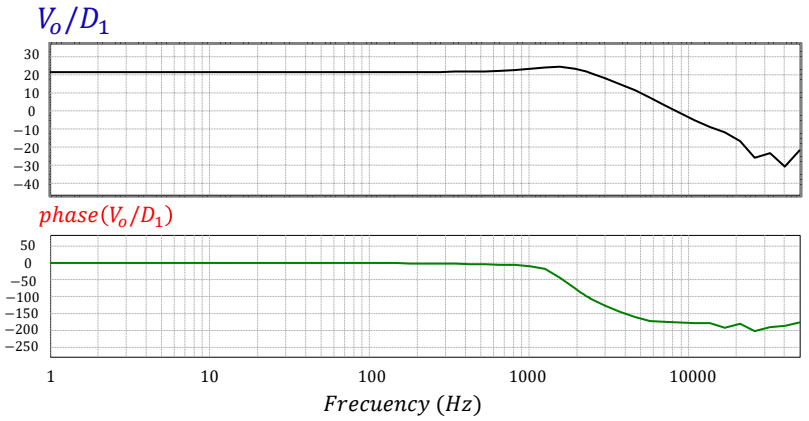

Figure 7. Open-loop Bode diagram of the system.

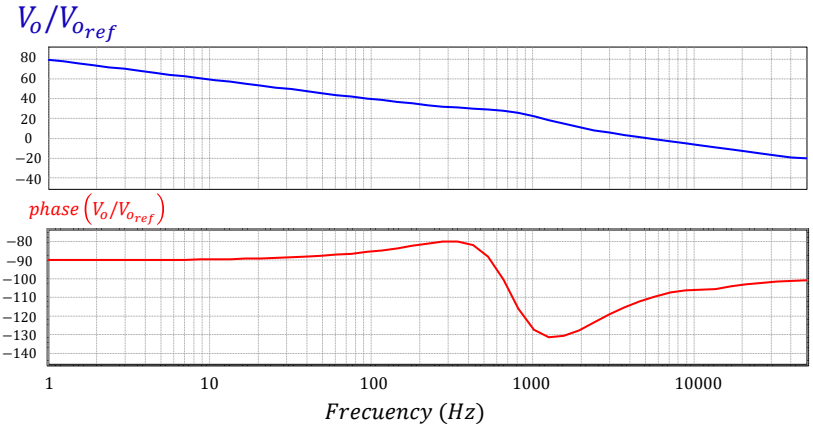

Figure 8. Closed-loop Bode diagram of the system.

From Figure 7, it can be noted that the phase margin in the open-loop operation of the converter is zero as well as the gain margin; then the system is instable and requires a feedback controller. When the voltage controller is included, the Bode diagram (Figure 8) shows a phase margin of about 70° and an infinity gain margin (as the phase (Figure 8 bottom) never crosses the −180° line), then confirming the stability of the closed-loop system.

5. Experimental Results

To validate the proposed topology, a laboratory prototype with four flyback modules has been built. In this work, the maximum output power extracted from the converter is 4.7 kW; however, the prototype has been constructed considering a larger power for future research. Each transformer is rated at 5 kW, aiming to obtain 20 kW with four flyback stages. The semiconductors were also selected considering an output power of 20 kW. The full power converter is aimed to be used in electrical drives applications such as: electric traction using DC machines and DC supply for three-phase inverters driving AC machines among others. The experimental system is shown in Figure 9.

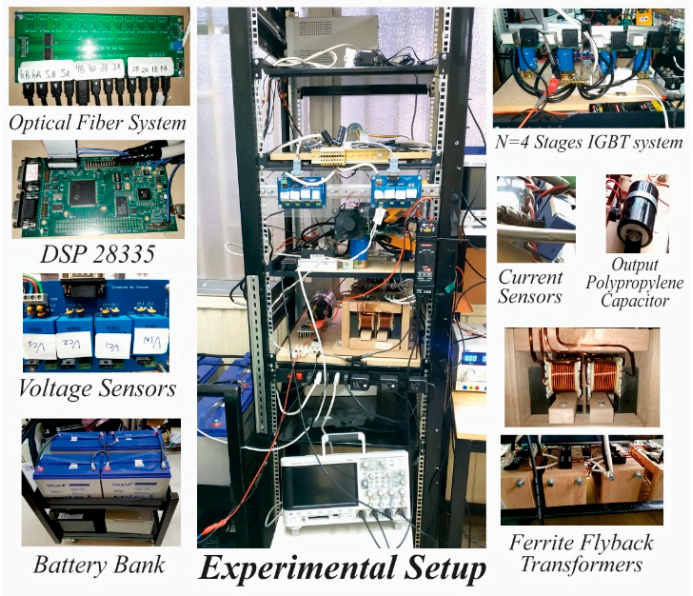

Figure 9. Experimental laboratory prototype.

The input supply consists of eight series-connected 12V AGM batteries. The main switches are IGBTs model STGW35HF60WD and the model of the main diode is STTH9012TV; the snubber switch is an IGBT model NGTB50N120FL2WG.

The flyback converter transformers (Figure 10) are built with a two-column ferrite core having a 3 [mm] airgap. The transformers parameters (referred to the primary side) are $R_p = 4[\text{m}\Omega]$ (primary coil resistance), $L_l = 10[\mu\text{H}]$ (leakage inductance), $L_m = 170[\mu\text{H}]$ (magnetizing inductance) and $R_c \approx 300[\text{k}\Omega]$ (resistance of core losses); the turns ratio is $24:24 \rightarrow a = 1$.

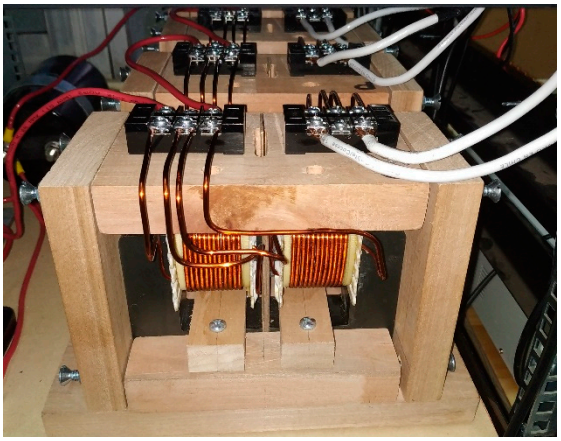

Figure 10. Ferrite core flyback transformers.

The output capacitor is a polypropylene-type for low equivalent series-resistance ($R_{se} = 2$ mΩ). The control system was implemented with a Texas DSP28335 microprocessor, and the gating signals are transmitted to the converter via optical fiber. The experimental parameters are shown in Table 1.

The converter has been tested at rated power in steady state operation. The time period for the experimental waveforms of Figures 11–14 is 200 μs. Figure 11 shows the currents of the main IGBT switches. The negative peaks are due to the regeneration process where energy is returned to the DC supply.

Table 1. Experimental parameters.

Variable	Description	Value	Variable	Description	Value
V_{in}	Input voltage	96 V	C_o	Output capacitor	320 µF
V_o	Rated output voltage	590 V	f_s	Switching frequency	10 kHz
L_m	Magnetizing inductance	170 µH	N	Number of stages	4
n_P/n_S	Transformers turns ratio	1	P_o	Rated power	4700 W

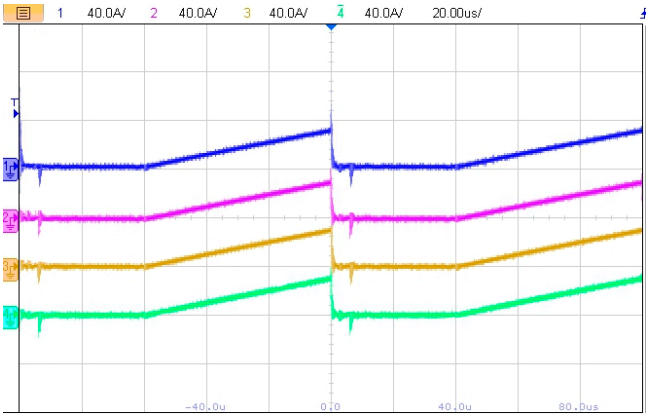

Figure 11. Main IGBT switches currents (Scale: 40 A/div).

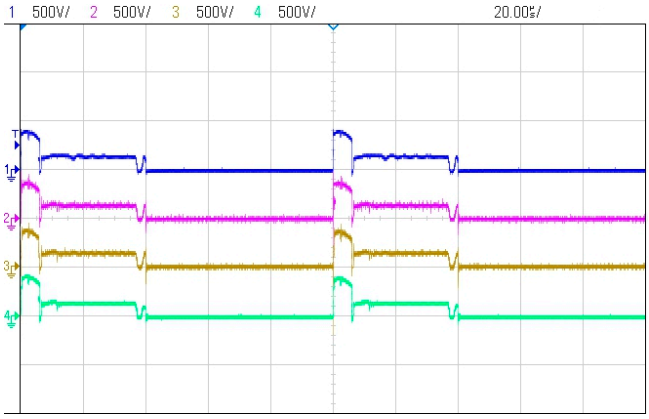

Figure 12. Main IGBT switches collector-emitter voltages (Scale: 500 V/div).

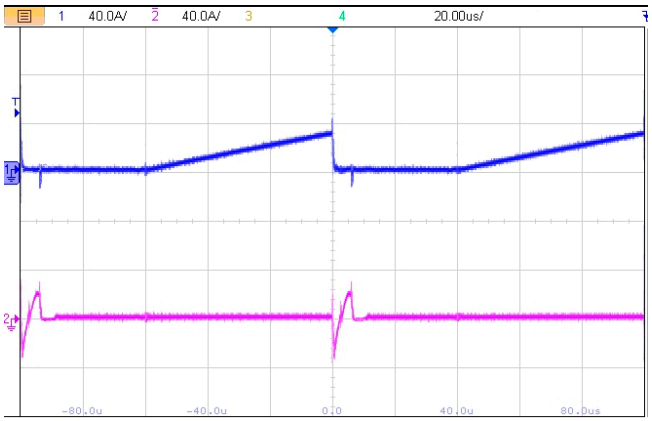

Figure 13. Main switch current (blue–Scale: 40 A/div) and snubber current (purple–Scale: 40 A/div).

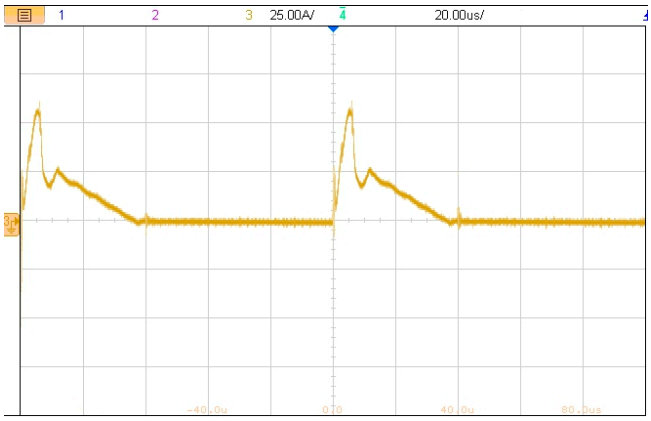

Figure 14. Main diode current (Scale: 25 A/div).

Figure 12 shows the collector-emitter voltage of the main switches while Figure 13 shows the current of a main switch (blue) along with the current of the corresponding snubber switch (purple). Figure 14 shows the main diode current. The similarity between the experimental waveforms (Figures 11–14) and the theoretical waveforms (Figures 4 and 5) is evident.

To study the performance of the voltage control scheme, reference voltage changes and load impacts have been tested. Figure 15 shows the output voltage (purple) where a gradual increment in the reference voltage from 0 to 500 V is applied at the beginning. Then, when steady state is achieved, a step change in the reference voltage from 500 V to 590 V is carried out. Figure 15 (blue) shows the output current which presents the same waveform as the output voltage due to the resistive characteristic of the load. This current finally stabilizes to ~8 A for an output power of 4720 W.

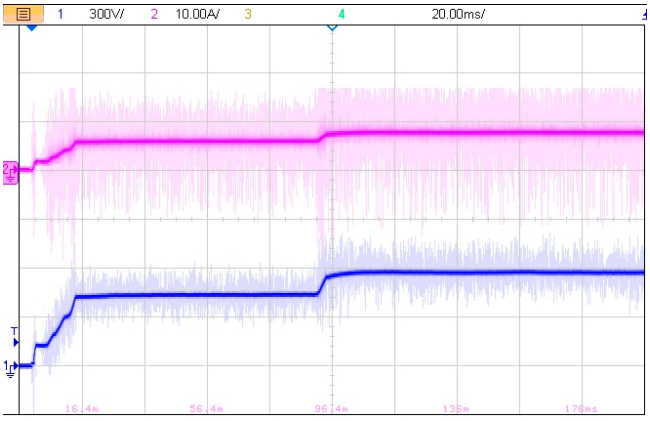

Figure 15. Output voltage V_o (purple-Scale: 300 V/div) and output current I_o (blue-Scale: 10 A/div). Total time: 200 ms.

Finally, Figure 16 shows the output voltage (blue) and current (purple) during a load impact. The voltage reference is set to 590 V and a load impact that increases the current from 1 A to 6 A is applied. The output voltage is stabilized in about 3 ms. Both Figures 15 and 16 verify the effectiveness of the voltage control strategy implemented.

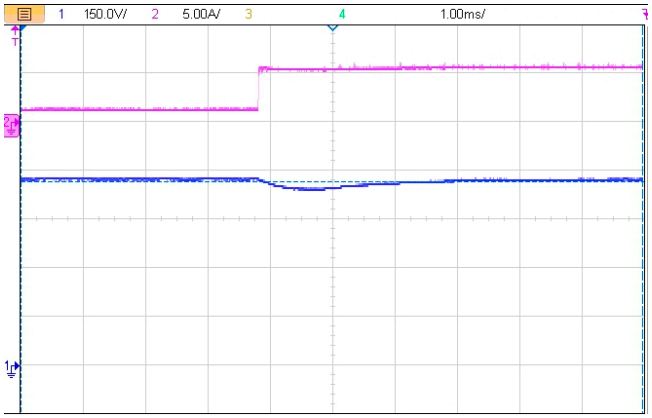

Figure 16. Output voltage V_o (blue-Scale: 150 V/div) and output current I_o (purple-Scale: 5 A/div). Total time: 10 ms.

A summary of values obtained from experimental and simulation results is shown in Table 2.

Table 2. Summary of experimental and simulation values obtained.

Power Device		Experimental Results	Simulation Results
Main Switch			
- Positive peak current	:	32 A	31.5 A
- Negative peak current	:	16 A	15.3 A
- Maximum collector-emitter voltage	:	400 V	398.5 A
Snubber Switch			
- Positive peak current	:	24 A	23.3 A
- Negative peak current	:	32 A	31.3 A
Main Diode			
- Maximum current	:	57 A	56.2 A

6. Efficiency Analysis

An efficiency study, based on experimental tests of the converter built, has been carried out. A first analysis was performed in open-loop operation of the converter, with constant load and different duty cycles. The results obtained are shown in Table 2, where P_o and P_{in} are the output and input power, respectively. The efficiency is calculated as $\eta = 100 \cdot \left(\frac{P_{out}}{P_{in}}\right)$. It is observed that the highest efficiencies are achieved by operating the converter with duty cycles in the range 0.6–0.7. For duty cycles over 0.7, the efficiency decreases due to higher conduction losses in the switches and passive elements. It is worth mentioning that, as stated in Section 4, for duty cycles over 0.65, the converter operates in CCM mode. This is done only for efficiency evaluation purposes.

A second analysis was carried out with closed-loop control operation. The output voltage V_o is kept constant and maximum (590 V), and the output current is variable (variable load). The results are presented in Table 3. A maximum efficiency of 95% is obtained for an output power of 4.77 kW. Figure 17 summarizes the results shown in Tables 3 and 4.

Table 3. Efficiency results with constant load.

D_1	V_o [V]	I_{in} [A]	P_o [W]	P_{in} [W]	η [%]
0.45	382	23.67	2091	2273	91.99
0.5	425	29.07	2581	2790	92.50
0.6	510	41.28	3717	3963	93.79
0.65	553	48.10	4362	4616	94.49
0.69	589	53.96	4916	5182	94.86
0.72	612	58.94	5353	5719	93.60
0.75	637	64.57	5808	6474	89.71

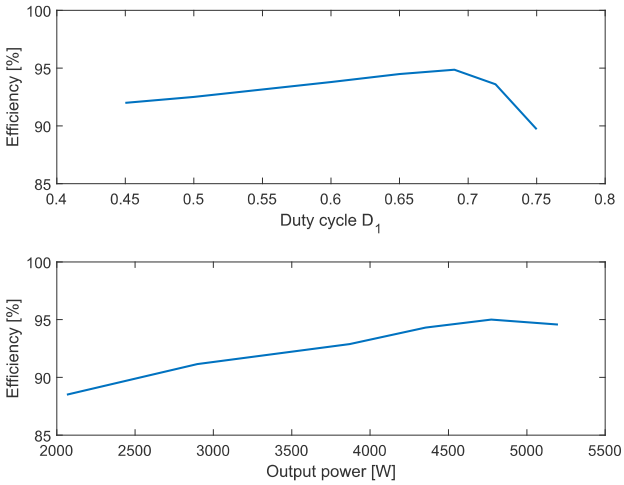

Figure 17. Efficiency of the converter for constant load/variable duty cycle (top) and constant duty cycle/variable load (bottom).

Table 4. Efficiency results with constant output voltage.

I_o [A]	I_{in} [A]	P_o [W]	P_{in} [W]	η [%]
3.5	24.3	2065	2333	88.51
4.91	33.1	2897	3178	91.15
6.56	43.41	3870	4167	92.88
7.38	48.09	4354	4616	94.32
8.09	52.34	4773	5024	95.00
8.81	57.25	5198	5496	94.57

7. Conclusions

In this paper, a DC-DC converter topology based on a standard flyback converter has been proposed. The converter proposed is modular and considers a reduced number of power devices compared to flyback interleaved topologies.

Active snubber circuits are included to avoid excessive voltages in the main power switches. The different operating modes of the converter are described and mathematically analyzed.

A simple voltage control scheme is proposed considering discontinuous conduction mode operation, obtaining a good performance under load impacts and voltage variations.

A laboratory prototype has been built and experimental results were obtained, showing a good performance of the converter and its control scheme in steady state operation as well as during transient operation.

The proposed converter results are competitive in terms of cost and efficiency with respect to the flyback interleaved topologies. The obtained full load efficiency of the proposed converter is 95% resulting in an attractive alternative for nowadays industrial requirements.

Author Contributions: Conceptualization, C.P. and R.P.; Methodology, C.M. and W.J.; software, C.P.; validation, C.P., C.M. and R.V.; formal analysis, R.P. and J.R.; investigation, C.P.; resources, C.P., R.P. and R.V.; data curation, C.M. and W.J.; writing—original draft preparation, J.R. and C.P.; writing—review and editing, J.R.

Funding: This research was funded by UNIVERSIDAD DE LA FRONTERA, project DIUFRO number DI19-0013 and by the Chilean Council of Scientific and Technological Research under projects CONICYT/FONDEF/ID17I10421, CONICYT/FONDECYT/11180092 and CONICYT/FONDAP/15110019.

Acknowledgments: In this section you can acknowledge any support given which is not covered by the author contribution or funding sections. This may include administrative and technical support, or donations in kind (e.g., materials used for experiments).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Singh, S.; Singh, B. Improved power quality flyback converter fed PMBLDCM drive. In Proceedings of the 5th IEEE India International Conference on Power Electronics (IICPE), Delhi, India, 6–8 December 2012; pp. 1–5.
2. Babadi, A.; Pour, A.; Amjadifard, R. Improved source-end current Power Quality performance of a BLDC motor drive using a novel DC-DC converter. In Proceedings of the Iranian Conference on Electrical Engineering (ICEE), Tehran, Iran, 2–4 May 2017; pp. 1360–1365.
3. Rizzoli, G.; Zarri, L.; Wang, J.; Shen, Z.; Burgos, R.; Boroyevich, D. Design of a two-switch flyback power supply using 1.7 kV SiC devices for ultra-wide input-voltage range applications. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016; pp. 1–5.
4. Perrin, R.; Quentin, N.; Allard, B.; Martin, C.; Ali, M. High-Temperature GaN Active-Clamp Flyback Converter with Resonant Operation Mode. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 1077–1085. [CrossRef]
5. Mazumdar, P.; Enjeti, P.; Balog, R. Analysis and Design of Smart PV Modules. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *2*, 451–459. [CrossRef]
6. Lodh, T.; Pragallapati, N.; Agarwal, V. Novel Control Scheme for an Interleaved Flyback Converter Based Solar PV Microinverter to Achieve High Efficiency. *IEEE Trans. Ind. Appl.* **2018**, *54*, 3473–3482. [CrossRef]
7. Kashif, M. Bidirectional flyback DC-DC converter for hybrid electric vehicle: Utility, working and PSPICE computer model. In Proceedings of the Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, Hyderabad, India, 5–7 December 2012; pp. 61–66.
8. Bhattacharya, T.; Giri, V.; Mathew, K.; Umanand, L. Multiphase Bidirectional Flyback Converter Topology for Hybrid Electric Vehicles. *IEEE Trans. Ind. Electron.* **2009**, *56*, 78–84. [CrossRef]
9. Shen, C.; Chiu, P. Buck-boost-flyback integrated converter with single switch to achieve high voltage gain for PV or fuel-cell applications. *IET Power Electron.* **2016**, *9*, 1228–1237. [CrossRef]
10. Yigeng, H.; Yu, W. A robust flyback converter based on high order sliding mode control for fuel cell. In Proceedings of the 40th Annual Conference of the IEEE Industrial Electronics Society (IECON), Dallas, TX, USA, 29 October–1 November 2014; pp. 3936–3940.
11. Cheng, H.; Chang, Y.; Chang, C.; Hsieh, S.; Cheng, C. A Novel High-Power-Factor AC/DC LED Driver with Dual Flyback Converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *7*, 555–564. [CrossRef]
12. Tseng, S.-Y.; Huang, P.-J.; Wu, D.-H. Power Factor Corrector with Bridgeless Flyback Converter for DC Loads Applications. *Energies* **2018**, *11*, 3096. [CrossRef]
13. Kazimierczuk, M. *Pulse-width Modulated DC–DC Power Converters*, 1st ed.; John Wiley & Sons: Hoboken, NJ, USA, 2008.
14. Lin, B.; Hsieh, F. Soft-Switching Zeta–Flyback Converter with a Buck–Boost Type of Active Clamp. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2813–2822.
15. Pagliosa, M.; Faust, R.; Lazzarin, T.; Barbi, I. Input-series and output-series connected modular single-switch flyback converter operating in the discontinuous conduction mode. *IET Power Electron.* **2016**, *9*, 1962–1970. [CrossRef]

16. Rezaei, M.; Lee, K.; Huang, A. A High-Efficiency Flyback Micro-inverter With a New Adaptive Snubber for Photovoltaic Applications. *IEEE Trans. Power Electron.* **2016**, *31*, 318–327. [CrossRef]
17. Tamyurek, B.; Kirimer, B. An interleaved high-power flyback inverter for photovoltaic applications. *IEEE Trans. Power Electron.* **2015**, *30*, 3228–3241. [CrossRef]
18. Zumel, P.; García, O.; Oliver, J.; Cobos, J. Differential-Mode EMI Reduction in a Multiphase DCM Flyback Converter. *IEEE Trans. Power Electron.* **2009**, *24*, 2013–2020. [CrossRef]
19. Dong, M.; Tian, X.; Li, L.; Song, D.; Wang, L.; Zhao, M. Model-Based Current Sharing Approach for DCM Interleaved Flyback Micro-Inverter. *Energies* **2018**, *11*, 1685. [CrossRef]
20. Pesce, C.; Blasco Gimenez, R.; Riedemann, J.; Andrade, I.; Pena, R. A DC-DC Converter Based on Modified Flyback Converter Topology. *IEEE Lat. Am. Trans.* **2016**, *14*, 3949–3956. [CrossRef]
21. Alganidi, A. A Comparison between Different Snubbers for Flyback Converters. Master's Thesis, The University of Western Ontario, London, ON, Canada, 2017. Available online: https://ir.lib.uwo.ca/etd/5153 (accessed on 22 May 2019).
22. Kreyszig, E. *Advanced Engineering Mathematics*, 10th ed.; John Wiley & Sons: Hoboken, NJ, USA, 2010.