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Self-Sustained Turn-Off Oscillation of SiC MOSFETs: Origin, Instability Analysis, and Prevention

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Abstract: This paper presents a comprehensive investigation on the self-sustained oscillation of silicon carbide (SiC) MOSFETs. At first, based on the double pulse switching test, it is identified that the self-sustained oscillation of SiC MOSFETs can be triggered by two distinct test conditions. To investigate the oscillatory criteria of the two types of self-sustained oscillation, a small-signal ac model is introduced to obtain the transfer function of the oscillatory system. The instability of the oscillation is thereby determined by the two conjugate pole pairs of the transfer function. By analyzing the damping ratios of the two pole pairs, the parametric sensitivity of various circuit and device's parameters on the two types of self-sustained oscillation are obtained. The analyses reveal the oscillatory criteria of the self-sustained oscillation for SiC MOSFETs. Based on the oscillatory criteria, necessary methods are proposed to prevent the oscillation. The proposed oscillation suppression methods are validated by the experiment at the end of the paper.

Keywords: SiC MOSFET; turn-off oscillation; small-signal model; self-sustained oscillation; instability

1. Introduction

The recent development of fast switching converters require the power switches to operate at a high switching frequency. With high breakdown voltages and fast switching speeds, the silicon carbide (SiC) MOSFETs seem to be a perfect choice for high frequency converter applications [1,2]. However, the utilization of SiC MOSFETs can also introduce some unwanted side-effects to the converter. Under certain test conditions, the self-sustained oscillation can occur in the turn-off transient of SiC MOSFETs [3,4]. As shown in Figure 1, during the oscillatory transient, the gate voltage rings back above the threshold voltage V_{th}, which gives rise to the the unexpected turn-on of the MOSFET. The unexpected turn-on draws additional energy from the power supply, which compensates the energy dissipated by parasitic resistance in the test circuit. As a results, the oscillation can maintain self-sustenance during the oscillatory transient. Since the self-sustained oscillation causes severe electromagnetic interference (EMI) problems and can completely disrupt the converter operation in the worst case, great care needs to be taken to suppress this kind of oscillation. To achieve this, it is necessary to investigate the underling mechanism and oscillatory criteria of the self-sustained oscillation for SiC MOSFET.

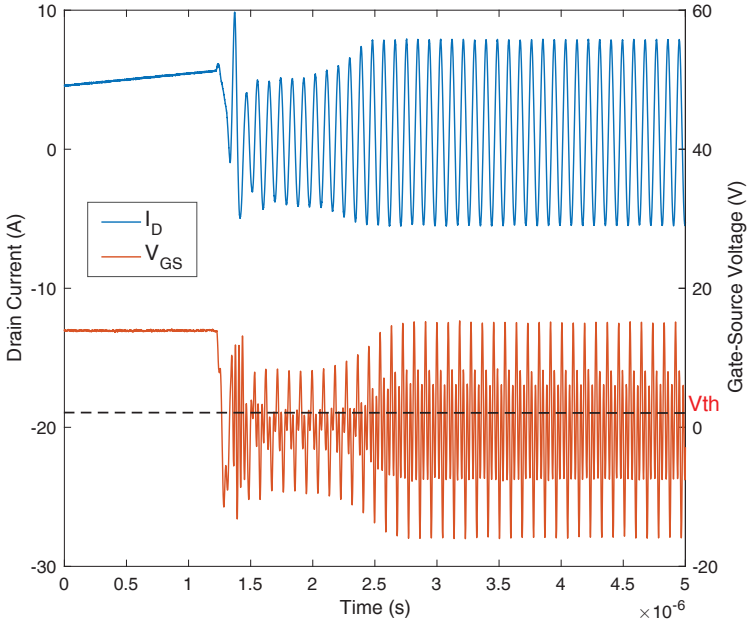


Figure 1. The self-sustained oscillation waveforms of gate voltage V_{GS} and drain current I_D.

Unfortunately, only few works have been presented to study the self-sustained oscillation phenomenon [3–7]. In [3,4]; with the common source inductance L_S being neglected, the papers studied the sensitivity of various circuit and device's parameters on the self-sustained oscillation of SiC MOSFETs by casting the switching circuit as the negative conductance oscillator. However, the studies have a few drawbacks. Firstly, since the voltage drop V_{Ls} on the inductance L_S can directly affect the gate voltage, the L_S has a very significant impact on the turn-off oscillation. The research proposed in Reference [8] demonstrated that the V_{Ls} can disrupt the positive feedback process of the oscillatory system and damp the turn-off oscillation. Under certain test conditions, the V_{Ls} can also induce the unexpected turn-on of the low-side MOSFET [7,9] and can excite the self-sustained oscillation during the turn-off transient [7]. Therefore, the inductance L_S should not be neglected in the analysis. Secondly, the potential mechanisms which can lead to the occurrence of the self-sustained oscillation were not revealed in the papers. Last but not least, some circuit parameters, like the stray inductances of gate and power loop, have a very strong impact on the turn-off oscillation [8]. Unfortunately, the parametric sensitivity of these parameters on the self-sustained oscillation were not investigated in the paper. In Reference [5], the self-sustained oscillation phenomenon of a GaN transistor in a half-bridge circuit was studied. The self-sustained oscillation was induced by the unique reverse conduction characteristics of the GaN devices. However, since the SiC MOSFETs do not have such kind of reverse conduction characteristics, the self-sustained oscillation presented in this research does not occur on the SiC MOSFETs. In Reference [6], with the gate-drain capacitance neglected, a simplified SiC MOSFET equivalent model was utilized to derive the transfer function of the oscillatory system. Based on the transfer function, an analytical oscillatory criteria of the self-sustained oscillation was obtained. Since the gate-drain capacitance was neglected, the oscillatory criteria was not very accurate and could only provide an approximate estimation on the occurrence condition of self-sustained oscillation for SiC MOSFETs. In Reference [7], the self-sustained oscillation induced by the the common source inductance L_S was reported for CoolMOS. The research revealed the critical impact of the common source inductance L_S on the self-sustained oscillation. However, the mechanism of the self-sustained oscillation was still unknown. The criteria of the oscillation was also not studied in the paper.

This paper presents a comprehensive study on the potential mechanisms and oscillatory criteria of the self-sustained oscillation for SiC MOSFETs. In Section 2, two distinct test conditions which can trigger the self-sustained oscillation are identified by the double-pulse test. The related positive feedback mechanisms which originate the oscillation are clarified based on the test results. With the

common source inductance L_S included, a small-signal ac model is proposed in Section 3 to obtain the transfer function of the oscillatory system. By studying the two pole pairs of the criteria transfer function, the impact of various circuit and device's parameters on the self-sustained oscillation is analyzed in Section 4. The theoretical analyses reveal the oscillatory criteria of the self-sustained oscillation. The methods to suppress the self-sustained oscillation are thereby obtained in Section 5 according to the oscillatory criteria. In Section 6, the experiment is performed to validate the proposed oscillation suppression methods.

2. Experimental Identification

The double pulse test is utilized to identify the characteristics of the self-sustained oscillation on the 1200V/25A SiC MOSFET with part number LSIC1MO120E0080. A SiC Schottky diode with part number C3D10170H is utilized as the freewheel diode. Figure 2 shows the schematic circuit for the double pulse test. In the circuit, the load inductor $L_0 = 350$ μH is utilized to maintain a nearly constant current throughout the switching cycle. A function generator is controlled by the computer to send pulse signal to the gate driver, which generates the gate voltage V_{gg} to drive the low-side transistor T_1. V_{DC} is the high voltage power supply, which is connected to a capacitor bank C_{DC}. R_G is the total gate resistance, which is the sum of internal and external gate resistances. L_S is the common source inductance. L_G is the gate loop inductance. L_C is the power loop inductance.

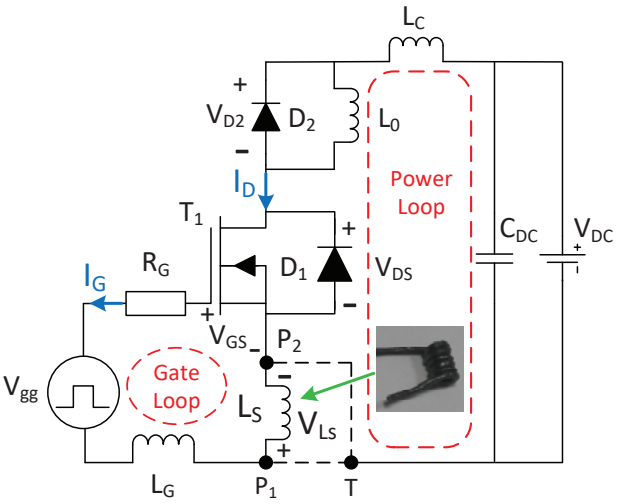


Figure 2. The schematic circuit of the double-pulse test.

The test results show that the self-sustained oscillation can be excited under two different test conditions depending on the common source inductance L_S. The two types of oscillation are driven by two distinct mechanisms, which are presented as follows.

2.1. The Type I Self-Sustained Oscillation

With the node T connected to node P_1, the type I oscillation can be triggered when an air-core coil with an inductance in tens of nanohenries is utilized as L_S, as shown in Figure 2. The type I oscillation waveforms of the I_D and V_{DS} are presented in Figure 3.

To investigate the oscillation mechanism, one oscillation cycle of V_{GS}, V_{Ls}, and I_D is divided into phases A and B, as shown in Figure 4. During the oscillatory transient, the voltage V_{Ls} on the inductance L_S has the same phase as the V_{GS}, as shown in Figure 4. This demonstrates that the V_{Ls} acts as the ac voltage source to drive the gate-source voltage V_{GS}. When the V_{GS} surpasses the threshold voltage V_{th} in the beginning of phase A, the MOSFET T_1 turns on, which give rise to the electron current injection in the drift region. At this time, the depletion region shrinks. Due to the displacement current induced by the discharging of the drain-source depletion capacitance, the I_D

still increases reversely in the initiation of this phase. However, since the electron current counteracts the displacement current, the dI_D/dt starts to increase and transfers its polarity from negative to positive in the end. With the positive dI_D/dt, a negative V_{Ls} is generated, which drives the V_{GS} to drop. When the V_{GS} rings down below the V_{th} in the initiation of phase B, the T_1 turns off. Accordingly, the depletion region starts to expand. Due to the displacement current generated by the charging of drain-source depletion capacitance, I_D still increases. However, with the great reduction of the MOS electron current, the dI_D/dt starts to decline and eventually transfers back into a negative value. Accordingly, a positive V_{Ls} is obtained, which drives the V_{GS} to increase. When the V_{GS} achieves V_{th} at the end of the phase, phase A starts again. As a result, the two phases occur alternatively and the self-sustained oscillation is generated.

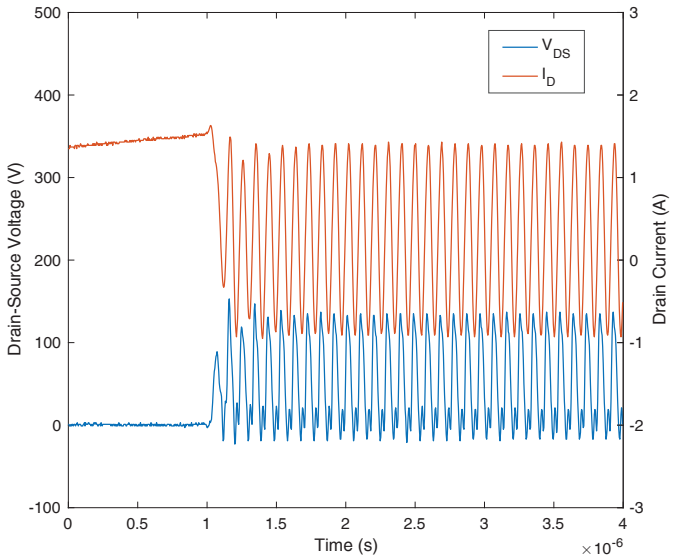


Figure 3. The type I oscillation waveforms of the I_D and V_{DS} (Polarities defined in Figure 2).

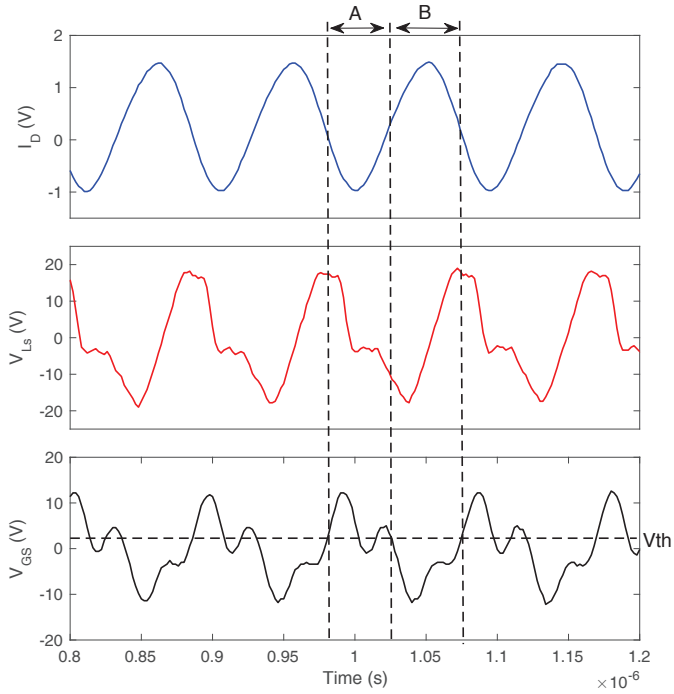


Figure 4. The type I oscillation waveforms of I_D, V_{GS}, and V_{Ls} (Polarities defined in Figure 2).

It should be noted that an underling positive feedback mechanism is included in the oscillation process presented above. During the oscillatory transient, the oscillation of I_D generates the ac voltage V_{Ls}. V_{Ls} drives the MOSFET T_1 turn-ons and -offs, which in return supports the oscillation of I_D. This gives rise to the positive feedback process, which excites the type I oscillation. This common source inductance-induced oscillation phenomenon has been reported previously in Reference [7] for the CoolMOS.

2.2. Type II Self-Sustained Oscillation

When the node T is connected to node P_2 (the end of the source lead), the common source inductance is minimized. In this scenario, the type II self-sustained oscillation can be triggered, as shown in the Figure 5.

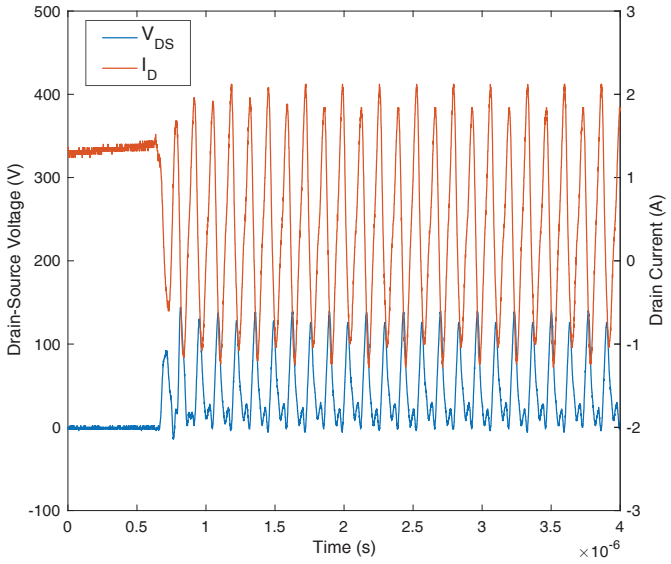


Figure 5. The type II oscillation waveforms of I_D and V_{DS}.

To investigate the mechanism of the type II oscillation, one oscillation cycle is divided into phases A and B, as shown in Figure 6. In phase A, the V_{GS} drops down below the threshold voltage V_{th}, MOSFET T_1 turns off. At this time, the drift layer is depleted, which gives rise to a very small gate-drain capacitance C_{GD}. Since the high impedance of C_{GD} isolates the gate loop from being affected by the power loop resonance, V_{GS} and I_G oscillate due to the resonance of gate loop RLC circuit. When V_{GS} rings back above the V_{th}, phase B starts. In this phase, the MOSFET turns on. The shrinking of the depletion region gives rise to the great increase of the C_{GD}. With a much larger C_{GD}, the power loop resonance can disturb the gate loop resonance. As shown in Figure 6, the gate current I_G increases abruptly a short time after the initiation of phase B and quickly becomes in phase with the drain current I_D. This demonstrates that a portion of the drain current I_D serves as a feedback current flows though the gate drive circuit, as shown Figure 7. This current feedback action induces the abrupt increase of I_G. With a high dI_G/dt, a positive voltage V_{Lg} is generated on the L_G, as shown Figure 7. The positive V_{Lg} can drive the gate voltage V_{GS}, which in turn supports the drain current I_D. As a result, a positive feedback process is generated. The type II oscillation thereby occurs. The self-sustained oscillation studied in Reference [3,4] is a type II oscillation.

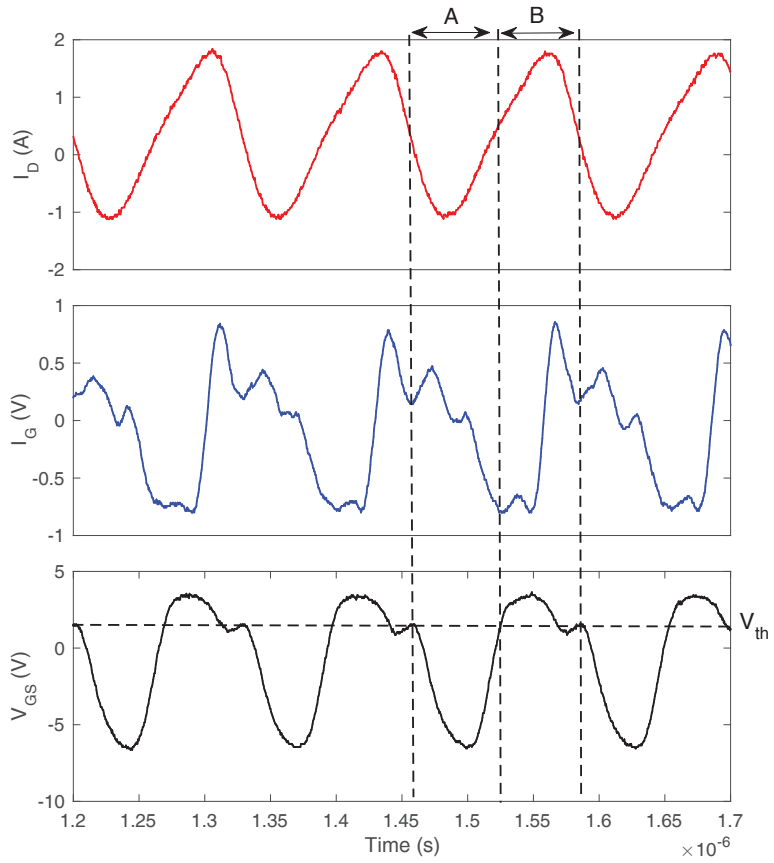


Figure 6. The type II oscillation waveforms of I_D, V_{GS}, and I_G (Polarities defined in Figure 2).

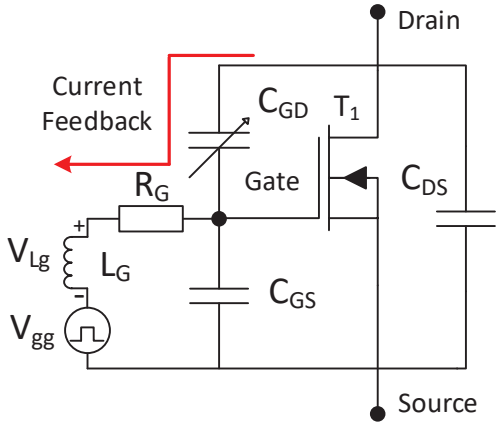


Figure 7. The current feedback process in phase B.

2.3. The Impact of dI_D/dt on Self-Sustained Oscillation

Traditionally, the turn-off oscillation is supposed to be triggered by the high dI_D/dt [8,10]. In this test, it is found that dI_D/dt does not have a significant influence on the two types of self-sustained oscillation. As shown in Figure 8, the self-sustained oscillation can be excited when the load current I_L reduces from 10 A to 1.5 A. In fact, since dI_D/dt does not have a significant impact on the positive feedback mechanisms which trigger the two types of self-sustained oscillation, the occurrence of self-sustained oscillation do not rely on the high dI_D/dt.

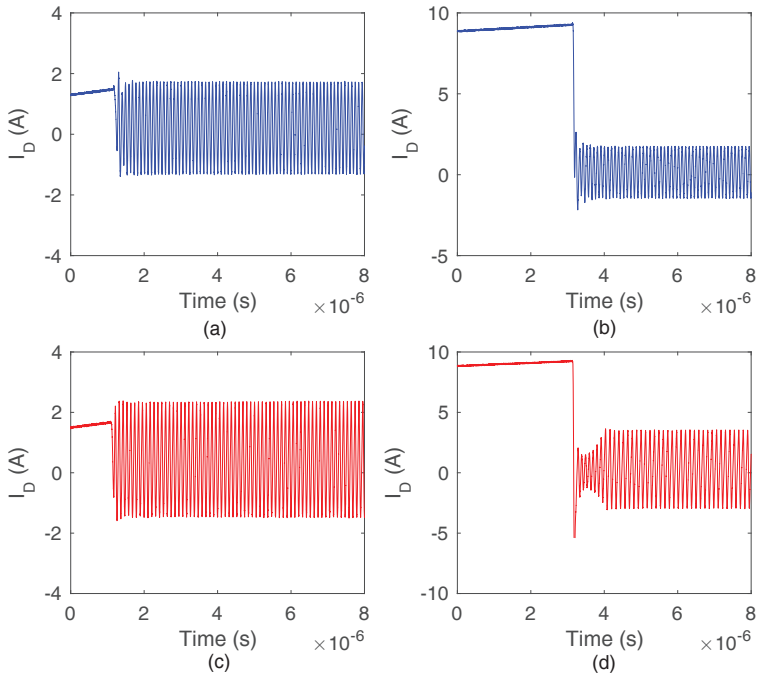


Figure 8. The oscillation waveforms of I_D for type I (blue) and type II (red) self-sustained oscillation. (**a**) $I_L = 1.5$ A. (**b**) $I_L = 10$ A. (**c**) $I_L = 1.5$ A. (**d**) $I_L = 10$ A.

3. The Small-Signal Ac Model

The instability of the self-sustained oscillation can be studied by the small-signal ac model [3–5]. To obtain the model, the test circuit presented in Figure 2 is transferred to the equivalent small-signal circuit shown in Figure 9a. In the circuit, the capacitor C_{DC} and voltage supply V_{DC} are short circuited. The diode D_2 is replaced as the diode junction capacitance C_{D2}. The transistor T_1 is replaced by its equivalent small-signal model. In the model, C_{GD}, C_{DS}, and C_{GS} are the gate-drain, drain-source, and gate-source capacitances, respectively. R_C is the stray resistance of power loop. $i_D = g_m \cdot v_{GS}$ is a small-signal MOS current. v_{GS} is the small-signal gate-source voltage. g_m is the transconductance of the power MOSFET. In order to simplify the equivalent circuit, the star connection at the node B is transformed to delta connection with the following equations:

$$\begin{aligned} X_{GD} &= (X_G X_S + X_S X_D + X_G X_D)/X_S \\ X_{GS} &= (X_G X_S + X_S X_D + X_G X_D)/X_D \\ X_{DS} &= (X_G X_S + X_S X_D + X_G X_D)/X_G \end{aligned} \tag{1}$$

where $X_G = R_G + sL_G$, $X_D = R_C + sL_C + 1/sC_{D2}$, $X_S = sL_S$. As a result, the initial small-signal model presented in Figure 9b can be obtained. In the model, $Z_{GD} = 1/sC_{GD}$, $Z_{GS} = 1/sC_{GS}$ and $Z_{DS} = 1/sC_{DS}$. After further simplification, the final small-signal model can be drawn, as shown in Figure 9c. In the model, $X'_{GD} = X_{GD}//Z_{GD}$, $X'_{GS} = X_{GS}//Z_{GS}$ and $X'_{DS} = X_{DS}//Z_{DS}$.

During the oscillatory transient, the small-signal model can be considered as single-input single-output feedback system [5,11]. Figure 10 shows the block diagram of the feedback system. The $i_D(s)$ and $v_{GS}(s)$ are the Laplace transform of the $i_D(t)$ and $v_{GS}(t)$, respectively. $v_{ggd}(s)$ is the Laplace transform of the pulse form small-signal disturbance voltage $v_{ggd}(t)$, which is introduced by the gate drive voltage. It should be noticed that the gate drive voltage is constant when the gate drive switches off. Therefore, the small-signal $v_{ggd}(t)$ becomes zero after the initial voltage disturbance.

The instability of the oscillation is thereby determined by the feedback system, not the input signal $v_{ggd}(t)$. The open-loop gain $G(s)$ of the feedback system is as follows:

$$G(s) = \frac{i_D(s)}{v_{GS}(s)} = g_m \tag{2}$$

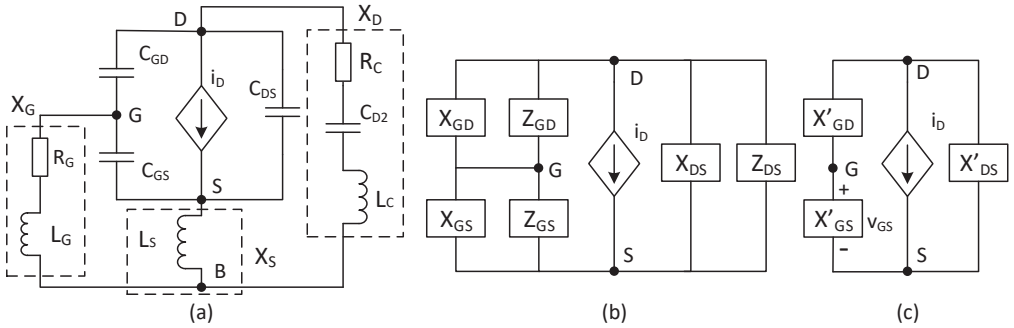


Figure 9. An equivalent ac model of the test circuit. (**a**) An equivalent small-signal circuit. (**b**) The initial small-signal model. (**c**) A simplified small-signal model.

The feedback factor $H(s)$ can be calculated by the small-signal model presented in Figure 9c:

$$H(s) = \frac{v_{GS}(s)}{i_D(s)} = -\frac{X'_{GS}X'_{DS}}{X'_{DS} + X'_{GD} + X'_{GS}} \tag{3}$$

The closed-loop transfer function $T(s)$ of the feedback system thereby can be obtained:

$$\begin{aligned} T(s) &= \frac{G(s)}{1 - G(s)H(s)} \\ &= \frac{g_m(a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0)}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \end{aligned} \tag{4}$$

where the coefficients a_i and b_i (i = 0,1,2,3,4) are presented in the Appendix A.

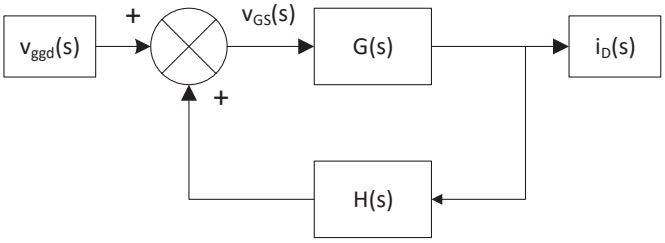


Figure 10. The positive feedback block diagram.

It should be noted that the dc operating point utilized for the small-signal model is included implicitly in Equation (4). In the model, the capacitances C_{GD} and C_{DS} are the functions of the drain-source voltage V_{DS}. The capacitance C_{D2} is the function of diode voltage V_{D2}. The transconductance g_m is the function of gate-source voltage V_{GS}. During the turn-off transient, the central tendency of the V_{DS} oscillation is the voltage supply V_{DC}. The capacitances C_{GD} and C_{DS} are thereby linearized at $V_{DS} = V_{DC}$. During the oscillatory transient, the freewheel diode D_2 is forward biased when the MOSFET T_1 turns off. When the T_1 turns on, the diode D_2 has to support the reverse voltage. Therefore, the diode voltage V_{D2} oscillates around the zero volts, as shown in Figure 11. The C_{D2} is thereby linearized at $V_{D2} = 0$ V. Following the approach presented in Reference [3,11], the transconductance g_m is linearized at $V_{GS} = V_{th}$.

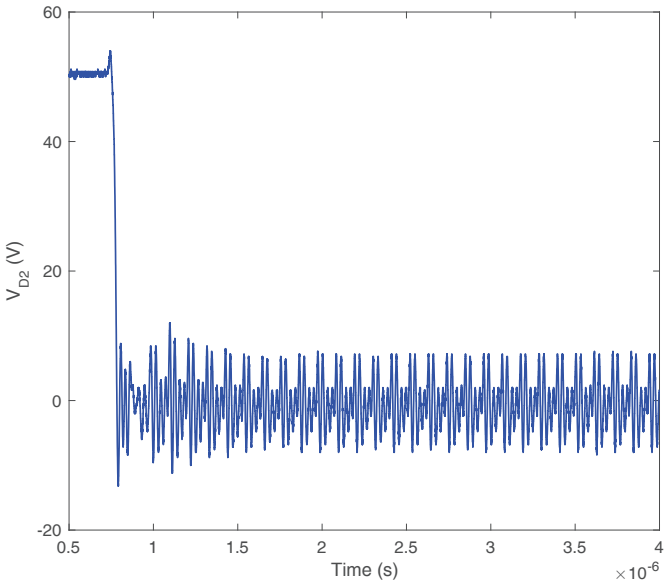
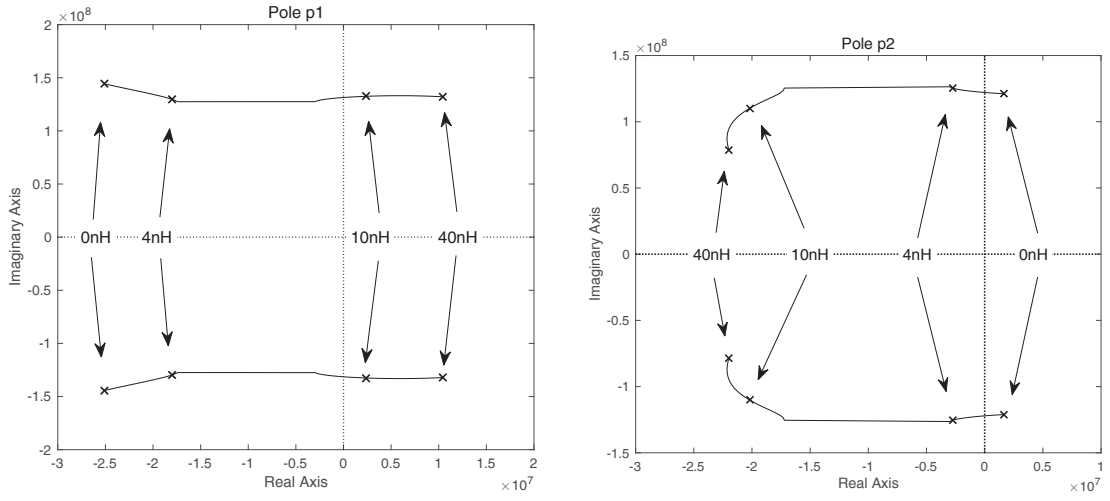


Figure 11. The waveforms of V_{D2} (Polarities defined in Figure 2).

4. The Analysis of Parametric Sensitivity on the Oscillatory Instability

The stability of the oscillation can be studied by the poles of the closed-loop transfer function $T(s)$. According to the well-known Routh–Hurwitz stability criterion, the oscillation is instable when the system has a conjugate pole pair at the right half of the s-plane [12]. In this case, the transfer function $T(s)$ has two complex conjugate pole pairs. The loci of the two pole pairs p_1 and p_2 when the common source inductance L_S varies from 0 nH to 40 nH are presented Figure 12. The specific parameters utilized in the analysis are presented in Table 1.



(**a**) Pole pair p_1. (**b**) Pole pair p_2.

Figure 12. The loci of the conjugate pole pairs when L_S varies from 0 nH to 40 nH.

As shown in Figure 12, when L_S becomes larger, the pole pair p_1 moves toward the right and reaches the right half of the s-plane when L_S is larger than 10 nH. Since the type I self-sustained oscillation is induced by the large L_S, the occurrence of the type I oscillation is thereby determined by p_1. The pole pair p_2, on the other hand, moves toward the opposite direction as p_1 and lies on the right half of the s-plane when L_S is eliminated. This shows that pole pair p_2 dictates the occurrence of type II oscillation. The parametric sensitivity of the two types of self-sustained oscillation can be studied by the two pole pairs.

Table 1. Parameters for the theocratical study.

Parameter	Value	Parameter	Value
g_m	0.1 S	L_G	25 nH
R_C	0.2 Ω	C_{D2}	824 pF
R_G	1 Ω	C_{GS}	2000 pF
L_S	0–40 nH	C_{GD}	25 pF
L_C	400 nH	C_{DS}	170 pF

In this section, the instability of the oscillation is described by the damping ratio $\zeta = \sigma/(\sigma^2 + \omega^2)$, where $-\sigma$ and ω are the real and imaginary parts of the poles. When $\zeta < 0$, the oscillation is instable and the smaller the ζ is, the faster the oscillation amplitude increases. When $\zeta > 0$, the oscillation is stable. With a larger ζ, the oscillation will return to equilibrium faster. $\zeta = 0$ indicates a constant-amplitude oscillation.

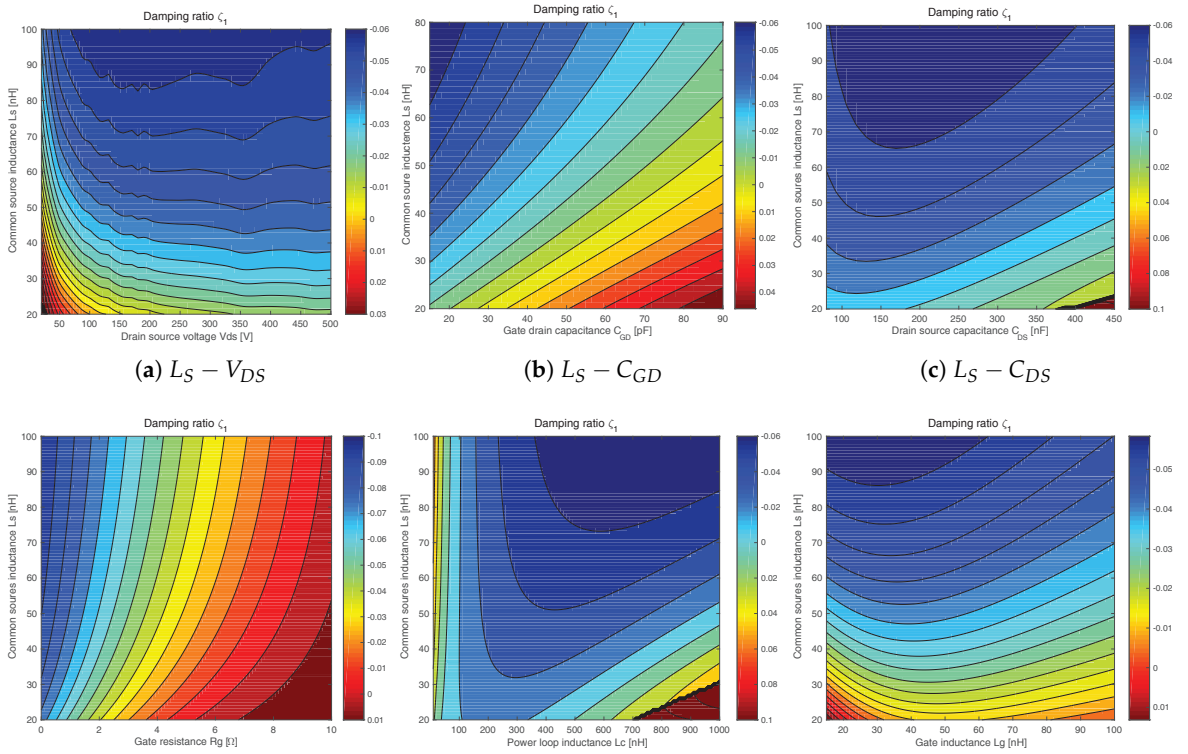
4.1. The Parametric Sensitivity of the Type I Oscillation

In this subsection, the damping ratio ζ_1 of pole pair p_1 is calculated to study the oscillatory criteria and the parametric sensitivity of the type I oscillation. The portion has $\zeta_1 < 0$ as the instable region which is susceptible to the self-sustained oscillation. The parameters in Table 1 are utilized to calculate ζ_1 with $R_G = 4\ \Omega$, and L_S varies from 20 to 100 nH. It should be noted that C_{GD} and C_{DS} also vary when the supply voltage V_{DC} changes. The $V_{DS} - C_{DS}$ and $V_{DS} - C_{GD}$ curves are extracted from the device's datasheet.

According to the oscillation mechanism presented in Section 2, the type I oscillation is driven by a common source inductance L_S. With a larger L_S, a higher oscillation amplitude can be obtained on V_{Ls} to excite the gate voltage oscillation. As a result, the positive feedback process is enhanced and the oscillatory system becomes more instable. Figure 12a has already demonstrated that the type I oscillation is driven by the L_S. This can also be validated by the damping ratio ζ_1. As shown in Figure 13, the ζ_1 decreases significantly with the increase of L_S.

The impact of the V_{DS} on the damping ratio is presented in Figure 13a. With the increase of the V_{DS}, the damping ratio ζ_1 has a short-term initial reduction and then approximately remains constant when V_{DS} is larger than about 150 V. The initial reduction of ζ_1 is due to the decrease of the capacitance C_{GD} and C_{DS}, as shown in Figure 13b,c. When C_{DS} reduces to about 150 pF (approximately corresponding to 150 V of V_{DS}), ζ_1 starts to increase with the reduction of C_{DS}, as shown in Figure 13c. Since it counteract the damping ratio decrease induced by a reduction of C_{GD}, ζ_1 approximately remains constant with the increase of the V_{DS} when $V_{DS} > 150$ V.

As shown in Figure 13d, the gate resistance R_G has a significant damping effect on type I oscillations. Few ohms of R_G can completely suppress the oscillation. Since R_G can damp the gate loop resonant and break down the feedback process, the damping effect is obvious. Figure 13e shows the impact of power loop parasitic inductances L_C on the type I oscillation. When L_C has a small value, the common source inductance L_S greatly loses its driving force and has no significant impact on the damping ratio. At this time, the ζ_1 greatly decreases with the increase in L_C. When L_C becomes large enough, L_S regains its driving force and becomes the dominant factor in determining the damping ratio ζ_1. At this time, the ζ_1 only increases slowly with the raise of the L_C. The impact of L_S greatly depends on the value of L_C. In order to reduce the driving force of the L_S, L_C should be as small as possible. The gate inductance L_G, on the other hand, has a much subtler influence on the damping ratio. As shown in Figure 13f, with the raise of L_G, the ζ_1 only slightly decreases at first and then undertakes a slow rising in the end. L_G is an insignificant factor for type I oscillations.



(**a**) $L_S - V_{DS}$ (**b**) $L_S - C_{GD}$ (**c**) $L_S - C_{DS}$

(**d**) $L_S - R_G$ (**e**) $L_S - L_C$ (**f**) $L_S - L_G$

Figure 13. The calculated damping ratio ζ_1.

4.2. The Parametric Sensitivity of the Type II Oscillation

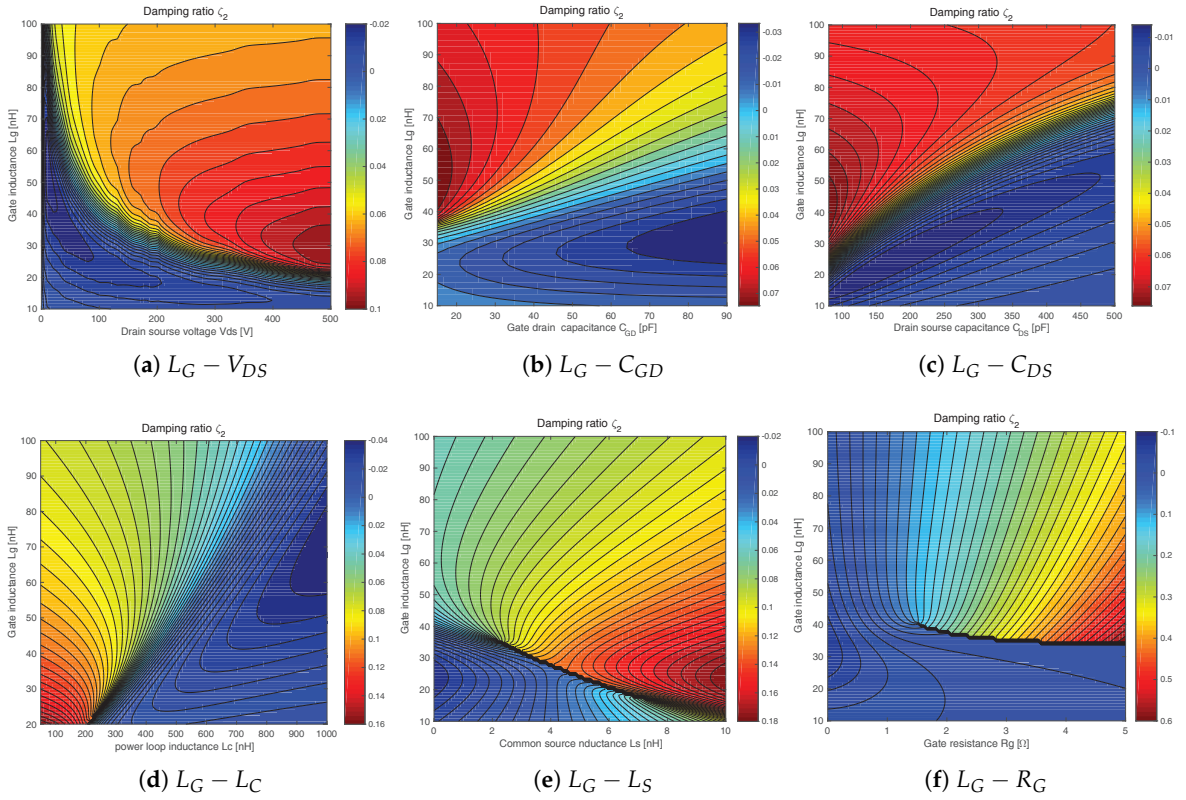
In this subsection, the damping ratio ζ_2 of pole pair p_2 is calculated to identify the oscillatory criteria and parametric sensitivity of a type II oscillation. The parameter set presented in Table 1 is utilized with $L_S = 0$ nH, and L_G varies from 10 to 100 nH.

Figure 14 shows the influenced of L_G on the damping ratio ζ_2. With the raise of L_G, the damping ratio ζ_2 decreases at first and then quickly increases to a large positive value at the boundary of the instable region. This phenomenon can be explained by the type II oscillation mechanism presented in Section 2: A slight increase in L_G can generate a higher voltage V_{L_g} to drive the gate voltage. This enhances the positive feedback process, and the oscillatory system becomes more instable. However, if L_G is too large, its high impedance can also hinder the drain current feedback process. The oscillation is thereby greatly suppressed.

Figure 14a presents the impact of V_{DS} on the ζ_2. As shown in Figure 14a, with the increase in V_{DS}, the instable region is greatly compressed. When V_{DS} is large enough, the instable region totally vanishes. In the instable region, the minimum damping ratio ζ_2 and the L_G which achieves the minimum ζ_2 decrease with the increase of V_{DS}. This phenomenon is due to the variation of the parasitic capacitances. As shown in Figure 14b,c, with the reduction of C_{GD} and C_{DS}, the similar variation tendency of ζ_2 is evident.

The influence of the inductance L_C on the damping ratio ζ_2 is presented in Figure 14d. When the L_C has a small value, the oscillation is completely suppressed. ζ_2 decreases with the raise of L_G. When L_C becomes enough large, the instable region starts to form and greatly expands with the increase of L_C. The minimum value of ζ_2 in the instable region decreases with the increase of L_C. In the vicinity of lower boundary of the instable region, the damping ratio ζ_2 slightly rises with the increase of L_C. Therefore, to minimize the instable region, the L_C should be as small as possible. The inductance L_S shows a very strong damping effect on the oscillation system. As shown in Figure 14e, with few nanohenries of L_S, a very large damping ratio can be achieved. At this time, the phase of the voltage

V_{Ls} across L_S is opposite the gate-source voltage V_{GS} [8,13]. This provide negative feedback to the oscillatory system [8], which significantly dampens the turn-off oscillation [14]. The impact of gate loop resistance on the damping ratio ζ_2 is shown in Figure 14f. The resistance R_G shows a significant damping effect on a type II oscillation. Since the resistance R_G dampens the gate loop resonate, the damping effect is reasonable.



(**a**) $L_G - V_{DS}$ (**b**) $L_G - C_{GD}$ (**c**) $L_G - C_{DS}$

(**d**) $L_G - L_C$ (**e**) $L_G - L_S$ (**f**) $L_G - R_G$

Figure 14. The calculated damping ratio ζ_2.

5. Oscillation Prevention

Based on the analyses presented in the previous section, the methods which can prevent a type I oscillation are summarized as follows:

(1) Reducing the inductance L_S: Since voltage V_{Ls} on the L_S is the major driving force of type I oscillations, the reduction of L_S can greatly reduce V_{Ls} and suppress type I oscillations.
(2) Reducing the inductance L_C: As shown in Figure 13e, the damping ratio ζ_1 significantly increases with the reduction of L_C. L_S can greatly lose its driving force when L_C is small enough. Therefore, the reduction of L_C is a very effective way to suppress type I oscillations.
(3) Increasing the gate resistance R_G: As shown in the Figure 13d, the damping ratio ζ_1 greatly increases with the raise of R_G. Increasing R_G is an obvious choice to avoid the self-sustained oscillation.

To suppress type II oscillations, the necessary measures which should be adopted are summarised as follows:

(1) Reducing the inductance L_C: With the reduction of L_C, the instable region significantly compresses, as shown in Figure 14d. When L_C is small enough, the type II oscillation can be eliminated.
(2) Optimizing the gate inductance L_G: The gate inductance L_G has a great impact on type II oscillations. Many researches on the gate driver design claim that the gate driver should be

very close to the MOSFET to avoid oscillations induced by the large L_G [15,16]. Reducing L_G is supposed to be the primary way to suppress the switching oscillation [8]. However, in this study, the analyses presented in Figure 14a,d reveal that the reduction of L_G does not necessarily suppress type II oscillations. Its influence greatly depends on the operating condition, which is determined by parameters like V_{DS} and L_C. Therefore, to suppress a type II oscillation, the value L_G should be carefully chosen based on the operating condition.

(3) Increasing the gate resistance R_G: As shown in Figure 14f, the gate resistance has a very strong damping effect on the type II oscillation. Few ohms of R_G are able to completely suppress the oscillation.

(4) Increasing the supply voltage V_{DC}: Since the V_{DS} oscillation is biased by the supply voltage V_{DC}, the increase of V_{DC} can elevate the central tendency of the V_{DS} oscillation. As shown Figure 14a, with a high V_{DS}, a type II oscillation can be suppressed.

It should be noted that increasing L_S can also greatly suppress a type II oscillation. However, a large L_S will significantly slow down the switching speed [8], which induces higher switching losses [17]. Moreover, a type I oscillation can also be triggered by the large L_S. Therefore, increasing L_S is not a very good option for oscillation suppression.

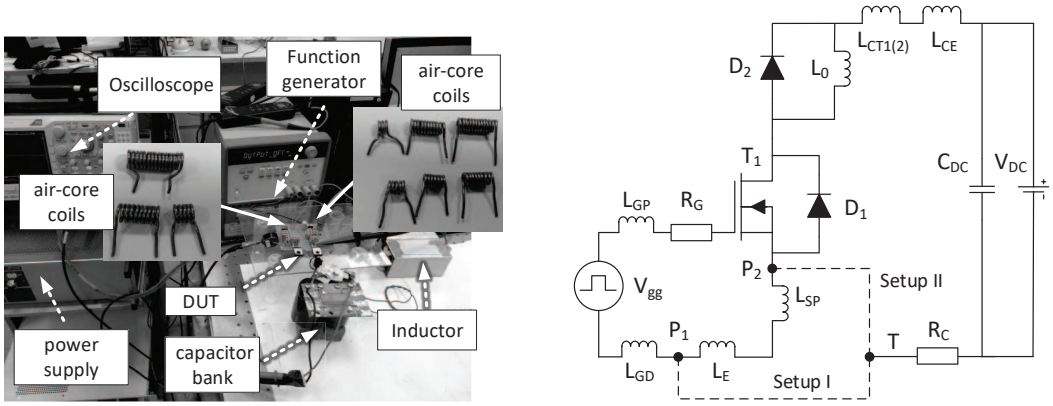
6. Experimental Validation

6.1. Experiment Setup

The double pulse switching test is performed to verify the oscillation suppression methods presented in the previous section. In the test, to ensure the safety of the gate driver and the DUT, the load current is 1.5 A. This is a reasonable setup, since Figure 8 has already demonstrated that the load current does not have a significant impact on the occurrence of self-sustained oscillation. The supply voltage V_{DC} is 50 V, which also varies from 50 V to 300 V to validate the influence of V_{DS} on a type II oscillation. Figure 15 shows the test platform and the schematic circuit for the test. In the test circuit, setups I and II are utilized to trigger the two type oscillation and various air-core coils are utilized to change the inductance of L_C, L_G, and L_S. As shown in Figure 15b, L_{CT1} and L_{CT2} are the stray inductances of the double-pulse tester for setup sI and II, respectively. The inductances of L_{CT1} and L_{CT2} can be extracted by dI_D/dt following the method presented in Reference [18]. L_{CE} and L_E are the external air-core coils utilized in the power and gate loops. Their inductances are extracted by the method presented in Reference [19]. The power loop inductance $L_C = L_{CT1(2)} + L_{CE}$. L_{SP} and L_{GP} are the source and gate package stray inductances. L_{GD} is the parasitic inductance of the gate drive circuit. The inductances of L_{SP}, L_{GP}, and L_{GD} are extracted by the Q3D extractor. The power loop parasitic resistance R_C is directly measured in the circuit. The parameters of the SiC MOSFET and schottky diode are extracted from the datasheet based on the dc operating point. All the parameters utilized in this validation are summarized in Table 2.

Table 2. Parameters for the validation.

Parameter	Value	Parameter	Value
g_m	0.1 S	C_{GS}	2 nF
R_C	0.2 Ω	C_{DS}	246 pF
C_{D2}	824 pF	C_{GD}	37 pF
$L_{S(G)P}$	7 nH	L_{GD}	8 nH
L_{CT1}	150 nH	L_{CT2}	200 nH
L_E	19, 34, 46, 60, 73, 90 nH		
L_{CE}	110, 170, 260, 330, 450 nH		



(**a**) The test platform utilizing the air-core coils.

(**b**) The schematic circuit.

Figure 15. The test platform and the schematic circuit with air-core coils.

6.2. Experiment Results

6.2.1. Type I Oscillation

In order to obtain a large L_S to trigger a type I oscillation, node T is connected to node P_1, as shown the setup I in Figure 15b. In this scenario, $L_G = L_{GD} + L_{GP} = 15$ nH and $L_S = L_{SP} + L_E$. Table 3 shows the number of oscillation cycles N_C and the damping ratio ζ_1 with various R_G and L_S for the type I oscillation. Figures 16 and 17 present the corresponding experimental waveforms. The self-sustained oscillation cycles is marked as "inf" in Table 3.

Table 3. A comparison between the ζ_1 and number of oscillation cycles N_C (**bold**) with various R_G and L_S with $L_C = 410$ nH.

R_G \ L_S	**26 nH**	**41 nH**	**53 nH**	**67 nH**	**80 nH**	**97 nH**
1.5 Ω	−0.019 (**9**)	−0.059 (**inf**)	−0.073 (**inf**)	−0.082 (**inf**)	−0.087 (**inf**)	−0.091 (**inf**)
2 Ω	0.007 (**8**)	−0.043 (**12**)	−0.059 (**inf**)	−0.070 (**inf**)	−0.076 (**inf**)	−0.081 (**inf**)
3 Ω	0.024 (**8**)	−0.017 (**8**)	−0.035 (**9**)	−0.049 (**11**)	−0.057(**inf**)	−0.063 (**inf**)
3.6 Ω	0.030 (**6**)	−0.005 (**7**)	−0.023 (**8**)	−0.037 (**9**)	−0.046 (**10**)	−0.053 (**inf**)
5 Ω	0.033 (**6**)	0.014 (**6**)	−0.001 (**6**)	−0.014 (**6**)	−0.023 (**7**)	−0.031 (**7**)

As in Figure 16, with $R_G = 3.6\ \Omega$, the number of oscillation cycles N_C increases when L_S becomes larger and the self-sustained oscillation is excited when $L_S = 97$ nH. This shows that a type I oscillation is driven by L_S. The driving force of L_S is captured by the calculated damping ratios, since ζ_1 decreases in accordance with the increase of N_C, as shown in Table 3. However, since the self-sustained oscillation occurs when $\zeta_1 \leq -0.053$, the ζ_1 underestimates the damping effect of the oscillation.

Figure 17 presents the damping effect of R_G on a type I oscillation. N_C decreases significantly when R_G becomes larger. With the reduction of N_C, ζ_1 increases accordingly, as shown in Table 3. The damping effect of R_G on a type I oscillation is also captured by the damping ratio ζ_1.

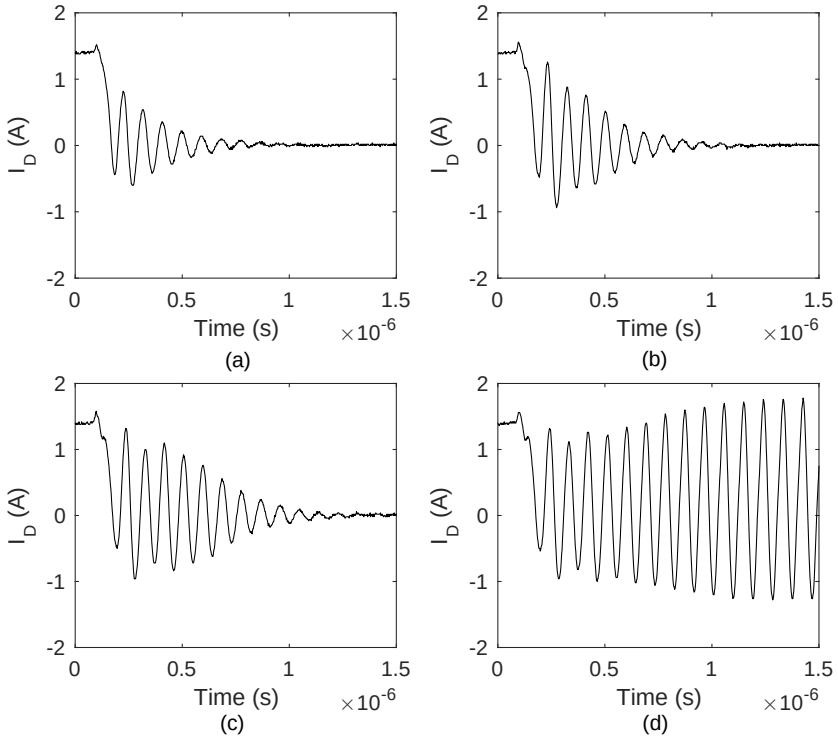


Figure 16. The experimental type I oscillation waveforms of the drain current I_D with various L_S with $R_G = 3.6\ \Omega$ and $L_C = 410$ nH. (**a**) $L_S = 26$ nH. (**b**) $L_S = 53$ nH. (**c**) $L_S = 80$ nH. (**d**) $L_S = 97$ nH.

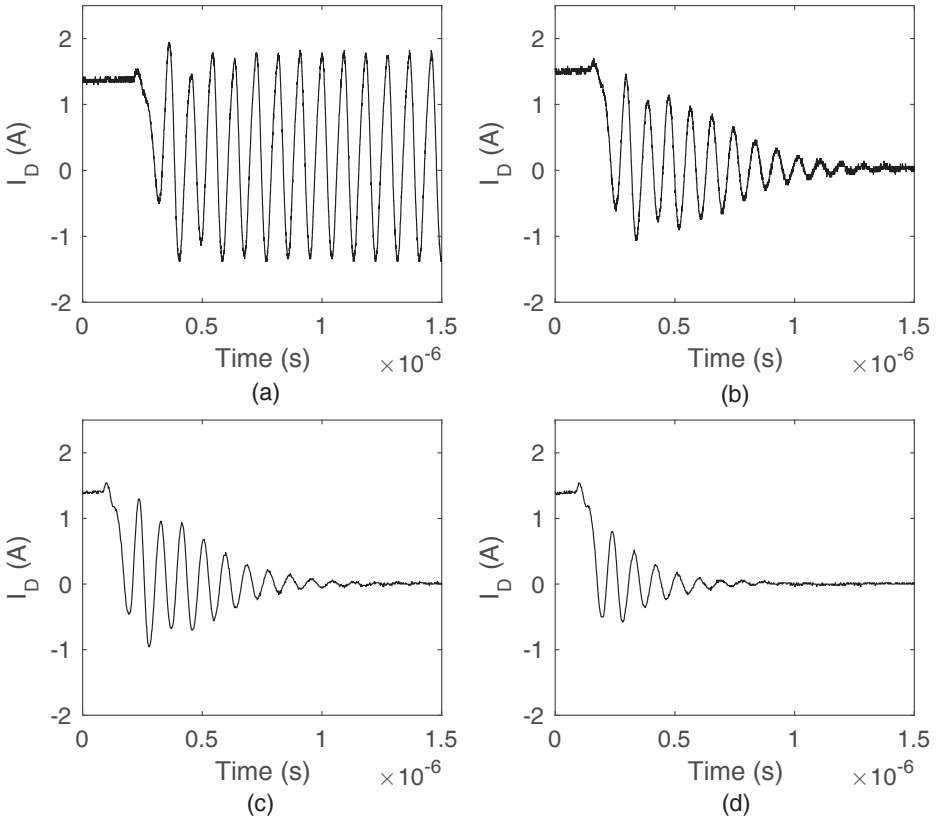


Figure 17. The experimental type I oscillation waveforms of the drain current I_D with various R_G with $L_S = 67$ nH and $L_C = 410$ nH. (**a**) $R_G = 2\ \Omega$. (**b**) $R_G = 3\ \Omega$. (**c**) $R_G = 3.6\ \Omega$. (**d**) $R_G = 5\ \Omega$.

Table 4 presents the N_C and ζ_1 of a type I oscillation with various L_C and L_S. The corresponding drain current oscillation waveforms are presented in Figure 18. As shown in Table 4, the instable region expands significantly with the increase of L_C. When the $L_C = 150$ nH, L_S does not have a very significant impact on the oscillation. The oscillation is suppressed to the nature dampened ring-down, as shown in Figure 18a. When L_C goes up to 260 nH, the L_S starts to drive the oscillation, and a self-sustained oscillation appears when $L_S = 67$ nH, as shown in Figure 18b. The instable region is further expanded when $L_C = 320$ nH, as shown in Table 4. When L_C increases to 410 nH, the instable region stops to expand. The oscillation is dampened when $L_S \leq 41$ nH. As shown in Figure 18c,d, with $L_S = 41$ nH, the N_C decreases when L_C increases from 320 nH to 410 nH. As shown in Table 4, the variation of ζ_1 shows the same trend as that of the N_C. The impact of L_C on the oscillation is captured by the calculated ζ_1.

Table 4. A comparison between the ζ_1 and number of oscillation cycles N_C (**bold**) with various L_C and L_S with $R_G = 2\ \Omega$.

L_C \ L_S	26 nH	41 nH	53 nH	67 nH	80 nH	97 nH
150 nH	−0.026 (**6**)	−0.033 (**6**)	−0.035 (**7**)	−0.037 (**7**)	−0.038 (**8**)	−0.039 (**8**)
260 nH	−0.028 (**9**)	−0.046 (**10**)	−0.053 (**12**)	−0.058 (**inf**)	−0.061 (**inf**)	−0.063 (**inf**)
320 nH	−0.021 (**9**)	−0.048 (**15**)	−0.058 (**inf**)	−0.065 (**inf**)	−0.069 (**inf**)	−0.072 (**inf**)
410 nH	0.007 (**8**)	−0.043 (**12**)	−0.059 (**inf**)	−0.070 (**inf**)	−0.076 (**inf**)	−0.081 (**inf**)

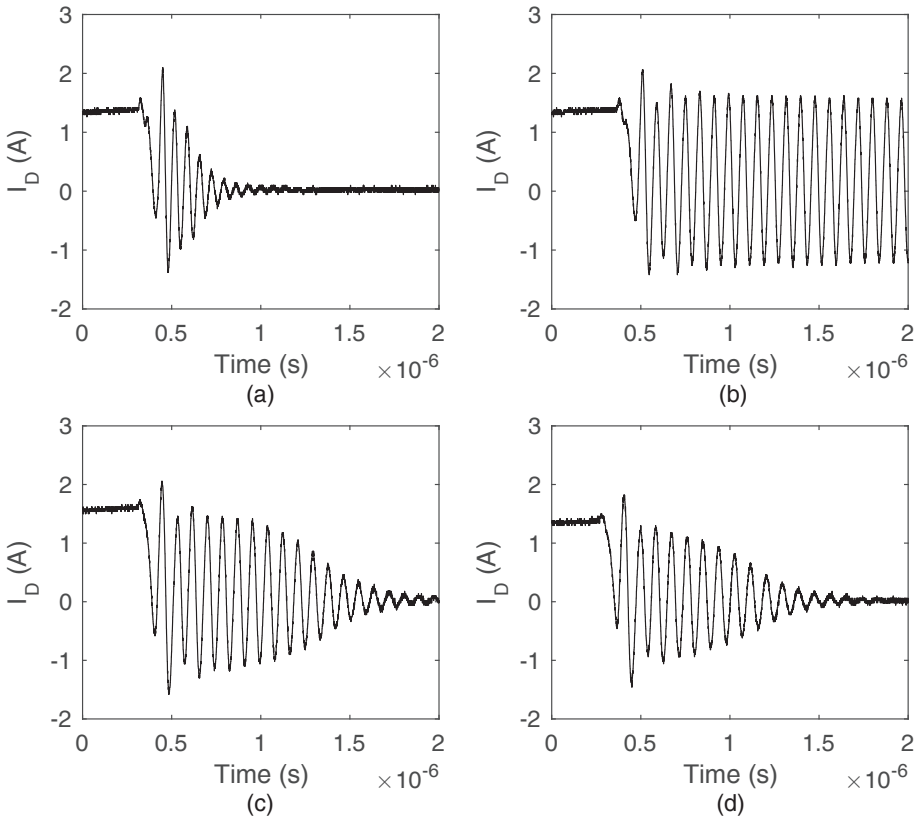


Figure 18. The experimental oscillation waveforms of the drain current I_D with $R_G = 2\ \Omega$. (**a**) $L_C = 150$ nH and $L_S = 67$ nH. (**b**) $L_C = 260$ nH and $L_S = 67$ nH. (**c**) $L_C = 320$ nH and $L_S = 41$ nH (**d**) $L_C = 410$ nH and $L_S = 41$ nH.

6.2.2. Type II Oscillation

To excite the type II oscillation, the inductance L_S should be eliminated. To achieve this, node T is connected to node P_2 in setup II, as shown in Figure 15b. In this case, $L_G = L_{GD} + L_{GP} + L_{SP} + L_E$, $L_S = 0$ nH. Table 5 shows the oscillation cycles N_C and calculated damping ratio ζ_2 of the type II oscillation with various L_C and L_G. The corresponding drain current oscillation waveforms are presented in Figures 19 and 20.

Table 5. A comparison between the ζ_2 and number of oscillation cycles N_C (**bold**) with various L_C and L_G with $R_G = 1.5\ \Omega$.

L_C \ L_G	**22 nH**	**41 nH**	**56 nH**	**68 nH**	**82 nH**
200 nH	0.020 (**5**)	0.153 (**5**)	0.137 (**5**)	0.127 (**7**)	0.118 (**8**)
310 nH	−0.003 (**inf**)	0.125 (**6**)	0.119 (**6**)	0.114 (**6**)	0.108 (**6**)
460 nH	−0.006 (**inf**)	−0.008 (**inf**)	0.021 (**8**)	0.072 (**6**)	0.086 (**5**)
530 nH	−0.006 (**inf**)	−0.013 (**inf**)	−0.003 (**inf**)	0.026 (**8**)	0.065 (**5**)
650 nH	−0.005 (**20**)	−0.015 (**inf**)	−0.018 (**inf**)	−0.011 (**inf**)	0.011 (**6**)

Figure 19 shows the influence of L_G on a type II oscillation when $L_C = 650$ nH. With the increase of L_G, N_C increases at first, and the self-sustained oscillation occurs when $L_G = 41$ nH. The self-sustained oscillation suddenly transfers into a natural damped ring-down when L_G increases from 68 nH to 82 nH, as shown in Figure 19c,d.

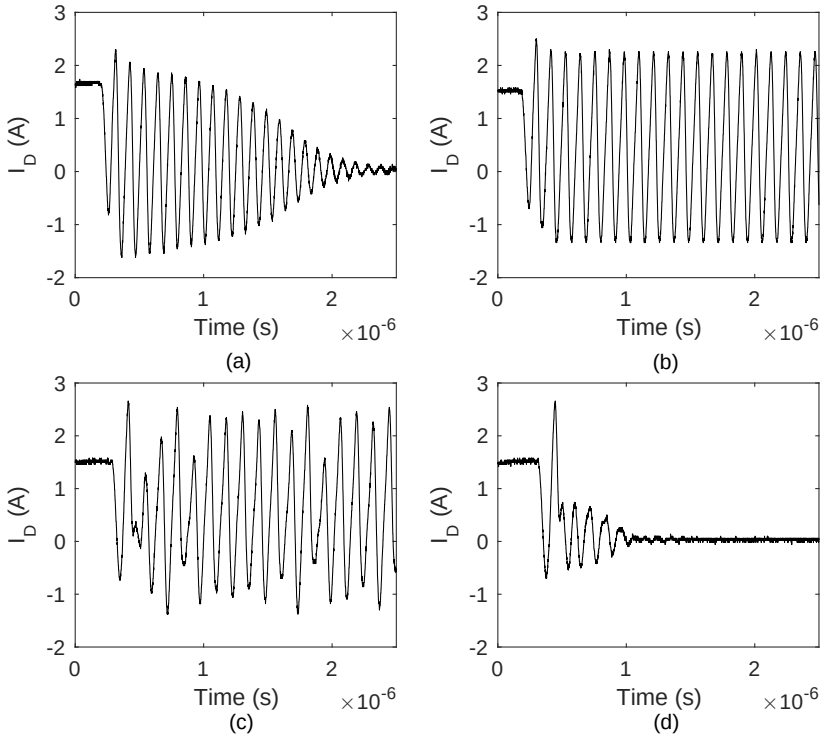


Figure 19. The experimental type II oscillation waveforms of the drain current I_D with $L_C = 650$ nH and $R_G = 1.5\ \Omega$. (**a**) $L_G = 22$ nH. (**b**) $L_G = 41$ nH. (**c**) $L_G = 68$ nH. (**d**) $L_G = 82$ nH.

As shown in Table 5, the instable region expands significantly with the increase in L_C. When $L_C = 200$ nH, the L_G does not have a significant impact on the oscillation. The oscillation is suppressed to a ring-down, as shown in Figure 20a. When L_C increases to 310 nH, the self-sustained

oscillation occurs when $L_G = 22$ nH, as shown in Figure 20b. When the L_C further increases to 460 nH, the instable region expands, and the self-sustained oscillation can be excited when $L_G = 41$ nH, as shown in Figure 20c. The instable region further expands when L_C increases to 530 nH and 650 nH, as shown in Table 5. However, on the lower boundary of the instable region ($L_G = 22$ nH), the oscillation is dampened when the L_C increases from 530 nH to 650 nH, as shown in Figures 19a and 20d. This damping effect is slightly underestimated by the calculated ζ_2, since ζ_2 only increases from -0.006 to -0.005, as shown in Table 5. Despite this discrepancy, the ζ_2 is in good accordance with the test results.

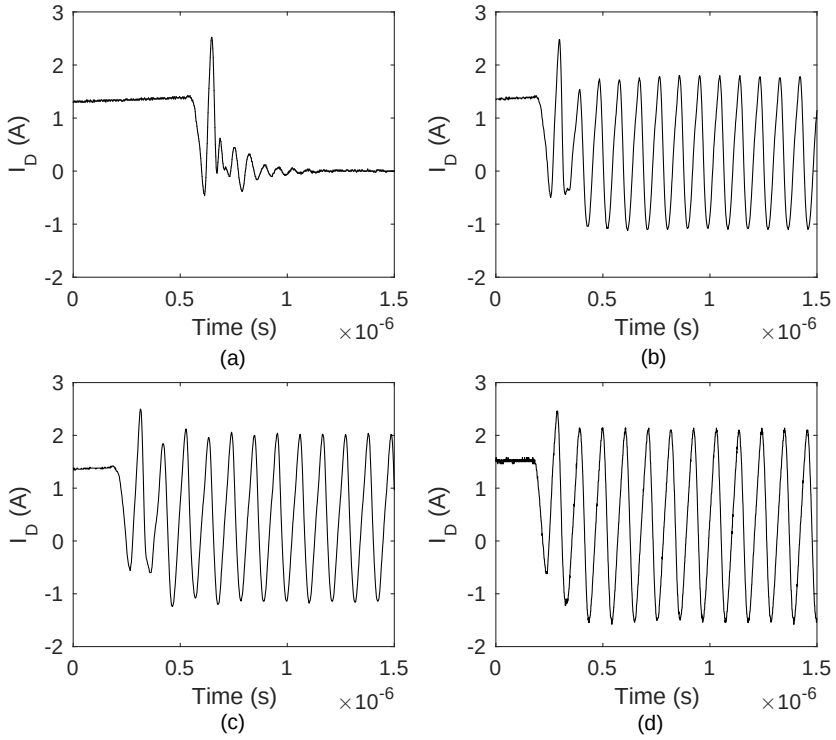


Figure 20. The experimental type II oscillation waveforms of the drain current I_D with $R_G = 1.5\ \Omega$. (**a**) $L_C = 200$ nH and $L_G = 22$ nH. (**b**) $L_C = 310$ nH and $L_G = 22$ nH. (**c**) $L_C = 460$ nH and $L_G = 41$ nH. (**d**) $L_C = 530$ nH and $L_G = 22$ nH.

Table 6 shows the N_C and ζ_2 with various L_G and V_{DC}. The corresponding drain current oscillation waveforms are presented in Figure 21. As shown in Table 6, the instable region greatly shrinks with the increase of the V_{DC}. As shown in Figures 20c and 21, with $L_G = 41$ nH, the self-sustained oscillation is suppressed to a nature damped ring-down when V_{DC} increases from 50 V to 100 V. The self-sustained oscillation can only occurs at $L_G = 22$ nH when V_{DC} reaches 100 V and 200 V, as shown in Figure 20b,c. When V_{DC} further increases to 300V, the self-sustained is completely suppressed, as shown in Figure 21d. The experimental data agree with the calculated ζ_2, as shown in Table 6.

Table 6. A comparison between the ζ_2 and number of oscillation cycles N_C (**bold**) with various L_G and V_{DS} with $L_C = 460$ nH, $R_G = 1.5\ \Omega$.

V_{DC} \ L_G	**22 nH**	**41 nH**	**56 nH**	**68 nH**	**82 nH**
50 V	−0.006 (**inf**)	−0.008 (**inf**)	0.021 (**8**)	0.072 (**6**)	0.086 (**5**)
100 V	−0.007 (**inf**)	0.017 (**7**)	0.094 (**7**)	0.099 (**7**)	0.097 (**7**)
200 V	−0.003 (**inf**)	0.110 (**5**)	0.114 (**4**)	0.109 (**6**)	0.103 (**6**)
300 V	0.007 (**5**)	0.130 (**4**)	0.121 (**5**)	0.114 (**5**)	0.106 (**4**)

Table 7 shows the N_C and ζ_2 with various L_G and R_G. The corresponding drain current oscillation waveforms are presented in Figure 22. As shown in Table 7, the instable region is greatly compressed with the increase of R_G. With $L_G = 22$ nH, the self-sustained oscillation is damped into ring-down when R_G increases form 1.5 Ω to 2 Ω, as shown in Figure 22a. The oscillation cycles N_C further reduces when R_G increases to 3 Ω, as shown in Figure 22b. As shown in Table 7, the calculated ζ_2 at $L_G = 22$ nH and $R_G = 2$ Ω underestimate the damping effect of the oscillation. Despite the underestimation, the other damping ratios agree with the test results.

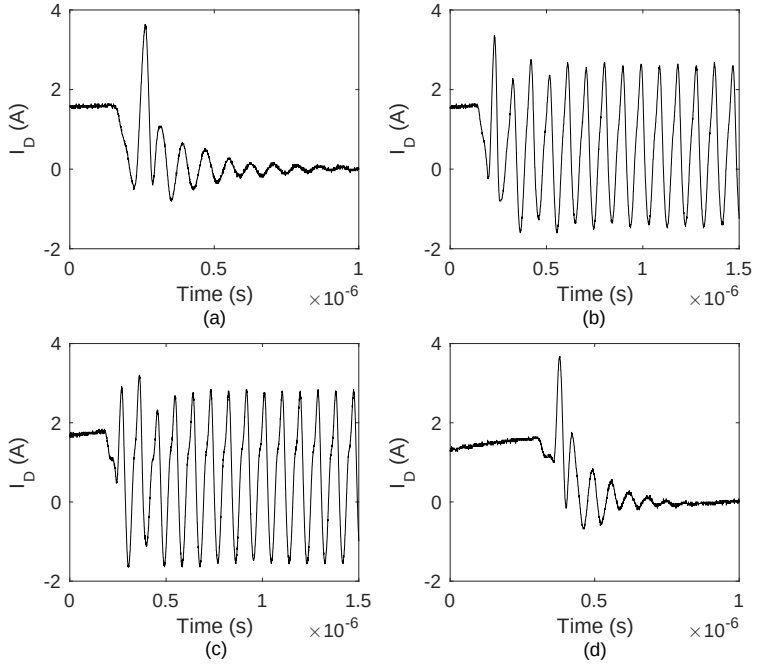


Figure 21. The experimental type II oscillation waveforms of the drain current I_D with $R_G = 1.5$ Ω. (**a**) $L_G = 41$ nH and $V_{DC} = 100$ V. (**b**) $L_G = 22$ nH and $V_{DC} = 100$ V, (**c**) $L_G = 22$ nH and $V_{DC} = 200$ V, (**d**) $L_G = 22$ nH and $V_{DC} = 300$ V.

Table 7. A comparison between the ζ_2 and number of oscillation cycles N_C (**bold**) with various L_G and R_G with $L_C = 460$ nH.

R_G \ L_G	**22 nH**	**41 nH**	**56 nH**	**68 nH**	**82 nH**
1.5 Ω	−0.006 (**inf**)	−0.008 (**inf**)	0.021 (**8**)	0.072 (**6**)	0.086 (**5**)
2 Ω	−0.001 (**11**)	0.002 (**7**)	0.033 (**8**)	0.123 (**4**)	0.127 (**4**)
3 Ω	0.007 (**6**)	0.014 (**6**)	0.034 (**7**)	0.234 (**7**)	0.212 (**5**)

The test results presented in Tables 3–7 validate the effectiveness of the proposed oscillation suppression methods. However, it can be noted that the calculated damping ratios ζ_1 and ζ_2 in Tables 3–7 underestimate the damping effect of the oscillation. During the oscillatory transient, the turn-on of MOSFET T_1 gives rise to the additional carrier injection in the drift region. The injected carrier will dampen the depletion formation in the drift region during the next turn-off process of T_1. As a result, the injected carrier acts as a damper during the oscillatory transient. This damping effect gives rise the underestimation of the damping ratios. Additionally, in this study, the nonlinearity of the parameters C_{GD}, C_{DS}, and C_{D2} are not considered in the model. The circuit and device's parameters are only approximately extracted. These factors can also give rise to the discrepancy between the predicted damping ratios and experimental data.

All in all, due to the reasons presented above, the calculated damping ratios have some errors. However, the proposed analytical treatment is still able to make reasonable predictions on the

instable region which is susceptible to a self-stained oscillation. The influences of the circuit and device's parameters on the self-sustained oscillation can also be analyzed by the proposed model. These analyses can provide effective guidelines to suppress the oscillation.

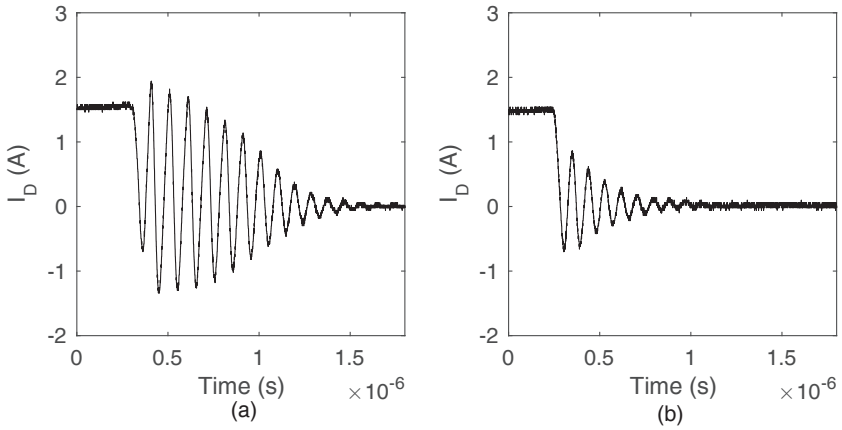


Figure 22. The experimental type II oscillation waveforms of the drain current I_D with $L_C = 460$ nH and $L_G = 22$ nH. (**a**) $R_G = 2\ \Omega$. (**b**) $R_G = 3\ \Omega$.

7. Conclusions

This paper has presented an analysis of self-sustained oscillations of the SiC MOSFETs. Based on the double pulse test, two distinct mechanisms which can excite the self-sustained oscillation are identified. By analyzing the parametric sensitivity of the oscillatory system, the influences of the circuit and deice's parameters on the self-sustained oscillation are revealed. The analyses clarify the criteria to avoid a self-sustained oscillation. A type I oscillation can be suppressed by reducing the common source inductance L_S and power loop inductance L_C or by increasing the gate resistance R_G. A type II oscillation can be eliminated by increasing the supply voltage V_{DC} and gate resistance R_G or by reducing the power loop inductance L_C. L_G should also be carefully chosen to avoid a type II oscillation. In the end, the proposed oscillation suppression methods has been validated by the experiment.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The coefficient a_i and b_i (i = 0,1,2,3,4) in (4) are as follows:

$$\begin{aligned}
a_4 &= C_{D2}(C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})(L_CL_G + L_CL_S + L_GL_S)\\
a_3 &= C_{D2}(L_CR_G + L_GR_C + L_SR_C + L_SR_G)(C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})\\
a_2 &= (L_G + L_S)(C_{DS}C_{GD} + C_{DS}C_{GS} + C_{D2}C_{GS} + C_{GD}C_{GS}) + C_{DS}C_{D2}(L_C + L_S)\\
&\quad + C_{D2}C_{GD}(L_C + L_G) + C_{D2}R_CR_G(C_{DS}C_{GD} + C_{DS}C_{GS} + C_{GD}C_{GS})\\
a_1 &= C_{D2}R_C(C_{DS} + C_{GD}) + R_GC_{GD}(C_{DS} + C_{D2}) + R_GC_{GS}(C_{DS} + C_{D2} + C_{GD})\\
a_0 &= C_{DS} + C_{D2} + C_{GD}\\
b_4 &= a_4\\
b_3 &= a_3 + g_mC_{D2}C_{GD}(L_CL_G + L_CL_S + L_GL_S)\\
b_2 &= a_2 + g_mC_{D2}C_{GD}(L_CR_G + L_GR_C + L_SR_C + L_SR_G)\\
b_1 &= a_1 + g_m(C_{GD}L_G + C_{D2}L_S + C_{GD}L_S + C_{D2}C_{GD}R_CR_G)\\
b_0 &= a_0 + g_mC_{GD}R_G
\end{aligned} \tag{A1}$$

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