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Research on the Filters for Dual-Inverter Fed Open-End Winding Transformer Topology in Photovoltaic Grid-Tied Applications

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Abstract: Owing to the necessity of the transformer for the multi-parallel inverters connected to the medium-voltage (MV) grid, the conventional multi-parallel inverter topology can be reconfigured to the dual-inverter fed open-end winding transformer (DI-OEWT) topology to obtain lower output voltage harmonics, which can reduce the requirement of the filter inductance. However, due to the special structure of the DI-OEWT topology, the arrangement scheme of the filter can be more than one kind, and different schemes may affect the filter performance. In this paper, research on the existing two kinds of filters, as well as a proposed one, for the DI-OEWT topology used in photovoltaic grid-tied applications is presented. The equivalent circuits of these filters are derived, and based on this, the harmonic suppression capability of these filters is analyzed and compared. Furthermore, a brief parameter design method of these filters is also introduced, and based on the design examples, the inductance and capacitance requirements of these filters are compared. In addition, these filters are also evaluated in terms of the applicability for fault tolerance. At last, the analysis is verified through an experiment on a 30 kW dual-three-level inverter prototype.

Keywords: dual inverter; open-end winding transformer; photovoltaic application; filter

1. Introduction

In recent years, the increasing exhaustion of traditional fossil energy has resulted in an emerging interest in the development of renewable energies, one of which is solar energy that has already obtained widespread applications. Among all types of commercial solar energy applications, photovoltaic grid-tied system plays an important role, and large-scale photovoltaic power plants have become dominant [1].

In the large-scale photovoltaic power plants, three-phase single-stage central inverters are widely used because of their many advantages, such as cost-effectiveness, simplicity in hardware design and easy maintenance. The two-level, three-level T-type, and three-level neutral point clamp (NPC) voltage source inverters (VSI) are the most widely used topologies among the current commercial central inverters [2]. Furthermore, to increase the transmission efficiency of the overall electrical equipment, the inverters are generally connected to a medium-voltage (MV) grid of a voltage level from 10 kV to 35 kV. Additionally, multi-parallel inverter topology, in which the inverters are connected in parallel through step-up MV transformers, are commonly used in these systems. A typical commercial application example is 1 MW MV turnkey station, which is composed of two 500 kW central inverters and one 1 MVA MV transformer [3]. Since the transformer is essential for the inverters connected to the MV grid, the multi-parallel inverter topology has the possibility to be reconfigured to the dual-inverter fed open-end winding transformer (denominated here as DI-OEWT) topology.

The dual-inverter topology was first proposed for the motor drive application in [4]. Since then, it has already been extended to many applications, such as STATCOM [5], active power filter [6], dynamic voltage restorer [7], photovoltaic grid-tied inverter [8]. It utilizes dual-inverter structure connected to the open-end windings of an induction motor or a three-phase transformer. Through proper modulation strategy, the harmonic cancellation effect can be realized among the two inverters, the dual-inverter topology with two N-level inverters can have the same output voltage levels as a (2N-1)-level inverter [9]. Therefore, lower dv/dt and lower harmonics in the output voltage can be obtained, which can reduce the filter requirement. It can also double the DC voltage utilization. A tdual-N-level inverter with half the DC link voltage (compared to a conventional single inverter scheme) is capable of producing the same AC voltage as a single (2N-1) level inverter, which will reduce the voltage capacity of the power switch devices and decrease the switching losses [10]. What is more, the DC sources requirement of the dual-inverter is minimal over other multilevel topologies [11–13]. The two inverters of the dual-inverter can also be supplied by one single DC source for cost saving [14]. Another merit of the dual-inverter topology is the availability of higher redundant switching state combinations compared to the single inverter, which can be used to achieve switching frequency reduction [15], common-mode voltages suppression [16], capacitor voltage balance [17]. Furthermore, it also offers the advantage of fault tolerance. In case of a fault in the inverter, the inverter can still work with some adjustment [18–20].

However, the advantages of the dual-inverter topology described above are not all applicable to the topology used in photovoltaic grid-tied applications. Firstly, the DC bus voltage is limited to the photovoltaic array voltage, which is usually 1000 V or 1500 V (open-circuit voltage). It is uneconomic to reduce this voltage because that will increase the system installation costs and narrow the maximum power point tracking (MPPT) voltage operation range [2]. In addition, it will be better for the dual-inverter to be supplied by two separate arrays (two DC sources), which can not only achieve multiple MPPTs, but also suppress the circulating current among the two inverters [21,22]. The fault tolerance capability cannot be a special advantage of the dual-inverter because the multi-parallel inverter topology has the same capability as well. To sum up, compared with the conventional multi-parallel inverter topology, the most attractive advantage of the DI-OEWT topology is the improvement of the harmonic quality in the output voltages, thus can reduce the filter requirement and save the filter costs.

However, there are few papers considering the selection or design of the filters used in DI-OEWT-based grid-tied applications at present. In [23–28], single inductor filter was adopted in these DI-OEWT based grid-tied systems, which is obviously not a good choice. Owing to the weak harmonic suppression capability, it needs a large inductance value to meet the grid standard. To reduce the inductance cost, high order filter is preferred [29]. In [30], two kinds of high order filters for DI-OEWT topology were proposed. One is the "individual capacitor type filter", that the two inverters of the DI-OEWT topology are connected to the open-end windings of the transformer through two individual inductor-capacitor filters. The other one is the "common capacitor type filter", which is also presented in [21,22], that the two inverters are connected to the open-end windings of the transformer through two individual inductors but one common capacitor. However, the authors in [30] were mainly focused on active damping methods of the two different filters, and the authors in [21,22] were mainly focused on the magnetic integration design of the filter inductors, none of these papers analyzed the harmonic suppression capability or the parameter design method of these filters.

In addition, the transformer's leakage inductance is a significant component of the filter, and for the transformer used in the high power MV grid-tied system, the value is usually no less than 6% [31]. This is a relatively big value and should be used properly in the selection and design of the filter, but none of the present literatures has paid attention to this. Another point deserves to be considered is the fault tolerance scheme of the DI-OEWT topology, which is very important for such multi-inverter type topology.

In light of the above, this paper aims to research the filters for the DI-OEWT topology used in photovoltaic grid-tied applications. First, the equivalent circuits of the existing two kinds of high order filters presented in [21,22,30] are derived, and based on this, the harmonic suppression capabilities of these filters are analyzed and compared. According to the analysis results, a new high order filter for DI-OEWT topology is also proposed. Furthermore, a brief parameter design method of the existing and the proposed filters for DI-OEWT is introduced and based on the design examples, the inductance and capacitance requirements of these filters are compared. Besides, these filters are also evaluated in terms of the applicability for fault tolerance.

The rest of the paper is organized as follows: The inductor-capacitor-inductor (LCL) filter used in multi-parallel inverters is presented in Section 2 as the comparison object. The model and harmonic suppression capability analysis of the existing and the proposed filters for DI-OEWT topology are shown in Section 3. The filter design method, together with the design examples, as well as the fault-tolerant scheme, are presented in Section 4. Experimental results are given in Section 5 to validate the filter parameters. Finally, the conclusions are summarized in Section 6.

2. LCL Filter for the Conventional Multi-Parallel Inverters

The system configuration of the conventional multi-parallel inverters used in photovoltaic applications is illustrated in Figure 1. The two inverters are connected in parallel to the low voltage side of the MV transformer through individual LC filters. The leakage inductance L_t' of the transformer and the grid inductance L_g' play the role of the grid-side filter inductor, so the two inverters can also be viewed as connecting in parallel through individual LCL filters.

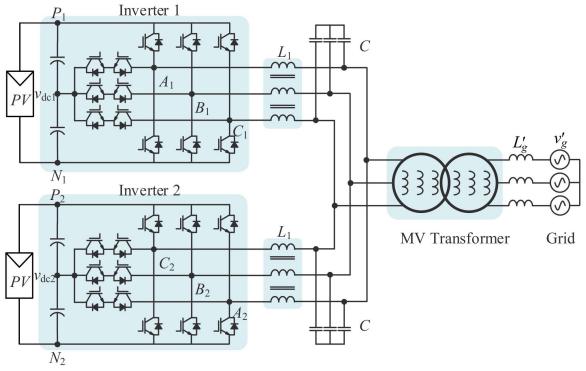

Figure 1. System configuration of the conventional multi-parallel inverters.

It is essential to derive the equivalent circuit of the filter based VSI for the filter design and harmonic suppression capability analysis. Since the LCL filter used in parallel inverters has no difference with that used in single inverters, the single-phase equivalent circuit of the LCL filter can be directly obtained from many existing papers [32,33], as shown in Figure 2. In the figure, the equivalent circuit is drawn referred to the low-voltage side of the transformer, v_{inv1} and i_{inv1} (take inverter 1 as an example) are the inverter output phase voltage and current, respectively. v_{g} and i_{g} are the grid voltage and current, respectively. The inverter-side inductor is represented as L_1, the combined inductance of the transformer leakage inductance L_{t} and the grid inductance L_{g} are represented as L_2, and the filter capacitor is represented as C.

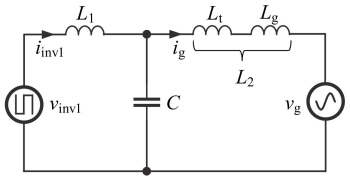

Figure 2. Single-phase equivalent circuit of the LCL filter.

While the inverter is working, the harmonics in i_{inv1} should be suppressed by the filter to limit the current ripple, and the harmonics in i_g should be suppressed to meet the grid standard [34]. Assuming that no harmonics exist in the grid voltage, the inverter output voltage v_{inv1} is the only harmonic source of the system, then the transfer functions $v_{inv1}(s)$ to $i_g(s)$ and $i_{inv1}(s)$ can be used to reflect the harmonic suppression capability of the LCL filter, as shown in Equations (1) and (2), respectively

$$i_g(s) = \frac{1}{L_1L_2Cs^3 + (L_1 + L_2)s} v_{inv1}(s) \tag{1}$$

$$i_{inv1}(s) = \frac{L_2Cs^2 + 1}{L_1L_2Cs^3 + (L_1 + L_2)s} v_{inv1}(s) \tag{2}$$

where $L_2 = L_t + L_g$. The value of L_t and L_g is related to the transformer impedance voltage V_k and the grid short-circuit ratio (SCR), respectively [35]. Therefore, L_2 can be calculated as

$$L_2 = \frac{3v_g^2}{2\pi f_0 P_{rated}} V_k + \frac{3v_g^2}{2\pi f_0 P_{rated} SCR} = \frac{3v_g^2}{2\pi f_0 P_{rated}} \left(V_k + \frac{1}{SCR} \right) \tag{3}$$

where P_{rated} is the system rated power, f_0 is the fundamental frequency.

3. Existing and Proposed Filters for the DI-OEWT Topology

3.1. Type-1 Filter for the DI-OEWT Topology

Direct replacing of the two-winding transformer in the multi-parallel inverter topology (as shown in Figure 1) with the open-end winding (OEW) transformer, can obtain the DI-OEWT topology with the "individual capacitor type filter" (here we call it "Type-1 filter"). The filter was proposed in [30], as illustrated in Figure 3. It is worth noting that the voltage of the low-voltage side of the OEW transformer is twice the voltage of the replaced transformer, since the AC sides of the two inverters are connected in series through the low-voltage side of the transformer [8]. Accordingly, the current level of the inverter remains unchanged, so the multi-parallel inverter topology can be easily reconfigured to the DI-OEWT topology.

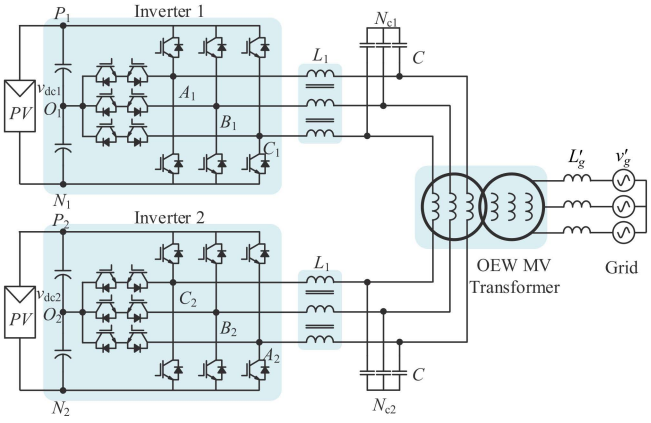

Figure 3. System configuration of the dual-inverter fed open-end winding transformer (DI-OEWT) topology with the Type-1 filter.

To analyze the Type-1 filter, firstly, the three-phase equivalent circuit of the DI-OEWT topology with the Type-1 filter is derived in Figure 4. The voltage source V_{X1O1} and V_{X2O2} represent the pole voltage of phase X_1 of inverter 1 and the pole voltage of phase X_2 of inverter 2, respectively ($X = A, B, C$). In a balanced and symmetrical three-phase system, for inverter 1, a common-mode (CM) voltage exists between the neutral point O_1 and the capacitor common point N_{c1}, this CM voltage is expressed as $V_{O1Nc1} = -1/3(V_{A1O1} + V_{B1O1} + V_{C1O1})$. Similarly, the corresponding CM voltage of inverter 2 is

expressed as $V_{O2Nc2} = -1/3(V_{A2O2} + V_{B2O2} + V_{C2O2})$. According to Kirchhoff's voltage law (KVL), the voltage across the two capacitor common points N_{c1}, N_{c2} can be derived as

$$V_{Nc1Nc2} = \frac{1}{3}\left[\begin{array}{l} -(V_{CA1} + V_{CB1} + V_{CC1}) + (V_{CA2} + V_{CB2} + V_{CC2}) \\ +(V_{L\sigma 1A} + V_{L\sigma 1B} + V_{L\sigma 1C}) + (V_{tA1} + V_{tB1} + V_{tC1}) \end{array}\right] \quad (4)$$

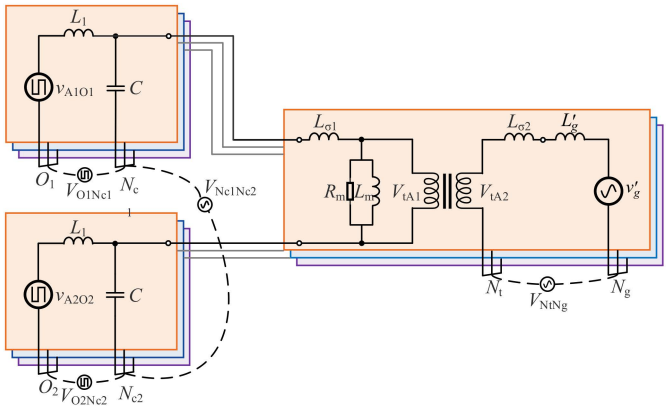

Figure 4. Three-phase equivalent circuit of the DI-OEWT topology with the Type-1 filter.

The voltage across the neutral point N_t of the transformer high voltage side and the neutral point N_g of the three-phase grid can be derived as

$$V_{NtNg} = \frac{1}{3}\left[\begin{array}{l} (V_{tA2} + V_{tB2} + V_{tC2}) + (V_{L\sigma 2A} + V_{L\sigma 2B} + V_{L\sigma 2C}) \\ +\left(V_{LgA} + V_{LgB} + V_{LgC}\right) + \left(v'_{gA} + v'_{gB} + v'_{gC}\right) \end{array}\right] \quad (5)$$

In Equations (4) and (5), V_{CX1} and V_{CX2} represent the voltage on the filter capacitor of phase X_1 and phase X_2, respectively. $V_{L\sigma 1X}$ and $V_{L\sigma 2X}$ represent the phase X voltage on the leakage inductance at low voltage side ($L_{\sigma 1}$) and high voltage side ($L_{\sigma 2}$) of the MV transformer, respectively. V_{LgX} represents the phase X voltage on the grid inductance L'_g. V_{tX1} and V_{tX2} represent the voltage of the low and high voltage side of the MV transformer, respectively. v'_{gX} is the phase X voltage of the MV grid. Considering only the line frequency component and the balanced three-phase system, it is easy to deduce that $V_{Nc1Nc2} = 0$ and $V_{NtNg} = 0$. Thus, N_{c1} can be connected to N_{c2} and N_t can be connected to N_g. Then, the single-phase equivalent circuit of the DI-OEWT topology with the Type-1 filter can be derived as shown in Figure 5 with further simplification. Where the inverter 1 output phase voltage $v_{inv1} = V_{A1O1} + V_{O1Nc1}$, the inverter 2 output phase voltage $v_{inv2} = V_{A2O2} + V_{O2Nc2}$, i_{inv1} and i_{inv2} represent the output phase current of inverter 1 and inverter 2, respectively.

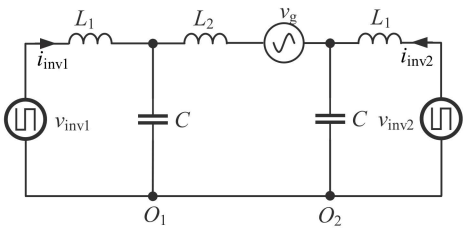

Figure 5. Single-phase equivalent circuit of the DI-OEWT topology with the Type-1 filter.

From Figure 5, the transfer functions $v_{inv1}(s)$, $v_{inv2}(s)$ to $i_g(s)$ and $i_{inv1}(s)$ can be, respectively, calculated as

$$i_g(s) = \frac{1}{L_1L_2Cs^3 + (2L_1 + L_2)s}[v_{inv1}(s) - v_{inv2}(s)] \quad (6)$$

$$i_{inv1}(s) = G_1(s)v_{inv1}(s) - G_2(s)v_{inv2}(s) \quad (7)$$

where

$$i_{\text{inv1}}(s) = G_1(s)v_{\text{inv1}}(s) - G_2(s)v_{\text{inv2}}(s)$$

$$G_2(s) = \frac{1}{L_1^2L_2C^2s^5 + \left(2L_1^2C + 2L_1L_2C\right)s^3 + (2L_1 + L_2)s}$$

Figure 6a shows Bode plots of the transfer function $v_{\text{inv1}}(s)$, $v_{\text{inv2}}(s)$ to $i_{\text{g}}(s)$ of both the LCL filter and the Type-1 filter, while the inverter-side inductor L_1, capacitor C, impedance voltage V_{k} and SCR are all the same in both filters. Figure 6b presents Bode plots of the transfer function $v_{\text{inv1}}(s)$, $v_{\text{inv2}}(s)$ to $i_{\text{inv}}(s)$ with the aforementioned parameters. According to Figure 6 and Equations (1), (2), (6), (7), the following can be obtained.

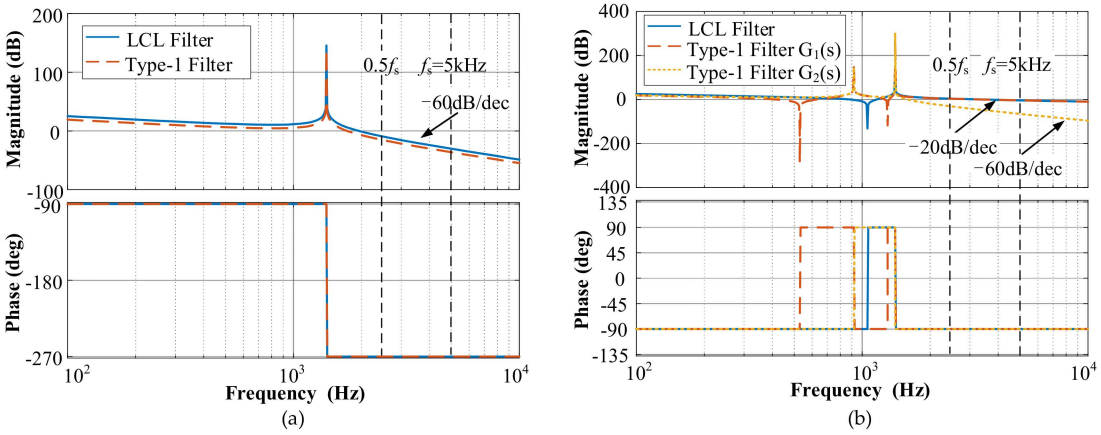

Figure 6. Bode plots of transfer function $v_{\text{inv1}}(s)$, $v_{\text{inv2}}(s)$ to $i_{\text{g}}(s)$ and $i_{\text{inv1}}(s)$ in LCL and Type-1 filters (**a**) $v_{\text{inv1}}(s)$, $v_{\text{inv2}}(s)$ to $i_{\text{g}}(s)$, (**b**) $v_{\text{inv1}}(s)$, $v_{\text{inv2}}(s)$ to $i_{\text{inv1}}(s)$.

(1) Figure 6a suggests that, for i_{g}, Type-1 filter has superior high-frequency harmonic suppression capabilities than the LCL filter. Meanwhile, compare Equation (6) with (1), the harmonic source of i_{g} in DI-OEWT topology is $v_{\text{inv1}} - v_{\text{inv2}}$, while in multi-parallel inverter topology is v_{inv1}. Owing to the harmonic cancellation effect in the output voltage of DI-OEWT, $v_{\text{inv1}} - v_{\text{inv2}}$ has lower harmonics than v_{inv1}. Thus, i_{g} in DI-OEWT can achieve a much better current quality than the multi-parallel inverter topology. Conversely, Type-1 filter can reduce filter requirement than LCL filter. Since L_2 is limit by the V_{k} and SCR, which cannot be reduced, so L_1 or C may be reduced.

(2) From Equation (7), for the inverter output phase current i_{inv1}, $G_1(s)$ and $G_2(s)$ can reflect the suppression capability of the Type-1 filter on v_{inv1} and v_{inv2}, respectively. From Figure 6b, in the high-frequency band, the harmonics attenuation rate of $G_2(s)$ is −60 dB/dec, way above the harmonics attenuation rate of $G_1(s)$, which is −20 dB/dec. Therefore, the harmonic source of i_{inv1} in DI-OEWT topology is mainly the v_{inv1}, the same as the voltage in multi-parallel inverter topology according to Equation (2). Meanwhile, the harmonics attenuation rate of LCL filter is also −20 dB/dec, thus, i_{inv1} of both the scheme has almost the same current quality. Because the current ripple of i_{inv1}, which is mainly suppressed by inverter-side inductor L_1, is strictly limited by the semiconductor current rating and loss requirement. Therefore, L_1 of Type-1 filter cannot be reduced.

In summary, compared with the multi-parallel inverter topology, the DI-OEWT topology with Type-1 filter can only reduce the value of filter capacitor C, showing that the Type-1 filter maybe not a better solution for the DI-OEWT topology.

Another way to explain why the Type-1 filter has the above characteristics can be shown as follows. Firstly, the reason why the DI-OEWT topology can achieve multilevel output and lower harmonics in output voltages is the harmonic cancellation effect between the two inverters. However, the two individual sets of shunt capacitors of the Type-1 filter break this cancellation loop. Some high-frequency harmonics, which should have been canceled, flow through these capacitors, leading

to the increase of filter burden. In other words, Type-1 filter does not make judicious use of the merit of the DI-OEWT topology.

3.2. Type-2 Filter for the DI-OEWT Topology

The above analysis suggests that the special working characteristic (the harmonic cancellation characteristic) of the DI-OEWT topology should be considered when designing the filter. The "common capacitor type filter" (here we call it "Type-2 filter") for DI-OEWT topology, which is presented in [21,22], seems to be a reasonable one, as illustrated in Figure 7. Two inverters are connected to a common shunt capacitor branch of the filter through the two inverter-side inductors, respectively. Then, the harmonic cancellation of the dual-inverter can be realized through the common capacitor branch. This common capacitor branch can be seen as the series connection of the two individual capacitor branches of the Type-1 filter, and the voltage rating of the former is the twice of the latter, so the actual value of the capacitor in Type-2 filter is half the value in Type-1 filter when the two has the same per unit (p.u.) value. Therefore, the capacitor here is represented as $C/2$.

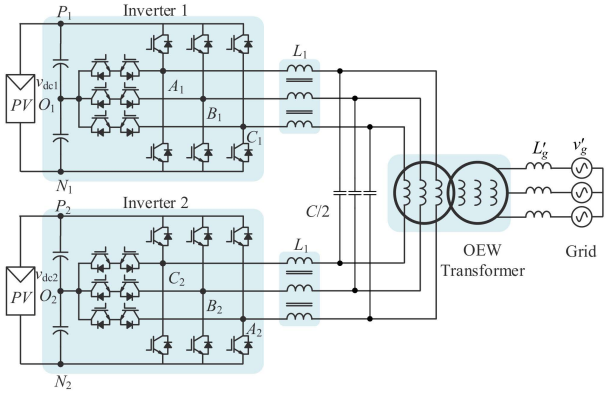

Figure 7. System configuration of the DI-OEWT topology with the Type-2 filter.

Figure 8 shows the three-phase equivalent circuit of the DI-OEWT topology with the Type-2 filter. With the same derivation method as described in Section 3.1, we can get the corresponding single-phase equivalent circuit as illustrated in Figure 9. From the figure, the transfer functions $v_{\text{inv1}}(s)$, $v_{\text{inv2}}(s)$ to $i_{\text{g}}(s)$ and $i_{\text{inv1}}(s)$ can be, respectively, calculated as

$$i_{\text{g}}(s) = \frac{1}{L_1L_2Cs^3 + (2L_1 + L_2)s}[v_{\text{inv1}}(s) - v_{\text{inv2}}(s)] \tag{8}$$

$$i_{\text{inv1}}(s) = \frac{(L_2C/2)s^2 + 1}{L_1L_2Cs^3 + (2L_1 + L_2)s}[v_{\text{inv1}}(s) - v_{\text{inv2}}(s)] \tag{9}$$

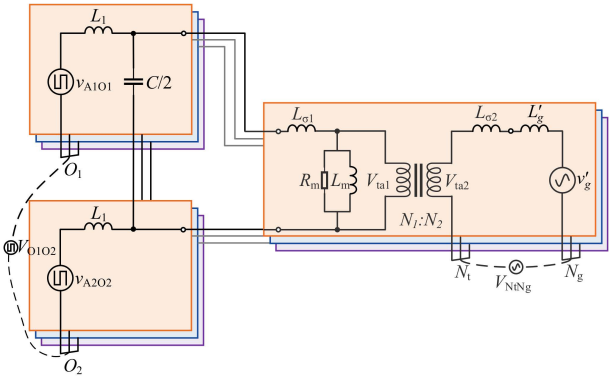

Figure 8. Three-phase equivalent circuit of the DI-OEWT topology with the Type-2 filter.

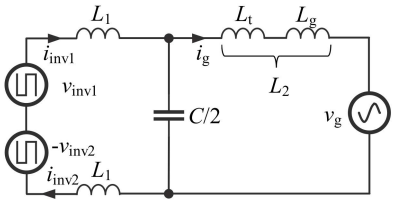

Figure 9. Single-phase equivalent circuit of the DI-OEWT topology with the Type-2 filter.

It can be found from Equations (8) and (9) that the harmonic source of i_g and i_{inv1} are all $v_{inv1} - v_{inv2}$, proves once again that the Type-2 filter does make judicious use of the merit of the DI-OEWT topology.

Figure 10 shows the bode plots of the transfer functions $v_{inv1}(s)$, $v_{inv2}(s)$ to $i_g(s)$ and $i_{inv1}(s)$ of both the LCL filter and the Type-2 filter (with the same corresponding parameters), respectively. The figures suggest that, for both i_g and i_{inv1}, Type-2 filter has superior high-frequency harmonic suppression capabilities than the LCL filter. That can lead to a decreasing in the total inductance, capacitance, and volume. Therefore, the Type-2 filter can be an option for the DI-OEWT topology.

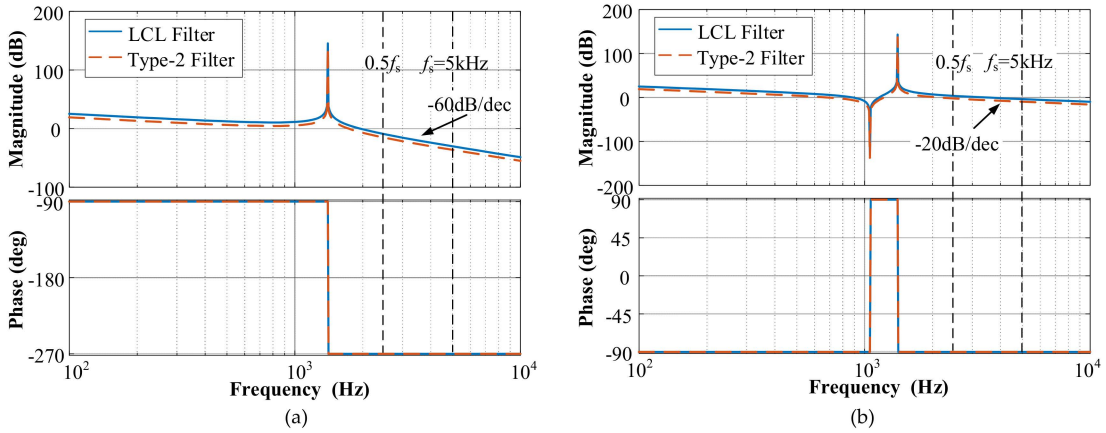

Figure 10. Bode plots of transfer functions $v_{inv1}(s)$, $v_{inv2}(s)$ to $i_g(s)$ and $i_{inv1}(s)$ in LCL filter and Type-2 filter. (**a**) $v_{inv1}(s)$, $v_{inv2}(s)$ to $i_g(s)$, (**b**) $v_{inv1}(s)$, $v_{inv2}(s)$ to $i_{inv1}(s)$.

Furthermore, look again at Figure 9, it shows that the two inverter-side inductors L_1 of the two inverters are actually connected in series, so these two inductors can merge into one single inductor, further reducing the volume and cost due to the saving of inductor magnetic cores. In this case, the complex magnetic integration method for reducing the inverter-side inductors' magnetic component size, which was proposed in [22], is actually unnecessary.

3.3. The Proposed Type-3 Filter for the DI-OEWT Topology

According to the above analysis of the existing filters for DI-OEWT topology, only Type-2 filter is suitable because its structure is fit for the working characteristic of the DI-OEWT topology. However, the leakage inductance of the transformer, which is a relatively large value in a high-power MV transformer, has not got special attention and rational utilization.

In Section 3.1, we have mentioned that the voltage of the low-voltage side of the OEW transformer is the twice of the replaced transformer. Then, it can be easy to deduce from Equation (3) that the leakage inductance of OEW transformer is four times as the replaced one (referred to the low-voltage side). Setting such a large inductance as the grid-side inductor may be not a cost-saving solution.

Therefore, in this paper, a new high order filter (here we call it "Type-3 filter") for DI-OEWT topology is proposed, as illustrated in Figure 11. The two inverters are directly connected to the low-voltage side of the OEW transformer, the shunt capacitor C'_H and grid-side inductor L'_H are set at the high voltage side of the OEW transformer. In this filter, the harmonic cancellation effect of the

DI-OEWT can be realized through the transformer, without any other shunt branch. The transformer leakage inductance L_t is used as the inverter-side inductor of the filter. If the initial value of L_t is not enough to suppress the inverter-side current ripple, it can be increased just by increasing the impedance voltage V_k of the transformer.

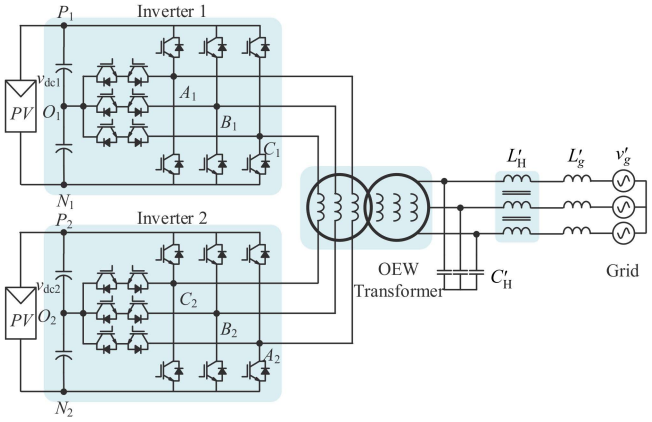

Figure 11. System configuration of the DI-OEWT topology with the Type-3 filter.

With the similar derivation method described above, here we directly give the single-phase equivalent circuit of the DI-OEWT topology with the Type-3 filter, as shown in Figure 12, where C_H and L_H represent the shunt capacitor and grid-side inductor referred to the low-voltage side, respectively.

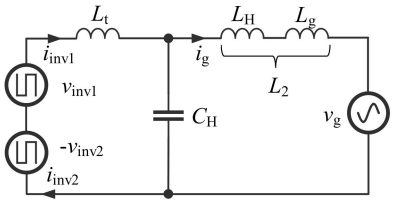

Figure 12. Single-phase equivalent circuit of the DI-OEWT topology with the Type-3 filter.

From Figure 12, the transfer functions $v_{inv1}(s)$, $v_{inv2}(s)$ to $i_g(s)$ and $i_{inv1}(s)$ can be, respectively, calculated as

$$i_g(s) = \frac{1}{(L_t L_2 C_H)s^3 + (L_t + L_2)s}[v_{inv1}(s) - v_{inv2}(s)] \tag{10}$$

$$i_{inv1}(s) = \frac{L_2 C_H s^2 + 1}{L_t L_2 C_H s^3 + (L_t + L_2)s}[v_{inv1}(s) - v_{inv2}(s)] \tag{11}$$

As can be seen from comparing Figures 9 and 12, the equivalent circuit of the Type-3 and Type-2 filter are actually the same, while the difference between them is the role of the leakage inductance of the OEW transformer. Due to this difference, the extra required capacitance and the inductance value of the two filters may be different. This different value should be compared with specific examples, which will be presented in the following section.

4. Parameter Design and Evaluations of the Filters

4.1. Parameter Design of the Filters

The design procedure of the Type-3 filter, together with the Type-1 and Type-2 filters, for the DI-OEWT topology is covered in the following. First, a 30 kW OEW dual-three-level (D3L) inverter, with 5 kHz switching frequency, 460 V~850 V (MPPT lower and upper limit voltage) DC voltage, 380 V line-to-line grid voltage is adopted. The primary side of the transformer is set as the OEW structure, and the secondary side of the transformer is connected in delta. It is worth noting that the primary

side line-to-line voltage of the transformer in conventional multi-parallel inverter topology is usually 315 V, so the phase voltage ratio of the OEW transformer used here is 364 V/380 V, where 364 V = 2 × 315 V/1.732. In the following, the filter components calculations are presented on a per-unit basis, and the corresponding base values are listed in Table 1.

Table 1. Per-unit base values of the system.

Symbol	Parameter	Formula	Value
P_B	Rated base power	-	30 kW
V_B	Ac base voltage	-	364 V
I_B	Ac base current	$P_B/(3V_B)$	27.5 A
f_B	Base frequency	-	50 Hz
Z_B	Base impedance	$3V_B^2/P_B$	13.2496 Ω
L_B	Base inductance	$Z_B/(2\pi f_B)$	42.17 mH
C_B	Base capacitance	$1/(2\pi f_B Z_B)$	240 μF

(1) Inverter-side Inductor: The inverter-side inductor value is determined by the requirement of the inverter-side current ripple, owing to the semiconductor current rating and efficiency requirement, this current ripple must be limited within a certain range. Besides, the equation for calculating the inductor value is related to the inverter topology as well as the modulation strategy, here the D3L inverter is modulated by the decoupled SVPWM strategy [17].

The decoupled SVPWM strategy has the characteristic that the total reference voltage signal is divided into two opposite parts for the two constituent inverters, and each of the inverter is switched independently of the other with the standard SVPWM strategy. Such characteristic is very appropriate for the two inverters tracking the individual MPPs. The space vector diagram of the individual three-level inverters is shown in Figure 13. In Figure 13, under the decoupled SVPWM strategy, the reference voltage space vector of the two inverters $\boldsymbol{V_{r1}}$ and $\boldsymbol{V_{r2}}$ are synthesized by the nearest three voltage vectors $\{\boldsymbol{V_0}, \boldsymbol{V_1}, \boldsymbol{V_2}\}$ and $\{V'_0, V'_3, V'_4\}$, respectively. The pulse sequence is symmetrical with seven pieces of segments in each switching cycle T_s and the dwell times for each of the voltage vectors satisfy the following expression.

$$\begin{cases} V_0T_0 + V_1T_1 + V_2T_2 = V_{r1}T_s \\ V'_0T'_0 + V'_3T'_3 + V'_4T'_4 = V_{r2}T_s \end{cases} \tag{12}$$

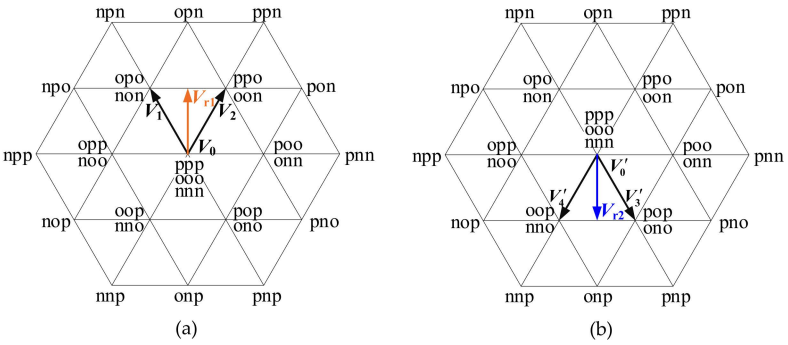

Figure 13. Space vector diagram of the individual three-level inverters. (**a**) Inverter 1, (**b**) inverter 2.

The peak to peak value of the inductor current ripple is defined by volt-seconds applied to the inductor over the switching period [32,35]. For Type-1 filter, as mentioned in Section 3.1, the harmonic source of the inverter-side current is mainly the output phase voltage of one inverter. Take inverter 1 as an instance, the maximum current ripple occurs when the zero vector $\boldsymbol{V_0}$ dwell time $T_0 = 0$, and the other two vectors $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$ equally divide the switching period, $T_1 = T_2 = T_s/2$. In such case, the modulation index M = 1/ $\sqrt{3}$ and the DC voltage of the inverter is slightly larger than the MPPT

upper limit voltage, the reference voltage vector $\boldsymbol{V_{r1}}$ is in the midway between $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$. The pulse sequence is degenerated into five pieces of segments and the corresponding inductor voltage and current waveform (take phase A1 as an example and $v_{L1} \approx v_{inv1}$) are shown in Figure 14.

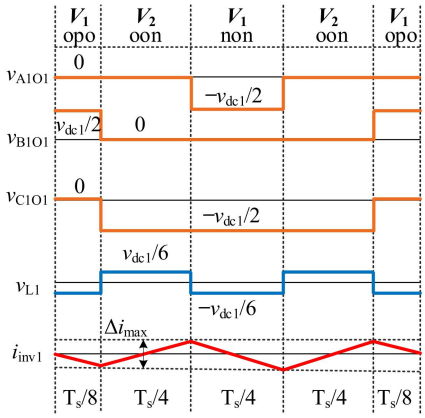

Figure 14. Phase A1 inductor voltage and current waveform.

According to the volt-second balance principle, the following expression can be got as:

$$L_1 \Delta i_{max} = \frac{v_{dc1}}{6} \frac{T_s}{4} \tag{13}$$

where Δi_{max} is the maximum current ripple.

From Equation (13), the minimum inverter-side inductor value of the Type-1 filter can be estimated by

$$L_{1min} = \frac{v_{dc1}}{24 \Delta i_{max} f_s} \tag{14}$$

where $f_s = 1/T_s$ is the switching frequency.

For Type-2 and Type-3 filter, the harmonic source of the inverter-side current is the difference between the output phase voltage of the two inverters ($v_{inv1} - v_{inv2}$). The maximum current ripple will occur in the case that the reference voltage vector $\boldsymbol{V_{r1}}$ is in the midway between $\boldsymbol{V_1}$ and $\boldsymbol{V_2}$, $\boldsymbol{V_{r2}}$ is in the midway between V′$_3$ and V′$_4$. In this case, $T_0 = T'_0 = 0$, $T_1 = T_2 = T'_3 = T'_4 = T_s/2$. For the convenience of analysis, assuming $v_{dc1} = v_{dc2} = v_{dc}$, then the inverter-side inductor voltage and current waveform of the Type-2 and Type-3 filter can be roughly derived as shown in Figure 15 (take phase A1-A2 as an example and $v_L \approx v_{inv1} - v_{inv2}$).

Accordingly, the minimum inverter-side inductor value of the Type-2 and Type-3 filter can be derived based on the volt-second balance across the inductor as

$$L_{min} = \frac{v_{dc}}{12 \Delta i_{max} f_s} \tag{15}$$

where $L = 2L_1$ for Type-2 filter and $L = L_t$ for Type-3 filter.

For the values $v_{dc} = 850$ V, $f_s = 5000$ Hz, and about 15% current ripple, the estimated minimum inverter-side inductor value for each filter can be calculated according to Equations (14) and (15) as follows:

Type-1 filter: two 0.02845 p.u. inductor;

Type-2 filter: one 0.0569 p.u. inductor;

Type-3 filter: transformer leakage inductance, 0.06 p.u..

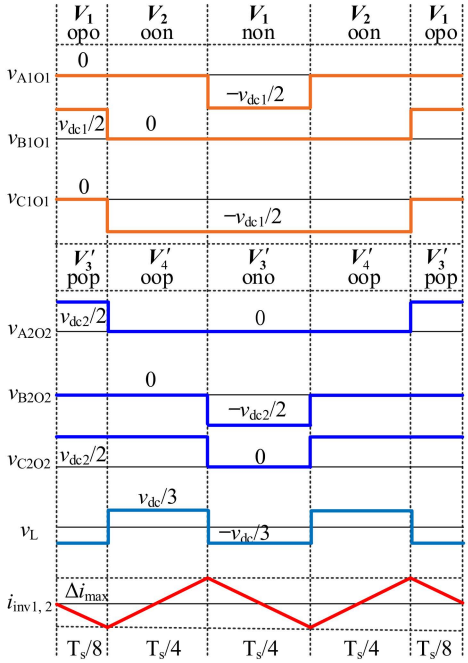

Figure 15. Phase A1-A2 inductor voltage and current waveform.

(2) Grid-side Inductor and Shunt Capacitor: The grid-side inductor and shunt capacitor together constitute a shunt network to suppress the grid current harmonics, so as to satisfy the standard. For example, recent published Chinese standard NB/T 32004-2018 [34] requires the harmonics greater than 35th should be less than 0.3% of the 30% of the rated fundamental current. Besides, the capacitor value is limited to the maximum absorbed reactive power at rated load and typically less than 5%. Moreover, the resonant frequency ω_{res} of the filter is often chosen as Equation (16) with the intention of not creating resonance problem in the lower and higher parts of the harmonic spectrum.

$$10 \times 2\pi f_B \le \omega_{res} \le 0.5 \times 2\pi f_s \tag{16}$$

where the value of ω_{res} is $\sqrt{(2L_1 + L_2)/L_1L_2C}$ for Type-1, Type-2 filter and $\sqrt{(L_t + L_2)/L_tL_2C_H}$ for Type-3 filter.

For Type-1 and Type-2 filter, the grid-side inductor value is limited by the transformer leakage inductance, and its value is 0.06 p.u. (neglect the grid inductance). The capacitor values of these two filters are computed considering the attenuation of the filter. For instance, the maximum harmonic of the grid current greater than 35th usually occurs around the switching frequency. To limit the maximum current harmonic lower than 0.3%, the capacitor value of these two filters can be computed from Equations (6) or (8) considering the most dominant harmonic $V(h)$ around the switching frequency in the inverter output voltage spectrum as

$$C \ge \frac{2\pi f_B h(2L_1 + L_2)\dfrac{I_B \times \sqrt{2} \times 30\% \times 0.3\%}{V(h)} + 1}{L_1L_2(2\pi f_B h)^3 \dfrac{I_B \times \sqrt{2} \times 30\% \times 0.3\%}{V(h)}} \tag{17}$$

where h is the most dominant harmonic order. For D3L inverter with the decoupled SVPWM, if the DC voltage and the power (or the modulation index) of the two inverters are all the same, the harmonic around the switching frequency can be totally cancelled. But when the two inverters are tracking the individual MPPs, the DC voltage and the power (or the modulation index) of the two inverters may be different, this total cancellation cannot be realized. Assuming the worst case that no harmonic

cancellation occurs around the switching frequency harmonics, the most dominant harmonic order $h = m_f - 2$, the value of the $(m_f - 2)$ order harmonic can be got from simulation on a single three-level inverter as $V(m_f - 2) \approx 0.055$ p.u. (20.2 V), where m_f is the modulation frequency index, and the value here is 100 (5000 Hz/50 Hz). Then from Equation (17) a minimum value of C can be calculated as 0.0175 p.u. Considering the constraints illustrated in Equation (16) and taking a certain margin, the final capacitor value of Type-1 and Type-2 filter is chosen as 0.0208 p.u.

For Type-3 filter, both the grid-side inductor and the shunt capacitor need to be designed. Usually, we choose a larger capacitor to reduce the requirement of the grid-side inductor for saving cost. Here the capacitor is starting with the value as 0.0416 p.u. With the same methodology as above, to ensure the grid current to satisfy the harmonic requirement, the grid-side inductor value can be computed from Equation (10) as

$$L_2 \geq \frac{2\pi f_B h L_t \frac{I_B \times \sqrt{2} \times 30\% \times 0.3\%}{V(h)} + 1}{2\pi f_B h \left[L_t C [2\pi f_B h]^2 - 1\right] \frac{I_B \times \sqrt{2} \times 30\% \times 0.3\%}{V(h)}} \tag{18}$$

Also, considering the value of the most dominant harmonic order $V(m_f - 2) \approx 0.055$ p.u., a minimum value of L_2 can be calculated as 0.0218 p.u.. Considering (16) and taking a certain margin, the final value of L_2 is selected as 0.0237 p.u.

4.2. Fault-Tolerant Configuration for DI-OEWT Topology

Like the multi-parallel inverter topology, one of the advantages of the DI-OEWT topology is the availability of fault-tolerant operation. Many papers have investigated the fault-tolerant method for the dual-inverter topology used in motor drives, such as hybrid modulation strategies [18], dual-inverter topology reconfiguring method [19], fault-tolerant direct thrust force control method [20]. However, these methods are not suitable for the DI-OEWT topology used in photovoltaic applications, due to the DC voltages and power of the two inverters in such case are often different for the separate MPPT purpose.

To realize fault-tolerant operation in these systems, a more reasonable way is to cut off the fault inverter while allowing the healthy inverter to continue working. However, only one inverter cannot supply the whole voltage of the transformer due to the DC voltage limit, so the OEW transformer need to be reconfigured. Figure 16 presents a possible configuration to achieve the above purpose. As shown in the figure, a center-tapped (at the low voltage side) OEW transformer is used here, S_1 and S_2 are the contactors of the respective inverters connecting to the open-end windings of the transformer, S_3 is the contactor to short the three-phase center-taps. In case of a fault in one inverter, the corresponding contactor (S_1 or S_2) of the fault inverter is switched off, and contactor S_3 is switched on, then half of the primary windings are connected in star across the healthy inverter. The healthy inverter only needs to supply half of the original AC voltage, so that it can still work properly without any change.

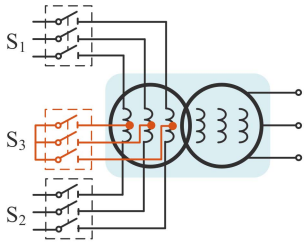

Figure 16. Fault-tolerant configuration of the DI-OEWT topology.

Nevertheless, considering the configurations of the filters described above, not all types of filters are applicable for the presented fault-tolerant scheme. For DI-OEWT topology with the Type-1 and the

proposed Type-3 filter, when a fault occurs in one inverter, the healthy inverter can still work through the modified filter. While for DI-OEWT topology with the Type-2 filter, fault-tolerant operation cannot be realized because the shunt capacitor cannot decouple from the faulty inverter.

4.3. Summary and Discussion

The designed parameters of the three kinds of filters, as well as the applicability of the presented fault-tolerant scheme on the filters, are summarized in Table 2.

Table 2. Comparison of the three kinds of filters.

Filters	Type-1 Filter	Type-2 Filter	Type-3 Filter
Inverter-side Inductor	0.02845 p.u. × 2 with 2 magnetic cores	0.0569 p.u. with 1 magnetic core	Tr leakage inductance 0.06 p.u.
Grid-side Inductor	Tr leakage inductance 0.06 p.u.	Tr leakage inductance 0.06 p.u.	0.0237 p.u.
Shunt CapacitoR	0.0208 p.u.	0.0208 p.u.	0.0416 p.u.
Total Inductance	0.1169 p.u.	0.1169 p.u.	0.0837 p.u.
Fault-tolerant applicability	Yes	No	Yes

Note: Tr represents the OEW transformer.

From analyzing the table, the followings can be seen.

(1) The Type-1 and Type-2 filter have the same filter parameters, but the inverter-side inductor of the Type-1 filter needs two magnetic cores while the Type-2 filter only needs one, which means the Type-2 filter has a smaller size and cost than the Type-1 filter.

(2) Besides the transformer leakage inductance, the value of the extra inductance requirement of the Type-3 filter is reduced by a factor of 58.35%, while the capacitance requirement is increased about 50%, compared to the Type-1 and Type-2 filter.

(3) The total inductance of the Type-1 and Type-2 filter is more than 10% of the system base inductance, which may cause a larger fundamental voltage drop across the inductor and increase the DC voltage lower limit value.

(4) Unlike the Type-1 and Type-3 filter, the DI-OEWT topology with the Type-2 filter cannot realize fault-tolerant operations with the presented fault tolerate scheme.

(5) In terms of the inductance requirement, magnetic cores numbers and the fault-tolerant applicability, the proposed Type-3 filter has a certain advantage over the existing Type-1 and Type-2 filter.

5. Experiment Results

5.1. Experiment Setup Description

To verify the above analysis and design methodology, a 30 kW three-phase D3L inverter fed open-end winding transformer prototype based on DSP TMS320F28377D controller is constructed, as shown in Figure 17. The D3L inverter is supplied by two rectifiers (DC Source 1 and 2) with the DC voltage v_{dc} = 850 V. The switching frequency of the inverter is 5 kHz. For the OEW transformer, the phase voltage ratio is 364 V/380 V, the leakage inductance is about 0.025 p.u., we compensate it to 0.06 p.u. through adding extra inductors.

The designed parameters of the three kinds of filters tabulated in Table 2 are tested by experiment. Here the D3L inverter with different filters are divided into three cases, where Case-1 represents the D3L inverter with the Type-1 filter, Case-2 represents the D3L inverter with the Type-2 filter, and Case-3 represents the D3L inverter with the Type-3 filter. In addition, the experimental analysis is carried out in two operating modes. One is the two inverters of the D3L inverter working at the power balance mode. Another one is the two inverters of the D3L inverter working at the power unbalance

mode. Here, the power ratio of the two inverters is chosen as 3/2, corresponding to a relatively large imbalance ratio of 33.33%. Besides, to suppress the resonance caused by the high order filter, the filter based active damping method [36] is used here.

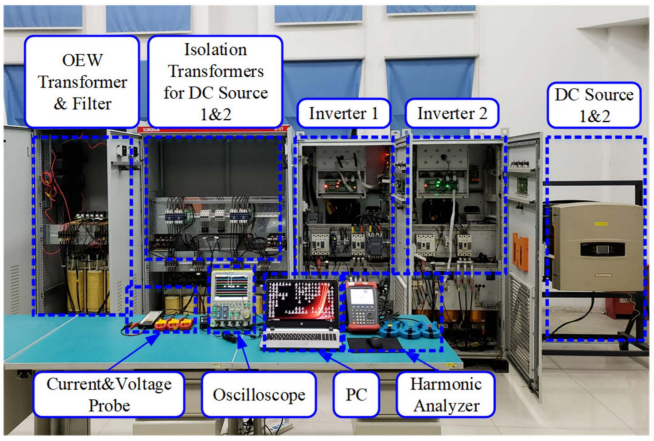

Figure 17. Experimental platform of the DI-OEWT grid-tied system.

5.2. Inverter-Side Current Analysis

Figures 18–20 show the experimental measured inverter-side currents and the corresponding fast Fourier transformation (FFT) waveforms of the three cases in power balance mode, respectively. From Figure 18a, Figure 19a, and Figure 20a, the inverter-side current ripple at the rated load in the three cases are around 14.9%, 14.6%, and 14.1%, respectively, which are roughly in agreement with the value calculated by Equations (14) and (15). From the FFT waveforms of the inverter-side currents as illustrated in Figure 18b, Figure 19b, and Figure 20b, it can be noticed that the current harmonics around the switching frequency are roughly canceled out in Case-2 and Case-3, but still exist in Case-1. The results demonstrate the analysis in Section 3 that the two individual sets of shunt capacitors of the Type-1 filter break the harmonic cancelation loop, causing the harmonics which should have been canceled still exist in the inverter-side current.

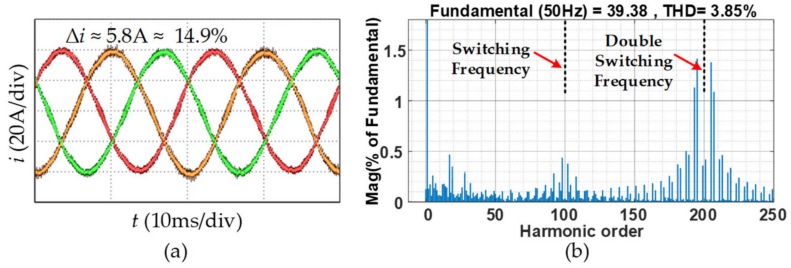

Figure 18. Inverter-side current experimental waveforms of Case-1 in power balance mode. (**a**) Inverter-side current and current ripples. (**b**) FFT waveforms of the inverter-side current.

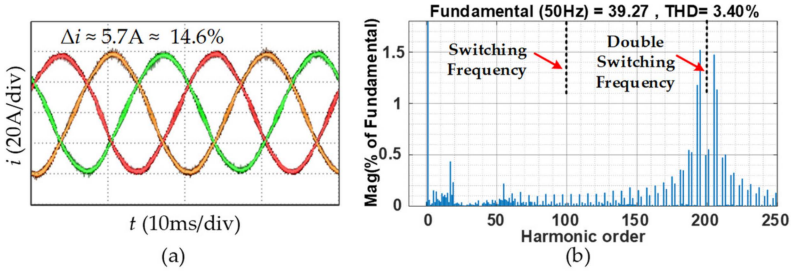

Figure 19. Inverter-side current experimental waveforms of Case-2 in power balance mode. (**a**) Inverter-side current and current ripples. (**b**) FFT waveforms of the inverter-side current.

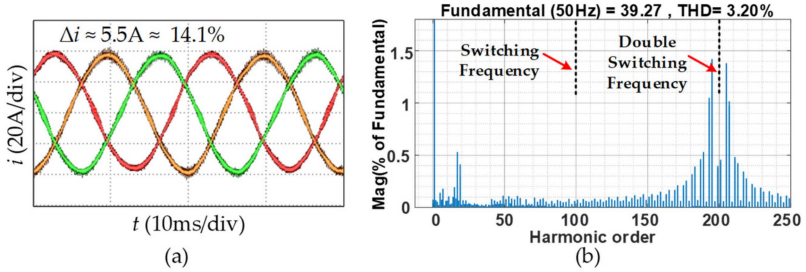

Figure 20. Inverter-side current experimental waveforms of Case-3 in power balance mode. (**a**) Inverter-side current and current ripples. (**b**) FFT waveforms of the inverter-side current.

The experimental measured inverter-side currents and the corresponding FFT waveforms of the three cases in power unbalance mode are shown in Figures 21–23, respectively. Observing these figures, when the D3L inverter is working in power unbalance mode, the inverter-side current ripple of the three cases are around 14.6%, 14.4%, and 13.8%, respectively, which are still within the design limit. Besides, as observed from Figures 22b and 23b, the harmonics around the switching frequency also exist in the inverter-side currents in Case-2 and Case-3, which means that the total harmonic cancellation around the switching frequency cannot be realized in power unbalance mode.

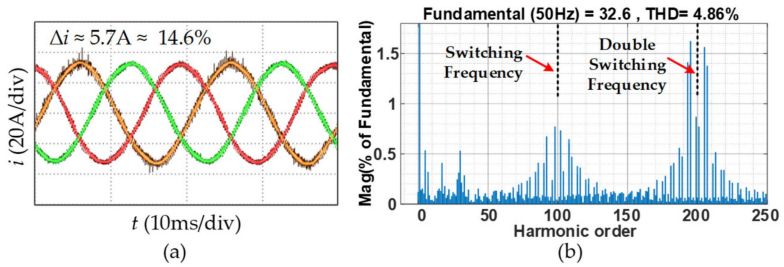

Figure 21. Inverter-side current experimental waveforms of Case-1 in power unbalance mode. (**a**) Inverter-side current and current ripples. (**b**) FFT waveforms of the inverter-side current.

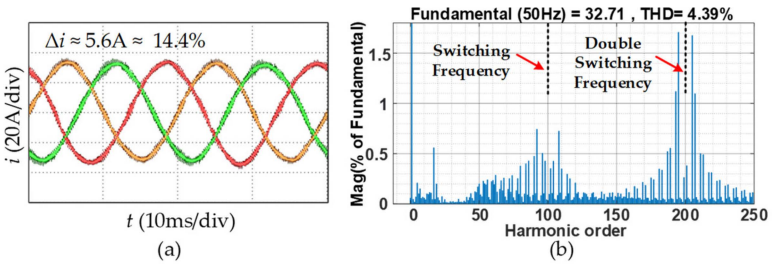

Figure 22. Inverter-side current experimental waveforms of Case-2 in power unbalance mode. (**a**) Inverter-side current and current ripples. (**b**) FFT waveforms of the inverter-side current.

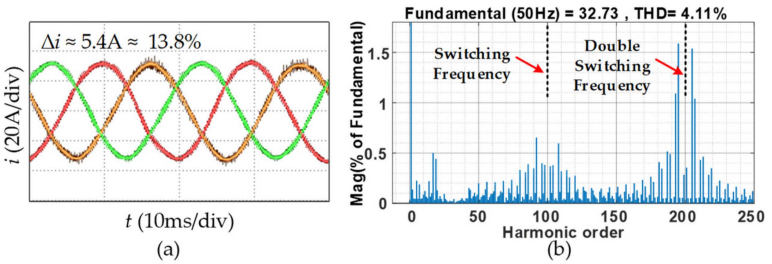

Figure 23. Inverter-side current experimental waveforms of Case-3 in power unbalance mode. (**a**) Inverter-side current and current ripples. (**b**) FFT waveforms of the inverter-side current.

5.3. Grid Current Analysis

The experimental tests for the grid current are conducted at 30% load to verify whether the current quality satisfies the grid standard [34]. Figures 24 and 25 show the grid current waveforms and the corresponding harmonic spectrums of the three cases in power balance mode, respectively. Figures 26 and 27 show the grid current waveforms and the corresponding harmonic spectrums of the three cases in power unbalance mode, respectively. The test cases along with the grid current THD and the dominating current harmonic amplitude percentage (higher than 35th) are summarized in Table 3. As observed from the table, even though the inverter is working at 30% load, the current THD are all still below the 5% [34] limit, and the dominant harmonics (higher than 35th) are all within the 0.3% limit as well.

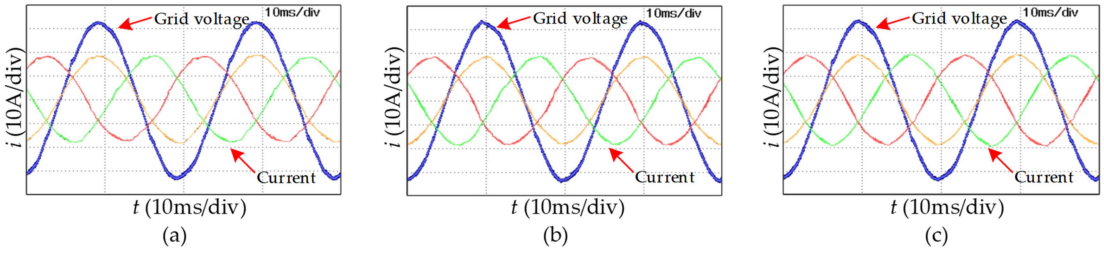

Figure 24. Grid current experimental waveforms of the three cases in power balance mode. (**a**) Case-1. (**b**) Case-2. (**c**) Case-3.

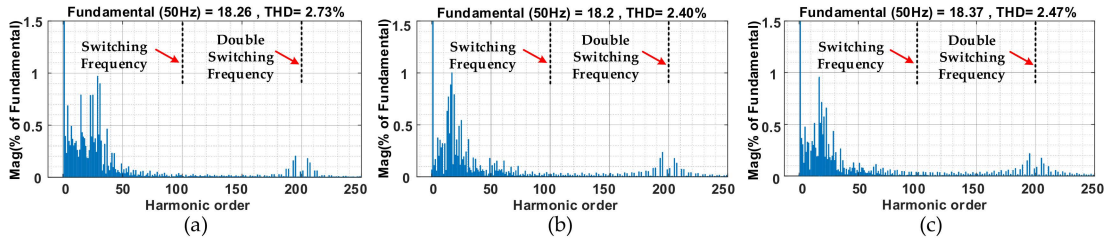

Figure 25. Grid current FFT waveforms of the three cases in power balance mode. (**a**) Case-1, (**b**) Case-2, (**c**) Case-3.

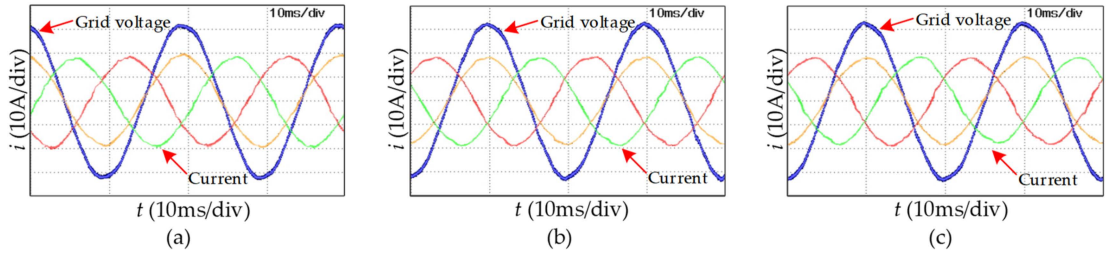

Figure 26. Grid current experimental waveforms of the three cases in power unbalance mode. (**a**) Case-1, (**b**) Case-2, (**c**) Case-3.

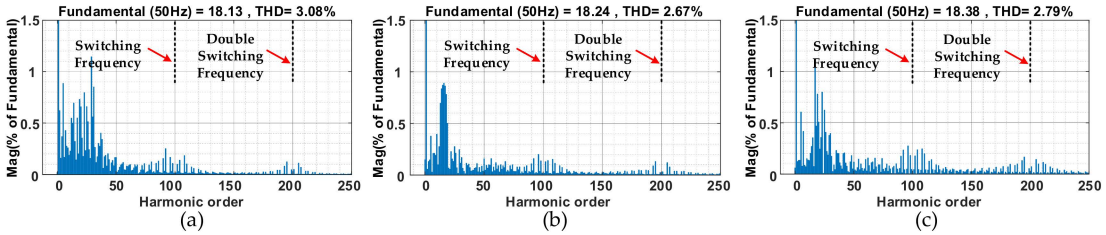

Figure 27. Grid current FFT waveforms of the three cases in power unbalance mode. (**a**) Case-1, (**b**) Case-2, (**c**) Case-3.

Table 3. THD and dominant harmonic percentage of grid current in different cases and modes.

Cases	**Case-1**		**Case-2**		**Case-3**	
Working Modes	Balance	Unbalance	Balance	Unbalance	Balance	Unbalance
THD	2.73%	3.08%	2.4%	2.67%	2.47%	2.79%
Dominant Harmonic Percentage	0.2%	0.25%	0.22%	0.2%	0.21%	0.28%

In summary, the analysis of the experimental inverter-side currents and the grid currents of all cases confirms the effectiveness of the filters' parameters designed using the proposed method. Consequently, the discussions in Section 4.3 can be confirmed as well.

6. Conclusions

This paper investigates the filters for the DI-OEWT topology used in the photovoltaic grid-tied applications. The equivalent circuits of the existing Type-1 and Type-2 filter are derived in detail, and the corresponding harmonic suppression transfer functions are given. Some findings can be obtained from analyzing these equivalent circuits and the transfer functions, as well as comparing with the LCL filter used in the multi-parallel inverter topology. It can be found that Type-1 filter does not make judicious use of the merit (output harmonic cancellation) of the DI-OEWT topology, because its two individual sets of shunt capacitors break the cancellation loop. Another finding is that the two inverter-side inductors of the Type-2 filter are actually connected in series and can be merged into one single inductor to further reduce the filter volume and cost.

From the analysis of the existing filters and with consideration of the large leakage inductance value of the high power MV transformer, a new high order filter (named Type-3 filter) for DI-OEWT topology is also proposed. Unlike the existing filters, in which the transformer leakage inductance is set as the grid-side inductor, the Type-3 filter set the leakage inductance as the inverter-side inductor. Such an arrangement can maximize the transformer leakage inductance utilization, so as to reduce the requirement of the extra inductance.

A brief parameter design method for the three kinds of filters is also introduced. With the design examples of the three filters, the extra inductance requirement of the Type-3 filter can have a 58.35% higher reduction than the Type-1 and Type-2 filters. In addition, a fault tolerance scheme for DI-OEWT topology is also presented in the paper, but only Type-1 and Type-3 filters are applicable for the scheme. Finally, through evaluating the three filters in terms of the inductance requirement, magnetic core number and applicability for the fault tolerance scheme, the proposed Type-3 filter has a certain advantage over the existing Type-1 and Type-2 filters.

Experimental results of a 30 kW D3L inverter prototype verify the effectiveness of the proposed filter design method and validity of the analysis.

Besides the stability analysis, damping methods of the dual-inverter with the filters are also important issues, we will focus on these topics in future research.

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Nomenclature

List of Abbreviations

LCL	inductor-capacitor-inductor
MV	medium-voltage
DI-OEWT	dual-inverter fed open-end winding transformer
NPC	neutral point clamp
VSI	voltage source inverter
MPPT	maximum power point tracking
SCR	short-circuit ratio
OEW	open-end winding
CM	common-mode
KVL	Kirchhoff's voltage law
FFT	fast Fourier transformation
p.u.	per unit

List of Symbols

v_{inv1}	inverter 1 output phase voltage
v_{inv2}	inverter 2 output phase voltage
i_{inv1}	inverter 1 output phase current
i_{inv2}	inverter 2 output phase current
v_{g}	grid voltage
i_{g}	grid current
L_1	inverter-side inductor
L_{t}	transformer leakage inductance
L_{g}	grid inductance
L_2	combined inductance of L_{t} and L_{g}
C	filter capacitor
C'_{H}	shunt capacitor of Type-3 filter
L'_{H}	grid-side inductor of Type-3 filter
C_{H}	shunt capacitor of Type-3 filter referred to the low-voltage side
L_{H}	grid-side inductor of Type-3 filter referred to the low-voltage side
V_{k}	impedance voltage
P_{rated}	system rated power
f_0	fundamental frequency
V_{X1O1}	pole voltage of phase X_1 of inverter 1, $X = A,B,C$
V_{X2O2}	pole voltage of phase X_2 of inverter 2
V_{O1Nc1}	CM voltage of inverter 1
V_{O2Nc2}	CM voltage of inverter 2
V_{Nc1Nc2}	voltage across the two capacitor common points N_{c1}, N_{c2}
V_{NtNg}	voltage across N_{t} and N_{g}
V_{CX1}	voltage on filter capacitor of phase X_1
V_{CX2}	voltage on filter capacitor of phase X_2
$V_{\text{L}\sigma\text{1X}}$	phase X voltage on the leakage inductance at transformer low voltage side ($L_{\sigma 1}$)
$V_{\text{L}\sigma\text{2X}}$	phase X voltage on the leakage inductance at transformer high voltage side ($L_{\sigma 2}$)
V_{LgX}	phase X voltage on the grid inductance
V_{tX1}	voltage of the low voltage side of the MV transformer
V_{tX2}	voltage of the high voltage side of the MV transformer
v'_{gX}	phase X voltage of the MV grid
v_{dc1}	DC voltage of inverter 1
v_{dc2}	DC voltage of inverter 2
ω_{res}	filter resonant frequency
T_{s}	switching period
f_{s}	switching frequency
m_{f}	modulation frequency index
h	dominant harmonic order

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