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Investigate on a Simplified Multi-Port Interline DC Power Flow Controller and Its Control Strategy

Wen Wu [1], Xuezhi Wu [1,2,*], Long Jing [1] and Jingyuan Yin [3]

[1] National Active Distribution Network Technology Research Center, Beijing Jiaotong University, Beijing 100044, China
[2] Collaborative Innovation Center of Electric Vehicles, Beijing 100044, China
[3] The Institute of Electrical Engineering Chinese Academy of Sciences, Beijing 100190, China
* Correspondence: xzhwu@bjtu.edu.cn; Tel.: +86-135-0129-1928

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Abstract: A DC power flow controller (DCPFC) can help to facilitate power flow routing in the multi-terminal high-voltage direct current (HVDC) transmission system. Realizing its multi-port output can effectively improve the device regulate range and capability. Based on analysis of the traditional multi-port interline DC power flow controller (MI-DCPFC), this paper presents a switches reduced topology of MI-DCPFC. In addition, for solving the problem of coupling of the port-output voltage of the traditional MI-DCPFC, a novel control strategy based on carrier phase shifting pulse width modulation (CPS-PWM) is proposed. It implements the decoupling of the port-output voltage of MI-DCPFC, which can ensure completely independent tracking of the power flow regulating commands for different controlled lines. Moreover, key relationships between the system state variables are also analyzed and detailed in this study. Finally, the performance of the proposed controller and control strategy are confirmed with the simulation and experiment studies under different conditions.

Keywords: multi-terminal HVDC transmission system; DC power flow control; multi-port topology; decoupling; control strategy

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1. Introduction

Realizing the development and utilization of green and clean energy has become a major trend to solve problems such as traditional energy shortages and environmental degradation. To ensure the consumption and efficient use of the large scale new energy, effective transmission technology is needed as a support [1]. As the multi-terminal high-voltage direct current (HVDC) transmission system has the advantages of long transmission distance capability, large capacity and a flexible operation mode, etc., it has therefore become one of the main means to facilitate grid connections of large-scale renewable energy [2].

Unreasonable distribution of the transmission line currents can introduce unnecessary transmission line losses, or even an overload of the converter station. In order to facilitate the power flow management inside the DC transmission network, inspired by the idea of power flow control devices developed in the AC transmission system, such as a unified power-flow controller (UPFC) and thyristor controlled series compensator (TCSC), a DC power flow controller (DCPFC) can be introduced in the multi-terminal HVDC transmission system [3]. However, since the DC system does not have reactive power, reactance and phase angle, its power flow control can only be realized by adjusting the resistance or DC voltage

of the transmission line. Therefore, there are two general design approaches for the DCPFC, which are a resistance control type and a DC voltage control type.

(1) For the resistance control type DCPFC, different implementation schemes have been designed in reference [4] and reference [5]. This kind of control scheme is simple to implement, but it can only adjust the equivalent resistance of the line in one direction, which limits its power flow control ability.

(2) For the DC voltage control type DCPFC, according to the voltage regulation means, it can be further divided into three main types, which are ① a DC transformer type [6–10], ② an auxiliary voltage source type [11–15] and ③ a capacitor-based interline energy-exchanged type [3,16–24]. In comparison, the DCPFC of capacitor-based interline energy-exchanged type has more advantages and better application prospects. For instance, it has fewer power devices; does not require an external power supply device; and can avoid withstanding the system-level high voltage and power, which help reduce the stress requirements of the power devices and system losses. Therefore, it has become a kind of DCPFC which is currently more researched and heavily focused on [3,20].

The capacitor-based interline energy-exchanged type DCPFC is usually called the interline DCPFC (IDCPFC). As shown in Figure 1, its main control idea is to exchange the power between different transmission lines by charging/discharging the capacitor of IDCPFC, thereby achieving the power flow control of the transmission lines. Based on the concept depicted in Figure 1a, two current flow controller (CFC) topologies were first proposed in reference [16], however, only the basic conceptualization is introduced, its working principles and control method are not investigated enough. Focus on one topology of the CFC, its control strategy and operation principles were discussed in reference [17]. Focus on the control method of another method was designed in references [18,19]. In addition, its operation states were analyzed, and an average mode which can be used for perform steady-state analysis was derived in reference [19]. Furthermore, in order to simplify the CFC circuit structure, an improved CFC topology was proposed in reference [20], and its characteristics were detailed compared to the traditional CFC topology proposed in reference [16]. Based on the concept depicted in Figure 1b, by increasing the DC capacitor number and introducing coupled inductors, a novel type of IDCPFCs with independent connections of the capacitor in two lines were respectively investigated in references [3,21–23]. In reference [24], the application modular multilevel converter (MMC) device was also considered, and an MMC-based IDCPFC was proposed. These schemes in reference [3,21–24] avoided the capacitor switching in the line. However, it should be noted that all the above existing topologies are characterized by two-port characteristics, which can only assist in regulating the current on one line. If the power flow control of multiple lines is required at the same time, the corresponding multi-port topology should be developed, and this problem is also an area that this paper deals with.

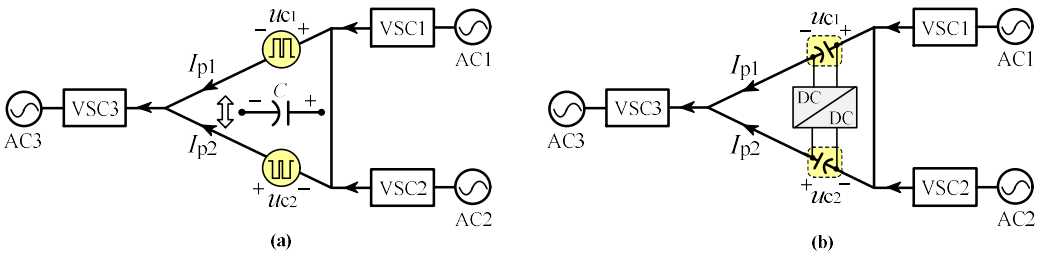

Figure 1. Schematic diagrams of the IDCPFC control principle: (**a**) The single-capacitor control type in references [16–20]; (**b**) The dual-capacitor control type in references [3,21–24].

Currently, the research on multi-port IDCPFC (MI-DCPFC) is still in its infancy. Based on the MMC-based IDCPFC proposed in reference [24], a MI-DCPFC topology based on MMC was developed in reference [25]. However, it requires multi-winding transformers and needs to connect MMC in each

control line, which leads to higher system costs. In addition, with the controlled line number being increased, its circuit topology and control system become relatively complicated. In reference [26], a MI-DCPFC topology based on identical insulated gate bipolar transistor (IGBT) half-bridge was proposed. Its system structure is simple, and the cost of the port expansion is low. However, as only a basic control method is introduced, it can not achieve independent tracking of the current regulation commands for each transmission line, where the power flow regulating has limited freedom.

Combining the precious work in reference [26], this paper presents a switches reduced topology of MI-DCPFC. In addition, for solving the problem of coupling of the port-output voltage of the traditional MI-DCPFC, a novel control strategy based on carrier phase shifting pulse width modulation (CPS-PWM) is proposed. This strategy achieved the decoupling of the port-output voltage, which can ensure independent tracking of the power flow regulating commands for different controlled lines. Moreover, key relationships between the system state variables were also detailed in this study. Finally, two five-terminal HVDC transmission systems were developed, and the performance of the proposed controller and control strategy were confirmed with the simulation and experiment studies under different conditions. The remainder of this paper is organized as follows: the traditional MI-DCPFC including its topology and control strategy is analyzed in Section 2. The topology and operation principles of the simplified MI-DCPFC are analyzed in Section 3. The novel control strategy is designed and the relationships between the system state variables are discussed in Section 4. The simulation and experiment verifications are respectively carried out in Section 5 and 6. Finally, a conclusion is given in Section 7.

2. Analysis of the Traditional MI-DCPFC

2.1. Multi-Terminal HVDC Transismion System

The following work actually can be applied to any high voltage direct current (HVDC) transmission system. For this study, in order to facilitate the verification of the three- and four-port multi-port interline DC power flow controller (MI-DCPFC) in the subsequent simulations and experiments, a monopole five-terminal HVDC transmission system, as shown in Figure 2, was adopted as an example to carry out the related analysis. The voltage source converter (VSC) 4 is set as the DC voltage regulator node, which operates in the constant DC voltage control mode; The VSC1-3 and VSC5 are set as power regulator nodes, which operate in the constant power control mode.

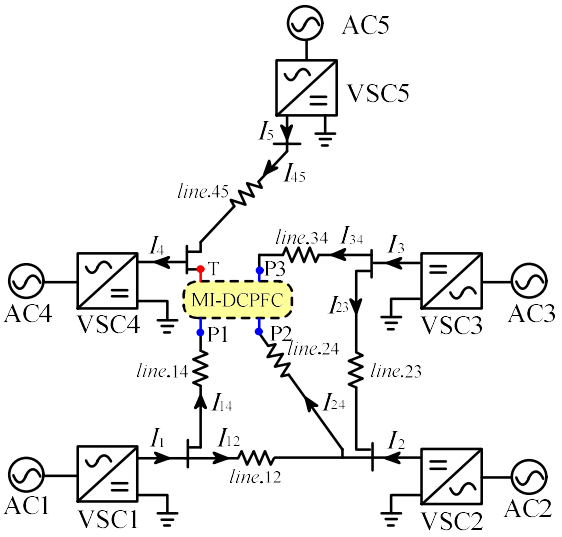

Figure 2. Diagram of the five-terminal HVDC transmission system with a three-port MI-DCPFC.

2.2. Traditional Topology

The schematic diagram of traditional MI-DCPFC is shown in Figure 3. For a three-port topology, it consists of six IGBT half-bridges (HBs) and a common capacitor C. S_{ai} (I = 1, 2, 3) and S_{bi} are the upper and lower switches of HB_0, HB_1, HB_2, respectively. S_{ci} and S_{di} are the upper and lower switches of HB_3, HB_4, HB_5, respectively. In addition, as depicted in Figure 2, when the MI-DCPFC is accessed in the transmission system, its terminal T is connected to the bus convergence point of the different power regulator nodes, that is, the DC bus side of VSC4. Meanwhile, its terminals P_i are respectively connected to the different transmission lines, that is, the DC bus side of VSC1 to 3.

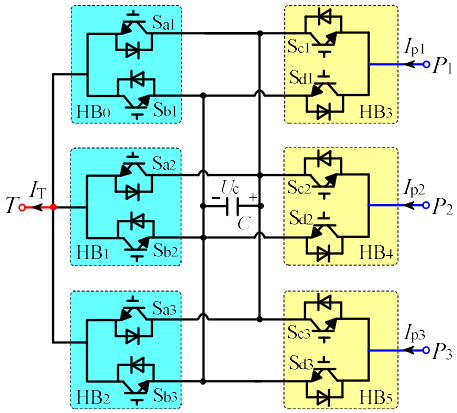

Figure 3. Topology of the traditional three-port MI-DCPFC [26].

2.3. Traditional Control Method

According to different line current directions and different control targets, there are total 12 working modes of the traditional three-port MI-DCPFC, which are shown in Table 1. Under the traditional control method, the switches S_{ai} (i = 1, 2, 3) and S_{bi} are pulsed by the obtained PWM signals under the forward and reverse direction, respectively. On this basis, all other swtiches remain in the on or off state, where the specific conduction states of the switches S_{ci} and S_{di} are shown in the Table A1 in the Appendix A. Take the working-modes 1 and 6 as examples to provide further analysis, respectively.

Table 1. Working-modes of the traditional three-port MI-DCPFC.

Mode	Direction	Reduced	Increased	Switching States					
				S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}
1	forward	I_{p1}	I_{p2} and I_{p3}	(Command) I_{pi}^* + − PI Comp S_{ai} ; I_{pi} (Reduced current)			off		
2	forward	I_{p2}	I_{p1} and I_{p3}						
3	forward	I_{p3}	I_{p1} and I_{p2}						
4	forward	I_{p1} and I_{p2}	I_{p3}						
5	forward	I_{p1} and I_{p3}	I_{p2}						
6	forward	I_{p2} and I_{p3}	I_{p1}						
7	reverse	I_{p1}	I_{p2} and I_{p3}	off			(Command) I_{pi}^* + − PI Comp S_{bi} ; I_{pi} (Reduced current)		
8	reverse	I_{p2}	I_{p1} and I_{p3}						
9	reverse	I_{p3}	I_{p1} and I_{p2}						
10	reverse	I_{p1} and I_{p2}	I_{p3}						
11	reverse	I_{p1} and I_{p3}	I_{p2}						
12	reverse	I_{p2} and I_{p3}	I_{p1}						

Figure 4 shows the conduction diagrams of the traditional MI-DCPFC under working-mode 1. The shunt branches connected to the terminals P_1, P_2 and P_3 are respectively named line 1, line 2 and line 3. According to the conduction states of the switches S_{ai}, the working process can be divided into the following two stages:

(i) Stage 1: switches S_{ai} are truned-off. During this period, as shown in Figure 4a, the current I_{p1} is charging the capacitor through the feedback diodes of S_{b1} and S_{c1}, while the currents I_{p2} and I_{p3} are flowing out directly through the S_{d2}, feedback diode of S_{b2} and S_{d3}, feedback diode of S_{b3}, respectively.

(ii) Stage 2: switches S_{ai} are truned-on. During this period, as shown in Figure 4b, the current I_{p1} is flowing out directly through the S_{a1} and feedback diode of S_{c1}, while the currents I_{p2} and I_{p3} are discharging the capacitor through S_{a2}, S_{d2} and S_{a3}, S_{d3} respectively. The charging and discharging states are kept interchanging to transfer the power from line 1 to lines 2 and 3. As a result, the the current I_{p1} is reduced, I_{p2} and I_{p3} are increased.

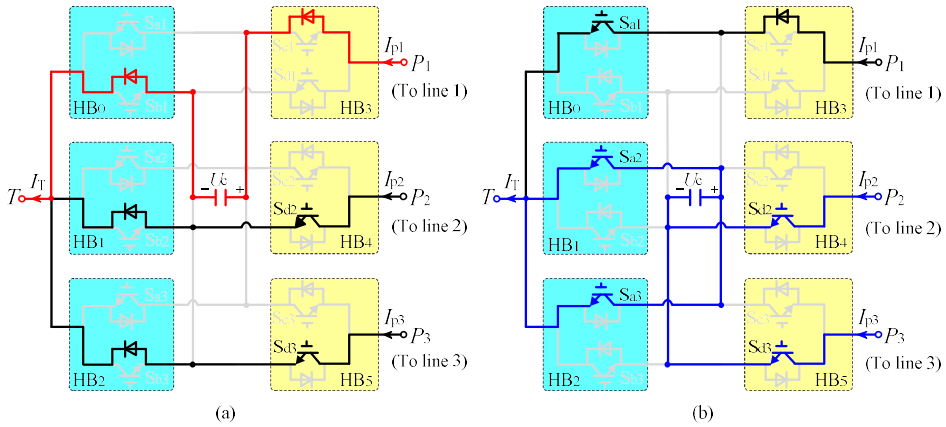

Figure 4. Conduction diagrams of the traditional MI-DCPFC under working-mode 1: (**a**) conduction diagram during stage 1; (**b**) conduction diagram during stage 2.

Figure 5 shows the conduction diagrams of the traditional MI-DCPFC under working-mode 6. According to the conduction states of the switches S_{ai}, the working process can also be divided into two stages. (i) Stage 1: switches S_{ai} are truned-off. During this period, as shown in Figure 5a, the current I_{p2} and I_{p3} is charging the capacitor, while the current I_{p1} is flowing out directly. (ii) Stage 2: switches S_{ai} are turned-on. During this period, as shown in Figure 5b, the current I_{p2} and I_{p3} was flowing out directly, while the currents I_{p1} was discharging the capacitor to transfer the power from lines 2 and 3 to line 1. As a result, the current I_{p1} was increased, while I_{p2} and I_{p3} were reduced.

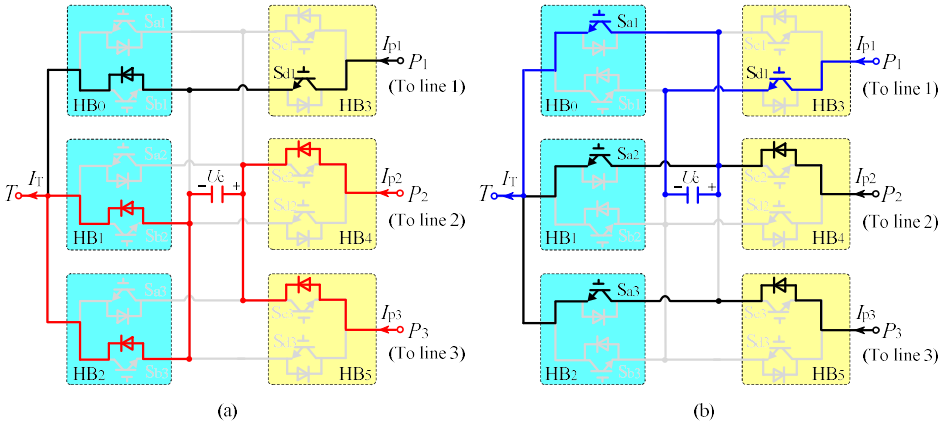

Figure 5. Conduction diagrams of the traditional MI-DCPFC under working-mode 6: (**a**) Conduction diagram during stage 1; (**b**) conduction diagram during stage 2.

2.4. Summarizing of the Traditional Topology and Control Strategy

Concluding the analysis in the previous section, we found that:

(1) When completing the conduction states selection for the switches S_{ci} and S_{di} in combination with Table A1, MI-DCPFC can achieve the power flow control by only pulsing the switches S_{ai} or S_{bi} under different working-modes. In addition, we can further observe that the switches S_{ai} and S_{bi} are always pulsed synchronously in the forward and reverse direction, respectively. Therefore, the switches S_{ai} and S_{bi} actually can be simplified as the upper switch and lower switch in one half-bridge, respectively.

(2) In the working-mode 1, the reduction control of I_{p1} can be realized by pulsing the switches S_{ai} with the obtained PWM signal. However, the lines 2 and 3 are always synchronized to discharge the capacitor, so the equivalent reverse polarity voltages introduced to the lines 2 and 3 are equal, which indicates that the specific increased amounts of the currents I_{p2} and I_{p3} cannot be controlled separately under the tradition control.

(3) In the working-mode 6, the reduction control of I_{p2} and I_{p3} can be simultaneously realized by also pulsing the switches S_{ai}. However, the lines 2 and 3 are always synchronized to charge the capacitor, so the equivalent forward polarity voltages introduced to the lines 2 and 3 are equal, which indicates that the specific reduced amounts of the currents I_{p2} and I_{p3} cannot be controlled separately under the tradition control.

(4) Generalizing the conclusions (ii) and (iii), it shows that among all the lines connected to MI-DCPFC, if there are multiple line currents that will be increased, an improved control strategy needs to be proposed to ensure that their respective increased values can be controlled independently. Similarly, if there are multiple line currents that will be reduced, the improved control strategy also needs to guarantee their respective reduced values can be independently controlled.

3. Topology and Operation Principles of the Simplified MI-DCPFC

3.1. Topology

According to the analysis in conclusions (1) in Section 2.4, a simplified MI-DCPFC topology is presented in this study. Its specific circuit diagram is shown in Figure 6. For an n-port MI-DCPFC, it consists of $n + 1$ identical IGBT half-bridges and a DC capacitor C. S_a and S_b are the upper and lower switches of HB_0, respectively. T_{ia} and T_{ib} (i = 1, 2... n) are the upper and lower switches of HB_i, respectively. Terminal T is taken from HB_0, and terminals P_i are taken out from HB_1 to HB_n, respectively, the terminal T and P_i respectively compose n different output ports TP_i of the MI-DCPFC. I_{Pi} are the DC currents flowing into MI-DCPFC through the different transmission lines; I_T is the DC current flowing out of MI-DCPFC.

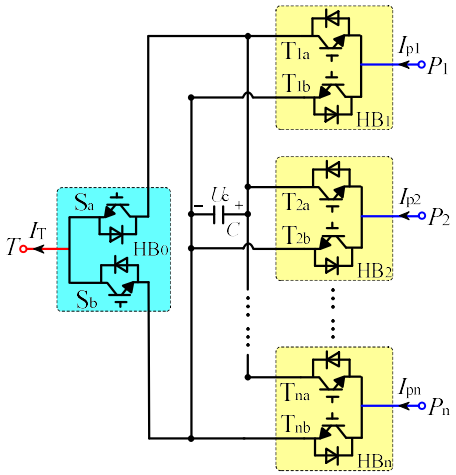

Figure 6. Topology of the simplified MI-DCPFC.

When the simplified MI-DCPFC is connected to a multi-terminal HVDC transmission system, the diagram can also be depicted as Figure 2. It should be noted that the adopted five-terminal HVDC transmission system is unipolar, so it is only necessary to consider adding the DCPFC to the positive pole or negative pole of the system. However, for the bipolar system, in order to ensure the symmetry of the system, DCPFC needs to be simultaneously added to the positive and negative pole of the system.

In addition, compared with the traditional MI-DCPFC, in order to achieve independent control of the current of all controlled lines, the new working principle of the simplified MI-DCPFC needs to be considered, which is detailed in the next section.

3.2. Operation Principles

For easy analysis, a three-port simplified MI-DCPFC was adopted as an example, and the shunt branches connected to the terminals P_1, P_2 and P_3 were also respectively named line 1, line 2 and line 3. Similar to the traditional MI-DCPFC, the three-port simplified MI-DCPFC has the same 12 working-modes, as shown in Table 1. In order to facilitate comparison with the traditional MI-DCPFC, we also chose working modes 1 (where control I_{p1} reduced; I_{p2} and I_{p3} increased) and 6 (where control I_{p1} increased; I_{p2} and I_{p3} reduced) to carry out detailed analysis.

3.2.1. Working-Mode 1

In this working-mode, according to the different conduction states of the switches in each half bridge, the working process of the MI-DCPFC can be divided into the following four stages. The conduction diagrams of the MI-DCPFC under this working-mode are depicted in Figure 7.

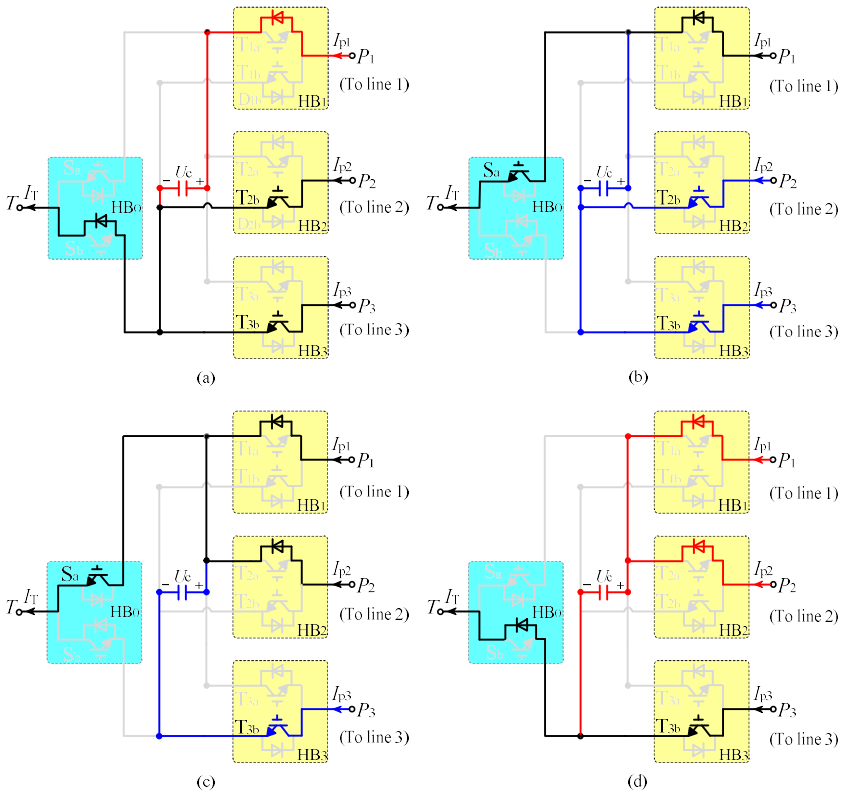

Figure 7. Conduction diagrams of the simplified MI-DCPFC under working-mode 1: (**a**) conduction diagram during stage 1; (**b**) conduction diagram during stage 2; (**c**) conduction diagram during stage 3; (**d**) conduction diagram during stage 4.

(i) Stage 1: turn on T_{2b} and T_{3b}. During this period, as shown in Figure 7a, the current I_{p1} is charging the capacitor through the feedback diodes of T_{1a} and S_b, while the currents I_{p2} and I_{p3} are flowing out of the terminal T directly.

(ii) Stage 2: keep T_{2b} and T_{3b} turned-on and turn on S_a. During this period, as shown in Figure 7b, the current I_{p1} is flowing out of the terminal T directly, while the currents I_{p2} and I_{p3} are discharging the capacitor through T_{2b}, S_a and T_{3b}, S_a respectively.

(iii) Stage 3: only keep T_{3b} and S_a turned-on. During this period, as shown in Figure 7c, the currents I_{p1} and I_{p2} are directly flowing out of the terminal T, while the current I_{p3} continues to discharge the capacitor through T_{3b} and S_a.

(iv) Stage 4: only keep T_{3b} turned-on. During this period, as shown in Figure 7d, the currents I_{p1} and I_{p2} are charging the capacitor through the feedback diode of T_{1a}, S_b and feedback diode of T_{2a}, S_b respectively, while the current I_{p3} is flowing out of the terminal T directly.

With charging and discharging by the line currents, we assumed that the capacitor voltage of MI-DCPFC is balanced at U_c. Concluding the analysis of the above, we can obtain the DC voltage introduced to the transmission line through the MI-DCPFC at various stages, as shown in Table 2.

Table 2. The DC voltage introduced to each line under working-mode 1.

Line	Stage 1	Stage 2	Stage 3	Stage 4
1	U_c	0	0	U_c
2	0	$-U_c$	0	U_c
3	0	$-U_c$	$-U_c$	0

It can be observed that compared to the traditional MI-DCPFC, the stages 3 and 4 are added by auxiliary pulsing the lower switch of HB_2. Based on this, the equivalent reverse polarity voltage introduced to the line 2 can be independently regulated, which indicates that the specific increased amounts of the currents I_{p2} and I_{p3} can be controlled individually at this time.

3.2.2. Working-Mode 6

In this working-mode, according to the different conduction states of the switches in each half bridge, the working process of the MI-DCPFC can also be divided into the following four stages. (i) Stage 1: only turn on T_{1b}; (ii) Stage 2: keep T_{1b} turned-on and turn on T_{3b}; (iii) Stage 3: keep T_{1b} and T_{3b} turned-on and turn on S_a; (iv) Stage 4: only keep T_{1b} and S_a turned-on. The conduction diagrams during stages 1 to 4 are shown in Figure 8a–d, respectively.

Referring the previous analysis method, we can obtain the DC voltage introduced into the transmission line at various stages under this working-mode, which are shown in Table 3. It can be found that with auxiliary controlling the lower switch of HB_3 in the simplified MI-DCPFC, the stages 2 and 3 are added to the operating process compared to the traditional MI-DCPFC. Based on this, the equivalent forward polarity voltages introduced to the lines 2 and 3 can be independently regulated, which indicates that the specific reduced amounts of the currents I_{p2} and I_{p3} can be controlled separately. In addition, according to the symmetry, when auxiliary pulsing the HB_2 lower transistor, we can also achieve the control of the I_{p1} that was increased and the I_{p2} and I_{p3} that were reduced.

Table 3. The DC voltage introduced to each line under working-mode 6.

Line	Stage 1	Stage 2	Stage 3	Stage 4
1	0	0	$-U_c$	$-U_c$
2	U_c	U_c	0	0
3	U_c	0	$-U_c$	0

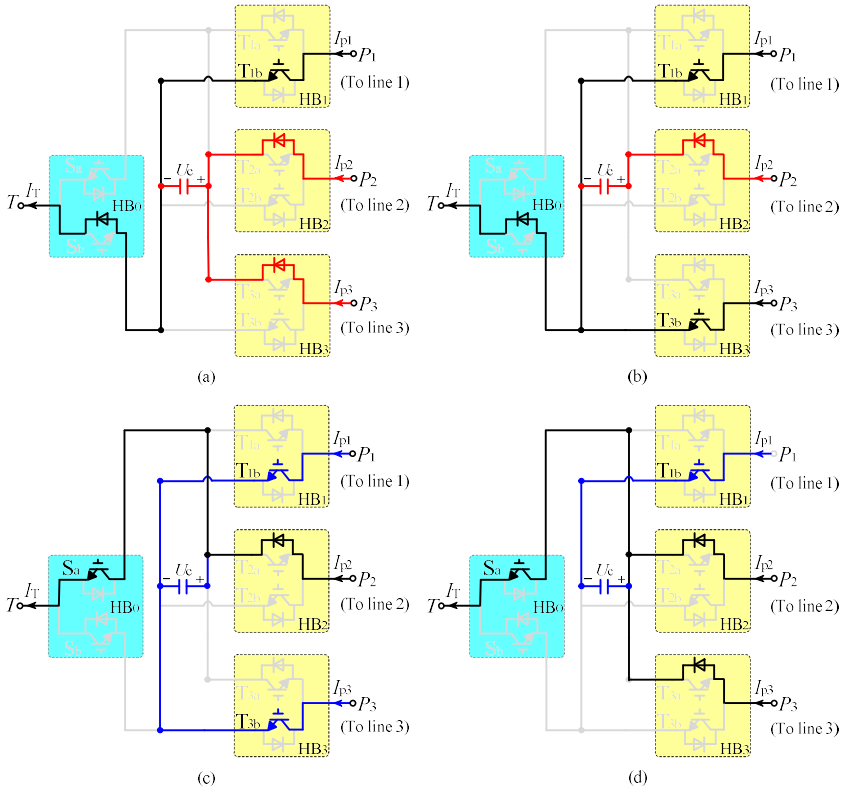

Figure 8. Conduction diagrams of the MI-DCPFC under working-mode 6: (**a**) conduction diagram during stage 1; (**b**) conduction diagram during stage 2; (**c**) conduction diagram during stage 3; (**d**) conduction diagram during stage 4.

3.2.3. Other Working-Modes

As shown in Table 1, there are four other working-modes including 2, 3, 4 and 5 besides the above two analyzed working-modes. Similarly, when the current direction is reversed, six other working-modes are also derived. However, their working principles are similar to the analyzed working-modes 1 and 6. The corresponding switching state of each transistor under different working-modes can be analyzed in a similar way. However, it is worth noting that since this type of MI-DCPFC cannot realize the reverse control of line current, when it is actually applied to a multi-terminal HVDC transmission system, it is relatively more suitable for the "multi-to-one" (such as multiple green and new energy are aggregated) or "one-to-many" (such as powering multiple zones) type of interconnected transmission structure.

Furthermore, when the MI-DCPFC is extended to the other ports number, its main working principle is similar to that of the three-port MI-DCPFC, which is reasonable to use to charge/discharge the capacitor on the different transmission lines. We will summarize the general control method of an arbitrary port MI-DCPFC in Section 4.3.

4. Novel Control Strategy and Relationship Analysis of the System State Variables

4.1. CPS-PWM Control Strategy

As analyzed in the Section 2.4, in order to achieve simultaneous tracking of the different current regulation commands for multiple transmission lines, the normal operation of MI-DCPFC needs to meet two regulation requirements: (i) When multiple line currents are increased, achieve independent amplification control of each line current (control-mode 1); (ii) When multiple line currents are reduced, achieve independent reduction control of each line current (control-mode 2).

To solve this problem, a control strategy that is easier to implement based on the CPS-PWM control was designed. Firstly, we describe the specific implementation of the two control-modes detailed in combination with the three-port MI-DCPFC.

4.1.1. Control-Mode 1

Combined with the previous analysis in Section 3.2.1, it can be seen that when MI-DCPFC is operating in working-mode 1, it is necessary to coordinate the amplification control of I_{p2} and I_{p3} by using the control-mode 1. Taking tracking the power flow regulating command of I_{p2} as an example, the control block diagram is shown in Figure 9. I_{p1}* is the regulation command of the current of line 1. It subtracts the sampling current I_{p1}, where the error is sent to a PI regulator. Its output is compared with the triangular carrier, thereby obtaining the driving pulse of transistor S_a. Meanwhile, the next step involves tracking the error between the regulation command I_{p2}* and sample current I_{p2} of line 2 with a PI regulator, and then scaling it by the coefficient k_1 ($k_1 = -T_s/2$, where T_s is the carrier period) to obtain the phase-shifted value of the original carrier. Finally, when comparing the phase-shifted carrier with the duty D of pulse signal of S_a, the driving pulse of transistor T_{2b} can be obtained by NXORing the result with the pulse signal of S_a.

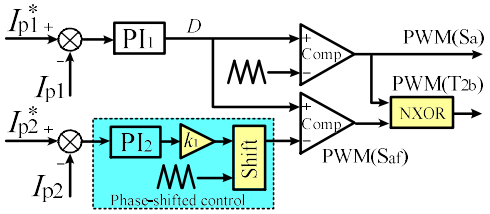

Figure 9. Block diagram of the control-mode 1 of the MI-DCPFC.

4.1.2. Control-Mode 2

When the MI-DCPFC is operating in working-mode 6, it needs to achieve the reduction control of I_{P3} synchronized with the I_{P2} reduction control by the control-mode 2. The control block diagram is shown in Figure 10.

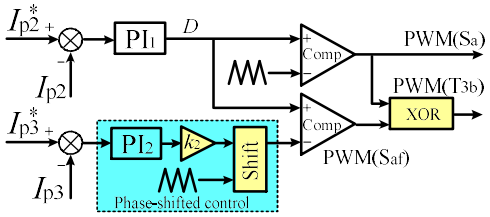

Figure 10. Block diagram of the control-mode 2 of the MI-DCPFC.

Similarly, we used the PI regulator tracking the correction current on line 2 and then comparing with the triangular carrier to obtain the drive pulse of the switch S_a. Also, we used the PI regulator tracking the correction current on line 3 and scaling it by the coefficient k_2 ($k_2 = T_s/2$) to obtain the phase-shifted value. Finally, the phase-shifted pulse signal XORs with the pulse signal of S_a can obtain the T_{3b} drive pulse.

4.2. Relationship of the System State Variable

According to Figure 9, the timing chart diagram of the driving pulses under control-mode 1 can be obtained as Figure 11a.

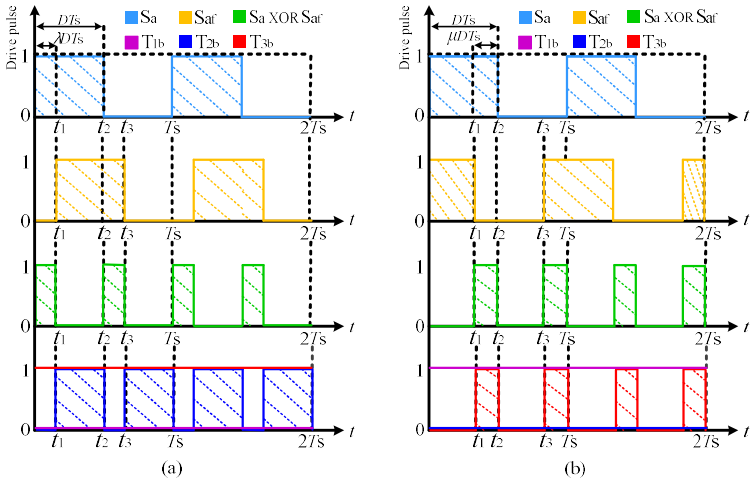

Figure 11. Timing chart diagram of the driving pulses: (**a**) timing chart diagram under control-mode 1; (**b**) timing chart diagram under control-mode 2.

Assuming that the phase-shifted time is t_1, T_{3b} and S_a will be in the on-state during 0–t_1, which corresponds to the stage 3 of working-mode 1. Further, the following equations can be established by combining Figure 7c:

$$V = -R_1 i_{P1} - L_1 \frac{\mathrm{d}i_{P1}}{\mathrm{d}t} + V_1 \tag{1}$$

$$V = -R_2 i_{P2} - L_2 \frac{\mathrm{d}i_{P2}}{\mathrm{d}t} + V_2 \tag{2}$$

$$V = -R_3 i_{P3} - L_3 \frac{\mathrm{d}i_{P3}}{\mathrm{d}t} + u_c + V_3 \tag{3}$$

$$i_{P3} = -C \frac{\mathrm{d}u_c}{\mathrm{d}t} \tag{4}$$

where V is DC side voltage of the converter node to which the terminal T is connected. V_1, V_2, and V_3 are the DC side voltages of the converter nodes to which the terminal P_1, P_2 and P_3 are connected, respectively. R_1, R_2, R_3 and L_1, L_2, L_3 are the equivalent resistance and inductance values of the transmission lines 1 to 3, respectively. i_{P1}, i_{P2}, i_{P3} are the instantaneous current of the transmission lines 1 to 3, respectively. u_c is the capacitor voltage of the MI-DCPFC.

By defining $x^T = [i_{P1}, i_{P2}, i_{P3}, u_c]$ as the state variable of the system, the Equations (1)–(4) can be rewritten to a matrix form, as shown in Equation (5).

$$\mathrm{Z} \times \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{P1} \\ i_{P2} \\ i_{P3} \\ u_c \end{bmatrix} = \begin{bmatrix} -R_1 & 0 & 0 & 0 \\ 0 & -R_2 & 0 & 0 \\ 0 & 0 & -R_3 & 1 \\ 0 & 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} i_{P1} \\ i_{P2} \\ i_{P3} \\ u_c \end{bmatrix} + \mathrm{E} \times \begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{5}$$

where:

$$\mathrm{Z} = \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & L_3 & 0 \\ 0 & 0 & 0 & C \end{bmatrix}, \ \mathrm{E} = \begin{bmatrix} -1 & 1 & 0 & 0 \\ -1 & 0 & 1 & 0 \\ -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{6}$$

Besides, it is easy to observe that the time periods t_1–t_2, t_2–t_3 and t_3–T_s in Figure 11a correspond to stage 2, stage 4 and stage 1 in the working-mode 1, respectively. Therefore, the system matrix equations in each time period can be written as Equations (7)–(9) in the same way, respectively.

$$\mathrm{Z}\times\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix} = \begin{bmatrix} -R_1 & 0 & 0 & 0 \\ 0 & -R_2 & 0 & 1 \\ 0 & 0 & -R_3 & 1 \\ 0 & -1 & -1 & 0 \end{bmatrix}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix}+\mathrm{E}\times\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{7}$$

$$\mathrm{Z}\times\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix} = \begin{bmatrix} -R_1 & 0 & 0 & -1 \\ 0 & -R_2 & 0 & -1 \\ 0 & 0 & -R_3 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix}+\mathrm{E}\times\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{8}$$

$$\mathrm{Z}\times\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix} = \begin{bmatrix} -R_1 & 0 & 0 & -1 \\ 0 & -R_2 & 0 & 0 \\ 0 & 0 & -R_3 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix}+\mathrm{E}\times\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{9}$$

In order to facilitate the subsequent analysis, the coefficient λ is introduced to establish the quantitative relationship between the phase-shifted time t_1 and the duty ratio D of $\mathrm{S_a}$ drive pulse:

$$\lambda = \frac{t_1}{DT_{\mathrm{s}}} \tag{10}$$

Combining Equation (10) and Figure 11a, we further obtained:

$$\frac{t_2 - t_1}{T_{\mathrm{s}}} = (1-\lambda)D \tag{11}$$

$$\frac{t_3 - t_2}{T_{\mathrm{s}}} = \lambda D \tag{12}$$

$$\frac{T_{\mathrm{s}} - t_3}{T_{\mathrm{s}}} = 1-(1+\lambda)D \tag{13}$$

Concluding Equations (5)–(13), the system state equation of MI-DCPFC in one control period $\mathrm{T_s}$ can be integrated as:

$$\mathrm{Z}\times\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix} = \begin{bmatrix} -R_1 & 0 & 0 & -1+D \\ 0 & -R_2 & 0 & (1-2\lambda)D \\ 0 & 0 & -R_3 & D \\ 1-D & -(1-2\lambda)D & -D & 0 \end{bmatrix}\begin{bmatrix} i_{\mathrm{P1}} \\ i_{\mathrm{P2}} \\ i_{\mathrm{P3}} \\ u_c \end{bmatrix}+\mathrm{E}\times\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{14}$$

When the system is operating stable, the change of the state variable can be ignored, and the Equation (14) can be further written as:

$$\begin{bmatrix} -R_1 & 0 & 0 & -1+D \\ 0 & -R_2 & 0 & (1-2\lambda)D \\ 0 & 0 & -R_3 & D \\ 1-D & -(1-2\lambda)D & -D & 0 \end{bmatrix}\begin{bmatrix} I_{\mathrm{P1}} \\ I_{\mathrm{P2}} \\ I_{\mathrm{P3}} \\ U_c \end{bmatrix}+\mathrm{E}\times\begin{bmatrix} V \\ V_1 \\ V_2 \\ V_3 \end{bmatrix} = 0 \tag{15}$$

Solving the matrix equation shown in Equation (15), we can obtain the average capacitor voltage expression of the MI-DCPFC as:

$$U_c = \frac{(1-D)(V_1-V) - DR_1\left[\frac{(1-2\lambda)(V_2-V)}{R_2} + \frac{(V_3-V)}{R_3}\right]}{(1-D)^2 + D^2R_1\left[\frac{(1-2\lambda)^2}{R_2} + \frac{1}{R_3}\right]} \tag{16}$$

In the same way, we can obtain the timing chart diagram of the driving pulses under control-mode 2 firstly, as shown in Figure 11b. Then, the coefficient μ characterizing the phase-shifted time in this control-mode is introduced, where $\mu = (t_2 - t_1)/DT_s$. Finally, the average capacitor voltage expression of MI-DCPFC under this case can be obtained as:

$$U_c = \frac{(1-D)(V_2-V) - DR_2\left[\frac{(1/D-1-2\mu)(V_2-V)}{R_3} + \frac{(V_1-V)}{R_1}\right]}{(1-D)^2 + D^2R_2\left[\frac{(1/D-1-2\mu)^2}{R_3} + \frac{1}{R_1}\right]} \tag{17}$$

Concluding Equations (16) and (17), it can be observed that when MI-DCPFC participates in the system power flow regulation, its capacitor voltage is related to the voltage drop and the rated parameters of the DC transmission line. This conclusion is also similar to the analysis results of the traditional CFC in reference [26]. In addition, it should be noted that as this type of MI-DCPFC cannot realize the reverse control of line current, the most extreme power regulation condition it faces is when all line currents are increased at the line with the largest line resistance. In other words, we can think that for the controlled lines, the capacitor voltage provided by DCPFC is the largest voltage under this condition. In this way, we can estimate the capacity design requirements of the MI-DCPFC, so as to ensure that it will not be damaged by the capacitor overvoltage when it is inserted into the system under normal operation. Furthermore, since this capacitor voltage is also the voltage level that the MI-DCPFC switches need to withstand, it can help to select the suitable switching devices.

4.3. Control Method Extension of an Arbitrary Port MI-DCPFC

In previous analysis, we take a three-port MI-DCPFC as the example, its basic working principle and implementation of control method are analyzed in detail. To make the results more general, we extend for an arbitrary port MI-DCPFC in this section.

Assuming that n shunt lines are connected to the MI-DCPFC, and m line currents need to control reduced, the other $n - m$ lines currents that need to be controlled increased. This result can follow the following main control principles during the implementation process:

(1) Selection of controlled lines: all lines that currents need to be reduced and $n - m + 1$ lines that currents need to be increased are under an active-controlled state. In this way, by tracking the current regulation commands of $n - 1$ branches, the overall control of n line currents can be realized;

(2) Generation of HB_0 drive pulse: to appropriately balance the carrier phase-shifted margin between both of the control-modes, the branch that he current reduced was centered among the m branches can be selected as a reference, and then generated the drive pulse of HB_0;

(3) Generation of HB_i drive pulse: on this basis of step (2), the remaining $n - 2$ active-controlled branches are tracking the current reduced and increased regulation commands through the control-mode 1 and -mode 2, respectively. Then generate the corresponding driving pulses of HB_i, respectively. In addition, the upper and lower switches of the only one branch that remained are kept turned-off and turned-on, respectively.

According to the above ideas, it should be assumed that the branches 1 to m are current reduced lines, and the branches $m + 1$ to n are current increased lines. Taking the forward current direction as the example, Figure 12 shows the overall control block diagram of the MI-DCPFC when the branch 1 is adopted as the reference branch.

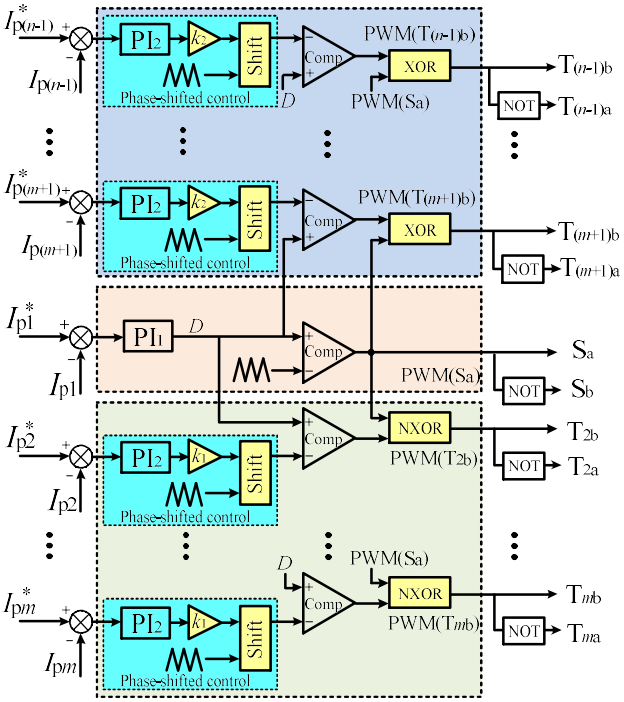

Figure 12. General control diagram of the arbitrary port MI-DCPFC.

5. Simulation Results

To confirm the proposed MI-DCPFC topology and control strategy, the related verification was carried out in MATLAB/SIMULINK. The five-terminal HVDC transmission system as shown in Figure 1 (repainting it as Figure 13a) and a more complicated five-terminal HVDC transmission system with four-port MI-DCPFC as shown in Figure 13b were developed, respectively.

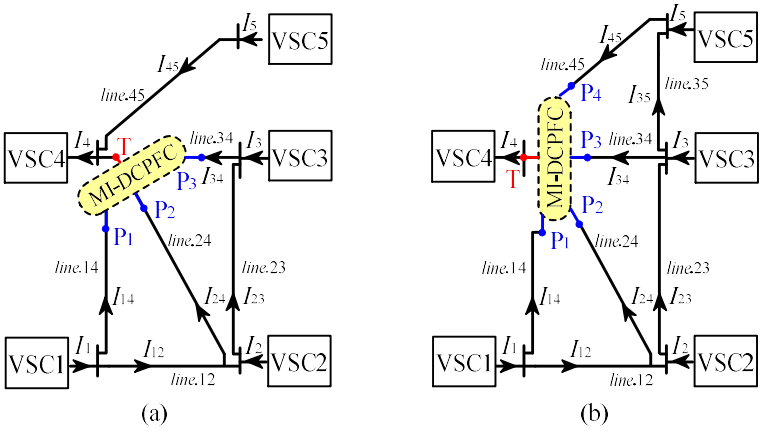

Figure 13. Schematic diagrams of the tested five-terminal DC transmission system: (**a**) topology with the three-port MI-DCPFC; (**b**) topology with the four-port MI-DCPFC.

The converter node VSC4 controls the systems DC bus voltage at 200 kV. The converter nodes VSC1 to VSC3 and the converter node VSC5 respectively inject P1 = 80 MW, P2 = 100 MW, P3 = 60 MW and P5 = 80 MW active power into the system. The main parameters of each transmission line are shown in Table 4.

Table 4. Line parameters of the five-terminal HVDC transmission systems.

Transmission Line	Length/km	Resitance/Ω	Inductance/mH	Capacitance/uF
line.14	200	2.0	80	240
line.24	100	1.0	40	120
line.34	300	3.0	120	360
line.45	150	1.5	60	180
line.12	120	1.2	48	144
line.23	100	1.0	40	120
line.35	100	1.0	40	120

5.1. Three-Port MI-DCPFC Verified Results

5.1.1. Case 1

The working-mode 1 (I_{14} is reduced; I_{24} and I_{34} are increased) was verified in this case. In addition, to make it easy to compare and analyze each one, the simplified MI-DCPFC with the traditional and novel control methods were both tested, respectively.

The performance of the MI-DCPFC with the traditional control method in this case is shown in Figure 14a–c. The MI-DCPFC is accessed into the system at 0.2 s, and with the command controlling line.14 current reduces to I_{14} = 0.1 kA. It can be seen that before adjusting the line currents, the system is operating at a stable rate, and the values of each line current are about I_{14} = 0.35 kA; I_{24} = 0.62 kA; I_{34} = 0.23 kA; I_{45} = 0.40 kA; I_{12} = 0.06 kA; I_{23} = −0.07 kA, respectively. When the MI-DCPFC is inserted to the system at 0.2 s, the controlled line current I_{14} quickly respond to the command value and maintain stable operation, as shown in Figure 14a. In addition, as shown in Figure 14b,c, the voltage V_{TP1} introduced in the line 14 is stably switched between 0 and U_c; while the voltages introduced in line 24 and line 34 are synchronized to switch between 0 and $-U_c$, so I_{24} and I_{34} automatically respond to I_{24} = 0.82 kA and I_{34} = 0.28 kA, respectively. We found that the specific increased amounts of the currents I_{24} and I_{34} cannot be controlled separately at this time, which is consistent with the theoretical analysis in the previous section.

The performance of the MI-DCPFC with the novel control method is shown in Figure 14d–g. The MI-DCPFC is inserted to the system at 0.2 s, and with the command in control, I_{14} reduces to I_{14} = 0.1 kA and I_{24} remains unchanged. When operating to 1.2 s, the regulation command is re-changed, where with controlling I_{14} reduced to 0.1 kA, but control I_{24} increases to 0.7 kA. It can be observed that when the MI-DCPFC is accessed in the system, the controlled line current I_{14} can also quickly respond to I_{14} = 0.1 kA and maintain stable operation, as shown in Figure 14d. What is more, it can be found that unlike with the traditional control method, as the voltage V_{TP2} introduced in the line24 can be controlled and stably switched between U_c, 0 and $-U_c$, so the increased amounts of the current I_{24} can be controlled freely at the same time.

The above simulation results show that the simplified MI-DCPFC with the novel control strategy can achieve the power flow control quickly and stably under the working-mode 1. Furthermore, when compared to the traditional control strategy, on the basis of the reducing control of the line current, the increased value of other line currents can be also controlled freely at the same time. In addition, the capacitor voltage fluctuation is small, and the voltage state introduced in the connection line by the output port is consistent with the theoretical analysis.

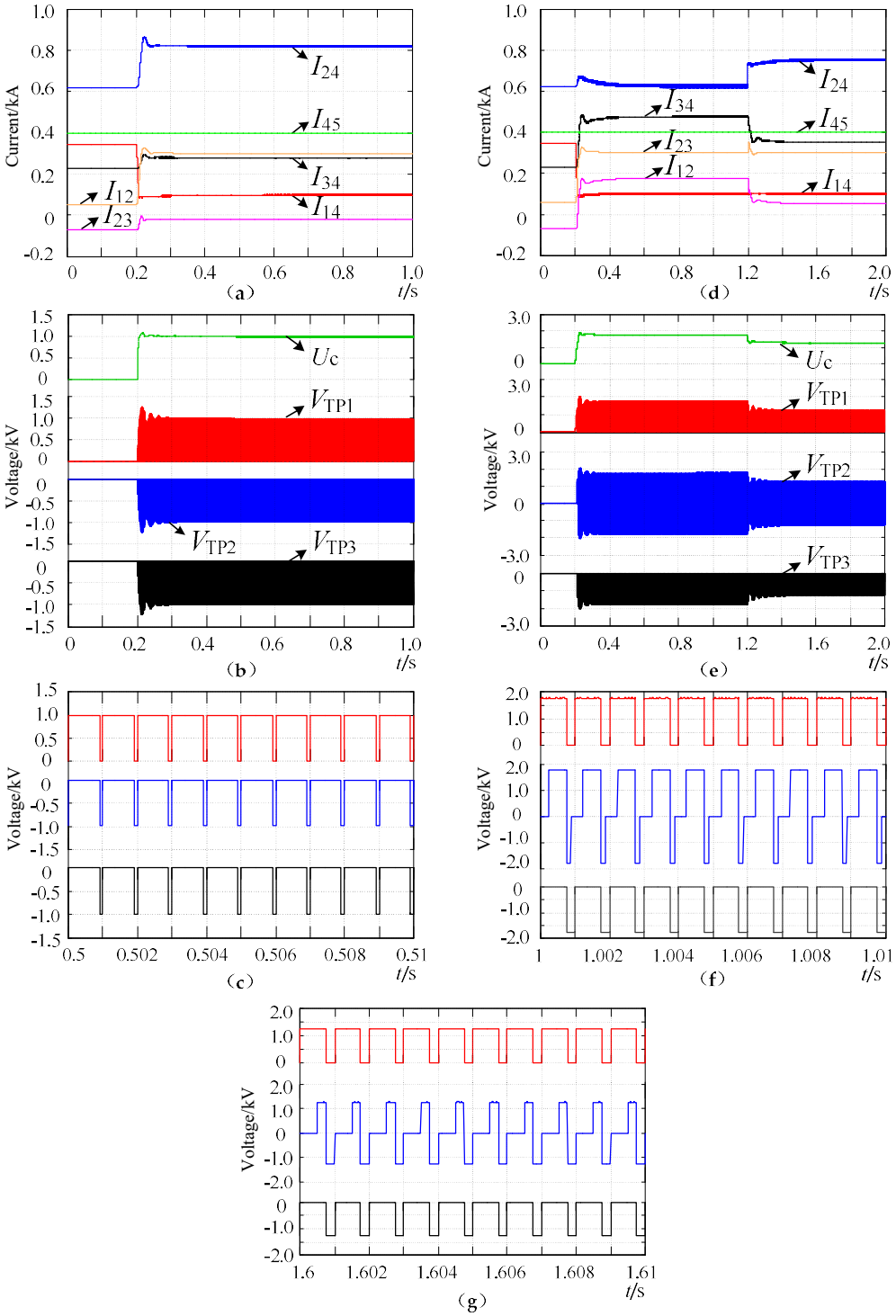

Figure 14. Simulation results of three-port MI-DCPFC under Case 1: (**a**) line currents with the traditional control method; (**b**) capacitor and port-output voltages with the traditional control method; (**c**) enlarged view of Figure 14b among 0.5–0.51 s; (**d**) line currents with the novel control method; (**e**) capacitor and port-output voltages with the novel control method; (**f**) enlarged view of Figure 14e among 1–1.01s; (**g**) enlarged view of Figure 14e among 1.6–1.61 s.

5.1.2. Case 2

The working-mode 6 (I_{24} and I_{34} are reduced; I_{14} is increased) was verified in this case. Similarly, to make it easy to compare and analyze the simplified MI-DCPFC with the traditional and novel control methods were tested, respectively.

The performance of the MI-DCPFC with the traditional control method in this case is shown in Figure 15a–c. The MI-DCPFC is accessed into the system at 0.2 s, and with the command controlling line 34, the current reduces to I_{34} = 0.15 kA. It can be observed that the controlled line current I_{34} quickly responds to the command value and maintains stable operation when the MI-DCPFC is accessed in the system at 0.2 s, as shown in Figure 15a. However, as shown in Figure 15b,c, since the voltage V_{TP2} introduced in the line 24 and voltage V_{TP3} introduced in line 34 are synchronized to switch between 0 and U_c, although the I_{34} is also reduced, its specific reduced amounts cannot be controlled separately at this time.

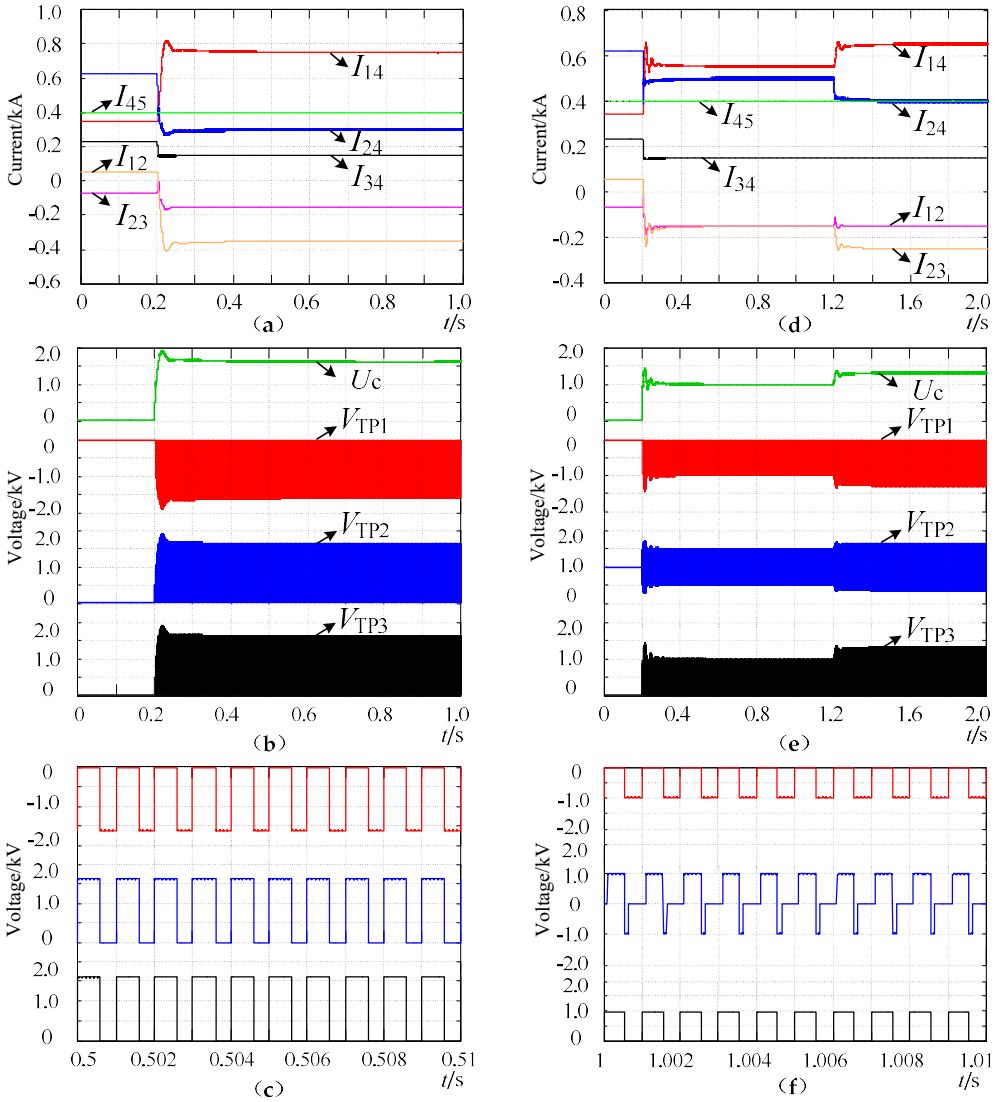

Figure 15. *Cont.*

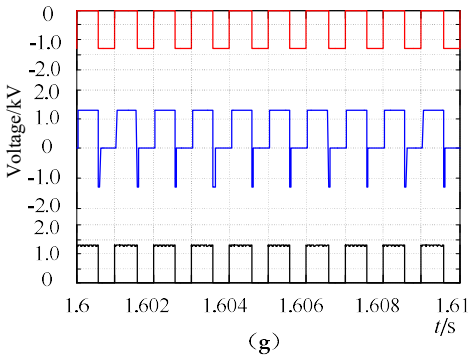

Figure 15. Simulation results of three-port MI-DCPFC under Case 2: (**a**) line currents with the traditional control method; (**b**) capacitor and port-output voltages with the traditional control method; (**c**) enlarged view of Figure 15b among 0.5–0.51 s; (**d**) line currents with the novel control method; (**e**) capacitor and port-output voltages with the novel control method; (**f**) enlarged view of Figure 15e among 1–1.01 s; (**g**) enlarged view of Figure 15e among 1.6–1.61 s.

The performance of the MI-DCPFC with the novel control method is shown in Figure 15d–g. The MI-DCPFC is accessed in the system at 0.2 s, and with the command in control, I_{24} and I_{34} are reduced to I_{24} = 0.5 kA and I_{34} = 0.15 kA, respectively. When operating to t_4, the power flow control command is re-changed, where with controlling occurring, I_{34} was reduced to 0.15 kA, but control I_{24} further reduces to 0.4 kA. It can be observed that when the MI-DCPFC is accessed in the system, the controlled line current I_{34} quickly responded to I_{34} = 0.15 kA and maintained stable operation, as shown in Figure 15d. What is more, the reduced amounts of the current I_{24} can simultaneously be controlled freely with the reducing control of I_{34}. Correspondingly, the voltage V_{TP2} introduced in the line 24 is controlled and stably switched between U_c, 0 and $-U_c$, as shown in Figure 15e–g.

The simulation results in this case show that the simplified MI-DCPFC with the novel control strategy can achieve the power flow regulation quickly and stably under the working-mode 6. Furthermore, compared to the traditional control strategy, independent reduction control of each line current can be achieved when multiple line currents are reduced. Meanwhile, the capacitor voltage fluctuation is small, and the voltage state introduced in the connection line by the output port is consistent with the theoretical analysis.

5.2. Four-Port MI-DCPFC Verified Results

In order to further test the performance of the MI-DCPFC, the verification of a four-port MI-DCPFC was carried out. When the system starts up normally, it is tested with the following three different conditions, and the performance of the MI-DCPFC is shown in Figure 16; the measurement values of each line current under different test conditions are shown in Table 5.

(1) At 0.2 s, control I_{14} reduces to 0.05 kA, and control I_{24} and I_{45} increase to 0.7 kA and 0.5 kA, respectively;
(2) At 0.2 s, control I_{14} and I_{45} reduce to 0.2 kA and 0.3 kA, respectively; and control I_{24} increases to 0.7 kA;
(3) At 0.2 s, control I_{14}, I_{45} and I_{24} reduce to 0.2 kA, 0.3 kA and 0.4 kA, respectively.

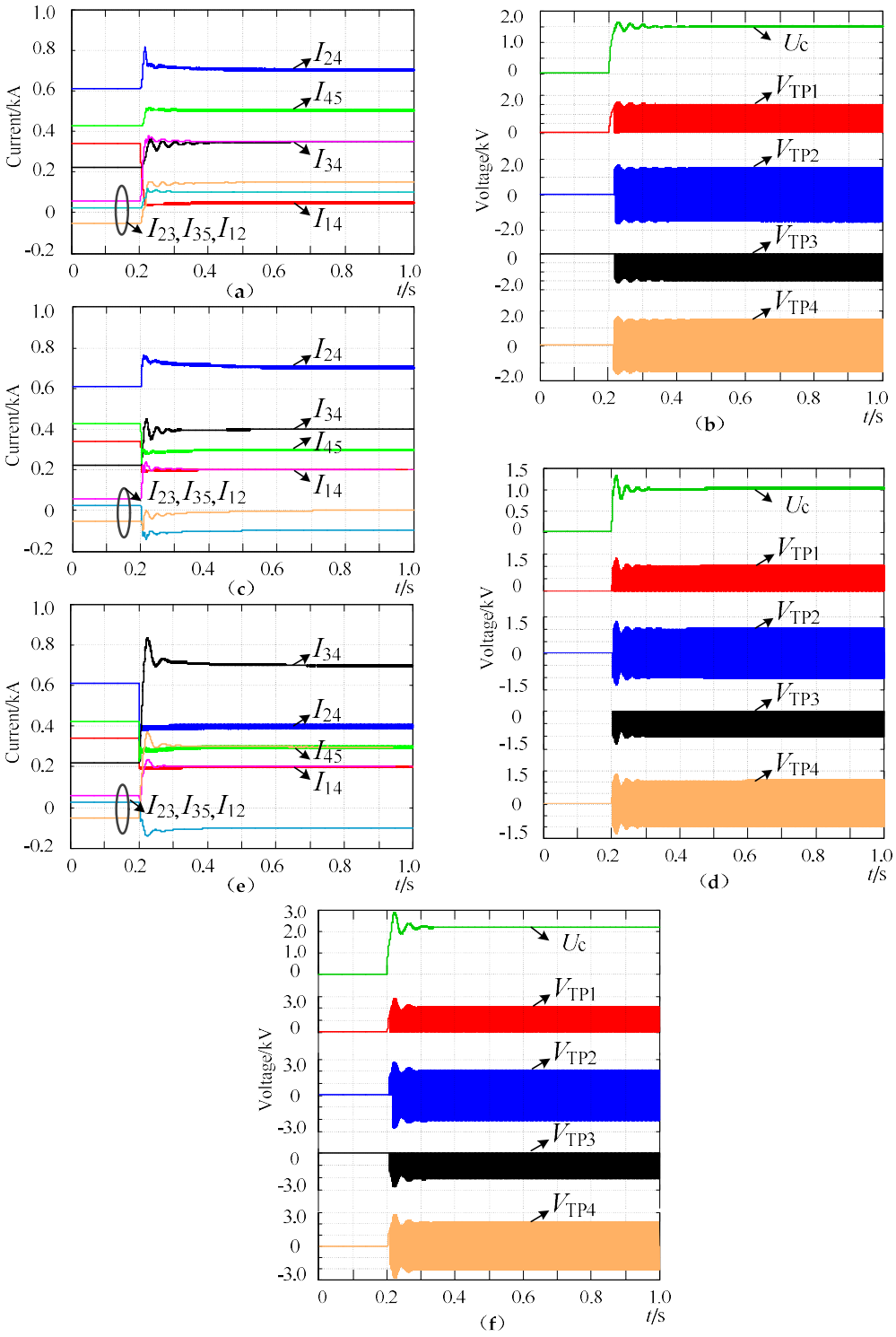

Figure 16. Simulation results of four-port MI-DCPFC: (**a**) line currents under condition 1; (**b**) capacitor and port-output voltages under condition 1; (**c**) line currents under condition 2; (**d**) capacitor and port-output voltages under condition 2; (**e**) line currents under condition 3; (**f**) capacitor and port-output voltages under condition 3.

Table 5. The measurement values of each line current under different test conditions.

Line Current/kA	No Command/kA	Condition 1/kA	Condition 2/kA	Condition 3/kA
I_{14}	0.33	0.05	0.20	0.20
I_{45}	0.43	0.50	0.30	0.30
I_{24}	0.62	0.70	0.70	0.40
I_{34}	0.21	0.35	0.40	0.70
I_{23}	−0.06	0.15	0	0.30
I_{12}	0.07	0.35	0.20	0.20
I_{35}	0.03	0.10	−0.10	−0.10

It can be observed that under the different control conditions, the controlled lines can all quickly track the corresponding power flow control commands, and then maintain stable operation. In addition, we can note that in the test conditions 1 and 3, MI-DCPFC only operates in control-mode 1 and control-mode 2, respectively; in test condition 2, control-mode 1 and -mode 2 participate in the regulation work simultaneously.

Concluding all previous simulation studies in this section, it can be seen that with the CPS-PWM control strategy proposed in this paper, the simplified MI-DCPFC can achieve effective power flow control under different power flow regulation requirements and its response speed is faster.

6. Experiments

To verify the proposed MI-DCPFC topology and control strategy, the five-terminal HVDC transmission system consistent with the simulation was built in the laboratory. Figure 17 shows the photograph of the platform. Each module in the Units 1 to 3 has half-bridge and full-bridge as two different topology modes that could be selected. Different MI-DCPFC topologies can be formed by an appropriate selection and combination, as shown in Table 6. VSC1–VSC5 adopts a ITECH programmable digital power IT series, where VSC4 controls the systems DC bus voltage at 80 V; VSC1 to 3 and VSC5 respectively inject I_1 = 8 A, I_2 = 10 A, I_3 = 6 A and I_5 = 8 A into the system. The transmission line parameters are shown in Table 7. In addition, in order to facilitate the comparison and verification of the simulation results, the verified cases in the experiment are the same as for the simulation.

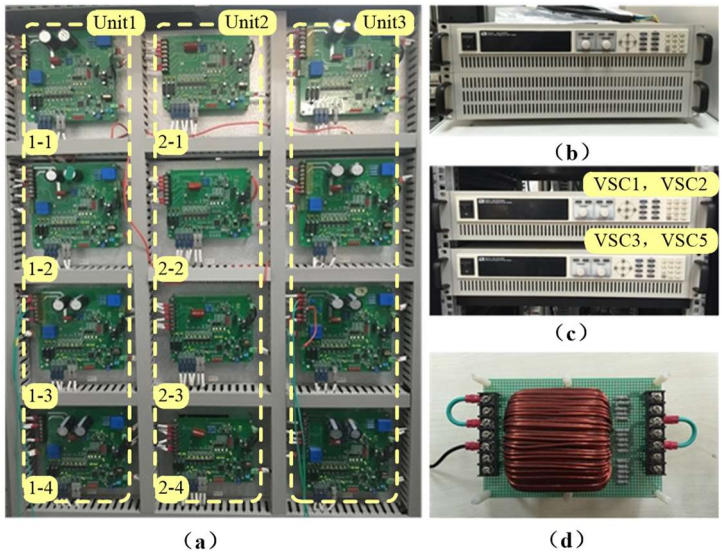

Figure 17. Photograph of the MI-DCPFC platform: (**a**) MI-DCPFC prototype; (**b**) VSC4; (**c**) VSC1-3 and 5; (**d**) line impedance module.

Table 6. Implementation of the MI-DCPFC topology in the experiment.

Topology	Selected Module Topology	Used Modules
Traditional three-port MI-DCPFC	Full-bridge	1-1; 2-1 to -2
Proposed three-port MI-DCPFC	Half-bridge	1-1; 2-1 to -3
Proposed four-port MI-DCPFC	Half-bridge	1-1; 2-1 to -4

Table 7. Line parameters in the experiment.

Transmission Line	Resitance/Ω	Inductance/mH
line.14	2.0	4.0
line.24	1.0	3.0
line.34	3.0	5.0
line.45	1.5	4.0
line.12	1.2	3.0
line.23	1.0	3.0
line.35	1.0	3.0

6.1. Three-Port MI-DCPFC Verified Results

6.1.1. System Test

With the topology of the transmission system shown in Figure 13a, Figure 18 shows the line currents of the transmission system with no MI-DCPFC accessed under the normal operation. It can be observed that the system operates in a stable manner when it starts up. The measured values of each line current are about I_{14} = 7 A; I_{24} = 12.8 A; I_{34} = 4.8 A; I_{45} = 4 A; I_{12} = 1.2 A; I_{23} = −1.4 A, respectively.

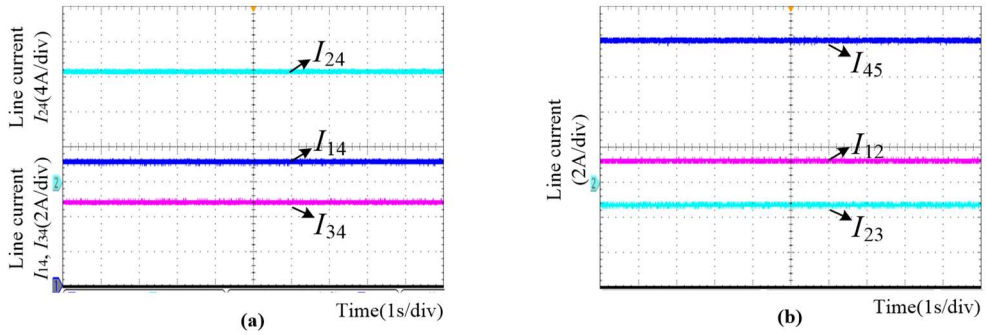

Figure 18. Experiment results under normal operation: (**a**) line currents part 1; (**b**) line currents part 2.

6.1.2. Case 1

The working-mode 1 (I_{14} is reduced; I_{24} and I_{34} are increased) was confirmed in this case. The performance of the MI-DCPFC with the traditional control method in this case is shown in Figure 19a–c. The MI-DCPFC is accessed into the system at t_1, and with the command controlling I_{14} reduces to I_{14} = 2 A. It can be seen that before adjusting the line currents, the system is operating in a stable manner. When the MI-DCPFC is inserted to the system at t_1, the controlled line current I_{14} quickly responded to the command value and maintained stable operation, as shown in Figure 19a. In addition, as shown in Figure 19b,c, the voltage V_{TP1} introduced in line 14 stably switched between 0 and U_c; the voltages introduced in line 24 and line 34 were synchronized to switch between 0 and $-U_c$, so I_{24} and I_{34} automatically responded to I_{24} = 16.8 A and I_{34} = 6 A respectively, where the specific increased amounts of the currents I_{24} and I_{34} cannot be controlled separately at this time.

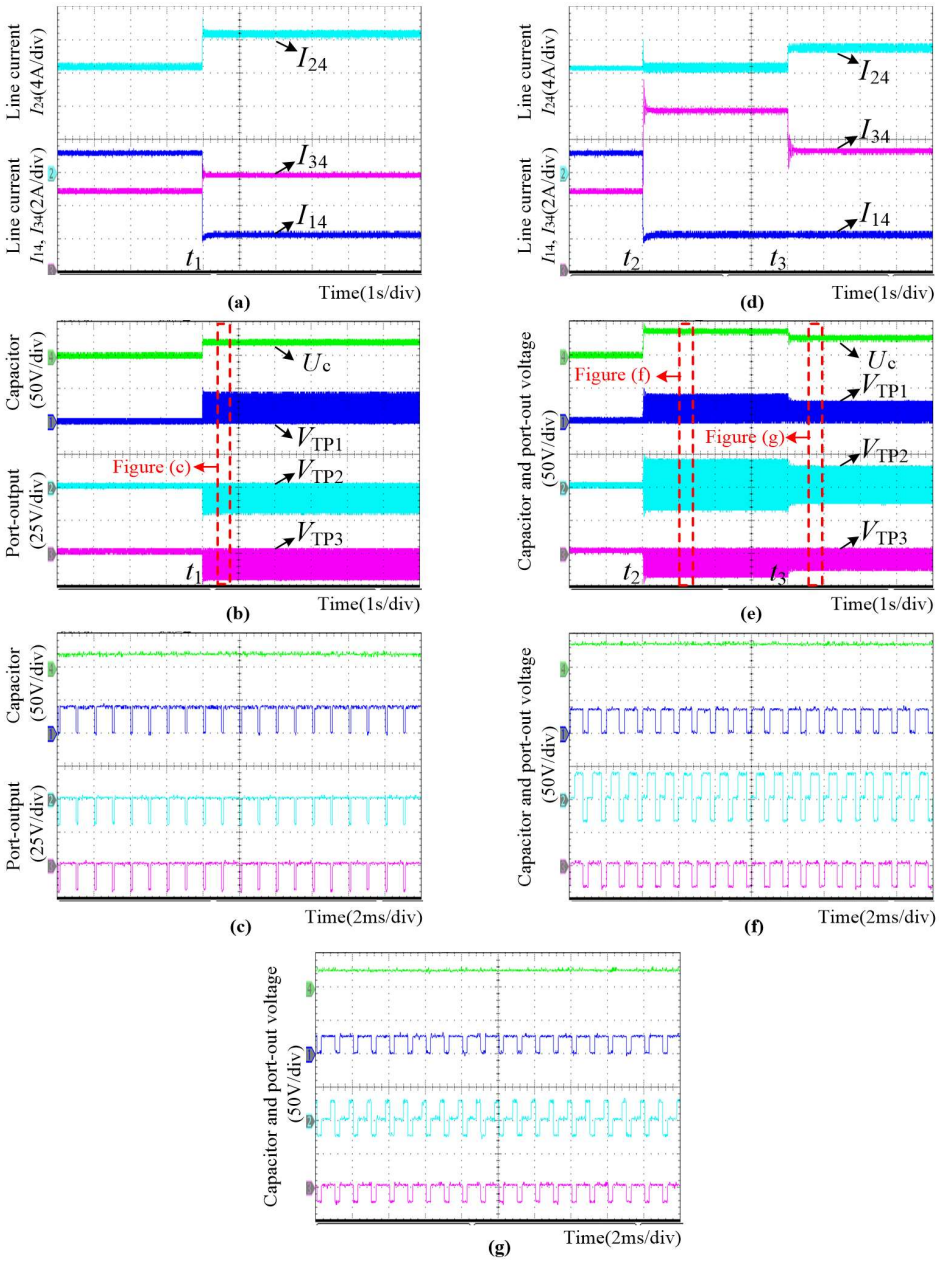

Figure 19. Experiment results of three-port MI-DCPFC under Case 1: (**a**) line currents with the traditional control method; (**b**) capacitor and port-output voltages with the traditional control method; (**c**) enlarged view of Figure 19b; (**d**) line currents with the novel control method; (**e**) capacitor and port-output voltages with the novel control method; (**f**) enlarged view 1 of Figure 19e; (**g**) enlarged view 2 of Figure 19e.

The performance of the MI-DCPFC with the novel control method is shown in Figure 19d–g. The MI-DCPFC is inserted to the system at t_2, and with the command in control, I_{14} reduces to I_{14} = 2 A and I_{24} remains unchanged. When operating to t_3, the regulation command is re-changed, where with controlling I_{14} reduced to 2 A, but control increased I_{24} to 15 A. It can be observed that when the MI-DCPFC is accessed into the system, the controlled line current I_{14} also quickly responded to 2 A and maintained stable operation, as shown in Figure 19d. What is more, unlike with the traditional control method, since the voltage V_{TP2} introduced in line 24 can be controlled stably switched between U_c, 0 and $-U_c$, the increased amounts of the current I_{24} can also be controlled freely at the same time.

6.1.3. Case 2

The working-mode 6 (I_{24} and I_{34} are reduced; I_{14} is increased) was confirmed in this case. The performance of the MI-DCPFC with the traditional control method in this case is shown in Figure 20a–c. The MI-DCPFC is accessed into the system at t_4, and with the command controlling I_{34} reduces to I_{34} = 3 A.

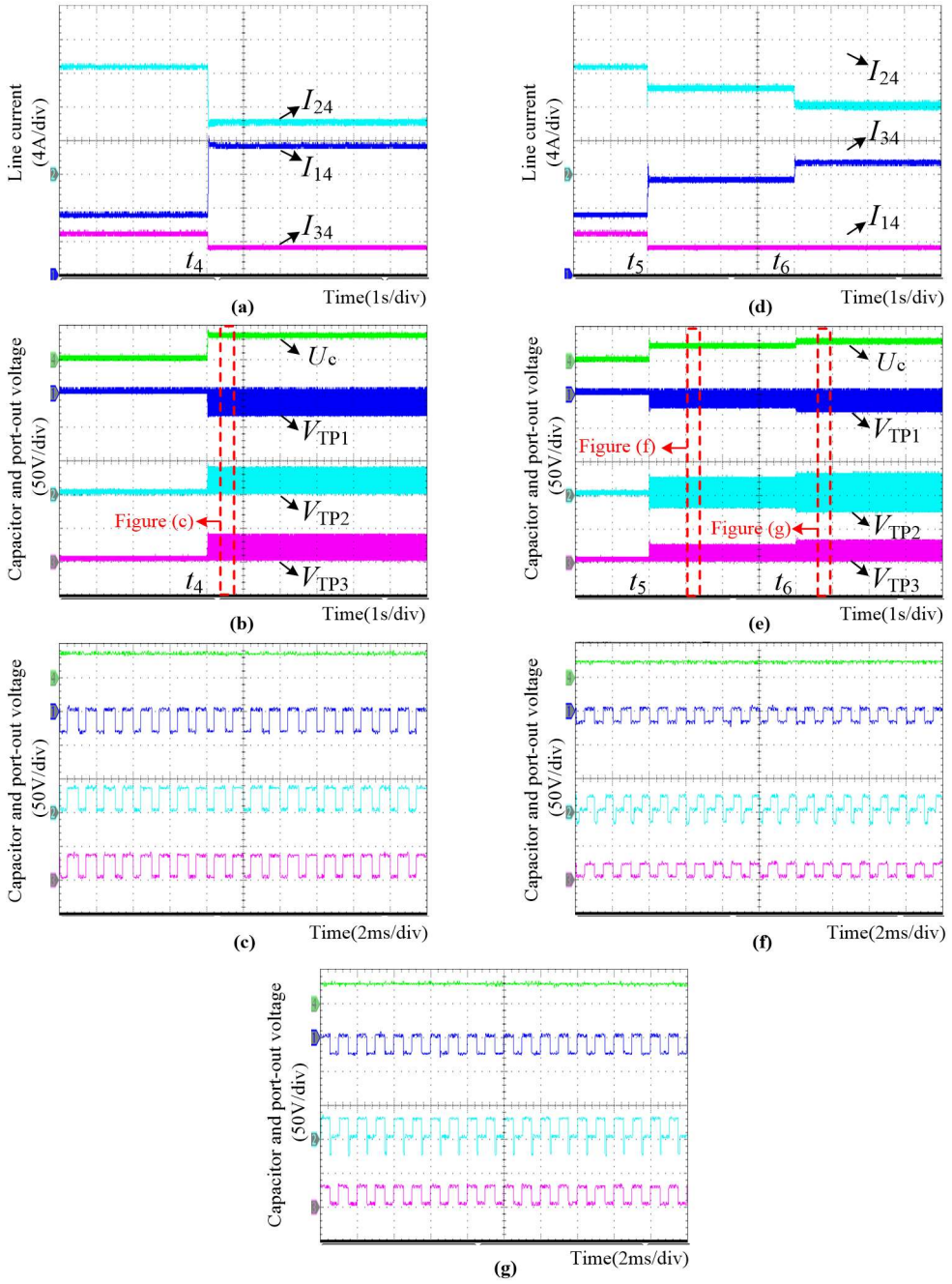

Figure 20. Experiment results of three-port MI-DCPFC under Case 2: (**a**) line currents with the traditional control method; (**b**) capacitor and port-output voltages with the traditional control method; (**c**) enlarged view of Figure 20a; (**d**) line currents with the novel control method; (**e**) capacitor and port-output voltages with the novel control method; (**f**) enlarged view 1 of Figure 20e; (**g**) enlarged view 2 of Figure 20e.

It can be observed that the controlled line current I_{34} quickly responded to the command value when the MI-DCPFC was inserted to the system at t_4, as shown in Figure 20a. However, as shown in Figure 20b,c, as the voltage V_{TP2} introduced in line 24 and voltage V_{TP3} introduced in line 34 were synchronized to switch between 0 and U_c, although the I_{34} is also reduced, its specific reduced amounts could not be controlled separately at this time.

The performance of the MI-DCPFC with the novel control method is shown in Figure 20d–g. The MI-DCPFC is accessed into the system at t_5, and with the command controlling I_{24} and I_{34} are reduced to I_{24} = 3 A and I_{34} = 10 A, respectively. When operating to t_6, the power flow control command is changed again, where with controlling, I_{34} reduced to 3 A, but control further reduces I_{24} to 8A. It can be observed that when the MI-DCPFC is accessed into the system, the controlled line current I_{34} also quickly responded to 3 A, as shown in Figure 20d. What is more, the reduced amounts of the current I_{24} can simultaneously be controlled freely with the reducing control of I_{34}. Correspondingly, the voltage V_{TP2} introduced in line 24 is controlled and stably switched between U_c, 0 and $-U_c$, as shown in Figure 20e–g.

6.2. Four-Port MI-DCPFC Verified Results

6.2.1. System Test

With the topology of the transmission system shown in Figure 13b, Figure 21 shows the line currents of the transmission system with no MI-DCPFC accessed under the normal operation. It can be observed that the system operates stable when it starts up. The measured values of each line current are about I_{14} = 6.8 A; I_{24} = 12.5 A; I_{34} = 4.8 A; I_{45} = 8.6 A; I_{12} = 1.2 A; I_{23} = −1.2 A; I_{35} = 0.6 A, respectively.

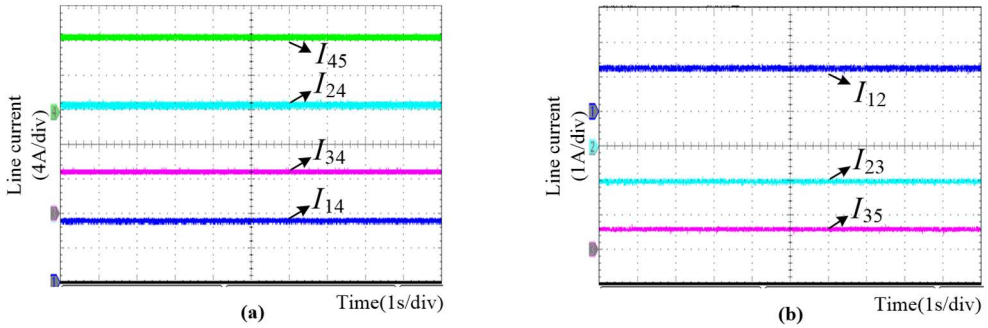

Figure 21. Experiment results under normal operation: (**a**) line currents part 1; (**b**) line currents part 2.

6.2.2. Case Studies

The four-port MI-DCPFC is confirmed in this section. Same as the simulation, the following three different cases are respectively confirmed when the system starts up normally.

(1) At t_1, control I_{14} reduces to 1 A, and control I_{24} and I_{45} increase to 14 A and 10 A, respectively;
(2) At t_2, control I_{14} and I_{45} reduce to 4 A and 6 A, respectively; and control I_{24} increases to 14 A;
(3) At t_3, control I_{14}, I_{45} and I_{24} reduce to 4 A, 6 A and 8 A, respectively.

The main experiment results are shown in Figure 22; the measurement values of each line current under different test conditions are shown in Table 8. It can be observed that under the different control conditions, the controlled lines can all quickly track the corresponding power flow control commands, and then maintain stable operation. In addition, the capacitor voltage fluctuation is small, and the voltage state introduced in the connection line by the output port is stable.

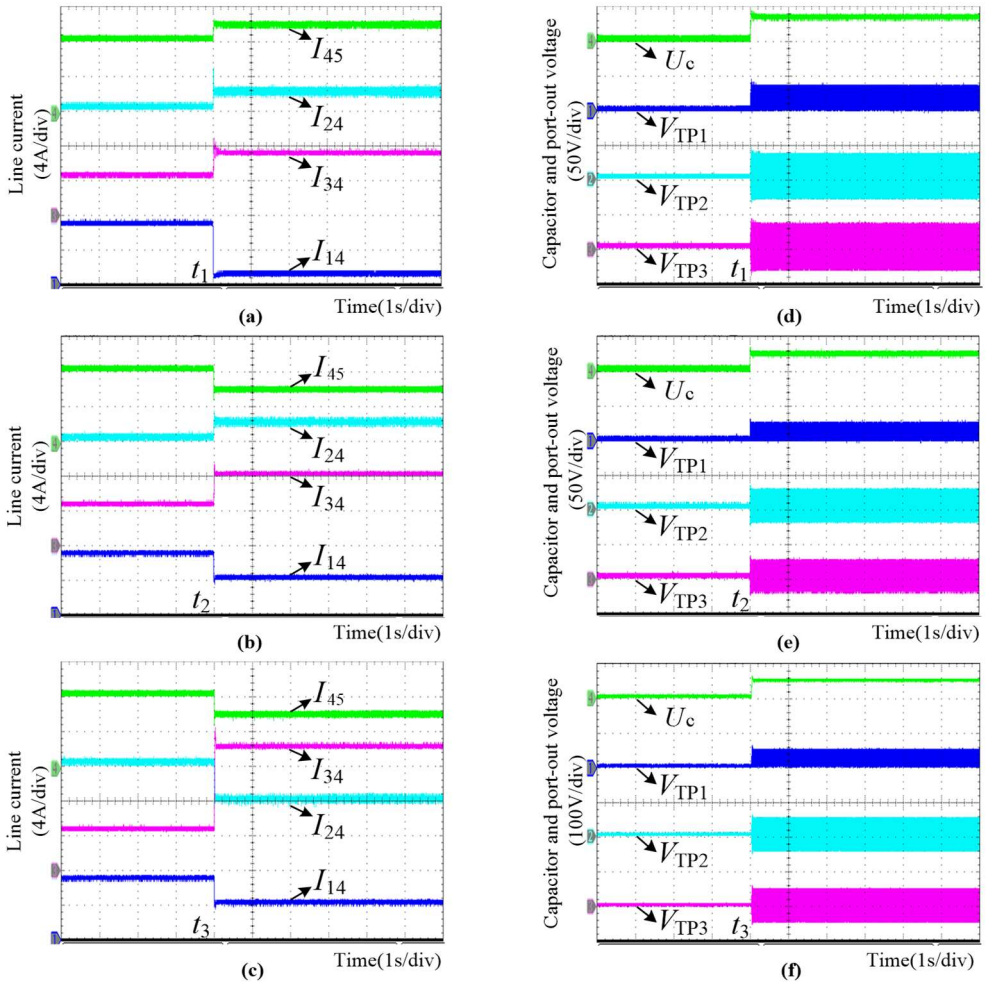

Figure 22. Experiment results of four-port MI-DCPFC: (**a**) line currents under case 1; (**b**) capacitor and port-output voltages under case 1; (**c**) line currents under case 2; (**d**) capacitor and port-output voltages under case 2; (**e**) line currents under case 3; (**f**) capacitor and port-output voltages under case 3.

Table 8. The measurement values of each line current under different test conditions in the experiment.

Line Current/kA	No Command /A	Case 1/A	Case 2/A	Case 3/A
I_{14}	6.8	1	4	4
I_{45}	8.6	10	6	6
I_{24}	12.5	14	14	8
I_{34}	4.8	7	8	14
I_{23}	-1.2	3	0	6
I_{12}	1.2	7	4	4
I_{35}	0.6	2	−2	−2

Concluding all previous experiment studies in this section, it can be seen that the performances of the MI-DCPFC under different conditions are consistent with the results in the simulation. This shows that the simplified MI-DCPFC can achieve effective power flow control under different power flow regulation requirements.

7. Conclusions

The dc power flow control issue in multi-terminal HVDC transmission system was investigated in this paper. The main works and contributions can be summarized as:

(1) Under the background of a interline dc power flow controller, the topology and operation principles of the traditional MI-DCPFC were analyzed. The analysis revealed that the upper and lower switches of the left half-bridge of the MI-DCPFC are always pulsed synchronously during the operating process, respectively. Based on this, this paper presents a switches reduced topology of MI-DCPFC.

(2) To solve the problem of coupling of the port-output voltage of the MI-DCPFC, a novel general control strategy based on CPS-PWM was proposed in this paper. It can help with realizing the decoupling of the port-output voltage of MI-DCPFC, which ensures completely independent tracking of the power flow regulating commands for different controlled transmission lines. In addition, key relationships between the system state variables were derived and analyzed in this study, and the relevant expression of the capacitor voltage of MI-DCPFC under steady state was obtained.

(3) Two five-terminal HVDC transmission systems were developed in the MATLAB/SIMULINK environment and experiment platform. Taking the three-port and four-port topology as examples, the performance of the power flow controller and related control strategy were verified under various test conditions. The results show that the transmission system with proposed MI-DCPFC can operate in a stable manner, and the controller can quickly and efficiently track the power flow regulation commands.

(4) The simplified topology and capacitor voltage decoupling control strategy of the traditional MI-DCPFC were studied in this paper. However, the question of how to further improve the controller and realize the self-control of the capacitor voltage and the line current reversal is the next research area to investigate.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Table A1. Conduction states of the traditional three-port MI-DCPFC.

Mode	Direction	Reduced	Increased	Switching States					
				S_{c1}	S_{c2}	S_{c3}	S_{d1}	S_{d2}	S_{d3}
1	forward	I_{p1}	I_{p2} and I_{p3}	off			off	on	on
2	forward	I_{p2}	I_{p1} and I_{p3}				on	off	on
3	forward	I_{p3}	I_{p1} and I_{p2}				on	on	off
4	forward	I_{p1} and I_{p2}	I_{p3}				off	off	on
5	forward	I_{p1} and I_{p3}	I_{p2}				off	on	off
6	forward	I_{p2} and I_{p3}	I_{p1}				on	off	off
7	reverse	I_{p1}	I_{p2} and I_{p3}	on	off	off	off		
8	reverse	I_{p2}	I_{p1} and I_{p3}	off	on	off			
9	reverse	I_{p3}	I_{p1} and I_{p2}	off	off	on			
10	reverse	I_{p1} and I_{p2}	I_{p3}	on	on	off			
11	reverse	I_{p1} and I_{p3}	I_{p2}	on	off	on			
12	reverse	I_{p2} and I_{p3}	I_{p1}	off	on	on			

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