High Step-up Coupled Inductor Inverters Based on qSBIs

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Abstract: In this paper, two types of high step-up coupled inductor inverters based on qSBIs (quasi-switched boost inverters) are proposed. By applying the coupled inductor to the qSBIs, the voltage gain of the proposed inverter is regulated by turn ratio and duty ratio. Thus, a high voltage gain can be achieved without the circuits operating at the extreme duty cycle by choosing a suitable turn ratio of the coupled inductor. In addition, the proposed circuits have the characteristics of continuous input current and low voltage stress across the passive components. A boost unit can be added to the proposed inverters for further improvement of the voltage gain. In this paper, the working principle, steady state analysis, and the comparisons of the proposed inverter with other impedance-source inverters are described. A 200 W prototype was created and the experimental results confirm the correctness of the analysis in this paper.

Keywords: inverter; high voltage gain; coupled inductor; DC–AC converter

1. Introduction

As the world's energy structure has changed, renewable energy sources have been widely used in power generation, especially solar energy, such as photovoltaic (PV) power generation. Inverters with high voltage gain ability are used to connect new energy sources to the grid. This requires a PV generation system with high efficiency and high reliability. The Z-source inverter (ZSI) was first proposed in [1] to implement single-stage converter conversion with a buck-boost function. However, due to some shortcomings of the Z-source network, such as limiting boosting capability, discontinuous input current, no common ground, large starting current, and high voltage stress of the passive components, these features limit its wide application. Therefore, researchers have proposed many switching boost/quasi-switch boost inverters [1–6] instead of Z-source/quasi Z-source inverters (ZS/qZSIs). A switched boost inverter (SBI), which consists of one more active switch and a lower number of passive components than the ZSI, is proposed in [7]. In particular, its switch is only an auxiliary switch for which the voltage and current stress are low, unlike the switch of the cascade circuit. However, in the SBI, the voltage stress of the capacitor is equal to the DC link voltage. As the output voltage increases, the voltage stress across the capacitor becomes higher. Furthermore, the high voltage level capacitor increases the cost of the circuit. In addition, the input current is discontinuous in this circuit. Compared with the SBI, the quasi-SBI (qSBI) [2] has low voltage stress of the capacitor and continuous input current. Two embedded-type qSBIs are shown in Figure 1. The voltage gain is defined by:

$$B = \frac{V_{PN}}{V_{in}} = \frac{1}{1 - 2D} \tag{1}$$

D is the duty cycle in a period and denotes the peak DC-link voltage.
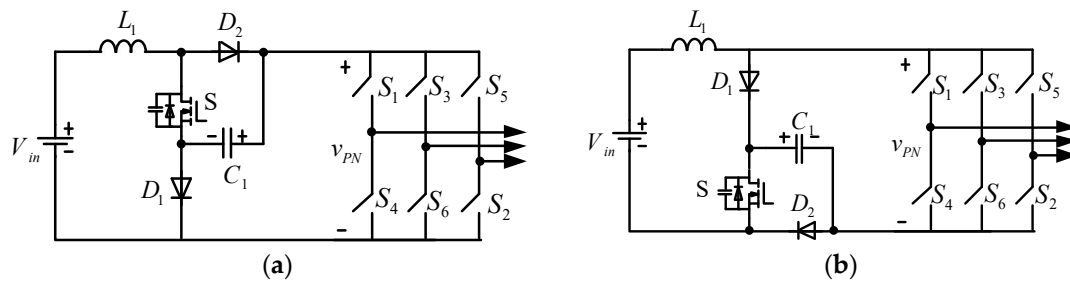
Figure 1. (**a**) Type I qSBI and (**b**) type II qSBI (qSBIs: quasi-switched boost inverters).

To increase the boost ability of the qSBI, many improvements have been proposed in recent years. Many passive elements are applied to the qSBI. In [8] the diode-assisted/capacitor-assisted extended-boost, qZSI (DA/CA-qZSI) has been proposed; however, its voltage gain is not very high even though some passive elements are applied. A switched-inductor (SL) cell was added to the qSBI in [9,10] for a higher output voltage, but the voltage stress across the capacitor, diode, and switch is large, which is equal to the output voltage. A switched capacitor (SC) has been used in the qSBI [11], but the voltage gain does not achieve the desired effect and the voltage stress of the switch S_0 is also high. Moreover, conventional boost converters generally cannot achieve very high voltage gains, and the duty cycle is extremely high due to parasitic parameters [12].

Determining how to properly apply components to obtain a high output voltage with low voltage stress across the switch and acheive a suitable non-extreme duty cycle has become a hot issue in research. In order to solve the above problems, this paper proposes a new type of qSBI inverter based on the coupled inductor. In the converters, with a reasonable design of the turn ratio of the coupled inductor, the high voltage gain can be achieved while avoiding extreme duty cycles [13–18]. Moreover, in the proposed circuit, the switch only plays a supporting role, so the voltage and current stresses of the switch can be low. Therefore, the proposed inverters have the features of high voltage gain and small voltage stress across the components. In addition, the converters have the advantage of a voltage gain that can also be increased by adjusting the turns ratio of the coupled inductor, so that a high boost ability can be obtained with a suitable duty cycle, and the voltage and current stress of the switch is low. It is also possible to extend the proposed inverter by adding cascade cells to increase voltage gain.

The organization of this paper is as follows. Firstly, the research background is introduced, and the idea of applying a coupled inductor to a qSBI circuit is proposed. The second chapter analyzes the principle of the circuit, including the converter's operating mode, the voltage gain, device voltage and current stress, and the modulation scheme. The third chapter compares the proposed circuit with other similar circuits. The fourth chapter constructs an experimental platform and analyzes the experimental results. The final chapter is the conclusion, summarizing the full paper and demonstrating the effectiveness of the proposed circuit.

2. Proposed Inverter Topologies

The proposed converters are shown in Figure 2, where one capacitor (C_2), one coupled inductor (N_1, N_2), and one diode (D_3) are applied to the qSBIs. Type 1 circuit is shown in Figure 2a, and the ground node of its input voltage is directly connected to the negative node of the three-phase bridge circuit. The other is shown in Figure 2b, in which the ground node of the input voltage is not directly connected. The two circuits all consist of the coupled inductor (N_1 and N_2), an active switch (S), two capacitors (C_1 and C_2) and three diodes (D_1, D_2 and D_3), with a three-phase bridge unit. In this paper, the type 1 topology of the proposed inverters is analyzed and verified as an example.
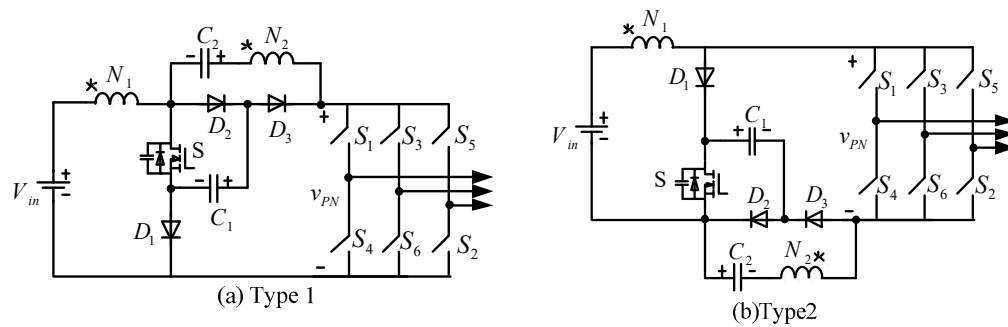
Figure 2. The topology of the proposed inverters (**a**) Type 1; (**b**) Type 2.

2.1. Operation Modes

The equivalent circuit of the proposed type 1 converter is shown in Figure 3. In order to facilitate the circuit analysis of the proposed converter, some preconditions are shown as follows:

(1)   The coupled inductor of the equivalent circuit can be composed of an ideal transformer with a turn ratio of $n = N_2:N_1$, a parallel magnetizing inductor L_M, and a leakage inductance inductor L_K.
(2)   The value of the capacitor is large enough to keep the capacitor voltage constant for one switching cycle.
(3)   The diodes are ideal, but the parasitic capacitance of the switch S cannot be ignored.
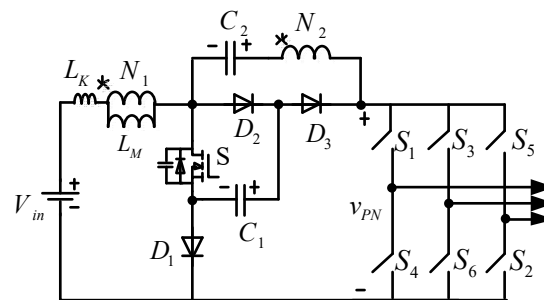
Figure 3. Equivalent circuit of the proposed type 1 inverter.

Based on the above assumptions, Figure 4 shows a partial waveform of the proposed converter in one switch cycle. The analysis of the four stages of operation is as follows.

Stage I [t_0, t_1]: As shown in Figure 5a, the switch S turns on and the three-phase bridge unit operates in the shoot-through (ST) state. During this time period, diode D_3 is turned on and diodes D_1 and D_2 are turned off. Input source V_{in} and the capacitor C_1 are connected in series to charge the leakage inductance L_k and magnetizing inductance L_M, thus the current I_{N1} increases linearly. At the same time, the energies of coupled inductor N_2 and the capacitor C_1 are released to the capacitor C_2.

Stage II [t_1, t_2]: In this time interval, the three-phase bridge unit operates in the non-through state (NST) and the switch S is turned off. Figure 5b shows the current-flow path. The diodes D_1 and D_2 are reverse-biased, and the diodes D_3 forward-biased. The parasitic capacitor of the switch begins charging by winding of N_1 and N_2. The capacitor C_2 is still working in the charging state. When the voltage of the parasitic capacitor of switch S is higher than the voltage of the capacitor C_1 at t_2, the diode D_2 starts to conduct and this stage ends.

Stage III [t_2, t_3]: During this stage, the switch S is turned off and the three-phase bridge unit operates in the NST state. The diode D_3 is reverse-biased and diodes D_1 and D_2 are forward-biased, as shown in Figure 5c. During this time interval, the capacitor C_1 is charged by the input voltage V_{in} and the winding of N_1. Meanwhile, the input source V_{in}, the capacitor $C_{2,}$ as well as the coupled inductor (N_1 and N_2), are in series to provide a high output voltage to the load.

Stage IV [t_3, t_4]: At t_3, the switch S starts to turn on and the three-phase bridge unit operates in the shoot-through mode. During this transition interval, the current of N_2 cannot be suddenly changed due to the presence of leakage inductance. As shown in the Figure 5d, the diodes D_1 and D_2 are reverse-biased because of the voltage of capacitor C_1. In this stage, the winding of N_1 is charged by the capacitor C_1 and the input voltage V_{in}. When the current I_{N1} decreases to zero and begins to flow in the opposite direction, this stage ends, and the next switching period begins.
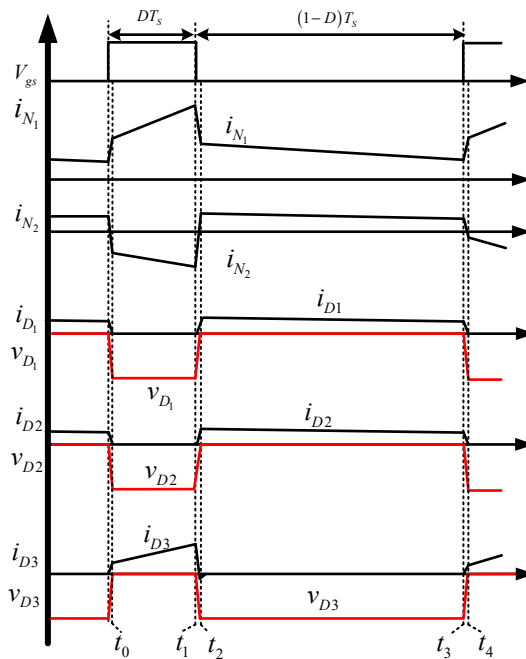

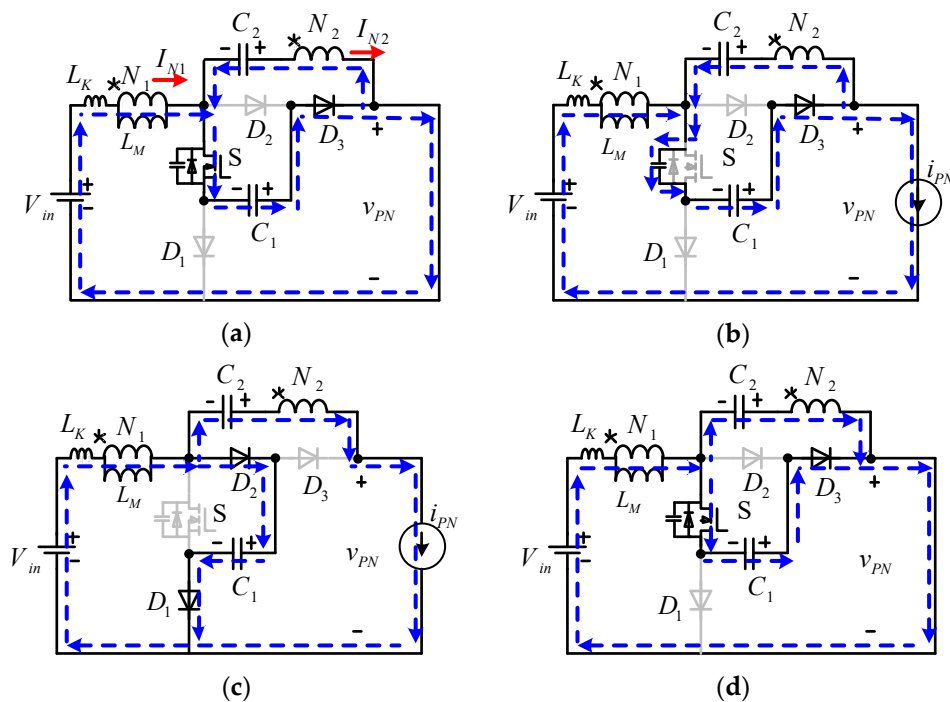**Figure 4.** Typical waveforms of the proposed converter during one switching period.

Figure 5. Operating modes of the proposed inverter. (**a**) stage I; (**b**). stage II; (**c**). stage III; (**d**). stage IV.

2.2. Math Derivations

In order to simplify the analysis of the proposed converter, the transient stage II and stage IV are neglected.

According to Figure 5a, the voltage relationship during stage I can be expressed as:

$$V_{LM} = V_{in} + V_{C1} \tag{2}$$

$$\frac{N_2}{N_1} V_{LM} = V_{C2} - V_{C1} \tag{3}$$

In the time period of stage III, the following equations can be obtained based on Figure 5c:

$$V_{LM} = V_{in} - V_{C1} \tag{4}$$

$$\frac{N_2}{N_1} V_{LM} = V_{C1} + V_{C2} - V_{PN} \tag{5}$$

Applying the volt-second balance principle to the inductor, the following formula can be verified:

$$(V_{in} + V_{C1})DT + (V_{in} - V_{C1})(1 - D)T = 0 \tag{6}$$

According to Equations (2)–(6), the voltages of capacitor C_1 and capacitor C_2 can be expressed as:

$$V_{C1} = \frac{1}{1 - 2D} V_{in} \tag{7}$$

$$V_{C2} = \frac{2\frac{N_2}{N_1}(1 - D) + 1}{1 - 2D} V_{in} \tag{8}$$

Thus, in stage III, the peak DC-link voltage V_{PN} can be written as:

$$V_{PN} = \frac{2\frac{N_2}{N_1} + 2}{1 - 2D} V_{in} \tag{9}$$

The boost factor can be defined as:

$$B = \frac{V_{PN}}{V_{in}} = \frac{2\frac{N_2}{N_1} + 2}{1 - 2D} \tag{10}$$

When the modulation index of the inverter is denoted as M, the duty cycle D will be limited to $(1 - M)$, thus in this case, the peak voltage of the phase voltage $\widetilde{v}_o$ in the AC side can be expressed as:

$$\widetilde{v}_o = MV_{PN} = \frac{2\frac{N_2}{N_1} + 2}{2M - 1} \tag{11}$$

2.3. Voltage and Current Stress Analysis

For the sake of analysis, the capacitor voltage ripple has been ignored. From Figure 1a, the voltage stress of the diodes D_1 and D_2 can be expressed as:

$$V_{D1} = V_{C1} = \frac{1}{1 - 2D} V_{in} \tag{12}$$

$$V_{D2} = V_{C1} = \frac{1}{1 - 2D} V_{in} \tag{13}$$

During stage III, the voltage stress on the diode D_3 and the switch S can be derived from:

$$V_{D3} = V_{PN} - V_{C1} = \frac{2\frac{N_2}{N_1} + 1}{1 - 2D} V_{in} \tag{14}$$

$$V_S = \frac{1}{1 - 2D} V_{in} \tag{15}$$

The circuit on the AC side can be replaced by an equivalent resistance R_l on the DC side, when the three-phase bridge unit operates in a non-through state. Then, based on the calculation method in [2], the average DC link current I_{PN} of the proposed inverter is:

$$I_{PN} = \frac{(1-D)V_{PN}}{R_l} = \frac{(1-D)(2\frac{N_2}{N_1} + 2)}{(1-2D)R_l} V_{in} \tag{16}$$

Applying the principle of conservation of magnetic flux to the coupled inductor, the relationship between the inductor currents at different times can be expressed as:

$$I_{N1}^{[t_0 - t_2]} + \frac{N_2}{N_1} I_{N2}^{[t_0 - t_2]} = -I_{N1}^{[t_2 - t_4]} - \frac{N_2}{N_1} I_{N2}^{[t_2 - t_4]} \tag{17}$$

Meanwhile, the relationship between $I_{N1}^{[t_0 - t_2]}$ and $I_{N1}^{[t_2 - t_4]}$ can be expressed by the following formula:

$$V_{in}I_{N1}^{[t_0 - t_2]}D + V_{in}I_{N1}^{[t_2 - t_4]}(1 - D) = V_{PN}I_{PN} \tag{18}$$

According to the charge and discharge balance of the capacitor C_2, the values of $I_{N2}^{[t_0 - t_2]}$ and $I_{N2}^{[t_2 - t_4]}$ can be derived from:

$$I_{N2}^{[t_0 - t_2]} = -\frac{I_{PN}}{D} \tag{19}$$

$$I_{N2}^{[t_2 - t_4]} = \frac{I_{PN}}{1 - D} \tag{20}$$

According to Equations (17)–(20), the following equations can be obtained:

$$I_{N1}^{[t_0 - t_2]} = I_{PN}\left(\frac{N_2}{N_1 D} - \frac{2\frac{N_2}{N_1} + 2}{(1 - 2D)^2}\right) \tag{21}$$

$$I_{N1}^{[t_2 - t_4]} = I_{PN}\left[\frac{2\frac{N_2}{N_1} + 2}{(1 - 2D)^2} - \frac{N_2}{N_1(1 - D)}\right] \tag{22}$$

Therefore, the average current value of the diode D_1, D_2, D_3 and S during the on-state period can be expressed as:

$$I_{D3} = I_S = I_{PN}\left[\frac{N_1 + N_2}{DN_1} - \frac{2\frac{N_2}{N_1} + 2}{(1 - 2D)^2}\right] \tag{23}$$

$$I_{D1} = I_{D2} = I_{PN}\left[\frac{2\frac{N_2}{N_1} + 2}{(1 - 2D)^2} - \frac{N_2 + N_1}{N_1(1 - D)}\right] \tag{24}$$

2.4. Modulation Scheme

The proposed inverter was modulated by the scheme of Space Vector Pulse Width Modulation (SVPWM). The synthesis voltage vector of the three-phase sinusoidal voltage is a rotating vector which can be called the reference voltage vector. Similar to the Z-source inverter, the proposed inverter has eight traditional non-through voltage vectors and one short-through zero voltage vector, as shown

in Figure 6a. The non-through vectors are composed of six active vectors and two non-through zero voltage vectors, where the vertices of the six active voltage vectors form a regular hexagon. Note that the shoot-through vectors and non-through zero voltage vectors produce the same zero voltage to the load terminal. Therefore, the non-through zero vectors can be partially replaced with the short-through zero vector without affecting the load.
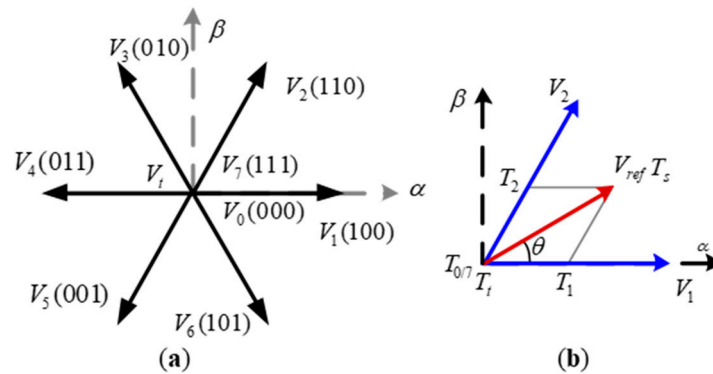

Figure 6. (**a**) Space vector distribution; (**b**) vector synthesis.

As shown in the Figure 6a, the reference voltage vector at any location can be synthesized by two adjacent effective voltage vectors and zero voltage vectors. The effective time of the two adjacent effective voltage vectors required in one cycle can be obtained by the principle of vector synthesis. Taking the reference voltage vector in the first sector as an example, the synthesis of the reference vector has been shown in Figure 6b. Then, the following formula can be obtained:

$$V_{ref} = \frac{T_1}{T_s}V_1 + \frac{T_2}{T_s}V_2 + \frac{T_{0/7}}{T_s}(V_0, V_7) + \frac{T_t}{T_s}V_t \tag{25}$$

where T_s represents a time period, T_1 and T_2, respectively, represent the time of the effective voltage vectors V_1 and V_2. $T_{0/7}$ and T_t are the time of the NST zero vector (V_0 or V_7) and ST zero vector V_t. The value of T_1, T_2, T_0 and T_t can be calculated as:

$$\begin{cases} T_1 = \frac{2}{\sqrt{3}}\frac{|V_{ref}|}{|V_1|}T_s \cdot \sin(\frac{\pi}{3} - \theta) \\ T_2 = \frac{2}{\sqrt{3}}\frac{|V_{ref}|}{|V_2|}T_s \cdot \sin\theta \\ T_t = T_s D \\ T_{0/7} = T_s - T_1 - T_2 - T_t \end{cases} \tag{26}$$

Compared with five-part SVPWM, the seven-part SVPWM can reduce the THD of output voltages and currents. The vectors sequence of the seven-part SVPWM scheme used in the proposed inverters is shown in Figure 7. The time of shoot-through zero vectors is divided into six segments and placed into voltage vector transition.

It can be seen that the seven-part SVPWM has an additional short-through state compared to the traditional SVPWM modulation; however, each phase leg still switches on and off once per switching cycle. The partial time of the non-through zero vectors is replaced by the short-through zero vectors, thus the active states time interval does not change. The short-through zero vectors increase the voltage of V_{PN}, so at the same input voltage V_{in} and modulation M, the proposed inverter can output a higher AC voltage. According to the section of math derivations, the peak voltage of the phase voltage $\widetilde{v}_o$ in the AC side was decided by D and M. That is to say, the desired output voltage can be realized by adjusting the short-through state time in SVPWM modulation while the voltage V_{in} has an obvious fluctuation, or not enough to directly generate a desired output voltage.
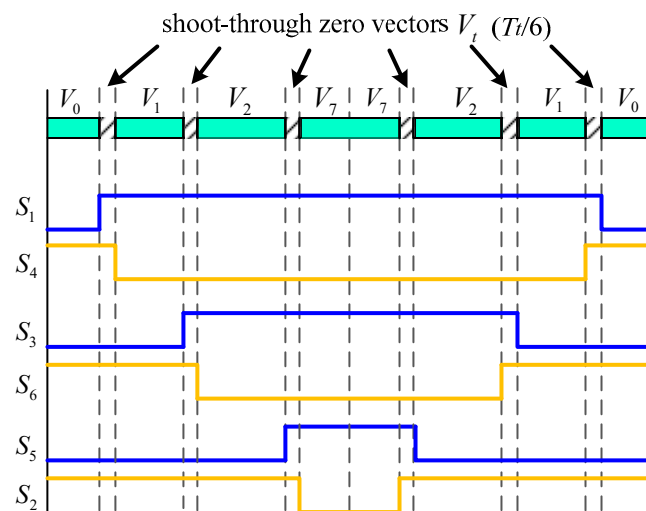
Figure 7. The vectors sequence of seven-part SVPWM scheme. (SVPWM: Space Vector Pulse Width Modulation).

2.5. Extended Circuit

The proposed circuit can be extended for a higher output voltage. In this proposed extended circuit, two capacitors (C_3 and C_4) and two diodes (D_4, D_5), with the winding N_3 are regarded as one cell. The voltage gain of the extended circuit will greatly increase as the number of cells increases. The extended circuit is shown in Figure 8.
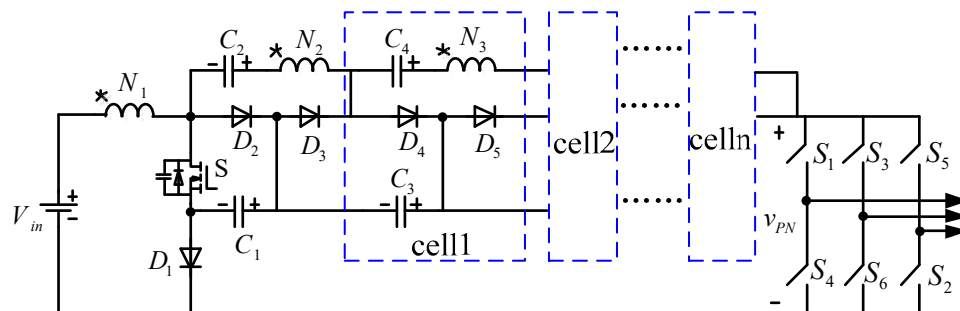
Figure 8. Extended circuit of the proposed inverter.

3. Performance Comparisons

In order to better reflect the advantages of the proposed circuit, as shown in the Table 1, the proposed inverter has been compared with several other circuits, such as qSBI [2], ASC/SL-qZSI (Active-Switched-Capacitor/Switched-Inductor Quasi-Z-Source Inverters) [10], the converter in [19] and ASC/SCL-ZSI (Active-Switched-Capacitor/Switched-Capacitor-Inductor Z-Source Inverters) [20]. N_2/N_1 is represented by the parameter n in the comparison. Some important parameters in the circuit, such as the boost factor, switch stresses, maximum stresses of the diode and capacitor, and number of components are summarized in Table 1.

**Table 1.** Comparison of the proposed converter with similar prototypes.

	qSBI [2]	ASC/SL-qZSI [10]	ASC/SCL-ZSI [20]	Converter in [19]	Proposed Inverter
Diode	2	5	5	5	3
Inductor	1	2	2	3	2
Capacitor	1	1	2	3	2
Boost Factor	$\frac{1}{1-2D}$	$\frac{1+D}{1-3D}$	$\frac{1-D}{1-(n+3)D}$	$\frac{2+n}{(1-D)^2}$	$\frac{2n+2}{1-2D}$
Maximum voltage stress of capacitors	V_{PN}	V_{PN}	$\frac{1-D}{1+D}V_{PN}$	$\frac{n+1-Dn}{2+n}V_{PN}$	$\frac{2n(1-D)+1}{2n+2}V_{PN}$
Maximum voltage stress of diodes	V_{PN}	V_{PN}	$\frac{1-D}{1+D}V_{PN}$	$\frac{1+n}{2+n}V_{PN}$	$\frac{2n+1}{2n+2}V_{PN}$
Voltage stress of active switches	V_{PN}	V_{PN}	$\frac{1-2D}{1+D}V_{PN}$	$\frac{1}{2+n}V_{PN}$	$\frac{1}{2n+1}V_{PN}$

3.1. Number of Components

According to Table 1, compared with the qSBI [2], the proposed converter adds a coupled inductor and capacitor to obtain high voltage gain. The proposed converter has fewer components than the converters in [10,19,20]. Specifically, the proposed converter uses a smaller number of diodes, reducing the circuit cost and size.

3.2. Boost Factor

The biggest advantage of the proposed circuit is its voltage-boosting capability. It can be seen from Figure 9 that the boost factor of the proposed circuit is larger than those of the other three circuits with the same duty cycle. Although the voltage gain of the circuit in [20] is larger than the proposed circuit when the duty ratio D is greater than 0.175, the duty ratio of the converter in [20] reaches the limit at 0.2; therefore, the adjustment range is not as large as the proposed converter. Furthermore, the direct connection to the voltage source is an inductor rather than a diode, so the input current is continual, which benefits the power electronics applications, such as photovoltaic (PV) power generation systems.
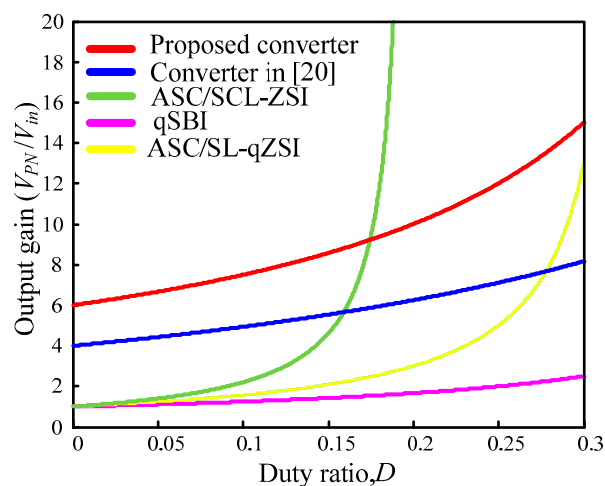

Figure 9. Boost factor comparisons.

3.3. The Voltage Stresses of the Components

In order to better observe the comparison results of the voltage stress of each component, several graphs are drawn according to Table 1. For a fair comparison, the turns ratio of the coupled inductor is the same: $n = 2$. It can be seen from Figure 10 that the maximum voltage stress of the switch of the proposed circuit is the smallest, which is an attractive advantage. Because it reduces the switching loss, and some low-voltage switches can be applied to the circuit to reduce the circuit cost. According to Figure 11, it can be found that the maximum voltage stress of the capacitors in the proposed circuit is smaller than the converters in [2,10], and is nearly equal to the converter in [19,20].
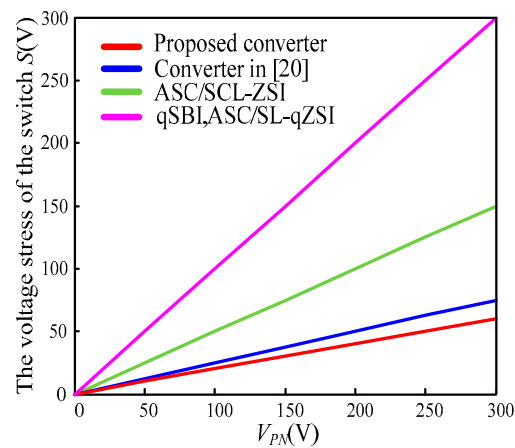
Figure 10. The voltage stress of the switch comparisons.
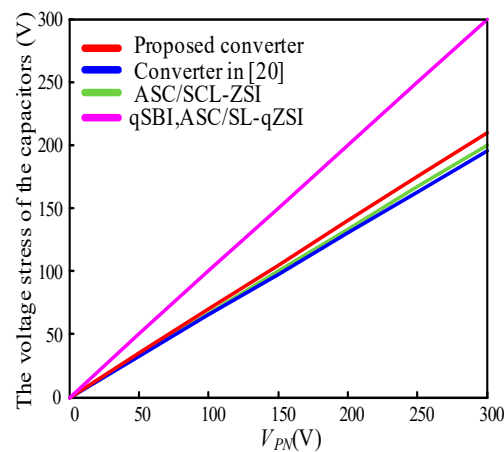
Figure 11. The voltage stress of the capacitors comparisons.

4. Experimental Results

In order to verify the correction of the analysis of the proposed inverter, an experimental circuit of 200 W was built and tested. The prototype of the experimental setup is shown in Figure 12, which includes the main circuit topology, switch drive circuit, modulation circuit, and DSP (Digital Signal Processing) control board. The parameters of the experiment are shown in Table 2. The power of the experimental circuit was 200 W, with an input voltage of 24 V, a duty ratio equal to 0.2, and a turn ratio of 2, which can be applied in photovoltaic power generation.
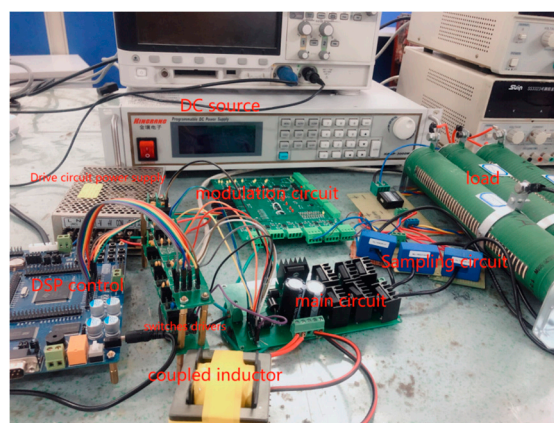

Figure 12. The prototype of the experimental setup.

Table 2. Parameters of the experiment.

Parameters	Values
Rated output power, P_o	200 W
Input voltage, V_{in}	24 V
Output voltage, V_{PN}	240 V
frequency, f	50 kHz
Capacitor C_1	100 uF
Capacitor C_2	47 uF
Turn ratio n	$N_2:N_1 = 2$
Switch (S)	IRFP4568

The results of the experiment are shown in the Figure 13. The input voltage V_{in} and peak DC-link voltages V_{PN} are shown in Figure 13a. Figure 13b shows the voltage of the capacitors C_1 and C_2. According to Figure 13c, the input current is continuous. It can be seen from Figure 13b,d that the voltage stresses of diode D_1 and D_2 are equal to the voltage of capacitor C_1. Figure 13e shows the voltage waveform and current waveform of the switch S. The result of the experiment shows that the voltage stress of the switch is equal to capacitor C_1 voltage, which is in line with the theoretical analysis results. The line voltage and phase current at the AC side of the converter are shown in Figure 13f. The efficiency of the proposed inverter under different loads is shown in Figure 14. The highest efficiency is 93.1% when the input voltage is 24 V and the output power is 250 W.
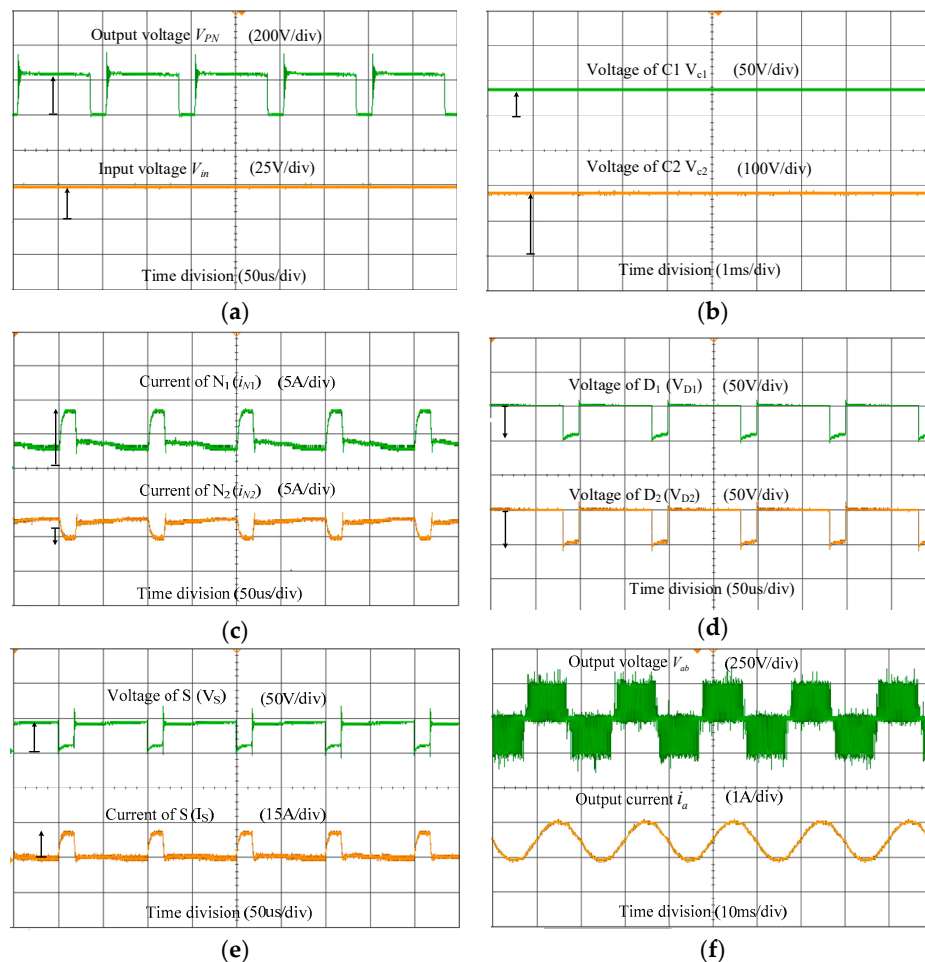
Figure 13. Experimental waveforms for the proposed inverter: (**a**) The input voltage V_{in} and the peak DC-link voltages V_{PN}; (**b**) The voltage of the capacitor C_1 and C_2; (**c**) The current of N_1 and N_2; (**d**) The voltage stresses of diode D_1 and D_2; (**e**) The voltage and current of the switch S; (**f**) The output voltage V_{ac} and the output current i_a.
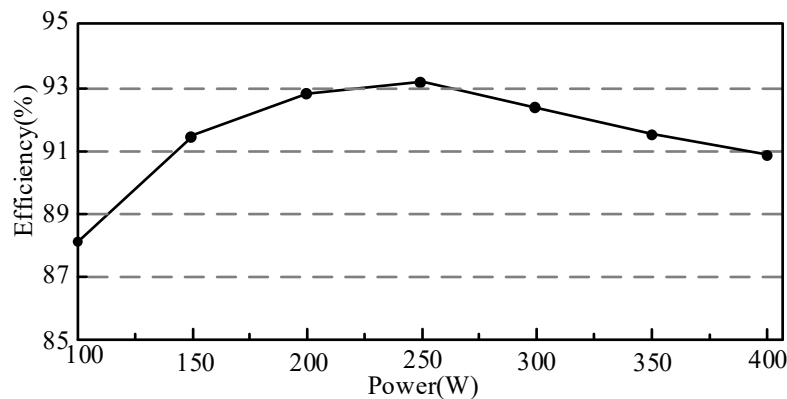
Figure 14. Measured efficiency of the converter.

5. Conclusions

Two novel high step-up coupled inductor inverters based on qSBIs were proposed in this paper. Compared with the qSBI, these circuits use a coupled inductor and add one capacitor and one diode. The proposed circuits have the characteristics of high voltage gain and low voltage stress across the passive components. Due to the application of the coupled inductor, a high voltage gain can be achieved without the circuits operating at the extreme duty cycle. The voltage stress of the switch S is small, which is beneficial to reduce the losses, and improve the efficiency of the converter. In addition, a repeating boost unit can be added to the proposed inverters for further improvement of the voltage gain. Therefore, the proposed converter can be widely applied to the field of new energy power generation. The experimental results of input voltage 24 V and output voltage 240 V verify the performance of the proposed inverter and the experimental waveforms verify the theoretical analysis. In future work, attention should be paid to reducing the voltage spike on the main switch caused by the use of the coupled inductor; a problem that often occurs in converters that are based on the coupled inductor, and one that affects the efficiency of the converter. The passive clamp circuit can be applied to reduce the effect of leakage inductance, and the high-performance MOSFET can be used to improve the converter efficiency.

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