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Improved Deadbeat FC-MPC Based on the Discrete Space Vector Modulation Method with Efficient Computation for a Grid-Connected Three-Level Inverter System

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Abstract: The utilization of three-level T-type (3L T-type) inverters in finite set-model predictive control (FS-MPC) of grid-connected systems yielded good performance in terms of current ripples and total harmonic distortions. To further improve the system's performance, discrete space vector modulation (DSVM) was utilized to synthesize a higher number of virtual voltage vectors. A deadbeat control (DBC) method was used to alleviate the computational burden and provide the optimum voltage vector selection. However, 3L inverters are known to suffer from voltage deviation, owing to the imbalance of the neutral-point voltage. We have proposed a simplified control strategy for balancing the neutral point in the FS-MPC with DSVM and DBC of grid-connected systems, not requiring a weighting factor or additional cost function calculation. The effectiveness of the proposed method was validated using simulation and experiment results. Our experimental results show that the execution time of the proposed algorithm was significantly reduced, while its current quality performance was not affected.

Keywords: deadbeat control; discrete space vector modulation; computation efficiency; model predictive control; grid connected system; three-level system; T-type inverter

1. Introduction

Model predictive control (MPC) has become an attractive alternative for controlling power electronic applications, such as motor drives and power converters [1]. There are two main categories of MPC: (1) continuous MPC (CMPC), in which output is generated and delivered to a modulator, and (2) finite-set MPC (FS-MPC), which can control a finite number of feasible switching states using a predefined cost function [2–5]. Among the two types, FS-MPC is preferable, owing to its many advantages, such as the fast dynamic response, intuitive appeal, inclusion of constraints and nonlinearities, and easy implementation. However, an important drawback of the original method is its variable switching frequency and large current ripples, which requires the use of large passive filter components [2,6].

Numerous studies aiming to improve the performance of classical FS-MPC for both power converters and motor drives have been performed. To reduce current ripples and alleviate harmonic distortion, an attempt was made in [7,8] to increase the prediction horizon of FS-MPC. Although good performance was achieved, intensive experimentation is still necessary for determination of correct weighting factors and control horizons [8], which is computationally demanding [9]. A deadbeat solution was suggested in Reference [10] for a two-level voltage-source inverter, which allows the computational load of FS-MPC to be reduced by reducing the complete enumeration for the whole

voltage vectors. Although this solution helped to address the problem of computational intensity, the large torque ripples could not be eliminated.

FS-MPC based on discrete space vector modulation (DSVM) was proposed in References [11,12] to reduce current ripples and guarantee a constant switching frequency. The main advantage of DSVM is that it allows the number of degrees of freedom to be increased by synthesizing various virtual voltage vectors in the space vector diagram [12]. Similarly to classical FS-PTC, the optimal voltage vector is selected to minimize the objective error in the respective cost function, and is applied to the inverter using space vector modulation (SVM). Nevertheless, the main issue associated with the DSVM approach is its high computational burden, owing to a large lookup table that holds the initialized virtual voltage vectors. To solve this problem, deadbeat control was utilized to consider a limited number of virtual voltage vectors, regardless of their number [13]. In this way, the calculation time was significantly reduced, making the method suitable for realistic applications.

Although two-level inverters (2L inverters) are extensively used for power converters and motor drives for generation of voltage vectors applied to terminals [14], they suffer from some issues. Two-level inverters require a very high switching frequency; hence, a higher harmonic current distortion is generated, owing to the limitation of voltage levels. In addition, the maximal DC link voltage is constrained due to the rating of the semiconductors. Therefore, multilevel inverters (ML inverters) have been considered an attractive solution capable of solving the above-mentioned problems and synthesizing output voltages with several discrete levels. Three-level inverters (3L inverters), such as neutral-point clamped (NPC) and T-type inverters, are the most prominent topologies of ML inverters. Compared with 2L inverters, the number of degrees of freedom for obtaining the voltage vectors is higher, which yields better current quality and better control. Despite the advantages of 3L inverters, neutral-point voltage balancing seriously affects their control performance [15], causing higher ripples and distortion of stator currents. Hence, 3L inverters require high-rated capacitors, owing to their unequal voltage distribution, which, in turn, results in a higher voltage stress on the semiconductor switches.

It is worth mentioning it is complicated to include a NPC voltage balance variable in the cost function when implementing DBC. Thus, an algorithm for the DC link capacitor voltage balance should be separately applied for proper 3L inverter operation [16–20]. For example, in Reference [16], a calculated zero-voltage sequence was used for neutral-point balancing, while in Reference [18], the time-offset injection method was used for the same purpose. In Reference [20], a deadbeat model of predictive control combined with the discrete space vector modulation method was used for grid-connected systems using T-type 3L inverters. Two cost functions were used: one for selecting the optimal voltage, and another for the compensated voltage offset, because the neutral-point voltage problem of 3L inverters cannot be included as a variable in the cost function, due to the use of DBC method. The optimal voltage vectors were then synthesized using the SVM method for the entire sampling duration. Nevertheless, the use of two cost functions increased the computational burden of the control system.

This paper proposes a simplified control method for balancing the neutral point in the FS-MPC with the DSVM and DBC of grid-connected systems. Therefore, unlike the approach in Reference [20], the proposed method does not require additional cost functions for balancing the capacitance voltage. The proposed method led to a significant reduction in computation time while maintaining the current quality performance. This method was simulated and experimentally verified on a grid-connected, three-level T-type voltage source inverter.

2. System Modeling

Essentially, there are three switching states for three-level topologies such as neutral-point clamped (NPC) and T-type inverters. Figure 1 shows the topology of a grid-connected, three-level T-type voltage source inverter. The output poles of the T-type inverter can be connected to three different levels of the source voltage, namely the positive bus bar "*P*," the negative bus bar "*N*," and the neutral point

"*0*" [21]. With three-phase to two-phase transformation, the model of the inverter in the stationary *d–q* frame is given by:

$$u = R \cdot \vec{i} + L \cdot \frac{di}{dt} + e. \tag{1}$$

In Equation (1), *R*, *L*, *u*, *i*, and *e*, are the load resistance, filter inductance, inverter voltage vector, output current vector, and grid voltage vector, respectively. Because the top capacitance voltage (V^{top}) and the bottom capacitance voltage (V^{bottom}) can become unequal in the three-level voltage source inverter (VSI) (and hence will produce poor-quality output current and distorted output voltage), the capacitor voltages should be observed and taken into account at every time step, to ensure that they become balanced. The dynamic equations of the two capacitor voltages are given by:

$$V^{top} = V^{top} + I_{NP} \cdot (T_s / C) \tag{2}$$

$$V^{bottom} = V^{bottom} + I_{NP} \cdot (T_s / C) \tag{3}$$

where *C* is the capacitance of each capacitor, T_s is the sampling time, and I_{NP} is the neutral-point current.

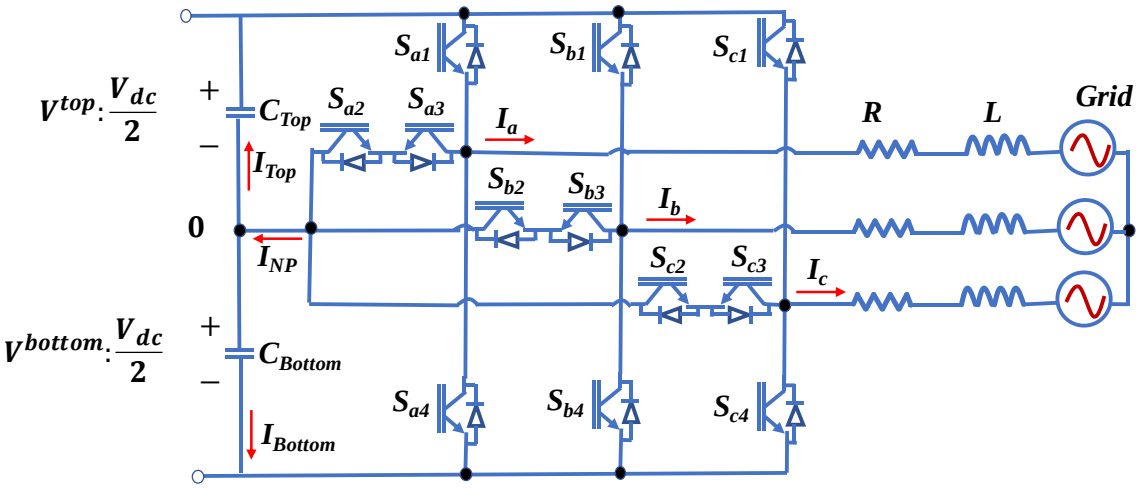


Figure 1. Circuit diagram of three-level T-type inverter.

3. FS-MPC Based DSVM with Deadbeat Control

3.1. Classical FS-MPC

The classical three-level FS-MPC uses only 19 voltage vectors as shown in Figure 2, defined by switching states, for prediction, and uses three stages: (1) estimation, (2) prediction, and (3) cost function optimization. An optimal control action is selected by minimizing a predefined cost function. All of the controlled objectives are included in the cost function in terms of errors; the errors are calculated by their respective references. The performance and the required computational burden of the model have been analyzed for the 3L T-type VSI.

To predict the future behavior of the inverter, the continuous-time model of Equation (1) should be approximated by a discrete-time model, using the normal forward Euler approximation with the sampling period T_s, as:

$$dy/dt = (y(k+1) - y(k))/T_s. \tag{4}$$

Thus, the discretized models of current are given as:

$$i_{dq}(k+1) = i_{dq}(k) + (T_s/L)\left(u_{dq}(k) - R \cdot i_{dq}(k) - e_{dq}(k)\right). \tag{5}$$

To predict $i(k+1)$ in Equation (5), $i(k)$, $e(k)$, and $v(k)$ are required. The current $i(k)$ is measured using the hardware sensors on the stationary d–q axis. Assuming that $e(k)$ does not change much during T_s, $e(k)$ can be estimated by shifting Equation (5) one step backward, as

$$e_{dq}(k) \approx e_{dq}(k-1) \tag{6}$$

$$e_{dq}(k) = u_{dq}(k-1) - (L/T_s)\left[(1-(R{\cdot}T_s/L)){\cdot}i_{dq}(k) - i_{dq}(k-1)\right]. \tag{7}$$

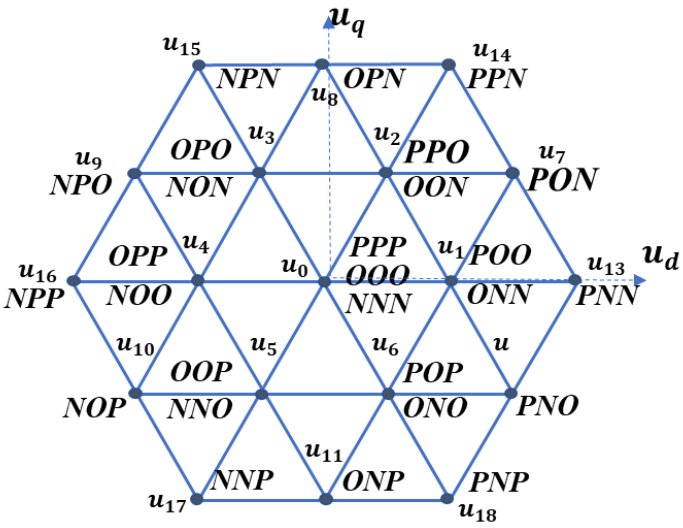


Figure 2. Space vector diagram of conventional finite-set model predictive control (FS-MPC).

As it is evident that there is a one-step delay in the digital control system, the voltage vector at time k will not be applied until time $k+1$. Therefore, to obtain the optimal voltage vector among the 19 voltage vectors, the cost function (*CF*) used to measure the errors between the references and the predictions in the stationary d–q frame was defined, as in Equation (8). To remove the delay, the voltage vector at time $k+2$ should be used in the cost function of Equation (8), instead of $k+1$:

$$CF = \left|i^*_d(k+2) - i_d(k+2)\right| + \left|i^*_q(k+2) - i_q(k+2)\right|. \tag{8}$$

The voltage vector, which yields the minimal *CF*, will be selected as the optimal vector u^{opt} and will be applied to the grid terminal by the inverter during the next sampling time.

3.2. FS-MPC Based on DSVM

The approach that uses FS-MPC based on the DSVM strategy follows the same route for predicting the state variables that is used in the classical FS-MPC approach, as described in the previous subsection, except that the selected voltage vectors are obtained from various virtual voltage vectors for prefix time intervals [20]. These virtual voltage vectors are obtained by subdividing the space vector diagram (SVD) into M equal parts.

For example, Figure 3 shows the virtual voltage vectors where the space vector diagram is subdivided into three equal parts. The overall number of voltage vectors (T) in the space vector diagram is:

$$T(M) = 3{\cdot}M{\cdot}(M+1) + 1. \tag{9}$$

According to Equation (9), the virtual voltage vectors, which are normally much higher, are calculated to obtain the current predictions and cost function. To enforce the actual output current vector to approach the reference current vector in the next step [20], the optimal voltage vector is applied to the inverter using the DSVM strategy during the entire time T_s. However, when taking

into account all of the candidate voltage vectors for the current prediction, the computational burden increases dramatically, and the method becomes unsuitable for actual control systems.

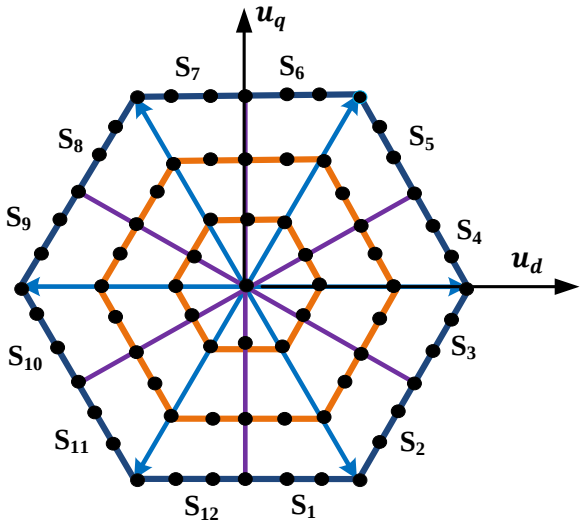


Figure 3. Space vector diagram of conventional model predictive control with discrete space vector modulation (DSVM-MPC).

3.3. Deadbeat Control Strategy

As mentioned earlier, considering all virtual voltage vectors significantly increases the computational burden on the prediction process. Therefore, a control method, namely deadbeat control (DBC), for alleviating the computational burden on the digital signal processor (DSP) is required. In addition, all of the voltage vector values in the stationary d–q frame should be predefined in a lookup table [16]. As a result, more complex lookup tables are required with increasing voltage vectors [16]. Thus, the deadbeat control method is utilized for reducing the computational burden associated with instantaneous computation of candidate voltage vectors.

The virtual voltage vectors in the stationary d–q frame are defined as [20]:

$$u_d(x, y) = (V_{dc}/6{\cdot}M)[(a + 2{\cdot}e){\cdot}x + 3b{\cdot}y] \tag{10}$$

$$u_q(x, y) = (\sqrt{3}{\cdot}V_{dc}/6{\cdot}M)[c{\cdot}x + (d + 2{\cdot}f){\cdot}y]. \tag{11}$$

In Equations (10) and (11), x and y are the coordinates of the different sectors, and the coefficients (a, b, … f) are obtained from Table 1 [20]. Figure 4 schematically shows the voltage vectors for sectors S_4, S_5, and S_6 for M = 3.

Table 1. Coefficients for Each Sector.

	a	*b*	*c*	*d*	*e*	*f*
S_1	1	1	−1	1	0	0
S_2	−1	1	1	1	0	0
S_3	0	0	0	0	1	1
S_4	0	0	0	0	−1	1
S_5	1	−1	1	1	0	0
S_6	−1	−1	−1	1	0	0
S_7	−1	−1	1	−1	0	0
S_8	1	−1	−1	−1	0	0
S_9	0	0	0	0	−1	−1
S_{10}	0	0	0	0	1	−1
S_{11}	−1	1	−1	−1	0	0
S_{12}	1	1	1	−1	0	0

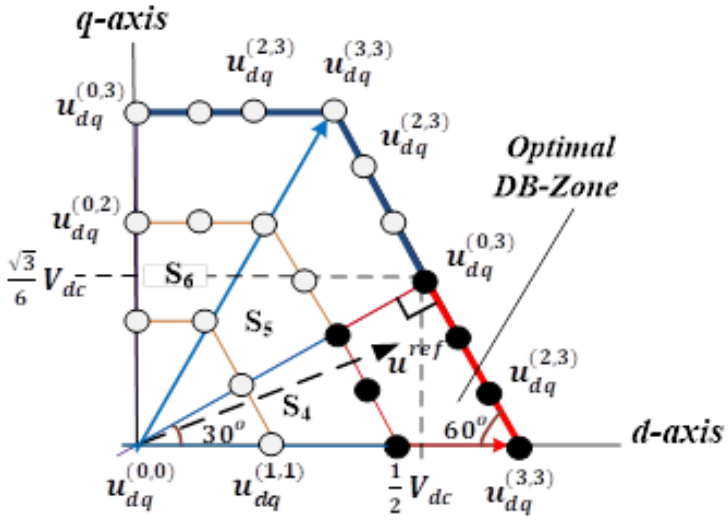


Figure 4. Space vector diagram of conventional DSVM-MPC.

To determine the candidate voltage vectors, the deadbeat method uses the reference inverter voltage vector phase (θ^*) and magnitude ($|u^*|$). Assuming that the control works correctly, it is possible to assume:

$$i(k+2) = i^*(k+2). \tag{12}$$

Under the assumption of Equation (12), it is possible to calculate the reference voltage vector as:

$$u_{dq}^*(k+1) = R{\cdot}i_{dq}^*(k+1) + (T_s/L)\Big(i_{dq}^*(k+2) - i_{dq}(k+1)\Big) + e_{dq}(k+1). \tag{13}$$

Hence, θ^* and u^* can be expressed as:

$$\theta^* = tan^{-1}\Big(u_d^*(k+1)/u_q^*(k+1)\Big) \tag{14}$$

$$\Big|u^*(k+1)\Big| = \sqrt{\Big(u_d^*(k+1)\Big)^2 + \Big(u_q^*(k+1)\Big)^2}. \tag{15}$$

Among the twelve sectors on the space vector diagram, a single sector is selected by θ^*. Since u^{opt} exists in the vicinity of the circle, this method determines two concentric hexagonal diagrams (SVD_1 and SVD_2), as given below:

$$SVD_1 = |u^*| \cdot (M/V_{dc}) \cdot (3/2) \tag{16}$$

$$SVD_2 = [|u^*| \cdot (M/V_{dc}) \cdot (3/2)] + 1. \tag{17}$$

Hence, only the voltage vectors within SVD_1 and SVD_2 are taken into account during the calculation and prediction processes. In this way, the candidate voltage vectors are restricted, which significantly reduces the computational burden on the DSP. Finally, the optimal voltage vector u^{opt} is selected at $k + 2$, using the cost function in Equation (8), before it is sent in the next sampling instant to the space vector modulator. To simplify our discussion in the next section, deadbeat DSVM-MPC was used to identify the FS-MPC with DSVM and deadbeat control.

4. Deadbeat DSVM-MPC with Proposed Neural Point Balancing Method

In this paper, the deadbeat DSVM-MPC used virtual voltage vectors obtained using the DSVM strategy, and their values were calculated instantly for the current prediction [20]. Although good performance can be obtained with deadbeat DSVM-MPC, the 3L T-type VSI topology can lead to an unbalanced neutral-point voltage, which increases the voltage stress on the switching device. It also

increases the total harmonic distortion (THD) of the output current, because a low-order harmonic will appear in the output voltage. A large deviation of the DC link capacitance voltage is caused by the inconsistency in switching or imbalance of DC capacitors, owing to the manufacturing tolerance [22].

It is worth mentioning that there are various modulation strategies to synthesize output voltages, which can be categorized into two common types: continuous-based modulation (CPWM), such as sine pulse-width modulation (SPWM), and discontinuous-based modulation, namely discontinuous pulse-width modulation (DPWM). To optimize the performance of the 3L T-type VSI system, the voltages of the in-series connected DC link capacitors should be balanced. Unlike our previous work [20], wherein the problem of balancing the capacitor voltages was treated using a separate cost function to modify the offset voltage in SPWM (increasing the computational burden), the proposed deadbeat DSVM-MPC implements a modification in DPWM using a hysteresis capacitance voltage control. The main advantage of this proposed method is that it is straightforward and easily implemented, without additional hardware or extensive computation. Furthermore, it is known that by using DPWM, the switching losses are reduced, and better harmonic characteristics can be obtained for high modulation indices, compared with inverters that use continuous pulse-width modulation [23–26]. Although there are several different DPWM methods, conventional 60° DPWM is most commonly used for systems with the unity power factor. The idea behind the 60° DPWM method is schematically shown in Figure 5. Therefore, the pole reference voltages to be applied to the VSI are described by:

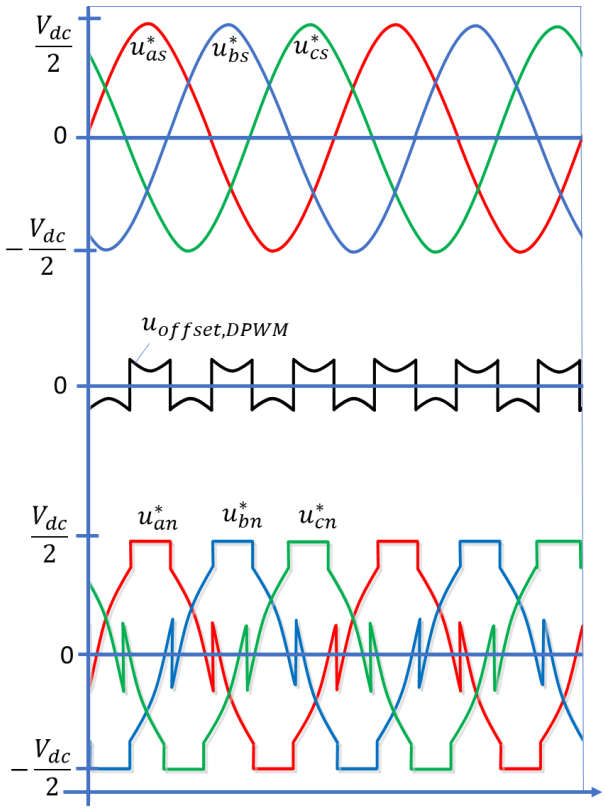


Figure 5. Reference voltage, offset voltage, and pole reference voltages of the conventional 60° discontinuous pulse-width modulation (DPWM).

$$\begin{aligned} u^*_{an} &= u^*_{as} + u_{offset,DPWM} \\ u^*_{bn} &= u^*_{bs} + u_{offset,DPWM} \\ u^*_{cn} &= u^*_{cs} + u_{offset,DPWM} \end{aligned} \tag{18}$$

where u^*_{an}, u^*_{bn}, and u^*_{cn} are the pole reference voltages to be applied to the VSI, whereas u^*_{as}, u^*_{bs}, and u^*_{cs} are the optimal reference voltages by deadbeat DSVM-MPC of each phase, respectively. The voltage $u_{offset,DPWM}$ is the offset voltage used in the DPWM, which is calculated as follows:

$$\begin{cases} u_{offset,DPWM} = \frac{V_{dc}}{2} - u_{\max}, & (u_{\max} + u_{\min} > 0) \\ u_{offset,DPWM} = -\frac{V_{dc}}{2} - u_{\min}, & (u_{\max} + u_{\min} < 0) \end{cases} \quad (19)$$

where u_{max} and u_{min} are, respectively, the maximum and the minimum values among the phase reference voltages.

Figure 6a depicts the imbalance of the DC link capacitor voltage for the 3L T-type VSI. Note that when the switch of the either phase is locked in the P state, the top DC link capacitor voltage V^{top} is decreased and the bottom DC link capacitor voltage V^{bottom} is increased. Conversely, if the switch of the same switch is locked in the N state, the top and the bottom DC link capacitor voltages are increased and decreased, respectively. Thus, clamping plays a major role in decreasing or increasing the top and bottom capacitance voltages. Figure 6b shows the proposed DPWM method using the hysteresis capacitance voltage band (ΔHB_{cv}). The proposed neutral-point voltage balancing method uses a compensated voltage offset ($u_{offset,cv}$) depending on the top and bottom capacitor voltages in the linear modulation range. The $u_{offset,cv}$ has an opposite influence from $u_{offset,DPWM}$ on changing the direction of the top and bottom voltages, which is given as:

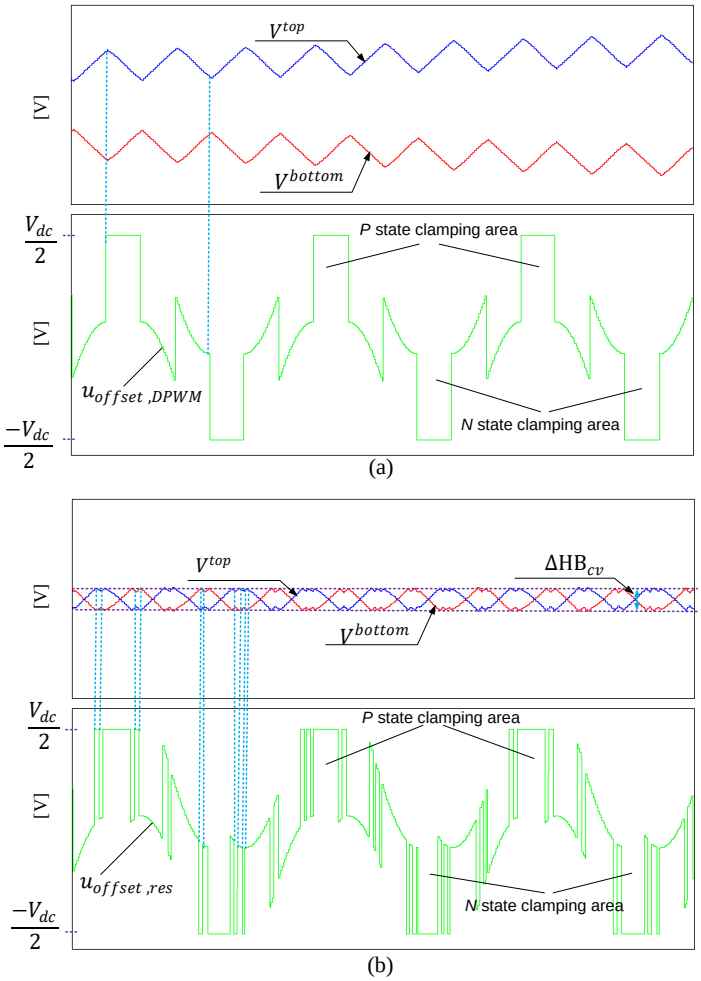


Figure 6. Behavior of top and bottom capacitance voltages with respect to: (**a**) conventional DPWM; (**b**) proposed DPWM.

$$\begin{cases} u_{offset,\mathrm{cv}} = \frac{V_{dc}}{2} - u_{\max}, & (V^{top} > V^{bottom}) \\ u_{offset,\mathrm{cv}} = -\frac{V_{dc}}{2} - u_{\min}, & (V^{top} < V^{bottom}) \end{cases}. \quad (20)$$

The proposed method seeks to maintain the advantage of diminishing the stress on transistors and minimizing the power loss, while simultaneously achieving a balanced DC link capacitance voltage with a stable and acceptable capacitance voltage error $|E_{cv}|$, which is defined as

$$|E_{cv}| = \left|V^{top} - V^{bottom}\right|. \quad (21)$$

The capacitance voltage error $|E_{cv}|$ is inevitable; thus, it should be limited to an acceptable error band ΔHB_{cv}, to avoid large deviations of the DC link capacitance voltage and high switching. The limited error band is defined as $|E_{limit}|$. The resultant voltage offset ($u_{offset,res}$) can then be designed depending on the following condition:

$$\begin{cases} u_{offset,res} = u_{offset,DPWM} + u_{offset,cv}, & (|E_{cv}| > |E_{\mathrm{lim}it}|) \\ u_{offset,res} = u_{offset,DPWM}, & (|E_{cv}| \le |E_{\mathrm{lim}it}|) \end{cases}. \quad (22)$$

According to Equation (22), if the capacitance voltage error $|E_{cv}|$ exceeds the limited error band, the $u_{offset,cv}$ will be injected into the $u_{offset,DPWM}$ to have an opposite effect on the clamped voltage, otherwise, the $u_{offset,DPWM}$ will continue with its normal operation.

The effect of the resultant voltage offset $u_{offset,res}$ on one of the pole reference voltages to be applied to the VSI is seen in Figure 6b. Note that the clamping areas are almost similar to the conventional DPWM; at the same time, the error of the DC link capacitance voltage is stable. In addition, there is a short clamping area injected by the $u_{offset,cv}$ to maintain the capacitance error range. It is noteworthy that the switching frequency of $u_{offset,res}$ and the non-switching area depend mainly on the setting of $|E_{\mathrm{limit}}|$; increasing the limited error band will result in a lower switching of $u_{offset,res}$ and will deteriorate the quality of the current, whereas reducing the limited error band will cause undesirable switching frequency of $u_{offset,res}$ and a small clamping area. Thus, it is recommended that the tradeoff error band limit for achieving desirable current control performance be determined.

5. Simulation Results

Simulations using the PSIM software tool were conducted to validate the proposed method. The system configuration was similar to that shown in Figure 1. The DC link voltage (V_{dc}) was 300 V, and was distributed equally between the top capacitance voltage (V^{top}) and the bottom capacitance voltage (V^{bottom}). The total DC link capacitance was 2200 µF and the switching frequency was 10 kHz. The value of $|E_{limit}|$ was set empirically at 2.6 V. The simulation parameters are given in Table 2. After synthesizing the reference voltage vectors with the minimized cost function using the deadbeat DSVM-MPC system, the reference voltage vector was applied to the grid-connected 3L T-type VSI.

Table 2. System parameters.

Variable	Description	Value	Unit
P_r	Rated power	2.1	kW
V_{dc}	DC link voltage	300	V
f	Fundamental frequency	60	Hz
e	Grid voltage	100	Vrms
T_s	Sampling time	100	μs
R	Load resistance	1	ohm
L	Filter inductance	2	mH
M	Modulation index	0.954	

Figure 7 shows the simulation results for the optimal voltage vectors in the *d*–*q* frame for the deadbeat DSVM-MPC, which followed the reference current using only four candidate voltage vectors [20]. Figure 8 shows the simulation results for the deadbeat DSVM-MPC using the balancing method in Reference [20] and using the proposed DPWM method. It can be seen that the current waveforms became highly distorted before implementation of the neutral-point balancing of capacitance voltage, owing to large voltage deviations. Obviously, the total harmonic distortion (THD was is significantly reduced using either one of the balancing methods. Nevertheless, the proposed balancing method performed better in terms of THD, as shown in Figure 8b.

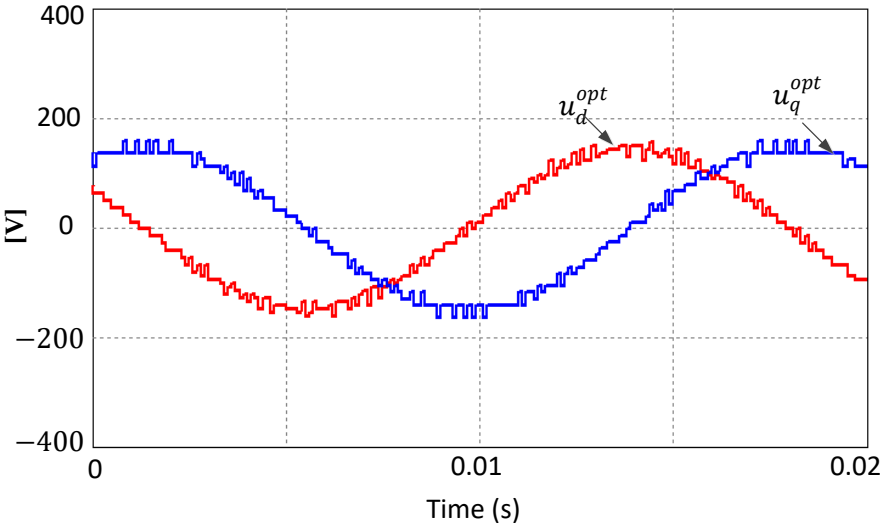
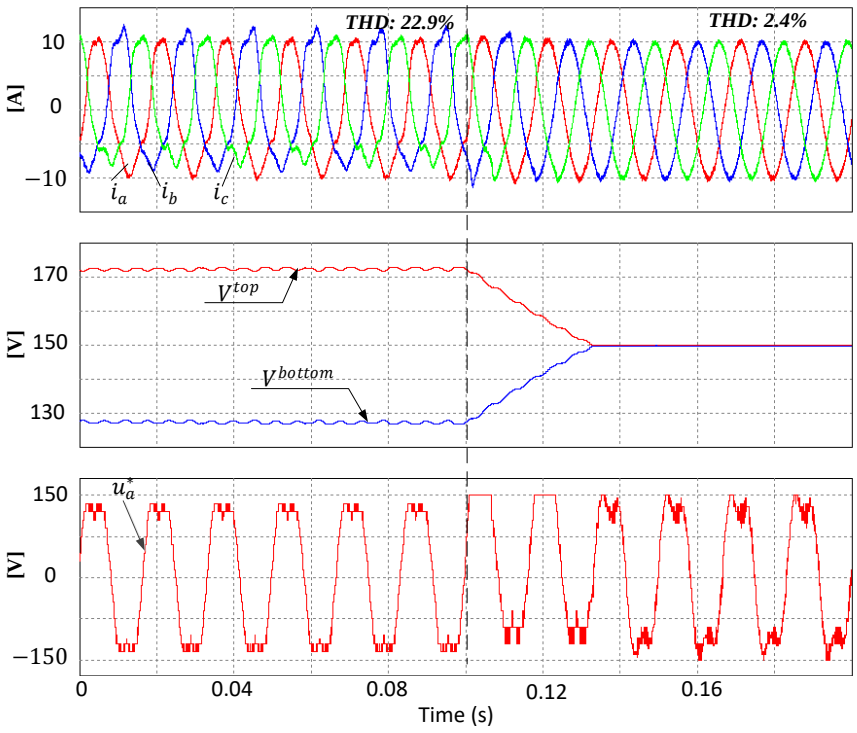
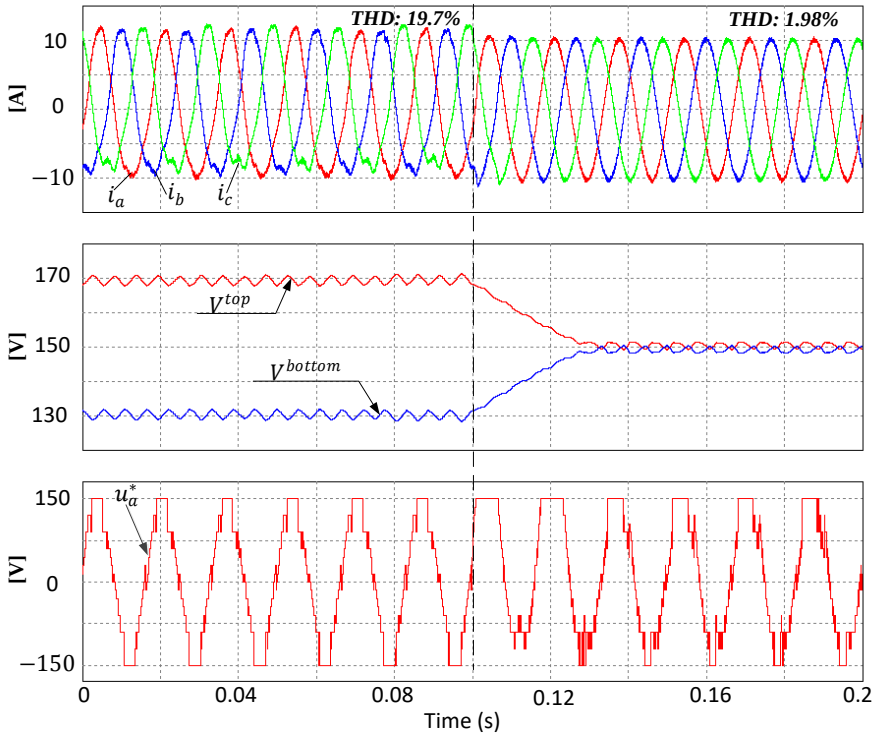


Figure 7. Simulation results of the optimal voltage vectors for the deadbeat FS-MPC with DSVM.



(**a**)

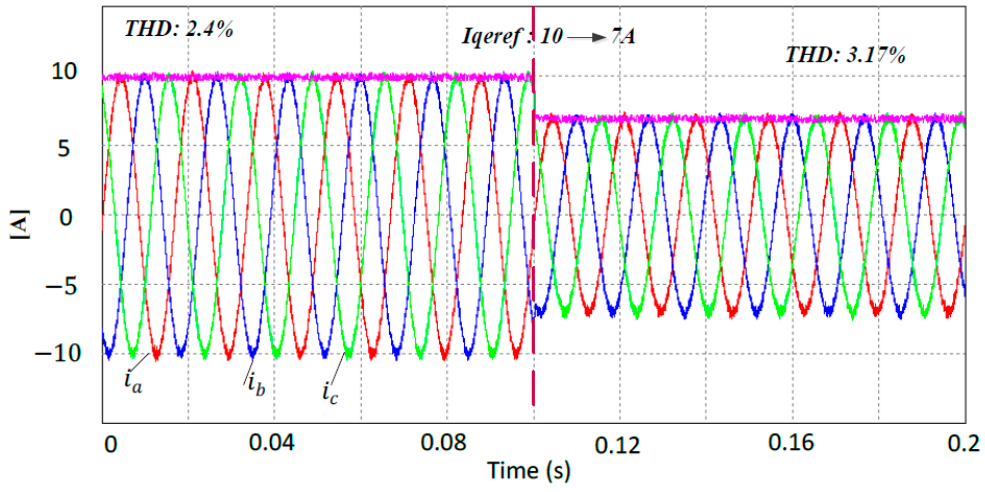
Figure 8. *Cont.*



(**b**)

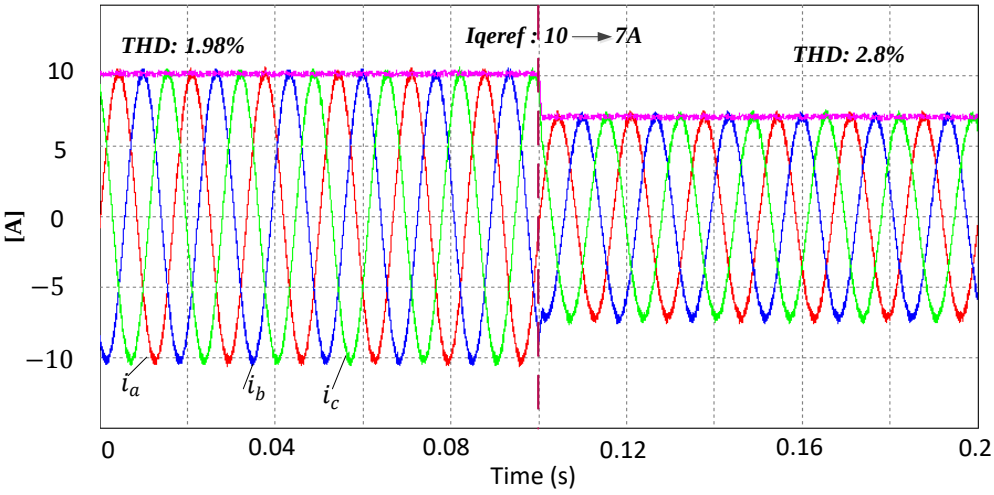
Figure 8. Simulation results of capacitance voltage balancing for deadbeat DSVM-MPC. (**a**) Conventional balancing method [20]. (**b**) Proposed balancing method.

Figure 9 shows the simulation results for dynamic response for the deadbeat DSVM-MPC system, using the two balancing methods. As can be seen, both methods exhibited a fast dynamic current response, because the MPC method was used. On the other hand, the proposed method exhibited smaller THD compared with the method in Reference [20].



(**a**)

Figure 9. *Cont.*



(**b**)

Figure 9. Simulation results of current dynamic response for deadbeat DSVM-MPC with (**a**) conventional balancing method [20] and (**b**) proposed balancing method.

The robustness of the proposed method was shown by varying the impedances of the grid connected system including the inductance (L) and resistance (R) (Figure 10). The values of resistance and inductance were increased (at t = 0.1 s) by 100% and 50% of the nominal values, respectively. It can be obviously seen that there was a negligible increase in the THD. Therefore, it was confirmed that the proposed balancing method in FS-MPC with DSVM and DBC is robust to the variations of impedances.

Figure 11a,b depicts the frequency spectrum of the phase voltage for the conventional method and proposed method, respectively. Apparently, the first harmonic component (i.e., switching frequency (f_{sw})) was greatly reduced with the proposed algorithm, compared to the conventional method. This indicates the proposed method has less switching frequency owing to the use of the DPWM modulator, as mentioned previously.

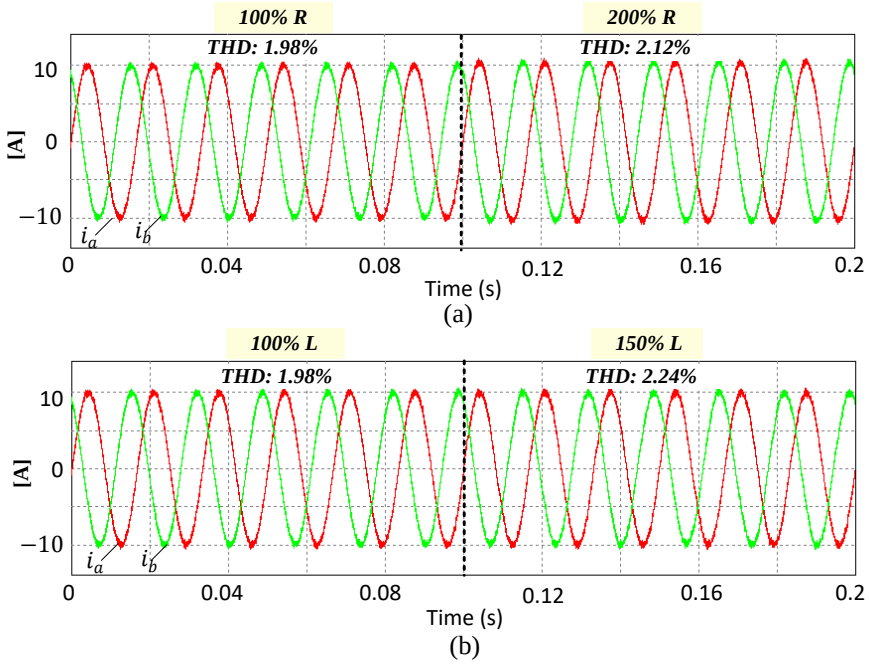


Figure 10. Simulation results of grid impedance variation for the proposed method.

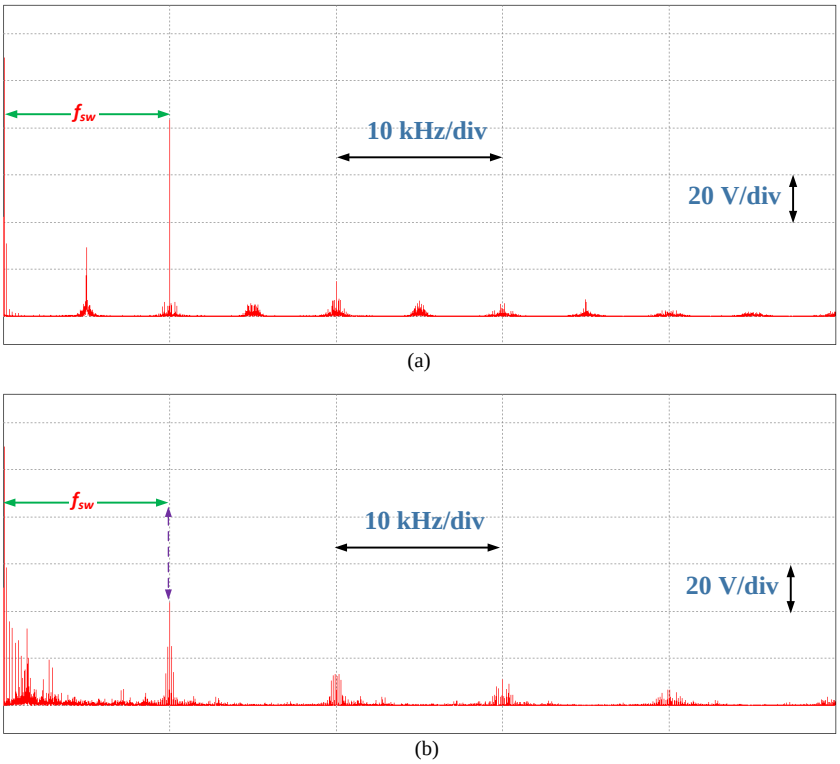


Figure 11. Simulation results of frequency spectrum for the phase voltage with (**a**) conventional balancing method [20] and (**b**) proposed balancing method.

6. Experimental Results

The proposed control system was further validated on a prototype grid-connected VSI that was used in a laboratory setup, as shown in Figure 12. The experimental parameters of the prototype were similar to those that were assumed in the simulation study, as shown in Table 2. The control system was configured using a DSP named TMS320F28377. In addition, 10-FZ12NMA080SH01-M260F-3 from Vincotech was employed to configure the three-level inverter system. To ensure a fair comparison of these methods, the experimental conditions were the same as those that were assumed in the simulation study. Thus, the limited error band $|E_{limit}|$ was also set at 2.6 V, which was similar to that in the simulation. To verify the effectiveness of the proposed method in the deadbeat DSVM-MPC, it was compared against the conventional neutral-point balancing method [20].

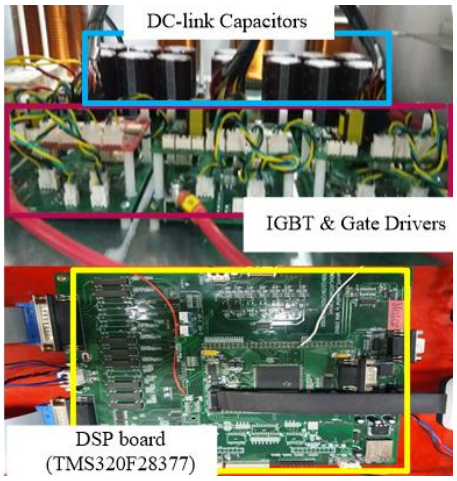


Figure 12. Experimental setup.

Figure 13 shows the experimental results for the grid current of the deadbeat DSVM-MPC, for both balancing methods. Similarly to the simulation results, it was observed that the proposed balancing method demonstrated a good capability of balancing the deviation of the top and bottom capacitance voltages. As can be seen, before applying either of the balancing methods, the difference between the top and bottom capacitor voltages was very high, and the output current became distorted owing to the neutral-point voltage imbalance. However, when the neutral-point voltage was balanced, the distortion of the output current disappeared. Figure 14 shows the experimental results for the dynamic current performance from 10 A to 7 A for the deadbeat DSVM-MPC system, using both the conventional and the proposed balancing methods. As can be seen, the settling time was very short because the MPC method was used. However, the proposed balancing method exhibited lower THD by around 4.9% before and after the current reference change, when compared with the conventional neutral-point balancing method [20].

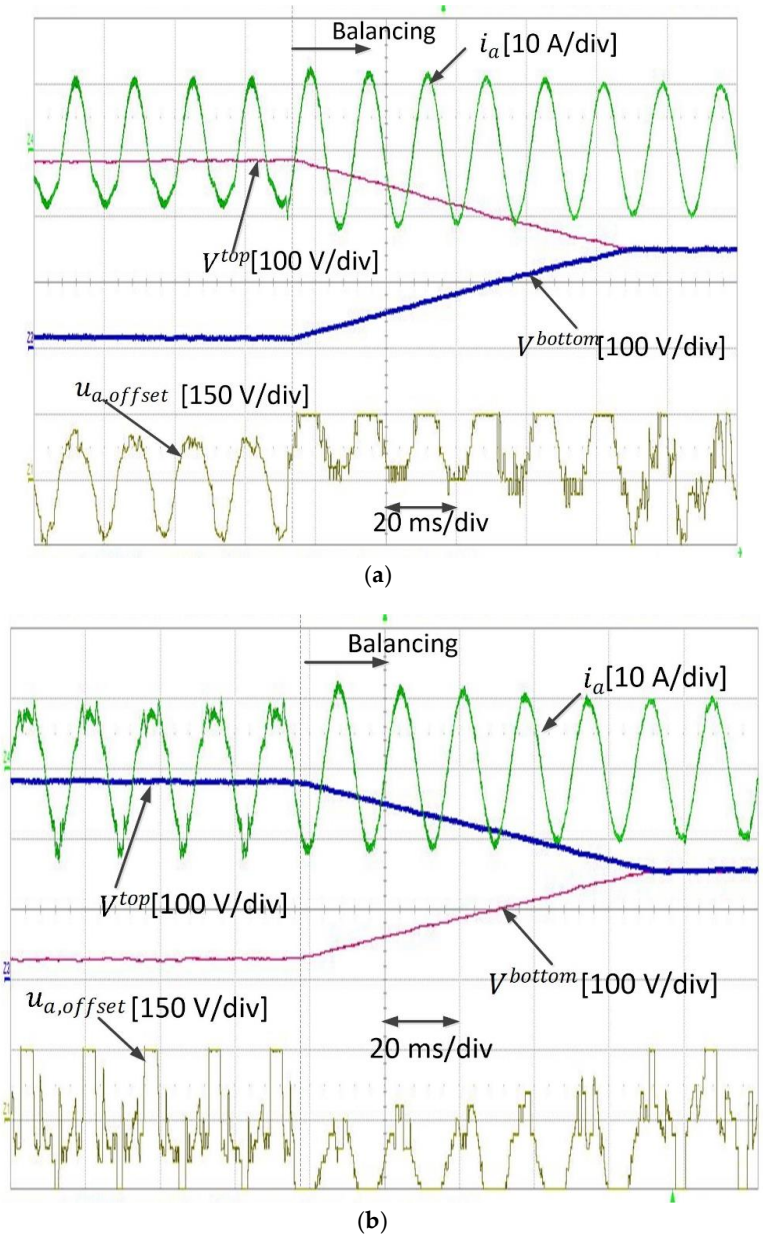


Figure 13. Experimental results of capacitance voltage balancing for deadbeat DSVM-MPC. (**a**) Conventional balancing method [20]. (**b**) Proposed balancing method.

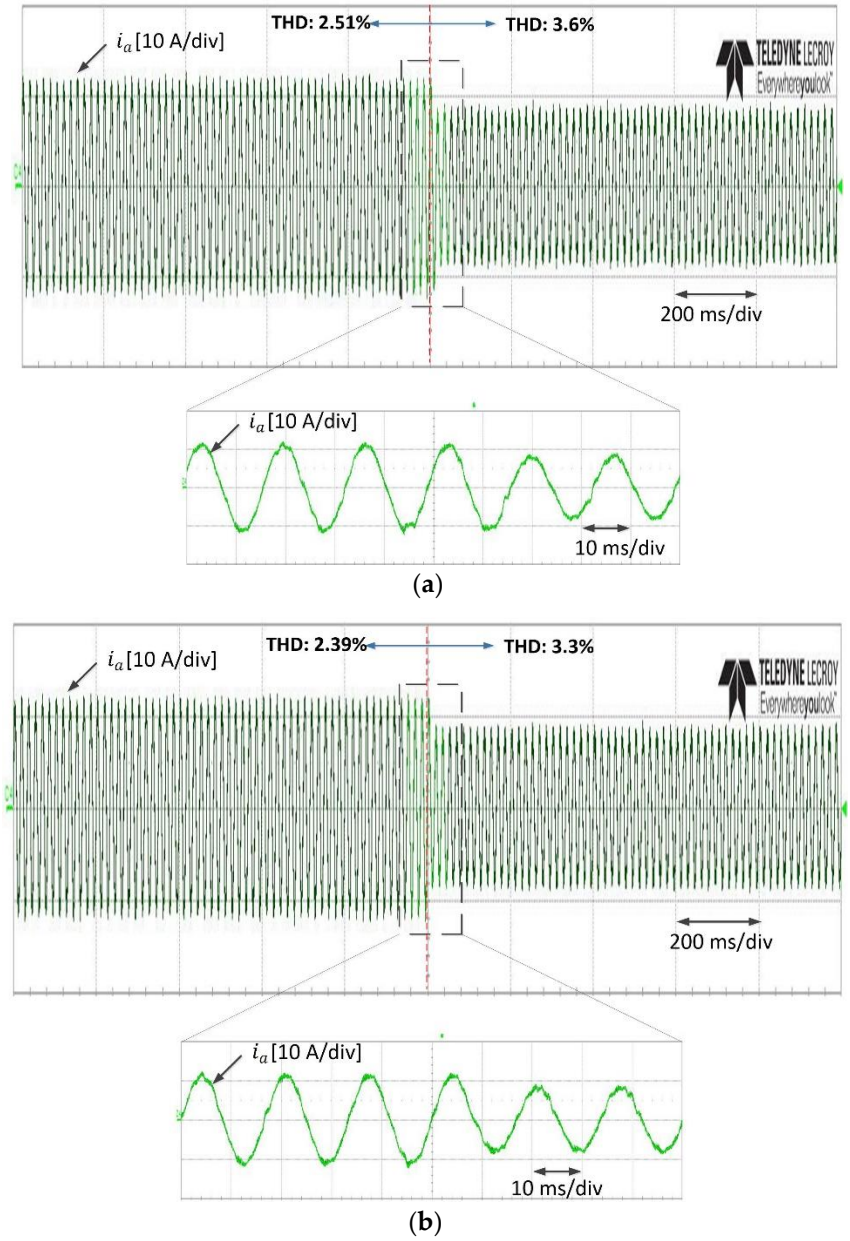
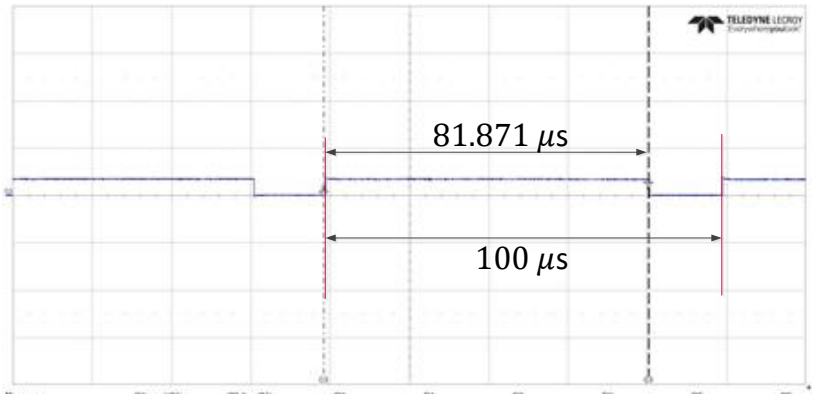
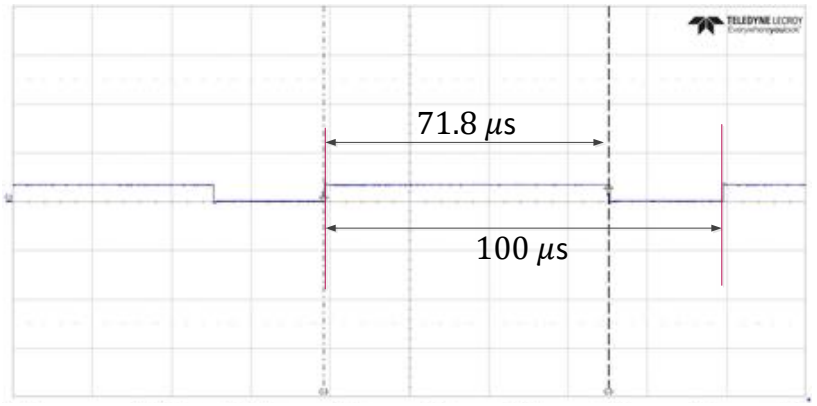


Figure 14. Experimental results of current dynamic response for deadbeat DSVM-MPC for the (**a**) conventional balancing method [20] and (**b**) proposed balancing method.

Figure 15 shows the comparison of the hardware computation time of the deadbeat DSVM-MPC system, without weighting factors, for the control method in Reference [20] and the proposed method. As can be seen, the computation time required by the proposed deadbeat DSVM-MPC method was reduced by 12.30% when compared to the method from Reference [20]. This indicates the simplicity of the proposed algorithm.



(a)



(b)

Figure 15. The hardware execution time. (**a**) Deadbeat FS-MPC with extra cost function [20]. (**b**) Proposed method.

7. Conclusions

This paper proposed a deadbeat DSVM-MPC with a simplified neutral-point balancing method for enhancement of the output current quality in three-level grid-connected voltage source inverters. The DSVM-MPC method produces various virtual voltage vectors by subdividing the space vector diagram, and selects the optimal voltage vector that minimizes the error with respect to the reference current. To alleviate the computational burden, a deadbeat control was applied to restrict the optimal region of candidate voltage vectors. In addition, this work introduced simplified neutral-point capacitance voltage balancing using a modified DPWM method without a need for an extra cost function, thus reducing the total computation time. The reduction in the computation time may be advantageous for incorporating additional estimation or protection algorithms. The modified DPWM method had a higher efficiency than the conventional CPWM method, owing to the reduced number of switching operations.

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