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A Family of Y-Impedance-Network Half-Bridge Converters with Additional Voltage Adjustment Function

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Abstract: Half-bridge converters have been widely used in multiple medium power level applications because of the advantages of having less switches and being easy to control. However, their inherent structure leads to low output amplitude and shoot-through problems. In this study, we propose a family of novel half-bridge converters implementing a Y-impedance-network with additional buck-boost voltage adjustment function with the aim of resolving these issues. In order to verify the effectiveness of the proposed topologies, simulations and experiments were conducted, the results which well validate the feasibility of the proposed converters.

Keywords: half-bridge-inverter; step-up cells; Y-impedance-network; additional voltage adjustment

1. Introduction

In terms of reducing the loss of transmission, building integrated photovoltaic (BIPV) systems reduce costs and increase efficiency as compared to a centralized PV plant [1], however they require high reliability, low cost, and high voltage gain. Traditional inverters are buck-type converters which can no longer satisfy BIPV requirements. Additionally, they are vulnerable to electromagnetic interference because their bridge, which contains series switches, can easily short-circuit with strong current of shoot-through. In order to increase the voltage gain, a traditional solution is to cascade a voltage pumping structure with only a few passive elements [2,3]. However, it results in low efficiency. Owing to their high efficiency, single-state inverters have been widely used which usually combine a transformer or passive elements into traditional inverters to achieve a higher voltage gain [2,4,5]. However, adding a transformer results in a bulky volume and low efficiency. Moreover, this solution has a narrow window of voltage adjustment since the transformer only has a fixed voltage ratio. Furthermore, they work under the threat of a shoot-through which leads to the need for controlling strategies. To provide an effective method to solve the shoot-through problem and increase output voltage systematically, the authors in [6] proposed an *LC* network named a Z-source inverter (ZSI), which performs a boost function and prevents components being destroyed when working during a shoot-through. However, applying a Z-source into a half-bridge inverter leads to the problem of an imbalance at the midpoint voltage of the input capacitors. Targeting this issue, authors in [7] proposed a novel Z-source half-bridge converter which also realizes buck-boost function. However, with a fixed structure, ZSI or quasi-Z-source inverter (qZSI) cannot realize a high enough voltage gain, which is a requirement in BIPV. Magnetic coupling is an effective method to improve the performance and efficiency. Many magnetically coupled impedance networks have been explored, such as T-source [8,9], Trans-Z-source [10], Γ-Z-source [11], flipped-Γ-Z-source [12], and A-source [13]. Their different winding placements lead to different advantages and applications. Combining their

advantages, a Y-source impedance network (also known as a Y-impedance-network) is proposed which has higher voltage gain and a smaller size with less passive components [14]. However, there is a severe problem: the existence of pulsed input currents. Addressing this issue, quasi-Y-source inverters with an additional inductor are proposed in [15–17], and they also have additional voltage gain. However, they can only vary voltage gain by adjusting the turns ratio and duty cycle which cannot meet special industrial requirements. Under the premise of solving the pulsed input currents problem, an improved quasi-Y-source converter was proposed with higher voltage gain [18]. However, the additional switch leads to difficultly regarding control.

In order to increase voltage gain and provide more degrees of adjustment to vary the voltage, the additional inductor in [15] is replaced by a general step-up cell. Combining the advantages of half-bridge converters and a Y-impedance network, we propose a novel family of high step-up Y-impedance-network half-bridge converters, coupled with a general step-up cell for additional voltage adjustment to solve the above problems.

The rest of this paper is organized as follows. Detailed descriptions and analyses of the proposed converters are given in Section 2. In Section 3, the proposed converter and conventional Z-source half-bridge converter are compared to demonstrate the unique features of the proposed solution. In Sections 4 and 5, the simulation and experimental studies are presented. Finally, a conclusion is drawn in Section 6.

2. Operating Principle And Analysis

The structure of the proposed topologies are depicted in Figure 1 and the step-up cells are illustrated in Figure 2, in which the step-up cell is a general cell, which can be a single inductor, a switched inductor, a quasi Z-source network, or a switched-coupled inductor [19]. The cell endows the proposed converters with an additional voltage adjustment function.

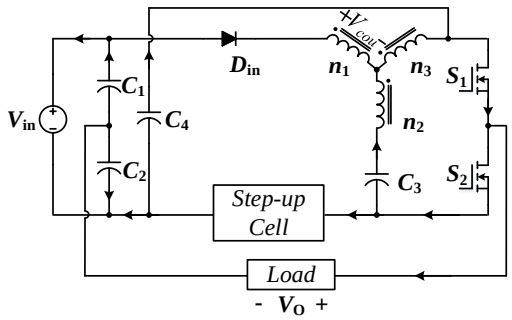

Figure 1. Proposed topology.

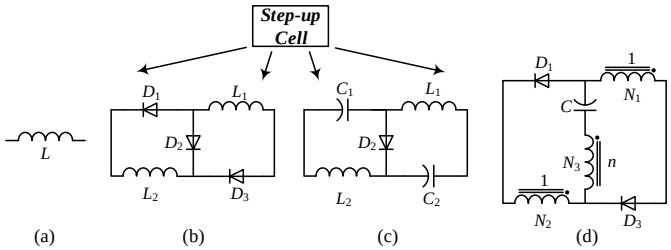

Figure 2. A step-up cell: (**a**) a single inductor; (**b**) switched inductor; (**c**) quasi Z-source network; (**d**) switched-coupled-inductor.

Since the operating principles of the proposed converters are the same as the conventional ones with the condition of $D_1 + D_2 \leq 1$, but not $D_1 + D_2 > 1$, the latter is analyzed in this study. Furthermore, different step-up cells perform the same boost function, so a switched inductor Y-impedance-network half-bridge converter is analyzed as a typical example. In detail,

a Y-impedance-network and a switched inductor are integrated into a conventional half-bridge inverter to form a new topology with three operating modes, as shown in Figure 3.

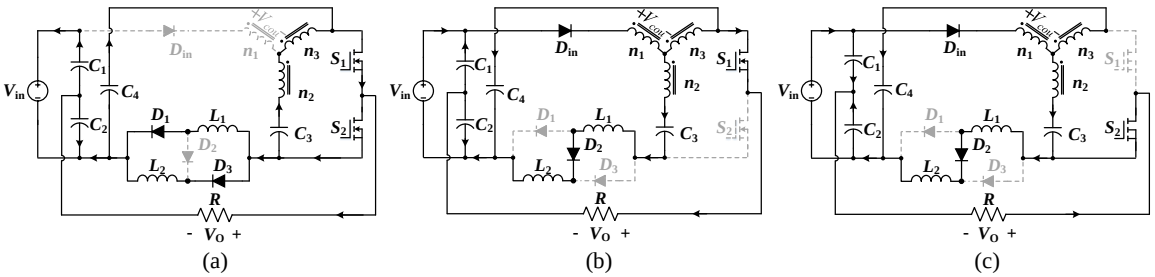

Figure 3. Equivalent circuits in (**a**) Mode 1: S_1 and S_2 are on; (**b**) Mode 2: S_1 is on and S_2 is off; (**c**) Mode 3: S_1 is off and S_2 is on.

Denote t_0 as the beginning of one period, t_1 as the turning point from Mode 1 to Mode 2, t_2 as the time from Mode 2 to Mode 3, and $t_3 = T_S$ as the end of the period. The operating process in one period is analyzed in detail in the following, and the output voltage v_o is deduced in each mode.

(1) Mode 1: $t \in [t_0, t_1]$.

As shown in Figure 3a, the proposed converter works in a shoot-through state. Diodes D_{in} and D_2 are reverse biased simultaneously, capacitors C_3 discharges energy to the coupled inductor, and capacitors C_4 and the input voltage source discharge energy to the switched inductor cell (L_1, L_2) and the load R. Voltages across inductors L_1, L_2, coupled inductor n_1, and output voltage can be deduced as

$$v_{L_1} = v_{L_2} = v_{C_4}, \tag{1}$$

$$v_{n_1} = \frac{n_{12}n_{13}}{n_{12} - n_{13}} v_{C_3}, \tag{2}$$

and

$$v_o = v_{L_1} - v_{C_2} = v_{C_4} - v_{C_2}, \tag{3}$$

where $n_{12} = n_1/n_2$ and $n_{13} = n_1/n_3$ are turns ratios of the three-winding coupled inductor.

(2) Mode 2: $t \in [t_1, t_2]$.

As shown in Figure 3b, switch S_1 is on and S_2 is off. Diodes D_1 and D_3 are reverse biased while D_{in} and D_2 conduct at time t_1. The input power V_{in} begins to transfer energy to the Y-impedance-network and recharge C_3, and the energy of L_1 and L_2 is delivered to C_2, C_4, and the load. The output voltage is the same as (3). Furthermore, the voltages across inductors L_1, L_2, and the coupled inductor n_1 are deduced as

$$v_{L_1} = v_{L_2} = \frac{V_{in} - v_{C_3} - \frac{1+n_{12}}{n_{12}} v_{n_1}}{2}, \tag{4}$$

and

$$v_{n_1} = \frac{1 + n_{13}}{n_{13}} (V_{in} - v_{C_4}). \tag{5}$$

(3) Mode 3: $t \in [t_2, t_3]$.

As shown in Figure 3c, switch S_1 is off and S_2 is on. Similar to Mode 2, D_1 and D_3 are reverse biased while D_{in} and D_2 conduct at time t_2. The voltage of inductors L_1, L_2, and the coupled inductor n_1 are same as (4) and (5), respectively. The energy that capacitor C_2 and the switched inductor cell (L_1, L_2) release to the resistive load and output voltage can be deduced as

$$v_o = 2v_{L_1} - v_{C_2}. \tag{6}$$

In terms of voltage-second property in $L_1(L_2)$ and n_1, one can obtain

$$\int_0^{T_S} v_{L_1} dt = 0 \tag{7}$$

and

$$\int_0^{T_S} v_{n_1} dt = 0. \tag{8}$$

By substitutig (1) and (4) into (7), we can deduce that

$$(D_1 + D_2 - 1)T_S \cdot V_{C_4} + (2 - D_1 - D_2)T_S \cdot (\frac{V_{\text{in}} - V_{C_3} - \frac{1+n_{12}}{n_{12}} v_{n_1}}{2}) = 0, \tag{9}$$

where D_1 and D_2 are duty cycles of switches S_1 and S_2, respectively.

Substitute (2) and (5) into (8), and we can deduce that

$$(D_1 + D_2 - 1)T_S \cdot \frac{n_{12}n_{13}}{n_{12} - n_{13}} \cdot V_{C_3} + (2 - D_1 - D_2)T_S \cdot \frac{n_{13}}{1 + n_{13}} \cdot (V_{\text{in}} - V_{C_4}) = 0. \tag{10}$$

One can obtain the voltages of C_3 and C_4, i.e., V_{C_3} and V_{C_4}, via the solution of (9) and (10). Similarly, in terms of ampere second property in capacitor C_2, one can obtain

$$\int_0^{T_S} i_{C_2} dt = 0, \tag{11}$$

where i_{C_2} is the current flowing through C_2.

Denote the errors of v_{C_1} and v_{C_2} as Δv_{C_1} and Δv_{C_2}, respectively. As shown in Figure 3, we can obtain that $v_{C_1} + v_{C_2} = V_{\text{in}}$, $\Delta v_{C_1} = -\Delta v_{C_2}$ and $i_{\text{o}} = i_{C_1} - i_{C_2}$. Therefore, it can be deduced that $i_{C_1} = -i_{C_2} = i_{\text{o}}/2$ on the basis of $i = Cdu/dt$, and (11) can be derived as

$$\frac{(V_{C_4} - V_{C_2})}{2R_L} D_1 T_S + \frac{(V_{\text{in}} - V_{C_2} - V_{C_3} - \frac{n_{23}(1+n_{12})}{1+n_{13}}(V_{\text{in}} - V_{C_4}))}{2R} (1 - D_1) \cdot T_S = 0, \tag{12}$$

where $n_{23} = n_2/n_3$ and R is the resistive load.

Thus, the output voltage V_{o} can be deduced as

$$V_{\text{o}} = \begin{cases} \dfrac{V_{\text{in}}(1 - D_1)(D_1 + D_2)}{2 + (K-1)(D_1 + D_2) - K(D_1 + D_2)^2} & , \text{ when } S_1 \text{ is on }, \\ \dfrac{-V_{\text{in}} D_1 (D_1 + D_2)}{2 + (K-1)(D_1 + D_2) - K(D_1 + D_2)^2} & , \text{ when } S_1 \text{ is off and } S_2 \text{ is on }, \end{cases} \tag{13}$$

where $K = (1 + n_{13})/(1 - n_{23}) = (n_1 + n_3)/(n_3 - n_2)$.

According to (13), it is noted that positive output voltage is equal to negative only if $D_1 = 0.5$. By adjusting the duty ratio of the switches and the winding ratio of the coupled inductors, we can obtain asymmetric and symmetric voltages, and positive and negative peak output voltages. When $v_{\text{o}}/V_d < 1$, the proposed converter performs as a buck converter; when $v_{\text{o}}/V_d > 1$, it functions as a boost converter. Therefore, it acts as a buck-boost converter.

In the same way, the output voltages of the inductor Y-impedance-network, quasi-Z-source, and switched-coupled-inductor Y-impedance-network are summarized in Table 1, in which $D_1 = 0.5$ and $D = D_1 + D_2$.

The key waveforms of the proposed converter are depicted in Figure 4, where Q_{S_1} and Q_{S_2} stand for the driving voltages of switches S_1 and S_2, respectively; $i_{D_{\text{in}}}$, i_{D_1}, and i_{D_2} are the currents across diodes D_{in}, D_1, and D_2, respectively; i_{L_1} and i_{L_2} are the currents across inductors L_1 and L_2, respectively; v_{C_1} and v_{C_2} are the voltages of capacitors C_1, C_2, respectively; and v_{o} is the output voltage.

As shown in Figure 4, it is obvious that the output voltage of the proposed converter exceeds the limited output voltages of the traditional half-bridge converter which are $V_{in}/2$ and $-V_{in}/2$.

Table 1. Output voltage and voltage gain of the proposed converters with different step-up cell.

Converters	V_{o+}	V_{o-}	Voltage Gain G
Inductor Y-impedance-network	$\frac{V_{in}(1-D_1)}{2+K-(1+K)(D_1+D_2)}$	$\frac{-V_{in}D_1}{2+K-(1+K)(D_1+D_2)}$	$\frac{1}{2(2+K-(1+K)D)}$
Switched inductor Y-impedance-network	$\frac{V_{in}(1-D_1)(D_1+D_2)}{2+(K-1)(D_1+D_2)-K(D_1+D_2)^2}$	$\frac{-V_{in}D_1(D_1+D_2)}{2+(K-1)(D_1+D_2)-K(D_1+D_2)^2}$	$\frac{D}{2(2+(K-1)D-KD^2)}$
Quasi Z-source Y-impedance-network	$\frac{V_{in}(1-D_1)}{3+K-(K+2)(D_1+D_2)}$	$\frac{-V_{in}D_1}{3+K-(K+2)(D_1+D_2)}$	$\frac{1}{3+K-(K+2)D}$
Switched-coupled-inductor Y-impedance-network	$\frac{V_{in}(1-D_1)}{2+(n+2)K-(2K+nK+1)(D_1+D_2)}$	$\frac{-V_{in}D_1}{2+(n+2)K-(2K+nK+1)(D_1+D_2)}$	$\frac{1}{2(2+(n+2)K-(2K+nK+1)D)}$

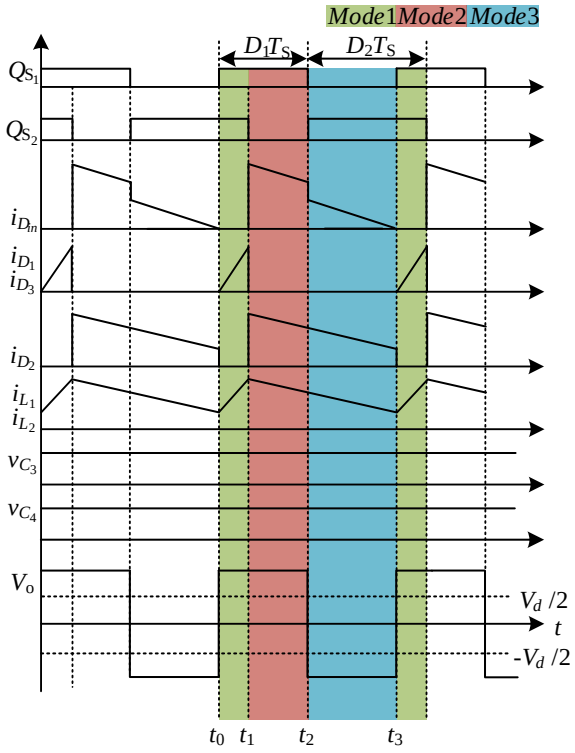

Figure 4. Key waveforms of the switched inductor Y-impedance-network half-bridge converter.

3. Voltage Gain Analysis

In order to demonstrate the characteristics of the proposed converter, a performance comparison of the conventional Z-source half-bridge converter and the proposed converter is presented in this section.

The authors in [7] proposed a topology that implements a Z-source impedance network into a half-bridge inverter. The Z-source half-bridge converter not only solved the conventional problems, but also the problem of imbalance at the midpoint of the voltage of input capacitors. However, the Z-source half-bridge converter achieves a limited voltage gain, so it can no longer satisfy the high-voltage-gain requirement of BIPV.

Compared to the above topology, a Y-impedance-network takes the place of the Z-source network in the proposed converter. Under the premise of solving the above problems, the proposed topology has a higher boosting capacity owing to the existence of the Y-impedance-network. The winding factors

are shown in Figure 5, which illustrate that with a large duty cycle and K value comes a large voltage gain, and as shown, the voltage gain can be several times higher than that of the conventional one.

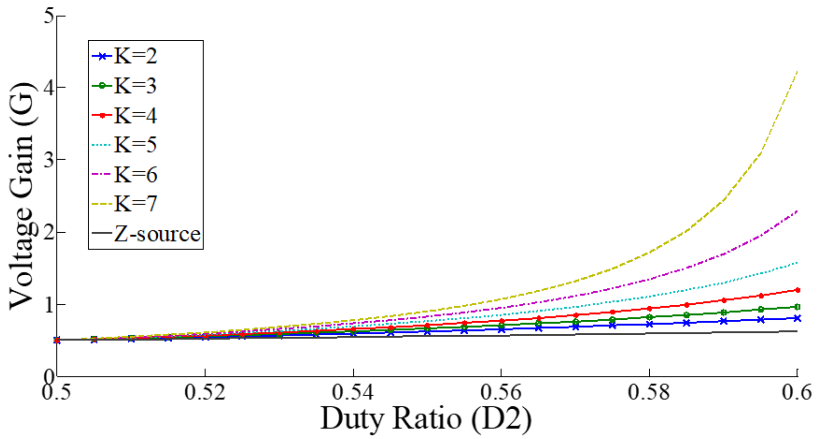

Figure 5. The relationship between the voltage gain and duty cycle: winding factors.

4. Simulation Verifications

To verify the feasibility and validity of the proposed converter, PSIM software was applied for the simulation.

The preassigned parameters are as listed as follows: input voltage $V_{\text{in}} = 10$ V, resistive load $R = 200\ \Omega$, permitted fluctuation range $x_C = 1\%$, $x_L = 10\%$, and period $T_S = 100$ µs. The high harmonic frequency of the capacitance and inductance are approximately equal to the switching frequency of the converter. Therefore, d_{v_C}, d_{i_L} and dt can be deduced as

$$d_{v_C} = x_C V_C, \tag{14}$$

$$d_{i_L} = x_L I_L, \tag{15}$$

and

$$dt \approx (D_1 + D_2 - 1)T_S. \tag{16}$$

Thus, capacitors and inductors are designed as

$$L = \frac{v_L dt}{di_L} = \frac{v_L(D_1 + D_2 - 1)T_S}{x_L I_L}, \tag{17}$$

and

$$C = \frac{i_C dt}{dv_C} = \frac{i_C(D_1 + D_2 - 1)T_S}{x_C V_C}. \tag{18}$$

Then, based on the analysis in Section 2, the parameters can be expressed as

$$\begin{cases} L_1 = L_2 = \dfrac{V_{C_4}(D_1 + D_2 - 1)T_S}{2x_L I_L}, \\ L_m = \dfrac{n_1}{n_3 - n_2} \cdot \dfrac{V_{C_3}(1 - D_2)T_S}{2x_L I_L}, \\ C_1 = C_2 = \dfrac{I_o(D_1 + D_2 - 1)T_S}{2x_C V_{C_1}}, \\ C_3 = \dfrac{I_{n_3}(D_1 + D_2 - 1)T_S}{x_C V_{C_3}}, \\ C_4 = \dfrac{(I_o + 2I_L)(D_1 + D_2 - 1)T_S}{x_C V_{C_4}}. \end{cases} \tag{19}$$

Therefore, the parameters of the converter are chosen as follows: $L_m = 470$ μH, n_1:n_2:n_3 = 5:1:3, $C_1 = C_2 = 47$ μF, $C_3 = C_4 = 470$ μF, and $L_1 = L_2 = 420$ μH.

Simulations are shown in Figure 6, and the output voltage of the proposed converter $V_o \approx 60$ V, which is consistent with the theoretical analyses, is shown in Figure 4. Under the same conditions, as documented in [7], the voltage gain of the conventional converter can be calculated as 0.735 and the output voltage $V_o \approx 7.35$ V, which coincides with the simulations in Figure 6b. As shown in Figure 6, by adjusting the turns ratio and duty cycle, the voltage gain of the proposed converter can be eight times higher than that of the conventional.

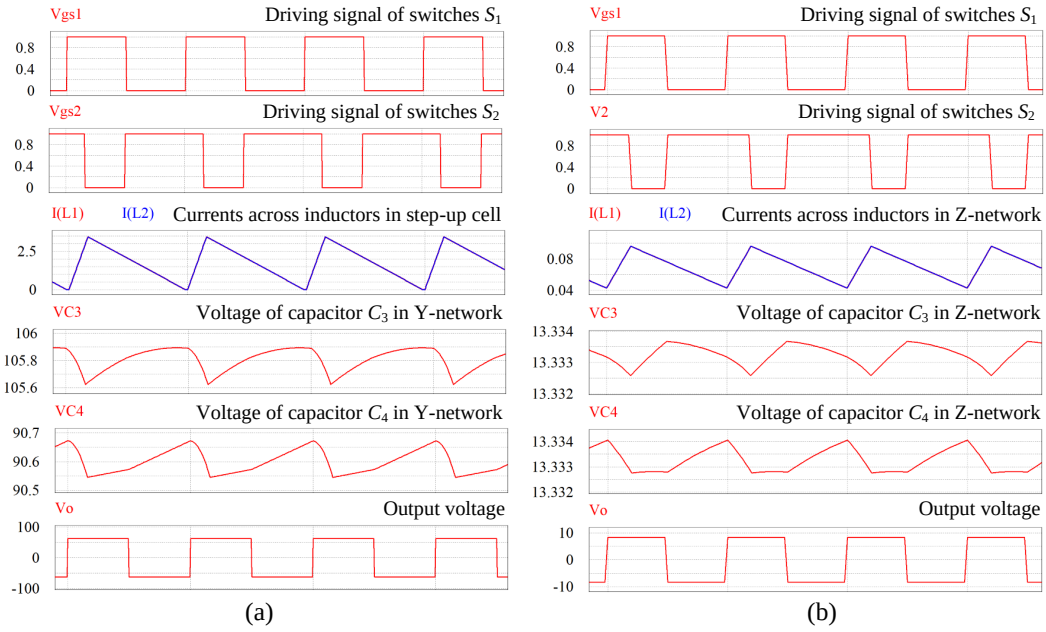

Figure 6. Simulation waveforms when $D_1 = 0.5$ and $D_2 = 0.66$ of (**a**) proposed converter and (**b**) traditional converter in [7].

5. Experimental Verifications

In this section, the experimental environment and physical prototype are established, which are shown in Table 2 and Figure 7, to verify the theoretical analyses. Experimental parameters are shown in Table 3.

Table 2. Experimental platform.

DC Power Supply	Oscilloscope	Voltage Probe	Current Probe
KIKUSUI PWR800L	Agilent DSO7104A	KEYSIGHT N2843A	Agilent 1147A

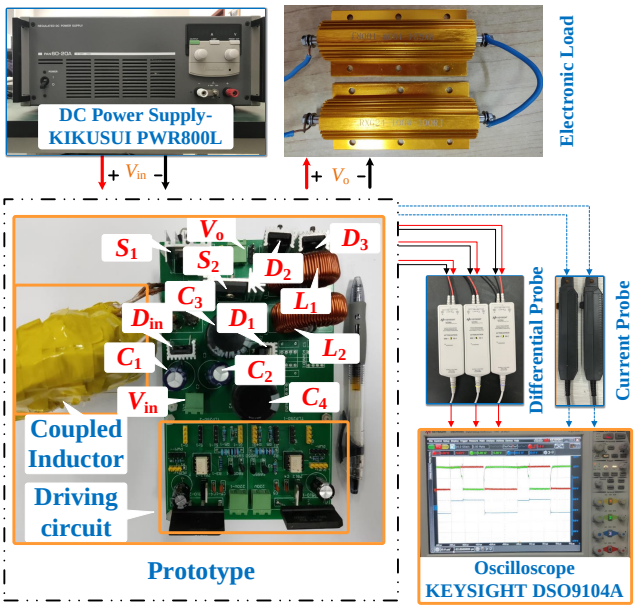

Figure 7. Prototypes with the experimental environment.

Table 3. Experimental Parameters

Parameters	Value	Parasitic Parameters
Input voltage V_{in}	10 [V]	
Output voltage V_o	60 [V]	
Switching frequency f_s	10 [kHz]	
Driving IC	TLP250	
MOSFET S_1,S_2	IXTQ88N30P	40 [mΩ]
Inductors L_1, L_2	420 [μH]	200 [mΩ]
Three winding-coupled inductor	Magnetizing inductance 470 [μH] Turns ratio 5:1:3	290 [mΩ]: 260 [mΩ]: 270 [mΩ]
Diodes D_1, D_2, D_3, D_{in}	MBRF20200CT	1 [V] / 0.05 [mΩ]
Capacitors C_1, C_2	47 [μF]/100 [V]	500 [mΩ]
Capacitor C_3, C_4	470 [μF]/250 [V]	200 [mΩ]
Resistive load	200 [Ω]	

The experimental results are shown in Figure 8, which contains gate-source voltages of switches V_{GS1}, V_{GS2}, the output voltage V_o. It is noted that the experimental results agree well with the theoretical analyses and simulation, demonstrating the functionality and feasibility of the proposed converter.

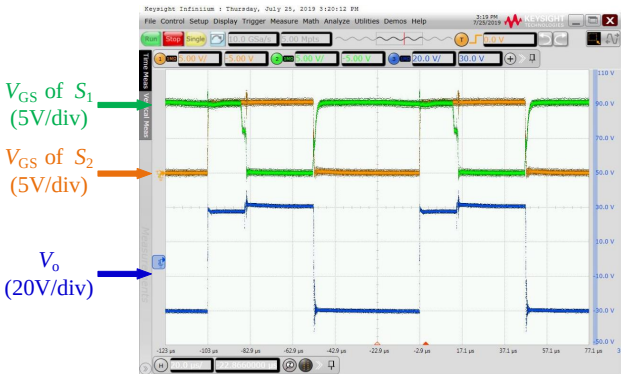

Figure 8. Experimental waveforms when the turns ratio is 5:1:3 and the duty ratio is $D_1 = 0.5, D_2 = 0.66$.

In order to demonstrate the practicality and implementability of the proposed converter comprehensively, key waveforms of the proposed converter with different turns ratios and duty ratios are shown in Figure 9. Therein, with small inductance of the coupled inductor, the proposed converter operates in discontinuous conduction mode (DCM), as shown in Figure 9a,b. When $D_1 \neq 0.5$, the negative and positive output voltages are asymmetric, as shown in Figure 9c,d, which agrees well with above theoretically analyses.

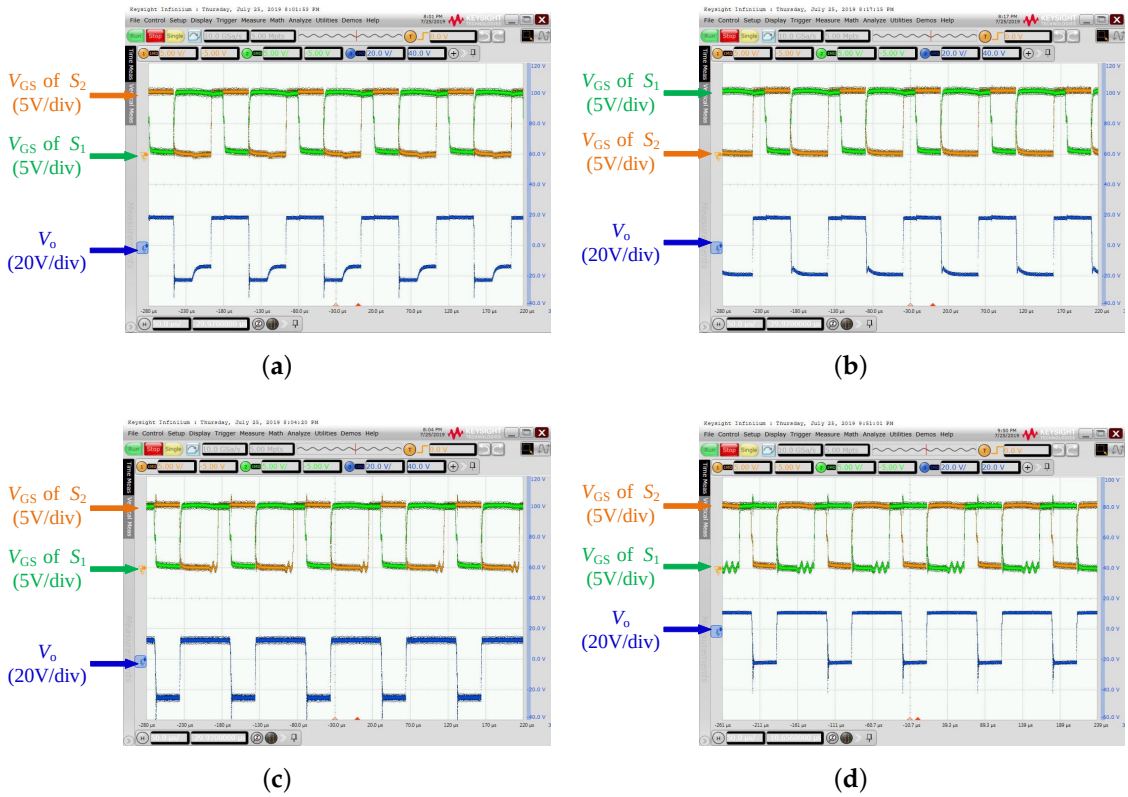

Figure 9. Experimental waveforms of the proposed converter in: (**a**) turns ratio 3:1:5, duty ratio $D_1 = 0.5, D_2 = 0.66$; (**b**) turns ratio 1:3:5, duty ratio $D_1 = 0.5, D_2 = 0.66$; (**c**) turns ratio 3:1:5, duty ratio $D_1 = 0.66, D_2 = 0.5$; (**d**) turns ratio 1:3:5, duty ratio $D_1 = 0.66, D_2 = 0.5$.

6. Conclusions

In this study, a novel buck-boost half-bridge converter is proposed, which combines a Y-impedance-network and a family of step-up cells with a conventional half-bridge inverter to

realize the additional voltage adjustment function. The simulation and experimental results show that by adjusting the turns ratio and duty cycle, they can achieve a high voltage gain which satisfies the high-voltage-gain requirement of BIPV, something which conventional inverters cannot achieve. In detail, the proposed Y-impedance-network-based half-bridge converter without additional step-up cells can realize 10 times the voltage adjustment function of traditional half-bridge converters. With additional step-up cells, the voltage adjustment range is enlarged, which also verifies the wide voltage adjustment functions of the proposed idea. Furthermore, the proposed converters can output symmetric or asymmetric positive and negative voltages, which validates its applicability and implementability for industrial applications. Therefore, the proposed solution in this paper can offer a potential voltage adjustment method in various industrial applications.

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Abbreviations

The following abbreviations are used in this manuscript:

BIPV	Building Integrated Photovoltaic
ZSI	Z-source inverter
DCM	discontinuous conduction mode
qZSI	quasi-Z-source inverter

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