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Wide Load Range ZVS Three-level DC-DC Converter: Modular Structure, Redundancy Ability, and Reduced Filters Size

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Abstract: In future dc distributed power systems, high performance high voltage dc-dc converters with redundancy ability are welcome. However, most existing high voltage dc-dc converters do not have redundancy ability. To solve this problem, a wide load range zero-voltage switching (ZVS) three-level (TL) dc-dc converter is proposed, which has some definitely good features. The primary switches have reduced voltage stress, which is only $V_{in}/2$. Moreover, no extra clamping component is needed, which results simple primary structure. Redundancy ability can be obtained by both primary and secondary sides, which means high system reliability. With proper designing of magnetizing inductance, all primary switches can obtain ZVS down to 0 output current, and in addition, the added conduction loss can be neglected. TL voltage waveform before the output inductor is obtained, which leads small volume of the output filter. Four secondary MOSFETs can be switched in zero-current switching (ZCS) condition over wide load range. Finally, both the primary and secondary power stages are modular architecture, which permits realizing any given system specifications by low voltage, standardized power modules. The operation principle, soft switching characteristics are presented in this paper, and the experimental results from a 1 kW prototype are also provided to validate the proposed converter.

Keywords: modular structure; ZVS; redundancy ability

1. Introduction

The dc distribution, with several good features, e.g., high system stability, high conversion and transmission efficiency, high flexibility and easy system control [1–3], seems to be the most attractive solution for future power systems with the increasing percentage of renewable energy sources, such as photovoltaic, wind power, and fuel cells. To improve the overall performance of a dc distribution, high dc input voltage is preferred. Therefore, dc-dc converters for high voltage dc distributions with good input and output characteristics, simple and compact circuit structure, good efficiency performance have already become hot issues in the power electronics society [4]. The main challenge caused by high dc input voltage is how to select proper power devices to fulfill power conversion task without system performance and reliability compensating [4]. Full bridge (FB) dc-dc topology with high voltage rating MOSFETs and IGBTs may be directly used in high voltage dc-dc conversion, but, high conduction loss and worse switching characteristics of these high voltage rating power devices may greatly degrade the conversion efficiency and power density. Moreover, high voltage dynamic transition would cause some electrical-magnetic compliable (EMC) problems, which is not preferred in the designing and producing procedure of the high input dc-dc power converters. Therefore, using series connected low voltage rating and high-performance power modules to sustain high dc bus voltage is still the

best solution in high voltage dc-dc applications. Several good research papers have been published, and these solutions can be concluded into two kinds, which are TL dc-dc converters [5–19] and input series cells dc-dc converters [20–32]. The first TL dc-dc converter was proposed in [5], which is a diode clamped half bridge (HB) dc-dc converter. In [5], the voltage stress on each primary switch is only $V_{in}/2$, and the primary switches can obtain zero-voltage switching (ZVS) with limited load range. A series of zero-voltage and zero-current switching (ZVZCS) TL dc-dc converters were proposed in [6], and the primary switches in this converter can achieve ZVZCS operation over wide load range; furthermore, a simple switching scheme is used in these converters, which makes these topologies more convenient to industrial customers. Then, many other good research results have been reported in following main aspects: new topologies for special applications [8–10], wide range soft switching technologies [6,10–16], and converters with reduced volume of the input and output filters [16–19]. All above mentioned papers have made the TL dc-dc converters more applicable.

Input series cells dc-dc converter (ISCDC) is another solution for high voltage dc-dc conversion, which is composed of several series connected cells to reduce the voltage stress on the primary switches. Compared to TL dc-dc converters, ISCDCs have a simple and compact primary circuit due to its modular structure, which is attractive to high input industrial applications. In [20,21], ISCDCs based on forward or fly-back cells were proposed, which can reduce the voltage stress on the primary switches. The main drawback of these converters is hard switching operation, which results low power transferring efficiency. Some resonant ISCDCs were presented in [22,23], and these converters can achieve good soft switching characteristics, as well as low voltage stress on the primary switches. Half bridge (HB) based ISCDCs were reported and analyzed in [24–26], and some of these converters have input voltage auto-balance ability. Input-series output-parallel dc-dc converters (ISOPDCs) are new type ISCDCs, which are considered as the most promising choice due to its truly modular structure, which means normal two-level modules can be directly connected for special high voltage applications [27,28]. The main challenge of ISOPDCs is the input voltage balance problem, which can be solved by many control strategies [29–31] with increased cost and circuit complexity. In [32], a flying capacitor is added to achieve input voltage auto-balance ability, which makes the ISOPDC more applicable [32]. Figure 1 shows the ISOPDC in [32], which is composed of two two-level FB cells series connected in the primary side and parallel connected in the secondary side. Two FB cells are synchronously switched with the PS switching scheme, and a flying capacitor is used to obtain auto-voltage balance ability.

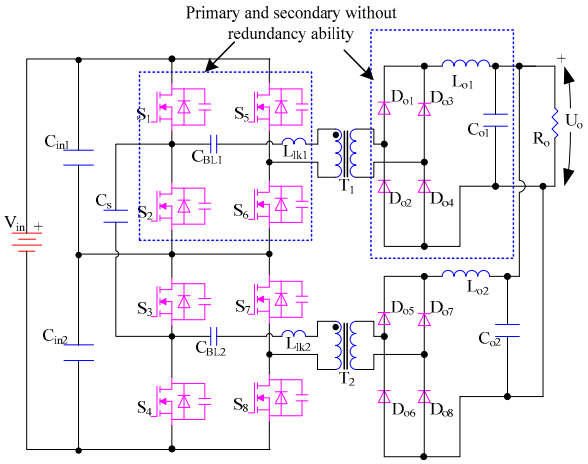

Figure 1. ISOPDC in [32].

However, limitations still exist. As shown in Figure 1, the midpoint voltage is still highly dependent on the states of the input series and output parallel connected modules. Any errors occurring in each module, i.e., S_1 is broken, would cause the converter halting due to the voltage of the input capacitors cannot be balanced again, which means the primary and secondary sides of the

converter in Figure 1 having no redundancy ability. In fact, this is a common problem of most ISCDCs. In addition, the converter in Figure 1 has some other disadvantages: the secondary rectifier voltage waveforms are still two-level, which needs a large output filter to minimize the output current ripple, and a large input EMI filter is also required; the ZVS load range is narrow, which results in high power loss especially under the light load condition. Therefore, it is still a worthy task to find new high voltage dc-dc converters with redundancy ability, modular structure, simple input voltage balance circuit, reduced volume of the output and input filters, and good soft switching characteristics.

In this paper, a wide load range ZVS high voltage dc-dc converter with redundancy ability, modular structure, simple input voltage balance circuit, reduced volume of the output and input inductors is proposed and investigated. The outline of this paper is concluded as follows. In Section 2, the configuration of the proposed converter is presented. Normal operation principle is discussed in Section 3. And in Section 4, module failure operation principle is analyzed to prove the redundancy ability. Some important technical issues are analyzed in Section 5. Experimental results are presented and discussed in Section 6. The main conclusions are given in the last section.

2. Circuit Configuration

Figure 2 shows the presented circuit. In the primary side, C_{in1} and C_{in2} are the input capacitors with the same value, which are used to split the input voltage. S_1-S_8 are the primary switches; D_1-D_8 are the anti-parallel diodes of S_1-S_8, and C_1-C_8 are corresponding parasitic capacitors of the primary switches. During the operation, OFF voltages across S_1-S_8 are directly clamped by C_{in1} and C_{in2}, thus, no extra clamping component is needed. C_{BL1} and C_{BL2} are two dc blocking capacitors, which is series connected with N_{1p} and N_{2p}. L_{lk1} and L_{lk2} are the leakage inductors of the transformers; L_{1m} and L_{2m} are magnetic inductors of the transformers, which is designed to a specific value to help the ZVS of S_1-S_8. In the secondary side, two parallel-connected rectifier modules are included. The first rectifier module is built of S_{s1}-S_{s2}, D_{o1}-D_{o6}, L_{o1} and C_{o1}; while, the secondary module is composed of S_{s3}-S_{s4}, D_{o7}-D_{o12}, L_{o2} and C_{o2}.

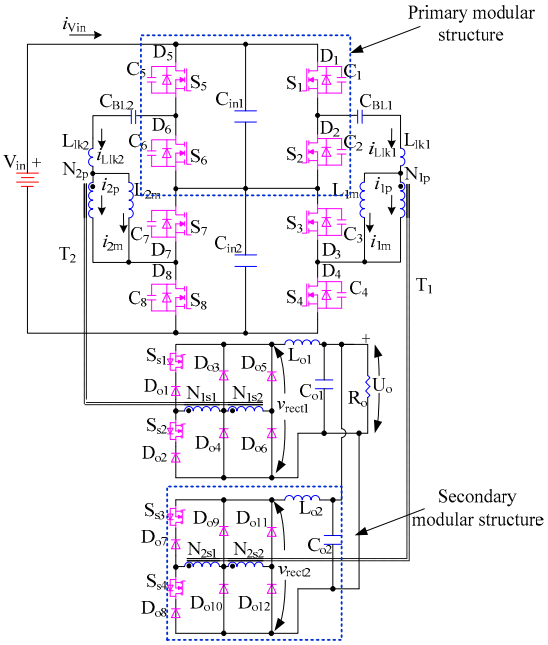

Figure 2. Proposed high voltage zero-voltage switching (ZVS) dc-dc converter with redundancy ability.

3. Normal Operation

Before the discussion, some assumptions are concluded as follows: (1) the on-resistance of the primary switches are neglected; (2) the voltage ripple on C_{in1}, C_{in2}, C_{BL1} and C_{BL2} can be

neglected due to high capacitance; (3) the output capacitance of the power devices is identical, and is represented by C_o; (4) L_{lk1} and L_{lk2} are identical, and are represented by L_{lk}; (5) L_{1m} and L_{2m} are identical, and are represented by L_m; (6) N_{1p} is identical to N_{2p}, and $N_{1s1} = N_{1s2} = N_{2s1} = N_{2s2}$; (7) $k_T = N_{1p}/N_{1s1} = N_{2p}/N_{2s1}$; (8) the current ripple of i_{Lo1} and i_{Lo2} is neglected; (9) With proper controlling, the output currents of the two paralleled connected modules can be identical, and the controlling method is not discussed in this paper. Therefore, $i_{Lo1} = i_{Lo2}$. i_{Lo1} and i_{Lo2} are represented by I_o ; (10) i_{in} is identical to $i_{Vin} + i_{Cin}$, and its AC content is defined as $\tilde{i}_{in}$. During the normal operation, the proposed converter can be controlled in the secondary side and primary side modulation modes. Figure 3 depicts the key waveforms, Tables 1 and 2 show the switching status in each stage.

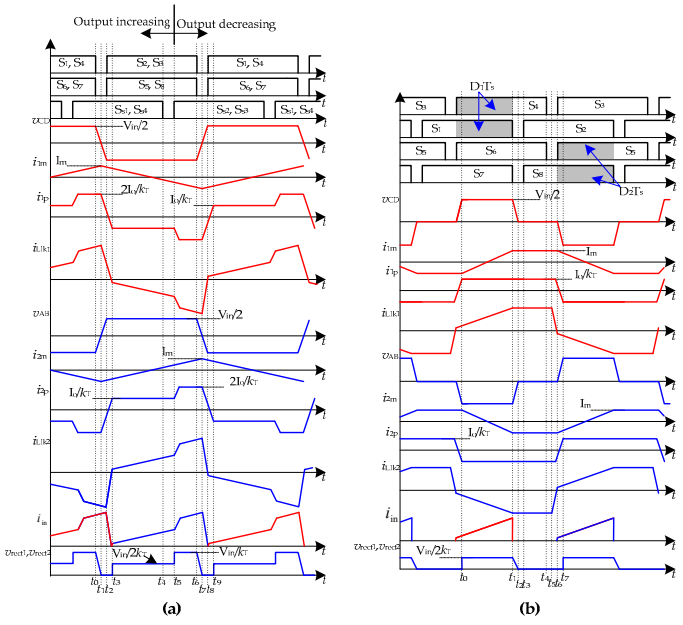

Figure 3. Key waveforms: (**a**) secondary side modulation; (**b**) primary side modulation.

Table 1. Switching scheme in the first half switching period (secondary side modulation mode).

Item	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{s1}	S_{s2}	S_{s3}	S_{s4}
Stage 1	ON	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF
Stage 2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
Stage 3	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
Stage 4	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON
Stage 5	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON
Stage 6	OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF

Table 2. Switching scheme in the first half switching period (secondary side modulation mode).

Item	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{s1}	S_{s2}	S_{s3}	S_{s4}
Stage 1	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
Stage 2	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
Stage 3	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
Stage 4	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Stage 5	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
Stage 6	OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF

3.1. Secondary Side Modulation

As shown in Figure 3a, the primary switches can be divided into two groups. The first group is S_1, S_4, S_6 and S_7; while another group is S_2, S_3, S_5 and S_8. The switches in each group are switched ON and OFF synchronously, and the switches in different groups are switched in the complementary

mode. In the secondary side, S_{s2} and S_{s3} are switched ON and OFF synchronously; while S_{s1} and S_{s4} are switched ON and OFF synchronously. S_{s1} and S_{s3} are switched in the complementary mode with S_{s2} and S_{s4}. V_o can be regulated by the phase angel between gate signals of S_{s1} and S_1, S_{s3} and S_5. When these angles equal 180°, $V_o = V_{in}/(2k_T)$. There are 12 operation stages in one switching cycle, and the operation stages in the first half switching cycle are illustrated in Figure 4.

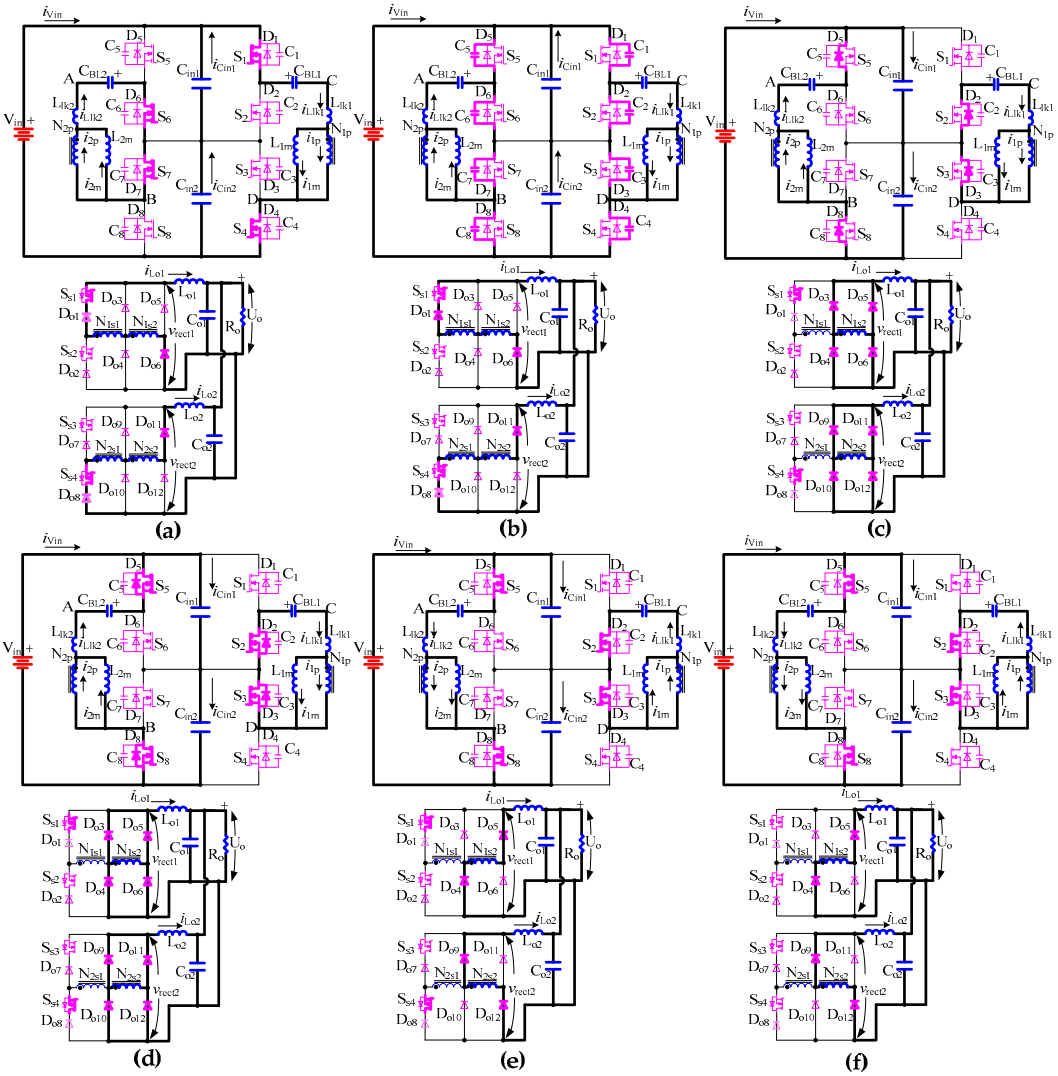

Figure 4. Operation stages of the secondary modulation: (**a**) stage 1; (**b**) stage 2; (**c**) stage 3; (**d**) stage 4; (**e**) stage 5; (**f**) stage 6.

Stage 1 [Figure 4a]: before t_0, the circuit is stable. Input source powers the load. In the primary side, S_1, S_4, S_6 and S_7 are ON; $v_{CD} = V_{in}/2$, and $v_{AB} = -V_{in}/2$; $i_{1p} = 2I_o/k_T$, and $i_{2p} = -2I_o/k_T$. i_{Llk1} and i_{Llk2} are

$$i_{Llk1}(t) = \frac{2I_o}{k_T} + i_{1m}(t_0) + \frac{V_{in}}{2L_m}(t - t_0) \quad (1)$$

$$i_{Llk2}(t) = -\frac{2I_o}{k_T} + i_{2m}(t_0) - \frac{V_{in}}{2L_m}(t - t_0) \quad (2)$$

$i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk1}. The DC content of i_{in} flows from the input source to the primary sides of the transformers directly. i_{Cin1} is partial AC content of i_{in} depends on the reactance distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and

C_{in2} is constant during this period. v_{S2} and v_{S5} are clamped by C_{in1}, and v_{S3} and v_{S8} are clamped by C_{in2}.

In the secondary side, S_{s1} and S_{s4} are ON; D_{o1}, D_{o6}, D_{o8} and D_{o11} are conducted; $v_{rect1} = v_{rect2} = V_{in}/k_T$.

Stage 2 [Figure 4b, t_0-t_1]: At t_0, S_1, S_4, S_6 and S_7 are switched OFF. In the primary side, the slope rates of i_{1m} and i_{2m} are very slow, and the absolute value of these currents is constant value I_m. Therefore, the absolute value of i_{Llk1} and i_{Llk2} during this period is

$$\left|i_{Llk1}(t)\right| = \left|i_{Llk2}(t)\right| = I_m + \frac{2I_o}{k_T} \tag{3}$$

i_{Llk1} charges C_1 and C_4, discharges C_2 and C_3; while i_{Llk2} charges C_6 and C_7, discharges C_5 and C_8. v_{S1}, v_{S4}, v_{S6} and v_{S7} are

$$v_{Si}(t) = \frac{I_m k_T + 2I_o}{2k_T C_o} t, \quad i = 1,\ 4,\ 6,\ 7 \tag{4}$$

v_{S2}, v_{S3}, v_{S5} and v_{S8} are

$$v_{Sk}(t) = \frac{V_{in}}{2} - \frac{I_m k_T + 2I_o}{2k_T C_o} t, \quad k = 2,\ 3,\ 5,\ 8 \tag{5}$$

According to (4) and (5), the voltage of S_1-S_8 is lower than $V_{in}/2$, before the end of this stage. This stage lasts until v_{S1} is $V_{in}/2$, and the interval is

$$T_{10} = \frac{V_{in} C_o k_T}{(I_m k_T + 2I_o)} \tag{6}$$

i_{Cin1} is identical to i_{Cin2}, which is $i_{Llk1} - i_{Llk2}$, and under ideal condition, this value is zero. Therefore, the midpoint voltage of C_{in1} and C_{in2} can also be stabled during this period.

In the secondary side, S_{s1} and S_{s4} are ON; D_{o1}, D_{o6}, D_{o8} and D_{o11} are conducted; $v_{rect1} = v_{rect2} = 2v_{CD}(t)/k_T = 2|v_{AB}(t)|/k_T$.

Stage 3 [Figure 4c, t_1-t_2]: At t_1, D_2, D_3, D_5 and D_8 are ON. In the primary side, $v_{CD} = -V_{in}/2$, and $v_{AB} = V_{in}/2$; L_{1m} and L_{2m} sustain negative voltage, and i_{1m} and i_{2m} are

$$i_{1m}(t) = I_m - \frac{V_{in}}{2L_m}(t - t_1) \tag{7}$$

$$i_{2m}(t) = -I_m + \frac{V_{in}}{2L_m}(t - t_1) \tag{8}$$

i_{Llk1} and i_{Llk2} are

$$i_{Llk1}(t) = \left(\frac{2I_o}{k_T} + I_m\right) - \frac{V_{in}}{2}\frac{L_m + L_{lk}}{L_m L_{lk}}(t - t_1) \tag{9}$$

$$i_{Llk2}(t) = -\left(\frac{2I_o}{k_T} + I_m\right) + \frac{V_{in}}{2}\frac{L_m + L_{lk}}{L_m L_{lk}}(t - t_1) \tag{10}$$

$i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk2}. The DC content of i_{in} will flow from the input source to the primary sides of the transformers directly. i_{Cin1} is partial AC content of i_{in} depends on the reactance distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S1} and v_{S6} are clamped by C_{in1}, and v_{S4} and v_{S7} are clamped by C_{in2}. S_2, S_3, S_5 and S_8 should be gated after t_1 to achieve ZVS operation.

In the secondary side, D_{o3}-D_{o6} and D_{o9}-D_{o12} are ON to free-wheel the secondary currents. $v_{rect1} = v_{rect2} = 0$.

Stage 4 [Figure 4d, t_2-t_3]: At t_2, S_2, S_3, S_5 and S_8 are switched ON with ZVS. In the primary side, i_{1m}, i_{2m}, i_{1p} and i_{2p} keep increasing in the reverse direction, and the increasing slope are defined as (13) to (16). $i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk2}. i_{Cin1} is partial AC content of i_{in} depends on the reactance

distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S1} and v_{S6} are clamped by C_{in1}, and v_{S4} and v_{S7} are clamped by C_{in2}.

In the secondary side, D_{o3}-D_{o6} and D_{o9}-D_{o12} are conducted to free-wheel the secondary currents. S_{s1} and S_{s4} are ON. As the currents through S_{s1} and S_{s4} are 0, thus, S_{s1} and S_{s4} can achieve ZCS turned on after this period. v_{rect1} and v_{rect2} are zero.

Stage 5 [Figure 4e) t_3-t_4]: At t_3, the absolute value of i_{1p} and i_{2p} is I_o/k_T. In the primary side, S_2, S_3, S_5 and S_8 are ON; $v_{CD} = -V_{in}/2$, and $v_{AB} = V_{in}/2$; $i_{1p} = -I_o/k_T$, and $i_{2p} = I_o/k_T$. i_{1m} and i_{2m} are

$$i_{1m}(t) = i_{1m}(t_3) - \frac{V_{in}}{2L_m}(t - t_3) \tag{11}$$

$$i_{2m}(t) = i_{2m}(t_3) + \frac{V_{in}}{2L_m}(t - t_3) \tag{12}$$

i_{Llk1} and i_{Llk2} are

$$i_{Llk1}(t) = -\frac{I_o}{k_T} + i_{1m}(t_3) - \frac{V_{in}}{2L_m}(t - t_3) \tag{13}$$

$$i_{Llk2}(t) = \frac{I_o}{k_T} + i_{2m}(t_3) + \frac{V_{in}}{2L_m}(t - t_3) \tag{14}$$

$i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk2}. i_{Cin1} is partial AC content of i_{in} depends on the reactance distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S1} and v_{S6} are clamped by C_{in1}, and v_{S4} and v_{S7} are clamped by C_{in2}.

In the secondary side, D_{o4}, D_{o5}, D_{o9} and D_{o12} are conducted; $v_{rect1} = v_{rect2} = V_{in}/(2k_T)$.

Stage 6 [Figure 4f, t_4-t_5]: At t_4, S_{s1} and S_{s4} are OFF with zero-current switching (ZCS). After t_5, the circuit will be operated into the secondary switching period, and detail analyses are not provided here for the sake of simplicity.

The ideal output-input voltage ratio in this mode is

$$\frac{V_o}{V_{in}} = \frac{(1 + D)}{2k_T} \tag{15}$$

3.2. Primary Side Modulation

When the phase angle between S_{s1} and S_1 is 180°, the secondary side modulation mode cannot further change the output voltage. To regulate output voltage down to zero, the converter must be controlled into the primary side modulation mode. In this mode, the secondary switches S_{s1}-S_{s4} are OFF; the primary switches are divided into two groups, which are S_1 to S_4 and S_5 to S_8. As shown in Figure 3b, the primary switches in each group are switched in the PS switching scheme, and S_1 and S_6 are switched with the same phase angle. D_1 and D_2 are duty ratios of S_1-S_4 and S_5-S_8, and with symmetrical switching pattern, $D_1 = D_2$. The output voltage is varied with the value of D_1 and D_2, when $D_1 = D_2 = 0$, the output voltage is zero. The key waveforms of this mode are depicted in Figure 3b, and the operation stages in the first half switching cycle are illustrated in Figure 6.

Stage 1 [Figure 5a]: before t_1, the circuit is operated in steady condition. Input source powers the load. In the primary side, S_1, S_4, S_6 and S_7 are ON; $v_{CD} = V_{in}/2$, and $v_{AB} = -V_{in}/2$; $i_{1p} = -I_o/k_T$, and $i_{2p} = I_o/k_T$.

i_{Llk1} and i_{Llk2} are

$$i_{Llk1}(t) = -\frac{I_o}{k_T} - I_m + \frac{V_{in}}{2L_m}(t - t_0) \tag{16}$$

$$i_{Llk2}(t) = \frac{I_o}{k_T} + I_m - \frac{V_{in}}{2L_m}(t - t_0) \tag{17}$$

$i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk1}. i_{Cin1} is formed by partial AC content of i_{in} depends on the reactance distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S2} and v_{S5} are clamped by C_{in1}, and v_{S3} and v_{S8} are clamped by C_{in2}.

In the secondary side, S_{s1}-S_{s4} are OFF; D_{o3}, D_{o6}, D_{o10} and D_{o11} are conducted; $v_{rect1} = v_{rect2} = V_{in}/(2k_T)$.

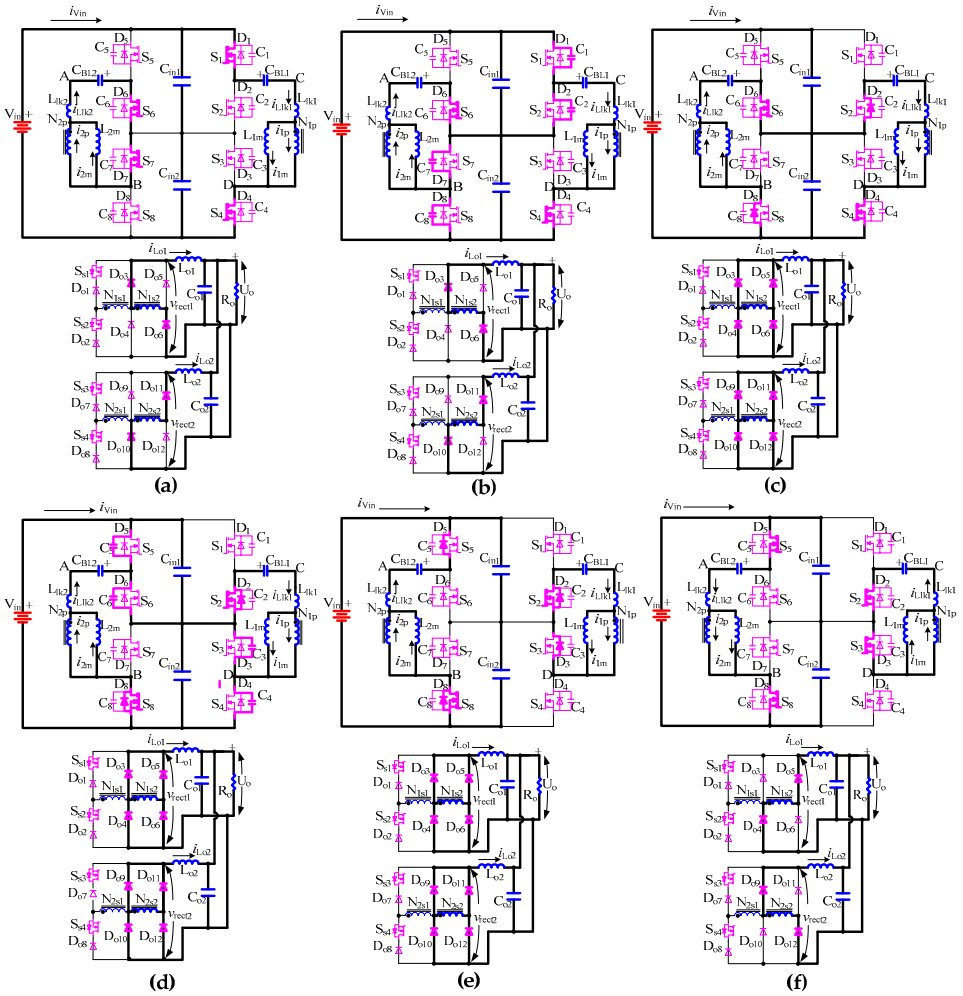

Figure 5. Operation stages of the primary side modulation mode: (**a**) stage 1; (**b**) stage 2; (**c**) stage 3; (**d**) stage 4; (**e**) stage 5; (**f**) stage 6.

Stage 2 [Figure 5b, t_1-t_2]: At t_1, S_1 and S_7 are switched OFF. In the primary side, S_1 and S_7 can obtain zero-voltage turned OFF due to existence of C_1 and C_7. i_{1m} and i_{2m} reach their maximum absolute value I_m. Therefore, the absolute values of i_{Llk1} and i_{Llk2} are

$$\left|i_{Llk1}(t)\right| = \left|i_{Llk2}(t)\right| = I_m + \frac{I_o}{k_T} \tag{18}$$

i_{Llk1} charges C_1, discharges C_2; while i_{Llk2} charges C_7, discharges C_8. v_{S1} and v_{S7} are

$$v_{Si}(t) = \frac{I_m k_T + I_o}{2k_T C_o} t, \quad i = 1,\ 7 \tag{19}$$

v_{S2} and v_{S8} are

$$v_{Sk}(t) = \frac{V_{in}}{2} - \frac{I_m k_T + I_o}{2k_T C_o} t, \quad k = 2,\ 8 \tag{20}$$

According to (19) and (20), v_{S1}, v_{S2}, v_{S7} and v_{S8} is lower than $V_{in}/2$ before the end of this stage. This stage ends until v_{S1} and v_{S7} is $V_{in}/2$, and the time is

$$T_{21} = \frac{V_{in} C_o k_T}{(I_m k_T + I_o)} \tag{21}$$

i_{Cin1} is identical to i_{Cin2}, which is i_{Llk1}-i_{Llk2}, and with symmetrical switching sequence i_{Cin1} is zero. Therefore, the midpoint voltage of C_{in1} and C_{in2} is constant during this period.

In the secondary side, D_{o3}, D_{o6}, D_{o10} and D_{o11} are conducted; $v_{rect1} = v_{rect2} = v_{CD}(t)/k_T = |v_{AB}(t)|/k_T$.

Stage 3 [Figure 5c, t_2-t_4]: At t_2, D_2 and D_8 are on. In the primary side, $v_{CD} = v_{AB} = 0$; i_{1m} and i_{2m} keep constant value I_m; i_{1p} and i_{2p} are with the same absolute value $|I_o/k_T|$, During this period, i_{Llk1} and i_{Llk2} are

$$i_{Llk1}(t) = \frac{I_o}{k_T} + I_m \tag{22}$$

$$i_{Llk2}(t) = -(\frac{I_o}{k_T} + I_m) \tag{23}$$

i_{Cin1} is identical to i_{Cin2} with the value of i_{Llk1}-i_{Llk2}, thus, with symmetrical switching cycle, i_{Cin1} and i_{Cin2} are zero, which means stable midpoint voltage of input capacitors can be achieved. Therefore, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S1} and v_{S5} are clamped by C_{in1}, and v_{S3} and v_{S7} are clamped by C_{in2}. S_2 and S_8 should be gated after t_2 to achieve ZVS operation, and according to Figure 3b, S_2 and S_8 are switched at t_3.

In the secondary side, D_{o3}-D_{o6} and D_{o9}-D_{o12} are ON to free-wheel the secondary currents. $v_{rect1} = v_{rect2} = 0$.

Stage 4 [Figure 5d, t_4-t_5]: At t_4, S_4 and S_6 are switched OFF. In the primary side, S_4 and S_6 can obtain zero-voltage turned OFF due to C_4 and C_6. The primary currents keep constant during this stage. i_{Llk1} charges C_4, discharges C_3; while i_{Llk2} charges C_6, discharges C_5. v_{S4} and v_{S5} are

$$v_{Si}(t) = \frac{I_m k_T + I_o}{2 k_T C_o} t, \quad i = 4,\ 5 \tag{24}$$

v_{S3} and v_{S6} are

$$v_{Sk}(t) = \frac{V_{in}}{2} - \frac{I_m k_T + I_o}{2 k_T C_o} t, \quad k = 3,\ 6 \tag{25}$$

This stage ends until v_{S4} and v_{S6} are $V_{in}/2$, and the time is

$$T_{54} = \frac{V_{in} C_o k_T}{2(I_m k_T + I_o)} \tag{26}$$

i_{Cin1} is identical to i_{Cin2} with the value of i_{Llk1}-i_{Llk2}, thus, with symmetrical switching cycle, the currents flowing through C_{in1} and C_{in2} are zero, which means stable midpoint voltage of input capacitors can be achieved. Therefore, the midpoint voltage of C_{in1} and C_{in2} is constant during this period.

In the secondary side, D_{o3}-D_{o6} and D_{o9}-D_{o12} are ON to free-wheel the secondary currents. $v_{rect1} = v_{rect2} = 0$.

Stage 5 [Figure 5e, t_5-t_6]: At t_5, D_3 and D_5 are ON. In the primary side, $v_{CD} = -V_{in}/2$, and $v_{AB} = V_{in}/2$; negative voltage is applied on magnetic inductors, and i_{1m} and i_{2m} are

$$i_{1m}(t) = I_m - \frac{V_{in}}{2L_m}(t - t_5) \tag{27}$$

$$i_{2m}(t) = -I_m + \frac{V_{in}}{2L_m}(t - t_5) \tag{28}$$

i_{Llk1} and i_{Llk2} are

$$i_{Llk1}(t) = (\frac{I_o}{k_T} + I_m) - \frac{V_{in}}{2}\frac{L_m + L_{lk}}{L_m L_{lk}}(t - t_5) \quad (29)$$

$$i_{Llk2}(t) = -(\frac{I_o}{k_T} + I_m) + \frac{V_{in}}{2}\frac{L_m + L_{lk}}{L_m L_{lk}}(t - t_5) \quad (30)$$

$i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk2}. i_{Cin1} is partial AC content of i_{in} depends on the reactance distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S1} and v_{S6} is clamped by C_{in1}, and v_{S4} and v_{S7} is clamped by C_{in2}. S_3 and S_5 should be gated after t_5 to achieve ZVS operation, and according to Figure 3b, S_3 and S_5 are switched at t_6.

In the secondary side, D_{o3}-D_{o6} and D_{o9}-D_{o12} are ON to free-wheel the secondary currents. $v_{rect1} = v_{rect2} = 0$.

Stage 6 [Figure 5f, t_6-t_7]: At t_7, i_{1p} equals $-I_o/k_T$, and i_{2p} equals I_o/k_T; the free-wheeling mode is over. Input source powers the load. In the primary side, S_2, S_3, S_5 and S_8 are ON; $v_{CD} = -V_{in}/2$, and $v_{AB} = V_{in}/2$. $i_{in} = i_{Vin} + i_{Cin1}$ with the value of i_{Llk1}. i_{Cin1} is partial AC content of i_{in} depends on the reactance distribution of the input source and input capacitors. As i_{Cin1} is identical to i_{Cin2}, the midpoint voltage of C_{in1} and C_{in2} is constant during this period. v_{S1} and v_{S3} are clamped by C_{in1}, and v_{S4} and v_{S7} are clamped by C_{in2}.

In the secondary side, S_{s1}-S_{s4} are OFF; D_{o4}, D_{o5}, D_{o9} and D_{o12} are conducted; $v_{rect1} = v_{rect2} = V_{in}/(2k_T)$.

The ideal output-input voltage ratio in this mode is

$$\frac{V_o}{V_{in}} = \frac{D}{2k_T} \quad (31)$$

4. Module Failure Operation

The most important feature of the proposed converter is the redundancy ability for the primary and secondary sides. In this part, the operation principle of module failure operation is briefly described to illustrate the redundancy ability. To simplified the description, S_6 is set to be broken, which causes a primary module failure. It should be pointed out that the proposed converter can also be operated with a secondary module failure. During the module failure operation, the proposed converter can also be operated in the secondary and primary side modulation switching schemes according to the output voltage, and key waveforms are given in Figure 6. The switching scheme of the secondary side modulation is illustrated in Table 3.

Table 3. Switching scheme in the first half switching period (secondary side modulation mode).

Item	S_1	S_2	S_3	S_4	S_{s1}	S_{s2}
Stage 1	ON	OFF	OFF	ON	ON	OFF
Stage 2	OFF	OFF	OFF	OFF	ON	OFF
Stage 3	OFF	OFF	OFF	OFF	ON	OFF
Stage 4	OFF	ON	ON	OFF	ON	OFF
Stage 5	OFF	ON	ON	OFF	OFF	OFF
Stage 6	OFF	ON	ON	OFF	OFF	OFF

4.1. Secondary Side Modulation

Figures 6a and 7 show the key waveforms and operation stages of the secondary side modulation. As shown in Figure 6a, S_6 is broken due to some unknown reasons. In the primary side, S_5-S_8 are stop, and S_1-S_4 are switched in the mode which is identical to the secondary operation mode of normal operation. According to Figure 7, the input capacitor currents remain zero during stages 3 to 6, the mid-point voltage of the input capacitors are balanced during these stages. In addition, during

stages 1 and 2, the input capacitor currents are identical to partial AC content of i_{in}, thus, the mid-point voltage of the input capacitors are also balance during stages 1 and 2. Therefore, a stable mid-point voltage can be obtained during the first switching cycle, and in the secondary half switching cycle, the same conclusion can also be achieved. The primary waveforms of v_{CD}, i_{Llk1}, i_{1m} and i_{1p} are quite similar to that of the normal operation, which is not analyzed here for the sake of simplicity. The OFF voltage of the primary switches is clamped by C_{in1} and C_{in2}, which is not higher than $V_{in}/2$.

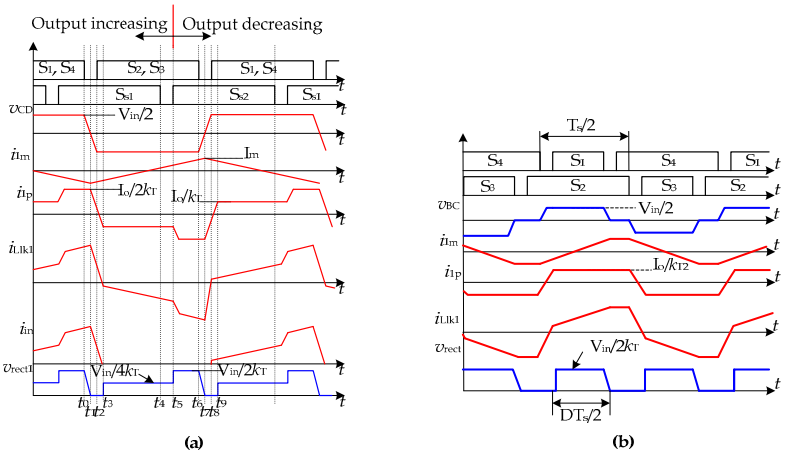

Figure 6. Key waveforms: (**a**) secondary modulation; (**b**) primary modulation.

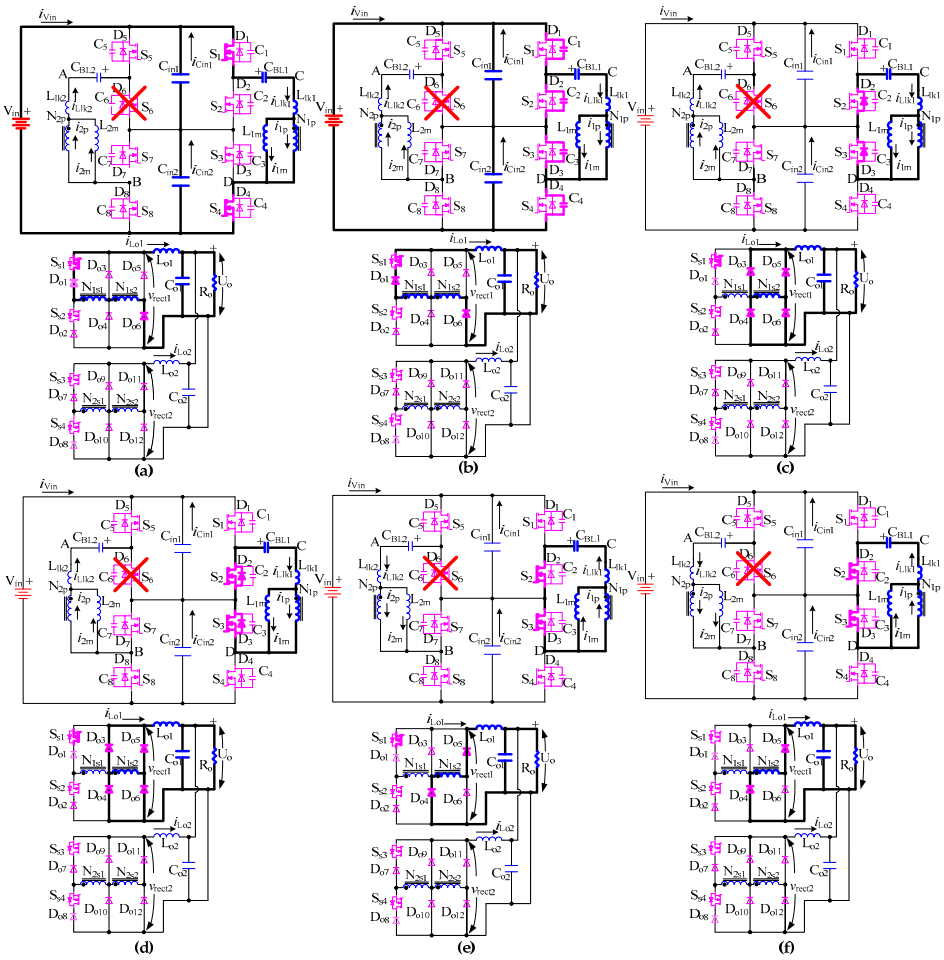

Figure 7. Stages of the secondary side modulation in failure mode: (**a**) stage 1; (**b**) stage 2; (**c**) stage 3; (**d**) stage 4; (**e**) stage 5; (**f**) stage 6.

In the secondary side, the down cell is stop, and the up cell operates in the same pattern with that of the normal operation, and detail analysis is not provided here for the sake of simplicity.

4.2. Primary Side Modulation

During the primary side operation, the proposed converter can be treated as a conventional TLDC in [8]. Figure 6b illustrates key waveforms. The output can be regulated down to zero by switching scheme in Figure 6b. The operation principle about this procedure is not provided here for the sake of simplicity and detail information can reference [8].

4.3. Output Range of the Module Failure Operation

The output voltage of the module failure mode is quite similar to that of the normal operation. When $V_{in}/k_T \geq V_o > V_{in}/2k_T$, the proposed converter is operated in the secondary side modulation, the output voltage is varied from V_{in}/k_T to $V_{in}/2k_T$ with the duty ratio D; When $V_{in}/2k_T \geq V_o > 0$, the proposed converter is operated in the primary side modulation, the output voltage is varied $V_{in}/2k_T$ to 0 with the duty ratio D.

5. Technical Analysis

5.1. ZVS of the Primary Switches

The soft switching characteristics of the normal and module failure operation are quite similar, thus, only the soft switching characteristics of the normal operation are analyzed in the following parts.

5.1.1. Secondary Side Modulation

When the converter is operated in the secondary side modulation mode, the primary switches can obtain ZVS down to zero load current with proper designing of i_{im}, $I = 1$ and 2. And the L_m should observe following equation [19]

$$L_m \leq \frac{\sqrt{3}T_s}{8}\sqrt{\frac{L_{lk}}{C_o}} \tag{32}$$

Figure 8 shows the required magnetizing inductance versus C_o, L_{lk} and T_s. It should be pointed out that I_m is irrelevant to the load current and increased with input voltage, hence, there is still enough energy stored in the leakage inductance to ensure ZVS for all primary switches under no loads or high input condition. Consequently, the proposed converter will have higher efficiency compared to its competitors under light loads and high input applications.

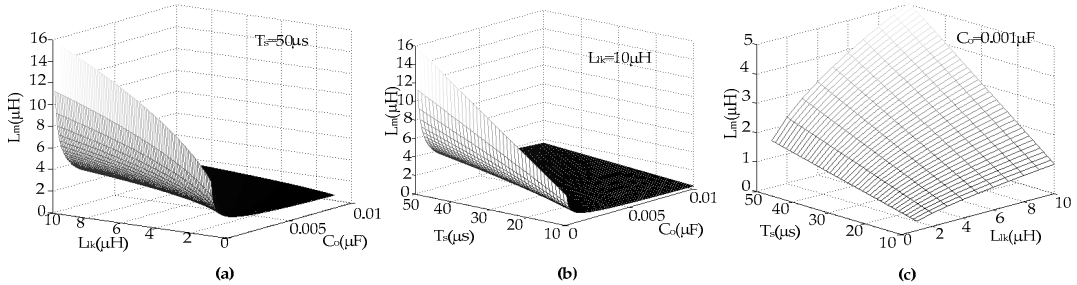

Figure 8. Required L_m to obtain ZVS versus C_o, L_{lk} and T_s: (**a**) T_s = 50 μs; (**b**) L_{lk} = 10 μH; (**c**) C_o = 0.001 μF.

5.1.2. Primary Side Modulation

During the primary side modulation, the primary switches are switched in the PS mode, S_1, S_4, S_6 and S_7 are controlled as the leading leg switches; while S_2, S_3, S_5 and S_8 are switched as the lagging leg

switches. Just as traditional PS FB converter, the leading leg switches can be switched with ZVS easily, and the ZVS criteria is

$$\frac{1}{2}L_{ip}{}'I_{Llki}{}^2 \geq \frac{C_o V_{in}{}^2}{4}, \quad i = 1,2 \tag{33}$$

where $L_{ip}{}'$ is the sum of L_{lki} and $k_T{}^2 L_{oi}$, with the help of the output inductance and magnetic inductance, these switches can be achieved ZVS down to no-load easily.

S_2, S_3, S_5 and S_8 are lagging leg switches, and with proper designing of L_{im}, i = 1 and 2, these switches can also be achieved ZVS down to no-load.

5.1.3. ZVS Load Range

The minimum ZVS load currents for the two operation modes are concluded in Table 4.

Table 4. Zero-voltage switching (ZVS) load range of the secondary and primary side modulation ($I_m = 60\% I_{p,\,rate}$).

Mode	Switches	Minimum ZVS Load Current	Added Conduction Loss (Ratio of Primary Side Rate Conduction Loss) [19]
Secondary side modulation	S_1 to S_8	0	12%
Primary side modulation	S_1, S_4, S_6 and S_7	0	112.8%
	S_2, S_3, S_5 and S_8	0	

As illustrated in Table 4, with the help of the magnetizing currents, all the primary switches can obtain ZVS down to 0 load currents, furthermore the added conduction loss in the secondary side modulation are quite smaller than that of the primary side modulation. Therefore, it is recommended that the proposed converter should be designed to operate into the secondary side modulation mode during most operation situations, and only to operate into the primary side modulation mode in some abnormal situation, such as overload, to regulated output down to zero.

5.2. ZCS of the Secondary Switches

During the secondary side modulation, all secondary switches can obtain ZCS independent of the load condition [19]. S_{s1} is selected as an example. As shown in Figure 3a, S_{s1} is on at this stage. But, the current flowing through S_{s1} is zero due to the reverse voltage applied to D_{o1}. As shown in Figure 3b, S_{se1} is switched off at zero current. Therefore, the switching loss of the secondary switches can be minimized.

5.3. Output Inductance

The reduction of the output inductance with TL secondary rectified voltage waveform has been discussed in [19]. According to these references, the required output inductance of the converters with TL secondary rectified voltage waveform is about one-third of that of conventional two-level converters. Therefore, the volume of the output filter in the proposed converter can be significantly reduced.

5.4. Voltage Balance Principle of the Input Capacitors

The initial voltage across the input capacitors is $V_{in}/2$ due to the configuration of the proposed converter. During the operation, the voltage across the input capacitors can be maintained if this capacitor can observe charge balance principle over each switching cycle. Tables 5 and 6 show the currents of the input capacitors, as proved in Tables 5 and 6, with symmetrical switching scheme, the input capacitors voltage can be stable properly. Detail descriptions have been provided in Section 3.

Table 5. Currents of the input capacitors during the secondary side modulation.

Item	Normal Operation		Module Failure Operation	
	i_{cin1}	i_{cin2}	i_{cin1}	i_{cin2}
Stage 1	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 2	$i_{Llk1} - i_{Llk2} = 0$		Partial of $\widetilde{i_{in}}$	
Stage 3	Partial of $\widetilde{i_{in}}$		0	
Stage 4	Partial of $\widetilde{i_{in}}$		0	
Stage 5	Partial of $\widetilde{i_{in}}$		0	
Stage 6	Partial of $\widetilde{i_{in}}$		0	
Stage 7	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 8	$i_{Llk1} - i_{Llk2} = 0$		Partial of $\widetilde{i_{in}}$	
Stage 9	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 10	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 11	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 12	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	

Table 6. Currents of the input capacitors during the primary side modulation.

Item	Normal Operation		Module Failure Operation	
	i_{cin1}	i_{cin2}	i_{cin1}	i_{cin2}
Stage 1	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 2	$i_{Llk1} - i_{Llk2} = 0$		i_{Llk1}	$-i_{Llk1}$
Stage 3	$i_{Llk1} - i_{Llk2} = 0$		i_{Llk1}	$-i_{Llk1}$
Stage 4	$i_{Llk1} - i_{Llk2} = 0$		i_{Llk1}	$-i_{Llk1}$
Stage 5	Partial of $\widetilde{i_{in}}$		0	
Stage 6	Partial of $\widetilde{i_{in}}$		0	
Stage 7	Partial of $\widetilde{i_{in}}$		0	
Stage 8	$i_{Llk1} - i_{Llk2} = 0$		$-i_{Llk1}$	i_{Llk1}
Stage 9	$i_{Llk1} - i_{Llk2} = 0$		$-i_{Llk1}$	i_{Llk1}
Stage 10	$i_{Llk1} - i_{Llk2} = 0$		$-i_{Llk1}$	i_{Llk1}
Stage 11	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	
Stage 12	Partial of $\widetilde{i_{in}}$		Partial of $\widetilde{i_{in}}$	

5.5. Comparison

The circuit and performance of the proposed converter and the converter in [32] are compared in this part, and the circuit of the converter for comparison is provided in Figure 1, and the detail operation principle about this converter can reference [32]. Tables 7 and 8 illustrate the components and performance comparison.

Table 7. Components comparison.

Item	Proposed	Figure 1
Primary side components		
Switches	8	8
Flying capacitors	0	1
Blocking capacitors	2	2
Input capacitors	2	2
Primary coils	2	2
Secondary side components		
Rectifier diodes	12	8
Secondary coils	4	2
Switches	4	0

Table 8. Performance comparison.

Item	Proposed	Figure 1
Voltage stress of the primary switches	$V_{in}/2$	$V_{in}/2$
Primary side redundancy ability	Yes	No
Secondary side redundancy ability	Yes	No
TL secondary rectified voltage waveform	Yes	No
Soft switching characteristics of the primary switches	Good	Normal
System dynamic response	Fast	Normal

5.5.1. Redundancy Ability

Compared to the converter in Figure 1, the redundancy ability is an obvious advantage of the proposed converter, which ensures higher system reliability. As shown in Figure 1, the primary side is built of two series connected modules, and the converter must be shut down when one primary switch is broken due to the remained switches would suffer higher voltage stress. However, as shown in Figures 6 and 7, the proposed converter can still be operated safely when one primary switch is broken.

5.5.2. Components Comparison

The primary side components number of the proposed converter is similar to that of the converter in Figure 1, and as proved in pervious sections, OFF voltage across each primary switch is directly clamped by the input capacitors, thus no added clamping device is required. The secondary structure of the proposed converter is a little complex than that of the converter in Figure 1 to achieve TL secondary rectified waveforms, which would result reduced volume of input and output filter. In addition, according to Table 8, the system dynamic response of the proposed converter is higher than that of the converter in Figure 1. As shown in Table 8, the voltage stress on the primary switches of the proposed converter and the converter in Figure 1 are identical with the value of $V_{in}/2$, thus, these two converters are well suitable for high input voltage dc-dc power conversion.

5.5.3. Soft Switching Characteristics

With proper designing, the ZVS load range of the primary switches in the proposed converter is down to zero, which is better for wide load range applications. Furthermore, the turn-off switching loss can be reduced by increasing output capacitance of the primary switches. However, as depicted in [32], the lagging switches in Figure 1 cannot achieve wide ZVS load range due to only the energy stored in the leakage inductance can be used [32]. And the turn-off switching loss cannot be optimized due to limited ZVS load range of the lagging switches. As illustrated in Table 8, the proposed converter features have better soft switching characteristics, which means higher power conversion efficiency especially under light load and high input voltage operation.

5.5.4. Power Loss

The power loss distributions of the proposed converter and the converter in Figure 1 are compared in Figure 9. The data is obtained by power analyzer (PW60001), and the converters for comparison are operated with V_{in} = 600 V and I_o = 2 A. As shown in Figure 9, the proposed converter has lower power loss due to good switching loss of MOSFETs, which is an attractive characteristic of the proposed converter. As illustrated in Figure 9, the conduction loss of the proposed converter is a little higher than that of Figure 1 due to higher magnetizing current and extra secondary MOSFETs. Therefore, the expected efficiency of the proposed converter is better.

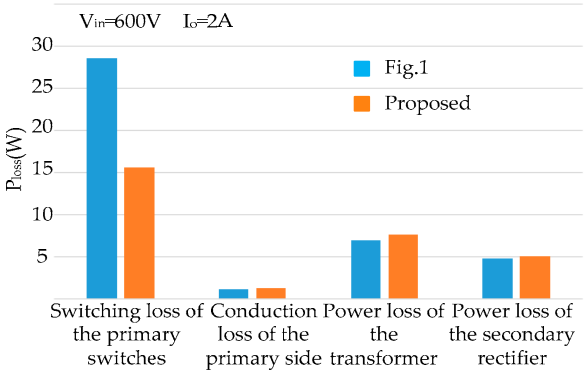

Figure 9. Power loss distribution.

6. Experimental Results

The performance of the proposed converter is verified by a 1kW prototype, and the main parameters of the prototype are provided in Table 9. Figures 10 and 11 give some experimental results. Figure 12 illustrated the prototype, and the control signals for the switches are generated by two UCC 3895s in synchronized mode. In the efficiency experiment, the power loss of control circuit and cooler system are considered. The proposed converter has several operation modes, and some key waveforms of these operation modes are quite similar. Therefore, only some typical experimental results are selected to validate the proposed converter for the sake of simplicity.

Table 9. Parameters of the prototype.

Item	Parameters
Input voltage	500–600 V
Output Voltage	250 V
Power rating	1 kW
f_s	100 kHz
Primary switches	IRFP460
k_T	3
L_{1m} and L_{2m}	300 μH
L_{o1} and L_{o2}	30 μH
C_{o1} and C_{o2}	220 μF
Secondary switches	IPP600N25N3G
Rectifier diodes	IDP18E120

As shown in Figure 10a, OFF voltage across the primary switches in the proposed converter is even in the secondary side modulation mode, and the midpoint voltage of the input capacitors is stable and equals $V_{in}/2$. Figure 10b proves the voltage stress across the primary switches and the midpoint voltage of the input capacitors is also even and stable in the primary side modulation mode.

As proved in Figure 10c, the voltage applied to the primary coils is $V_{in}/2$, and i_{Llk1} is not a constant value because i_{1m} is enlarged to help ZVS of the primary switches. As i_{1m} is not in phase with load current, the added primary RMS current is smaller. Thus, the added conduction loss is also smaller. As proved in Figure 10d, the duty ratio of v_{BC} is 100% and uncontrolled during the whole operation stages, which means zero primary circulating current.

As depicted in Figure 10e, the secondary rectified voltage is a TL waveform, which significantly reduces the volume of the output filter. The output voltage is adjusted by changing the time of high output voltage level. As there is no free-wheeling time, the input current ripple is also smaller. The voltages across the rectifier diodes are shown in Figure 10f,g.

The waveforms of the drain-source voltage and current of S_{s1} are shown in Figure 10h, and it is clearly that S_{s1} can obtain ZCS. The ZVS characteristics of the primary switches in the proposed

converter are test with zero load current. The waveforms of the gate signals and the drain-source voltage of switch S_1 is depicted in Figure 10i. In Figure 10i, the gate-source voltage of S_1 is much lower than the threshold voltage when the drain-source voltage of S_1 decreases to zero, thus, S_1 can obtain ZVS.

Figure 10j gives some experimental results of the failure mode operation, and it is similar to that of normal operation. From Figure 10j, we can conclude the proposed converter can be operated into the failure mode operation. Other waveforms in the failure mode operation is not provided in this paper for the sake of simplicity.

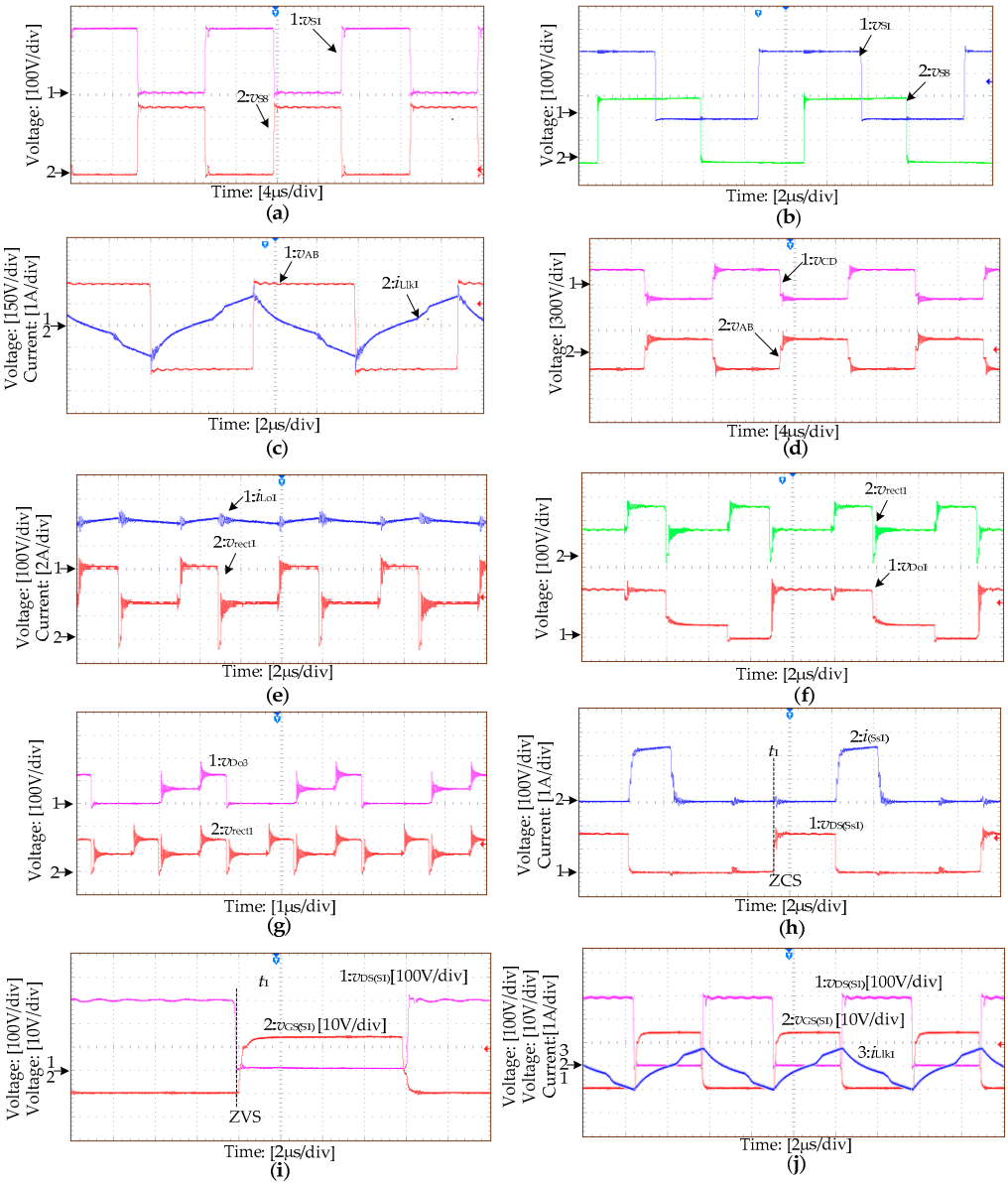

Figure 10. Experimental results: (**a**) v_{S1} and v_{S8} during the secondary side modulation (Normal operation); (**b**) v_{S1} and v_{S8} during the primary side modulation (Normal operation); (**c**) v_{AB} and i_{Llk1} during the secondary side modulation (Normal operation); (**d**) v_{CD} and v_{AB} during the secondary side modulation (Normal operation); (**e**) i_{Lo1} and v_{rect1} during the secondary side modulation (Normal operation); (**f**) v_{Do1} and v_{rect1} during the secondary side modulation (Normal operation); (**g**) v_{Do3} and v_{rect1} during the secondary side modulation (Normal operation); (**h**) ZCS of S_{s1}; (**i**) ZVS of S_1 with zero load current; (**j**) $v_{DS(S1)}$, $v_{GS(S1)}$ and i_{Llk1} during the secondary side modulation (Failure mode operation).

Figure 11a shows the efficiency comparison under different load current with 600V input voltage, and the comparison is carried out under the same base line. As all primary switches can obtain ZVS in wide load range, the proposed converter has higher efficiency with smaller load. In Figure 11b, the efficiency results under constant I_o and variable V_{in} condition are shown, and the proposed converter can obtain more optimum high input efficiency owing to the ZVS operation can still be assured with increasing of the input voltage.

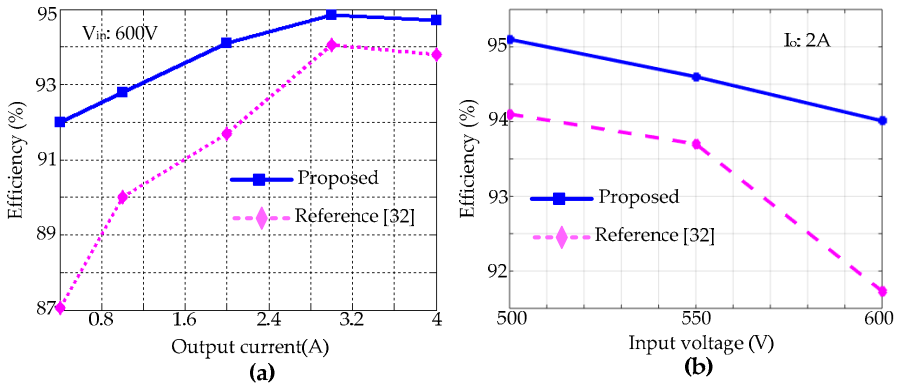

Figure 11. Efficiency comparison: (**a**) Efficiency with constant V_{in} and variable I_o; (**b**) Efficiency with constant I_o and variable V_{in}.

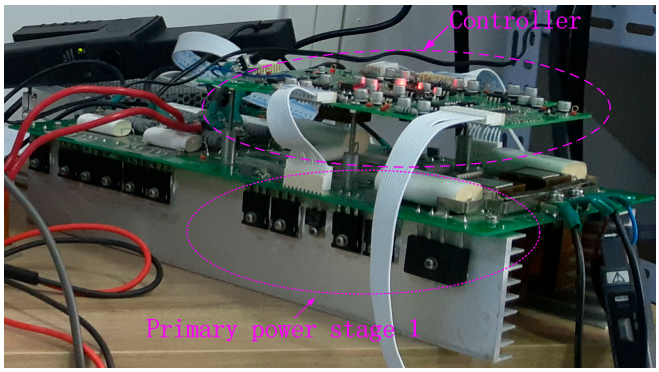

Figure 12. Photo of the prototype.

7. Conclusions

A wide load range ZVS high voltage dc-dc converter is proposed and analyzed in this paper. From above theoretical and experimental analysis, the advantages of the proposed converter can be concluded as follows: Low voltage stress on the primary switches with auto-balanced ability; Redundancy ability for the primary and secondary sides, which ensures high system reliability; Modular structure for the primary and secondary sides; Full ZVS load range for the primary switches, and less primary conduction loss is added; TL secondary rectified voltage waveform can be obtained, which reduce the volume of input and output filter size. The added secondary switches can obtain ZCS independent of the load current.

The main disadvantage of the proposed converter is that the VA rating of the transformers in the proposed converter is a little higher than that of Figure 1 under variable input and constant output condition.

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