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High-efficiency Bidirectional Buck–Boost Converter for Residential Energy Storage System

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Abstract: This paper proposes a bidirectional dc–dc converter for residential micro-grid applications. The proposed converter can operate over an input voltage range that overlaps the output voltage range. This converter uses two snubber capacitors to reduce the switch turn-off losses, a dc-blocking capacitor to reduce the input/output filter size, and a 1:1 transformer to reduce core loss. The windings of the transformer are connected in parallel and in reverse-coupled configuration to suppress magnetic flux swing in the core. Zero-voltage turn-on of the switch is achieved by operating the converter in discontinuous conduction mode. The experimental converter was designed to operate at a switching frequency of 40–210 kHz, an input voltage of 48 V, an output voltage of 36–60 V, and an output power of 50–500 W. The power conversion efficiency for boost conversion to 60 V was ≥98.3% in the entire power range. The efficiency for buck conversion to 36 V was ≥98.4% in the entire power range. The output voltage ripple at full load was <3.59 $V_{p.p}$ for boost conversion (60 V) and 1.35 $V_{p.p}$ for buck conversion (36 V) with the reduced input/output filter. The experimental results indicate that the proposed converter is well-suited to smart-grid energy storage systems that require high efficiency, small size, and overlapping input and output voltage ranges.

Keywords: dc–dc power conversion; buck/boost conversion; step up/down converter; bidirectional converter; pulse frequency modulation

1. Introduction

Distributed generation (DG) is the future of energy systems that provide system reliability and flexibility within local electric loads instead of centralized generation. DG mainly uses renewable energy sources, which provide irregular power depending on weather conditions. Therefore, to stabilize the power, DG (Figure 1) requires an energy storage system (ESS) consisting of a battery and a bidirectional converter (BDC) [1–5]. BDC is essential for the ESS because it needs to be able to charge the battery with the power supplied from DG and to transfer energy from the battery to the grid when the DG runs out of power.

The basic BDCs mainly use the combined half-bridge (CHB) and the cascade buck–boost (CBB) structures (Figure 2). The CHB converter (Figure 2a) has two power stages consisting of two half-bridge converters and a dc link capacitor C_{link} that operates as an energy-transfer unit [6–8]. One power stage performs the buck operation and the other stage performs the boost operation. An additional half-bridge converter can be connected to the C_{link} in order to use the converter as multiple inputs or outputs. The CBB converter [9–14] (Figure 2b) consists of one inductor and four switches.

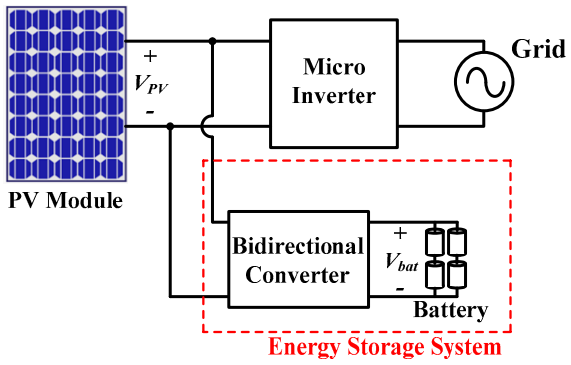


Figure 1. Photovoltaic (PV) generation using an energy storage system.

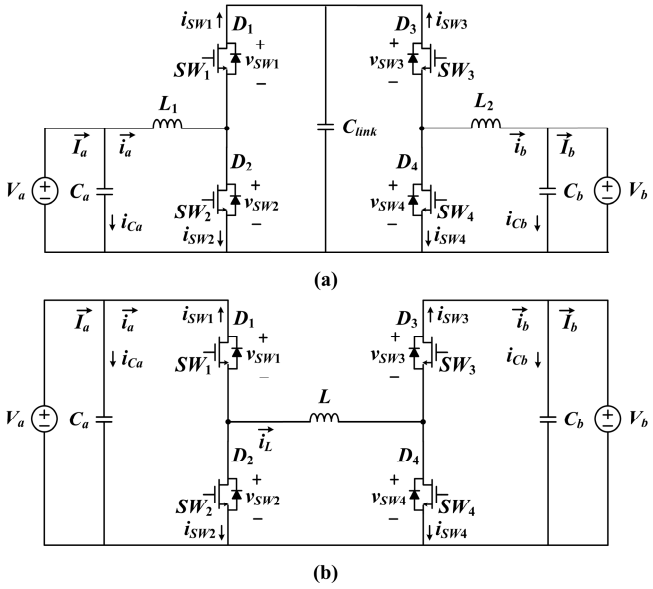


Figure 2. Circuit structures of (**a**) combined half-bridge (CHB) and (**b**) cascade buck–boost (CBB) bidirectional converters (BDCs). Figure 2a is reproduced with permission from Khan, M. A [8]; Figure 2b is reproduced with permission from Waffler, S [11].

In a similar way to CHB, the switches on the left leg are used for the buck operation and the switches on the right leg are used for the boost operation. The CBB converter can be implemented in a smaller size to the CHB converter because it uses only one inductor. These converters have simple structure and control method, but they have some drawbacks because the converter must be operated in discontinuous conduction mode (DCM) at full load for zero voltage turn-on. Further, (1) if the converter is operated at a fixed frequency, the inductor reverse current increases under light load conditions, increasing conduction losses; (2) the current ripple in the inductor causes core loss and increases output voltage ripple; and (3) the high-frequency operation of the converter is undesirable because the turn-off switching loss is significantly increased when the converter is not operating in DCM.

The converter of [15] used an inverse coupled 1:1 transformer and pulse-frequency modulation to solve the above problems. The converter consists of a 1:1 transformer, a dc-blocking capacitor C_b, a snubber capacitor C_s, and two switches SW_1 and SW_2 (Figure 3). The windings of the transformer are connected in a series-aiding configuration to minimize ripple of the magnetizing current i_{Lm}, which causes major core losses. C_s reduces the switching loss by lowering the turn-on and turn-off slopes of the switch voltages. The converter of [15] can improve the efficiency and operate at high switching frequency because the 1:1 transformer and C_s reduce the core loss and switching loss.

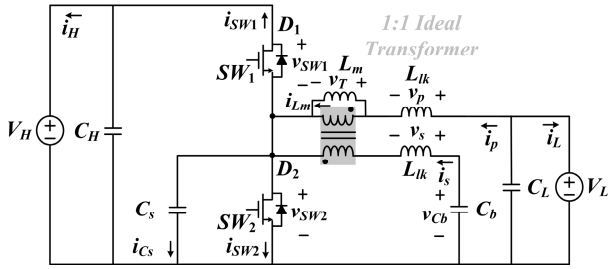


Figure 3. Circuit structure of the converter of [15]. Adapted from Choi, Y.G [15].

However, despite these advantages, the converter of [15] is difficult to use in ESSs. The circuit of [15] assumes $V_H > V_L$—that is, that the direction of the buck conversion is from left to right and the direction of the boost conversion is from right to left. Therefore, this converter cannot be used when the input voltage range overlaps with the output voltage range. A typical PV–ESS system for home applications has been built using PV panels with an operating voltage range of 25–50 V [16–18] and batteries with an operating voltage range of 42–58.8 V [19–21]. For a given solar irradiation dose, the converter of the PV–ESS system adjusts the switching duty D to convert the PV voltage $V_{PV} = V_{IN}$ to the battery charge voltage $V_{bat} = V_O$. For the buck conversion, V_{PV} decreases as D increases because the converter draws more current from the input filter capacitor C_{IN}. The photovoltaic power P_{PV} increases as V_{PV} decreases until V_{PV} reaches the maximum power point (MPP) voltage V_{MPP} (Figure 4); further reduction of V_{PV} reduces P_{PV}. MPP moves when the solar irradiation on the PV panel changes. For $V_{MPP} < V_{bat} < V_{OC}$, the range of the maximum power point tracking (MPPT) operation for the circuit of [15] is limited to $V_{bat} < V_{PV} < V_{OC}$ (Figure 4a). When 25 V $< V_{PV} <$ 50 V and 42 V $< V_{bat} <$ 58.8 V (i.e., the general operation range of PV–ESS), the circuit of [15] has to use three series-connected PV panels and one battery for buck mode operation, or one PV panel and two-series connected batteries for boost mode operation. Serially connected batteries have a balancing problem. Separate MPPT control is not possible for serially connected PV panels, which means that optimum MPPT efficiency cannot be achieved.

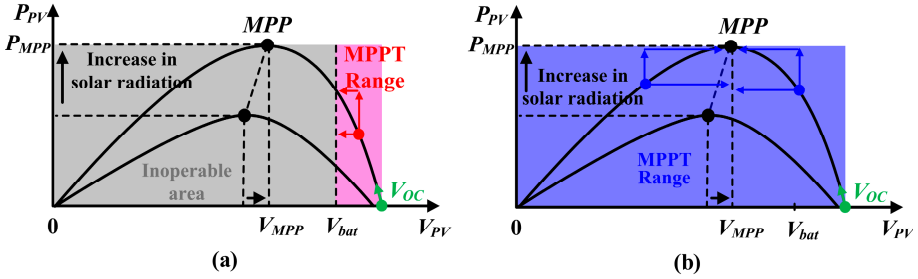


Figure 4. Maximum power point tracking (MPPT) range of (**a**) the converter of [15] and (**b**) the proposed CBB BDC for $V_{MPP} < V_{bat} < V_{PV}$.

To improve the aforementioned drawbacks of the existing converters, this paper proposes a CBB BDC circuit structure that is suitable for use in ESS for distributed generation. The proposed CBB BDC (Figure 5) uses the CBB BDC circuit in [10] as a basic structure, reduces the core loss by using a 1:1 transformer, decreases switching losses by using two small snubber capacitors C_{s1} and C_{s2}, and reduces filter size by using a dc-blocking capacitor C_B. Unlike the converter of [15], the proposed converter can have a MPPT range of $0 < V_{PV} < V_{OC}$, regardless of V_{bat} (Figure 4b), because the proposed CBB BDC works well for both $V_{IN} > V_O$ and $V_{IN} \leq V_O$. Therefore, the proposed circuit is suitable for PV–ESS, which requires high efficiency in the condition of overlapping input and output range. The circuit is controlled using pulse-frequency modulation (PFM) combined with pulse-width modulation (PWM), the load variation is accommodated using PFM, and the voltage gain is adjusted using PWM. The circuit structure, principle of operation, and design considerations of the proposed circuit are described

in Section 2. A digital controller is given in Section 3. Experimental results are given in Section 4. Conclusions are given in Section 5.

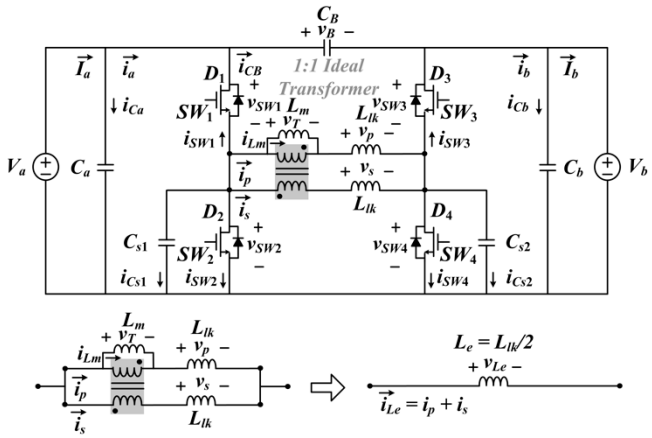


Figure 5. Circuit structure of the proposed CBB BDC.

2. Proposed Cascade Buck–Boost Bidirectional DC–DC Converter

2.1. Circuit Structure

The proposed CBB BDC (Figure 5) is composed of a 1:1 transformer; three capacitors C_{s1}, C_{s2}, and C_B; and four switches SW_1–SW_4. The transformer replaces the boost/buck inductor L in the conventional CBB BDC (Figure 2b), and it is modeled with a 1:1 ideal transformer, a magnetizing inductance L_{m}, and two leakage inductances L_{ik} that have the same value. To minimize ripple in the magnetizing current i_{Lm}, which causes major core losses, the windings of transformer are connected in parallel and in reverse-coupling configuration. In this configuration, $i_{Lm} = 0$ because the primary current i_p of the 1:1 transformer equals the secondary current i_s. C_{s1} and C_{s2} reduce the switching loss; they charge/discharge during the switch dead-time periods that enable the switches to have zero voltage switching (ZVS) turn-on and turn-off. The switching loss is reduced significantly, so the switching frequency f_s can be increased to reduce the conduction loss when load is light. C_B reduces the filter size by providing a bypass path for the transformer current.

2.2. Reduction of Core Loss

When the windings of the 1:1 transformer are connected in parallel and in reverse coupling configuration [15], the transformer satisfies the following equations:

$$L_{lk}\frac{di_p}{dt} - v_T = L_{lk}\frac{di_s}{dt} + v_T,$$

$$v_T = L_m\frac{di_{Lm}}{dt},$$

$$i_{Lm} = i_p - i_s.$$

These equations yield $v_T = 0$. Thus, the transformer can be represented with an equivalent inductance $L_e = L_{lk}/2$ (Figure 5).

The Steinmetz equation [22]

$$P_c = a f_s^c B_{ac}^d V_e$$

is used to estimate the core loss P_c, where a, c, and d are Steinmetz's constants, B_{ac} is the ac ripple field in the core, and V_e is the effective core volume. The inductor of the conventional CBB has

$$B_{ac} = \mu_0\mu_e N(I_{peak} - I_{avr})/l_e,$$

where μ_0 is the vacuum permeability, $\mu_e = (\mu_r l_e)/(S_a \mu_r + l_e)$ is the effective relative permeability, l_e is the mean magnetic path length, S_a is the air-gap length, I_{peak} is the peak current, and I_{avr} is the average current.

In the 1:1 transformer of the proposed circuit, the windings are connected in parallel and in reverse-coupling configuration, so there is no magnetic flux that passes only through the core. Each winding produces flux lines that pass through the window area of the core. Since the flux passes through a much longer air path, the 1:1 transformer has a much lower μ_e than the inductor of the conventional CBB BDC. As discussed in Section 2.5, the experimental converter uses an inductor (or 1:1 transformer) of L_e = 5.25 µH to operate at V_a = 48 V, V_b = 60 V, P_b = 500 W and f_S = 64 kHz. The inductor (or 1:1 transformer) was fabricated using the ETD 34 core from Magnetics Co., which has V_e = 7.64 cm^3, μ_r = 3000, and a core-window length $l_w \approx$ 7.5 mm. The core parameters resulted in l_e ≈ 3.9 cm and μ_e = 5 for the 1:1 transformer and $l_e \approx$ 7.8 cm and μ_e = 345 for the inductor, with an air gap S_a = 0.2 mm. To obtain L_e = 5.25 µH, the 1:1 transformer and inductor required N = 15 and 3, respectively. These core and winding parameters resulted in B_{ac} = 0.002 T for the 1:1 transformer and B_{ac} = 0.25 T for the inductor, and the Steinmetz equation yielded P_c = 1 mW for the 1:1 transformer and P_c = 5.2 W for the inductor. This result shows that even with a slight increase in the winding loss, the proposed converter can significantly reduce the core loss by storing most of the magnetic energy in the window area.

2.3. Principle of Operation

The proposed converter has four switching states (Table 1) depending on directions and modes of energy conversion. For given V_a and V_b, the switching state is the same for forward ($V_a \rightarrow V_b$) and backward ($V_b \rightarrow V_a$) conversions, so here the converter is analyzed for forward conversion only. To simplify analysis, $f_s = 1/T_s$ is assumed to be constant, although the converter uses PFM to accommodate for load variation.

Table 1. Switching states of the proposed converter.

Conversion Direction	Operating Mode	SW_1	SW_2	SW_3	SW_4
$V_a \rightarrow V_b$	*Boost*	1	0	1 – D	D
	Buck	D	1 – D	1	0
$V_b \rightarrow V_a$	*Boost*	D	1 – D	1	0
	Buck	1	0	1 – D	D

2.3.1. Boost Forward-Conversion ($V_a < V_b$)

For boost forward-conversion, SW_1 remains ON and SW_2 remains OFF. All switching cycles consist of four sequential modes, each with theoretical waveforms (Figure 6) and equivalent circuits (Figure 7).

Initially, $v_{SW4} = 0$ V, $i_{SW4} < 0$, and the body diode D_4 of SW_4 is turned on. The first mode (*Mode* 1, Figure 7) begins at $t = t_0$ by turning on SW_4, and ends at $t = t_1$ by turning off SW_4. The inductor current is given by

$$i_{Le}(t) = i_{Le}(t_0) + \frac{V_a}{L_e}(t - t_0), \tag{1}$$

because $v_{Le} = V_a$, where $i_{Le}(t_0)$ is the initial inductor current. The filtered output current $I_b = i_b - i_{Cb}$, the unfiltered output current $i_b = i_{CB} = -C_B dV_b/dt$, and the current of the output filter capacitor $i_{Cb} = C_b(dV_b/dt)$, so

$$i_{CB}(t) = i_b(t) = \frac{C_B}{C_B + C_b} I_b, \tag{2}$$

where i_{CB} is the current of dc-blocking capacitor C_B.

The second mode (*Mode* 2, Figure 7) begins at $t = t_1$ by turning off SW_4. During this mode, C_{s2} charges quickly from 0 V to V_b through L_e. Since

$$i_{Cs2}(t) \approx i_{Le}(t_1) = i_{Le}(t_0) + \frac{V_a}{L_e}(t_1 - t_0),$$

the time required to charge C_{s2} fully is

$$t_2 - t_1 = \frac{C_{s2}V_b}{i_{Le}(t_0) + V_a(t_1 - t_0)/L_e};$$

$t_2 - t_1 << 2\pi(C_{s2}L_e)^{1/2}$ is required to prevent oscillation between L_e and C_{s2}. *Mode* 2 ends at $t = t_2$ where the body diode D_3 of SW_3 turns on, so ZVS of SW_3 is possible.

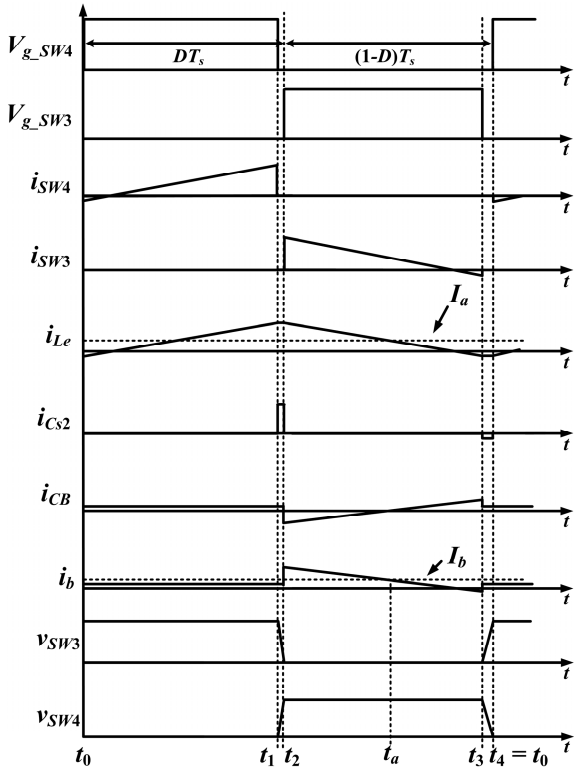


Figure 6. Voltage and current waveforms of the proposed converter for boost forward-conversion.

The third mode (*Mode* 3, Figure 7) begins at $t = t_2$ where D_3 turns on, and SW_3 turns on subsequently. Here, $i_{Le}(t_1) \approx i_{Le}(t_2)$, $v_{SW4} = V_b$, and $v_{Le} = V_a - V_b$, so $i_{Le}(t)$ is given by

$$i_{Le}(t) = i_{Le}(t_1) + \frac{(V_a - V_b)}{L_e}(t - t_2). \tag{3}$$

i_{CB} and i_b are calculated using $i_b = i_{Le} + i_{CB} = i_{Cb} + I_b$ and $i_{Cb} = C_b i_{CB}/C_B$ as:

$$i_{CB}(t) = \frac{C_B}{C_B + C_b}[I_b - i_{Le}(t)], \tag{4}$$

$$i_b(t) = \frac{C_b}{C_B + C_b} i_{Le}(t) + \frac{C_B}{C_B + C_b} I_b. \tag{5}$$

Mode 3 ends at $t = t_3$ by turning off SW_3.

The last mode (*Mode* 4, Figure 7) begins at $t = t_3$. During this mode, C_{s2} discharges quickly from V_b to 0 V by i_{Le}. Since

$$i_{Cs2}(t) \approx i_{Le}(t_3) = i_{Le}(t_1) + \frac{(V_a - V_b)}{L_e}(t_3 - t_2), \tag{6}$$

the time required to charge C_{s2} fully is

$$t_4 - t_3 = \frac{-C_{s2}V_b}{i_{Le}(t_1) + (V_a - V_b)(t_3 - t_2)/L_e}; \tag{7}$$

$t_4 - t_3 << 2\pi(C_{s2}L_e)^{1/2}$ is required to prevent oscillation between L_e and C_{s2}. *Mode* 4 ends at $t = t_4$ where D_4 turns on, so ZVS of SW_4 is possible.

After setting $t_2 - t_0 \approx t_1 - t_0 = DT_s$ and $t_4 - t_2 \approx t_3 - t_2 = (1 - D)T_s$, the voltage conversion ratio V_b/V_a is obtained using (1) and (3) as

$$\frac{V_b}{V_a} \cong \frac{1}{1 - D}, \tag{8}$$

which is the same as the voltage conversion ratio of the conventional boost converter.

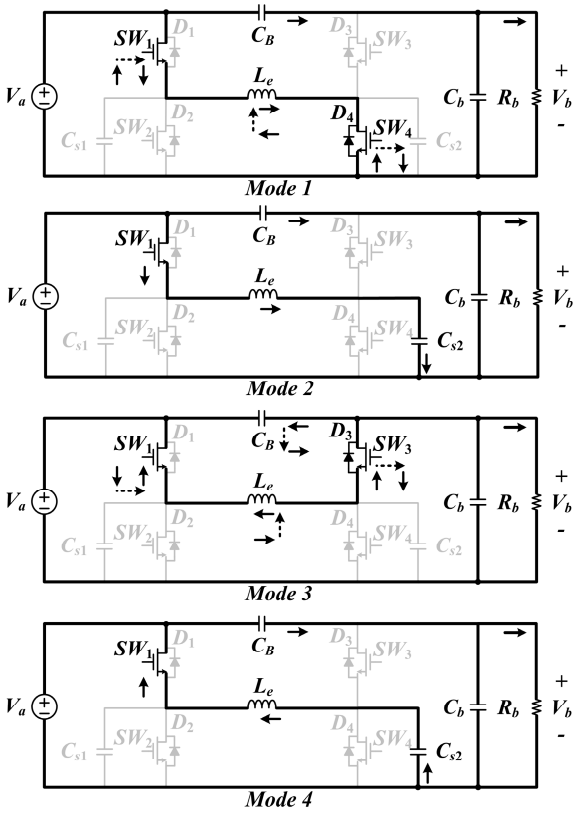


Figure 7. Circuit diagrams for the modes of operation for boost forward-conversion.

2.3.2. Buck Forward-Conversion ($V_a > V_b$)

For buck forward-conversion, SW_3 remains ON and SW_4 remains OFF. Like the boost forward-conversion, all switching cycles consist of four sequential modes, each with theoretical waveforms (Figure 8) and equivalent circuits (Figure 9). For each mode of operation, SW_1 and SW_2 for buck forward-conversion operate like SW_4 and SW_3 for boost forward-conversion, respectively.

Initially, $v_{SW1} = 0$ V, $v_{SW2} = V_a$, $i_{SW1} > 0$ A, and the body-diode D_1 of SW_1 is turned on. The first mode (*Mode* 1, Figure 9) begins at $t = t_0$ by turning on SW_1, and ends at $t = t_1$ by turning off SW_1. $v_{Le} = V_a - V_b$ in this mode, so

$$i_{Le}(t) = i_{Le}(t_0) + \frac{(V_a - V_b)}{L_e}(t - t_0). \tag{9}$$

Since $i_b = i_{Cb} + I_b$, $i_{Cb} = -C_b i_{CB}/C_B$ and $i_b = i_{Le} + i_{CB}$,

$$i_{CB}(t) = \frac{C_B}{C_B + C_b}[I_b - i_{Le}(t)] \tag{10}$$

and

$$i_b(t) = \frac{C_b}{C_B + C_b} i_{Le}(t) + \frac{C_B}{C_B + C_b} I_b. \tag{11}$$

The second mode (*Mode* 2, Figure 9) begins at $t = t_1$ by turning off SW_1. During this mode, C_{s1} discharges quickly from the input voltage V_a to 0 V through L_e. Since

$$i_{Cs1}(t) \approx i_{Le}(t_1) = i_{Le}(t_0) + \frac{(V_a - V_b)}{L_e}(t_1 - t_0),$$

the time required to charge C_{s1} fully is

$$t_2 - t_1 = \frac{C_{s1} V_a}{i_{Le}(t_0) + (V_a - V_b)(t_1 - t_0)/L_e}.$$

Mode 2 ends at $t = t_2$ where $v_{SW2} = 0$ V and the body diode D_2 of SW_2 turns on, so ZVS of SW_2 is possible.

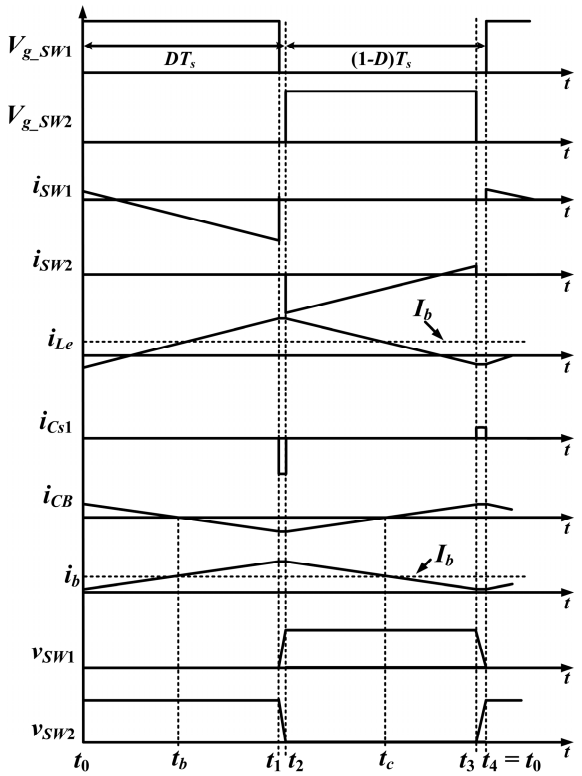


Figure 8. Voltage and current waveforms of the proposed converter for buck forward-conversion.

The third mode (*Mode* 3, Figure 9) begins at $t = t_2$ by turning on SW_2. During this mode $i_{Le}(t_1) \approx i_{Le}(t_2)$ and $v_{SW2} = 0$ V, so

$$i_{Le}(t) = i_{Le}(t_1) - \frac{V_b}{L_e}(t - t_2). \tag{12}$$

i_{CB} and i_b are obtained using $i_{Cb} = -C_b i_{CB}/C_B$ and $i_b = i_{Le} + i_{CB} = i_{Cb} + I_b$ as

$$i_{CB}(t) = \frac{C_B}{C_B + C_b}[I_b - i_{Le}(t)], \tag{13}$$

$$i_b(t) = \frac{C_b}{C_B + C_b} i_{Le}(t) + \frac{C_B}{C_B + C_b} I_b. \tag{14}$$

Mode 3 ends at $t = t_3$ by turning off SW_2.

The last mode (*Mode* 4, Figure 9) begins at $t = t_3$. During this mode, $v_{SW2} = 0$ V at $t = t_3$ and $i_{Le} < 0$ A. C_{s1} charges quickly from 0 V to V_a by i_{Le}. Since

$$i_{Cs1}(t) \approx i_{Le}(t_3) = i_{Le}(t_1) - \frac{V_b}{L_e}(t_3 - t_2),$$

the time required to charge C_{s1} fully is

$$t_4 - t_3 = \frac{-C_{s1} V_a}{i_{Le}(t_1) - V_b(t_3 - t_2)/L_e}.$$

Mode 4 ends at $t = t_4$ where D_1 turns on, so ZVS of SW_1 is possible.

After setting $t_2 - t_0 \approx t_1 - t_0 = DT_s$ and $t_4 - t_2 \approx t_3 - t_2 = (1 - D)T_s$, the voltage conversion ratio V_b/V_a is obtained using (9) and (12) as:

$$\frac{V_b}{V_a} \cong D. \tag{15}$$

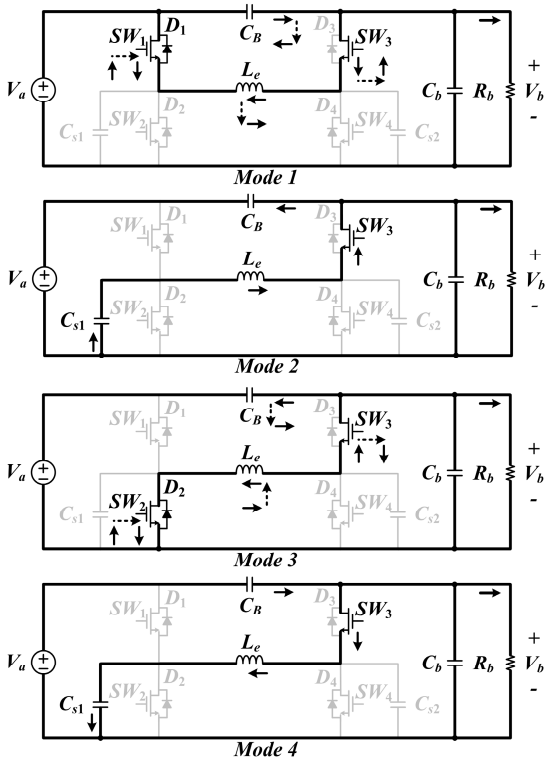


Figure 9. Circuit diagrams for the modes of operation for buck forward-conversion.

2.4. Output Voltage Ripple

The output voltage ripple ΔV_b for the boost forward-conversion is given by

$$\Delta V_b = \frac{1}{C_b}\int_{t_2}^{t_a} i_{Cb}(t)dt, \tag{16}$$

where t_a is the time at which $i_b = I_b$. Using (1), (3), (5) and $i_{Cb} = i_b - I_b$, i_{Cb} during *Mode* 3 is calculated as:

$$i_{Cb}(t) = \frac{C_b}{C_B + C_b}\left[I_a + \frac{V_a}{2L_e}DT_S + \frac{V_a - V_b}{L_e}(t - t_2) - I_b\right], \tag{17}$$

so

$$t_a = t_2 + \frac{(I_a - I_b)L_e + V_a DT_S/2}{V_b - V_a}. \tag{18}$$

ΔV_b is obtained using (16)–(18) as

$$\Delta V_b = \frac{[(I_a - I_b)L_e + V_a DT_S/2]^2}{2L_e(C_B + C_b)(V_b - V_a)}. \tag{19}$$

For the buck forward-conversion, i_{Cb} for $t_0 \le t \le t_2$ is obtained using (9), (11), and $i_{Cb} = i_b - I_b$ as:

$$i_{Cb}(t) = \frac{C_b(V_a - V_b)}{L_e(C_B + C_b)}\left[(t - t_0) - \frac{DT_S}{2}\right], \tag{20}$$

and i_{Cb} for $t_2 \le t < t_4$ is obtained using (12), (14), and $i_{Cb} = i_b - I_b$, i_{Cb} as

$$i_{Cb}(t) = \frac{C_b}{C_B + C_b}\left[\frac{-V_b}{L_e}(t - t_2) + \frac{V_a - V_b}{2L_e}DT_S\right]. \tag{21}$$

In Figure 9, $i_{Cb}(t) = 0$ at $t = t_b$ and t_c. t_b is calculated using (20) as:

$$t_b = t_0 + \frac{DT_S}{2}, \tag{22}$$

and t_c is calculated using (15) and (21) as

$$t_c = t_2 + \frac{(1 - D)T_S}{2}. \tag{23}$$

Thus, Equations (20)–(23) yield

$$\Delta V_b = \frac{1}{C_b}\int_{t_b}^{t_c} i_{Cb}(t)dt = \frac{(V_a - V_b)DT_S{}^2}{8L_e(C_B + C_b)}. \tag{24}$$

The proposed converter has $C_b = C_a$ so that it has the same output voltage ripple for both the forward and backward conversions. The ΔV_b vs. C_b (Figure 10) for forward conversion are calculated using a circuit simulator at V_a = 48 V, V_b = 60 V, D = 0.2, f_s = 64 kHz, $L_e = L$ = 5.25 μH, 10 μF ≤ C_B ≤ 30 μF, and P_b = 500 W. The proposed converter has ΔV_b = 2.44% at C_B = 30 μF, $C_a = C_b$ = 10 μF, but the conventional CBB (Figure 2b) has the same ΔV_b at $C_a = C_b$ = 40 μF. Capacitors C_a, C_b, and C_B act as input/output filters, so the proposed converter can have a smaller filter than the conventional CBB.

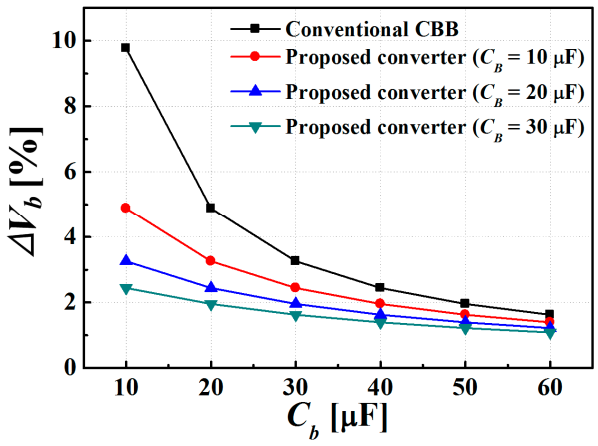


Figure 10. ΔV_b vs. C_b calculated using a circuit simulator at V_a = 48 V, V_b = 60 V, and P_b = 500 W.

2.5. Design Considerations

For boost forward-conversion, the condition $i_{Le}(t_0) < 0$ is required to turn on D_4 (i.e., to turn on SW_4 under a ZVS condition). $i_{Le}(t_0)$ is calculated using (1) and (3) as

$$i_{Le}(t_0) \approx I_a - \frac{V_a}{2L_e}DT_s = I_a + \frac{(V_a - V_b)}{2L_e}(1-D)T_s,$$

which yields

$$L_e < \frac{V_a}{2I_a}DT_s \tag{25}$$

For buck forward-conversion, the condition $i_{Le}(t_0) < 0$ and Equations (9) and (12) yields

$$L_e < \frac{(V_a - V_b)}{2I_b}DT_s. \tag{26}$$

When the converter operates at V_a = 48 V, 0.15 ≤ D ≤ 0.85, 36 V ≤ V_b ≤ 60 V, 40 kHz ≤ f_s ≤ 210 kHz, 1.04 A ≤ I_a ≤ 10.4 A and 0.83 A ≤ I_b ≤ 13.9 A, the conditions (25) and (26) are satisfied when L_e < 7.2 μH.

The 1:1 transformer was fabricated using an ETD 34 ferrite core from Magnetics Co. (Table 2), which has a window width W_w = 2.6 cm, an air-gap length S_a = 0.1 mm, a mean-length-per-turn MLT = 5.8 cm, and a space S = 1.7 cm between adjacent windings. L_e for a turns-number N = 15 is calculated as [15]:

$$L_e = \frac{\mu_0\mu_a N^2(MLT)(S+S_a)}{2W_w} = 5.39\ \mu\text{H},$$

where μ_0 is the vacuum permeability and μ_a = 1 is the relative permeability of the air gap; the actual transformer for experiments had L_e = 5.25 μH.

The C_B conditions for the allowed output voltage ripple ΔV_b are calculated using (19) and (24) as:

$$C_B > \frac{[(I_a - I_b)L_e + V_aDT_S/2]^2}{2L_e\Delta V_b(V_b - V_a)} - C_b$$

for boost forward-conversion, and

$$C_B > \frac{(V_a - V_b)DT_S{}^2}{8L_e\Delta V_b} - C_b$$

for buck forward-conversion. Allowing $\Delta V_b < 0.1V_b$, these conditions yield $C_B + C_b \geq 37.2$ μF for L_e = 5.25 μH under the aforementioned operating conditions. The experimental converter had $C_B = C_b$ = 20 μF.

Table 2. Magnetic data for transformer design.

Magnetic Data	Symbol	Value
Ferrite core type	-	ETD 34 (F material)
Relative permeability	μ_r	3000
Usable frequency	f	<1.5 MHz
Curie temperature	T_{Curie}	>210 °C
Power loss (in sine wave)	PL	70 mW/cm^3
Window width	W_w	2.6 cm
Effective cross-sectional area	A_c	0.97 cm^2
Mean magnetic path length	l_e	7.8 cm
Effective volume	V_e	7.65 cm^3
Steinmetz constants	*a*/*c*/*d*	0.0573/1.66/2.68

C_{s2} discharges by i_{Le} during *Mode* 4 of boost forward-conversion. The time required to discharge C_{s2} from V_b to 0 V is $|C_{s2}V_b/i_{Le}|$, so the allowed dead-time of switches is $\left|C_{s2}V_b/i_{Le}\right|+t_{d,off} < T_s/10$, where $t_{d,off}$ is the turn-off delay of SW_3. The turn-off transient t_f of SW_3 should be $<< |C_{s2}V_b/i_{Le}|$ to reduce the turn-off switching loss. Using (1), (3), (8), and $i_{Le}(t_3) \approx I_a - V_aDT_s/2L_e$, these requirements are represented as a design constraint for C_{s2}:

$$\left|\frac{I_a}{V_b} - \frac{(1-D)DT_s}{2L_e}\right| t_f << C_{s2} < \left|\frac{I_a}{V_b} - \frac{(1-D)DT_s}{2L_e}\right| (\frac{T_s}{10} - t_{d,off}). \quad (27)$$

During *Mode* 4 of buck forward-conversion, C_{s1} charges by i_{Le} and the time t_c required to charge C_{s1} from 0 V to V_a is $t_c = |C_{s1}V_a/i_{Le}|$. Using (9), (12), (15), and $i_{Le}(t_3) \approx I_b - V_b(1-D)T_s/2L_e$, the requirement $t_f << t_c < T_s/10 - t_{d,off}$ for SW_1 is represented as a design constraint for C_{s1}:

$$\left|\frac{I_b}{V_a} - \frac{(1-D)DT_s}{2L_e}\right| t_f << C_{s1} < \left|\frac{I_b}{V_a} - \frac{(1-D)DT_s}{2L_e}\right| (\frac{T_s}{10} - t_{d,off}). \quad (28)$$

The switches for the experiment (IPP200N15N3 nMOSFET, Infineon) had t_f = 6 ns and $t_{d,off}$ = 23 ns. The design constraints (27) and (28) yielded 0.2 nF << C_{s1} < 8.2 nF and 0.4 nF << C_{s2} < 11 nF for V_a = 48 V, 36 V ≤ V_b ≤ 60 V, 0.15 ≤ D ≤ 0.85, 40 kHz ≤ f_s ≤ 210 kHz, 1.04 A ≤ I_a ≤ 10.4 A, and 0.83 A ≤ I_b ≤ 13.9 A; the converter had $C_{s1} = C_{s2}$ = 2.2 nF.

3. Digital Controller

The control circuit (Figure 11) was implemented on a digital signal processor (DSP, TMS320F28335, Texas Instruments). The circuit controls the direction of energy transfer: Forward (Flag_ConStart = 1, D_mode = 1, $V_a \rightarrow V_b$) and backward (Flag_ConStart = 1, D_mode = 0, $V_b \rightarrow V_a$) directions. The circuit also determines switching duties D_{SW1}–D_{SW4} for SW_1–SW_4 such that $D_{SW1} = 1$, $D_{SW2} = 0$, $D_{SW3} = 1 - D$, and $D_{SW4} = D$ for $V_a < V_b$; and $D_{SW1} = D$, $D_{SW2} = 1 - D$, $D_{SW3} = 1$, and $D_{SW4} = 0$ for $V_a > V_b$. The inputs to the circuit are V_a, I_a, V_b, I_b, two reference voltages $V_{a,ref}$ and $V_{b,ref}$, two limit voltages $V_{a,lim}$ and $V_{b,lim}$, two limit currents $I_{a,lim}$ and $I_{b,lim}$, and a reference duty D_{ref}. The proportional-integral (PI) controller set $V_{PI,ref} = V_{b,ref}$ and $V_{PI} = V_b$ for forward-conversion, or $V_{PI,ref} = V_{a,ref}$ and $V_{PI} = V_a$ for backward-conversion. The PI controller calculates the error $V_{PI,ref}$ - V_{PI} and produces the PI output $U[n]$. Then, after $D[n] = U[n]+D_{ref}$ is calculated, $D[n]$ is multiplied by the switching period $T_s[n]$ to produce a PWM reference duty $Ref[n]$; $Ref[n]$ is the non-inverting input to the comparator that adjusts D to keep the voltage gain constant.

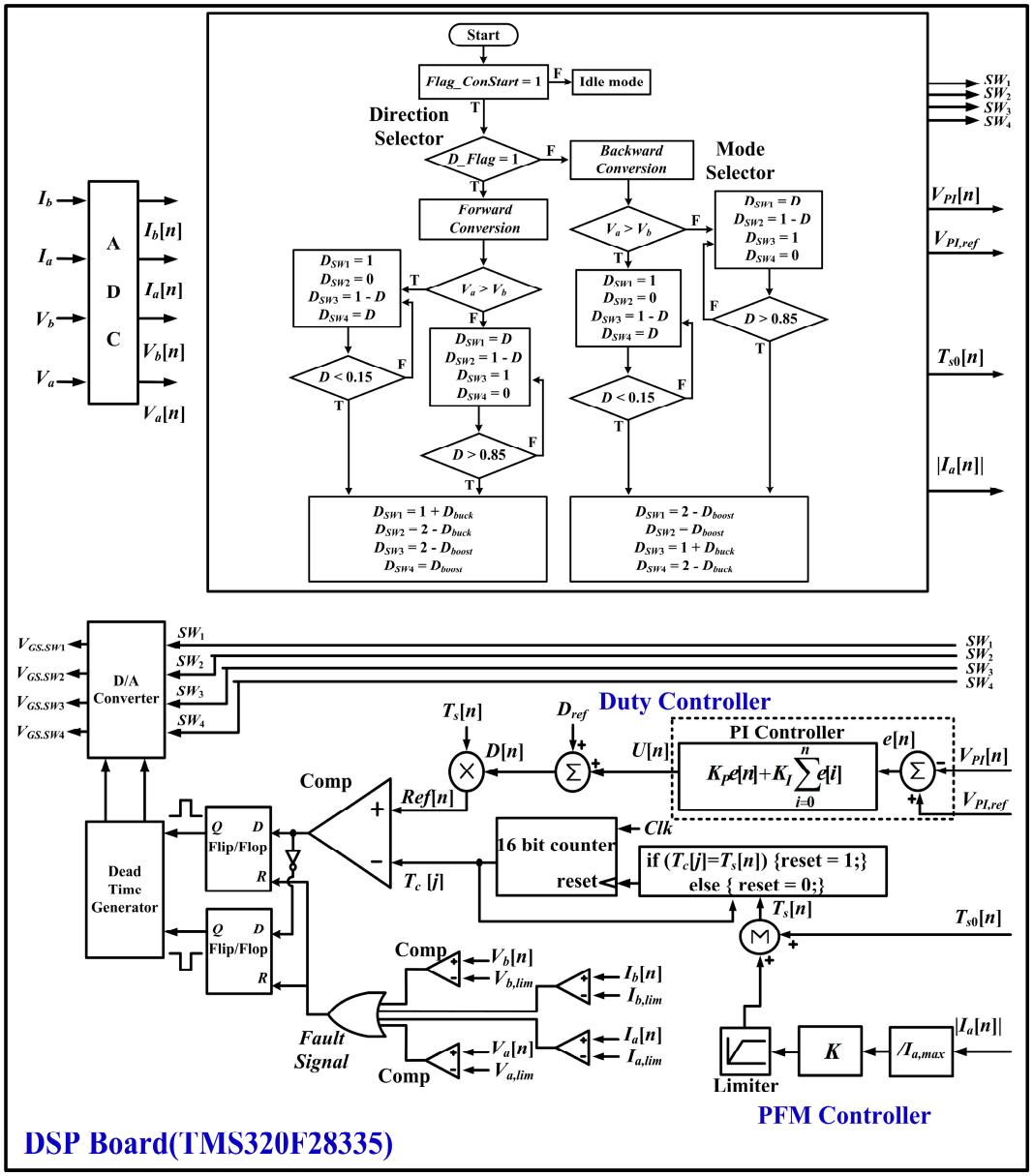


Figure 11. Block diagram of the digital controller. DSP: digital signal processor; PFM: pulse-frequency modulation.

The PFM controller calculates the switching period $T_s[n] = T_{s,min} + K|I_a|/I_{a,max}$ (where K is a constant, $T_{s,min}$ is the lowest switching period, and $I_{a,max}$ is the highest value of I_a), then resets the 16-bit counter when the counter output $T_c(j) = T_s[n]$. The converter must operate at 110 kHz $\leq f_s \leq$ 330 kHz, so the range of $T_s[n]$ was determined as $454 \leq T_s[n] \leq 1363$ for the clock frequency of the counter f_{clk} = 150 MHz. As the ratio V_b/V_a increases, f_s that ensures ZVS under full load decreases for the buck conversion but increases for the boost conversion. Therefore,

$$K = \frac{D}{\beta D_{\max}} T_{s.\max} - T_{s.\min} \tag{29}$$

for buck conversion and

$$K = \frac{1-D}{\beta(1-D_{\min})} T_{s.\max} - T_{s.\min} \tag{30}$$

for boost conversion, where β is a constant to adjust the slope of the frequency change ($D_{\min}$ = 0.15, $D_{\max}$ = 0.85, and β = 1 for buck- or boost-mode control).

When V_b/V_a is close to 1, the dead time prevents the converter from regulating the output voltage properly by using only buck-mode or boost-mode control. This problem was solved using a buck- and boost-mode alternating control either when D for buck mode conversion (D_{buck}) becomes >0.85, or when D for boost mode conversion (D_{boost}) becomes <0.15; the converter assumes V_a = 48 V, so it uses this buck–boost mode control for 40.8 V ≤ V_b ≤ 56.5 V. Under the buck–boost mode control, the volt-second balance for two switching periods yields

$$\frac{V_b}{V_a} = \frac{1 + D_{buck}}{2 - D_{boost}}. \tag{31}$$

The ripple current of i_{Le} for the buck–boost control increases as D_{boost} increases or as D_{buck} decreases. To have high η_e, D_{boost} should be minimized and D_{buck} should be maximized. The converter sets D_{boost} = 0 but adjusts D_{buck} from 0.7 to 0.85 for 40.8 V ≤ V_b ≤ 44.4 V, sets D_{buck} = 1, but adjusts D_{boost} from 0.15 to 0.31 for 51.89 V ≤ V_b ≤ 56.47 V, and sets D_{buck} = 0.75 but adjusts D_{boost} from 0.1 to 0.39 for 44.4 V < V_b < 51.89 V. The values of β were chosen as 1.1 for 40.8 V ≤ V_b ≤ 44.4 V, as 1.9 for 44.4 V < V_b < 51.89 V, and as 1.4 for 51.89 V ≤ V_b ≤ 56.47 V.

The comparator output becomes "high" whenever $T_c(j) = T_s[n]$; this produces the switching time-period $T_s = T_s(n)/f_{clk}$. The comparator output becomes "low" when $Ref[n] < T_c(j)$. The Flip/Flops and dead-time generator emit inverting and non-inverting gate signals for the switches.

4. Experimental Results

The proposed CBB BDC (Figure 12a) was fabricated using the chosen parameters (Table 3). It was designed to operate at V_a = 48 V, 0.15 ≤ D ≤ 0.85, 36 V ≤ V_b ≤ 60 V, 40 kHz ≤ f_s ≤ 210 kHz, 1.04 A ≤ I_a ≤ 10.4 A and 0.83 A ≤ I_b ≤ 13.9 A. The PI coefficients of the controller were optimized to k_p = 0.02 and k_i = 0.2. The sampling frequency for analog signals was 20 kHz, and the analog-to-digital converter had 12-bit resolution. When P_b increased from 50 to 500 W, f_s decreased from 210 to 40 kHz during buck conversion and from 201 to 64 kHz during boost conversion. The dead time for switch control was 110 ns. The switching devices were the IPP200N15N3 power MOSFETs (Infineon).

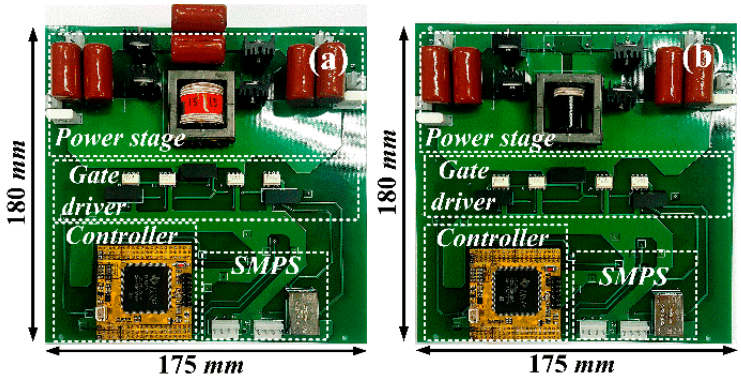


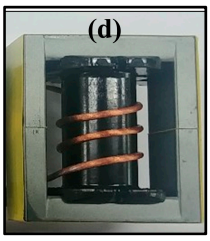
Figure 12. Photographs of (**a**) the proposed and (**b**) conventional CBB BDCs.

Table 3. Circuit parameters of the proposed converter.

Parameter	Symbol	Value
N-MOSFET	SW_1, SW_2, SW_3, SW_4	IPP200N15N3
Magnetizing inductance	L_m	110 μH
Leakage inductance	L_{lk}	10.5 μH
DC-blocking capacitor	C_B	20 μF
Snubber capacitor	C_{s1}, C_{s2}	2.2 nF
Filter capacitor	C_a, C_b	20 μF

The 1:1 transformer was fabricated using an ETD 34 ferrite core with N = 15, as discussed in Section 2.5. For comparison, the conventional CBB BDC in [10] (Figure 12b) was also fabricated using the IPP200N15N3 power MOSFETs and three different inductors with $L = L_{lk}/2$ = 5.25 µH (Table 4). Inductor 1 used an ETD 34 ferrite core and had an air-gap length S_a = 0.1 mm, which resulted in L = 5.25 µH when N = 3. This inductor had core saturation at high power operation. Inductor 2 used the same core, but increased S_a to 8 mm to prevent core saturation, which resulted in L = 5.25 µH when N = 15. Inductor 3 had N = 3 and S_a = 0.1 mm but prevented core saturation by increasing the core size. The filter capacitors for the conventional CBB BDC were $C_a = C_b$ = 40 µF.

Table 4. Transformer and inductors for the experimental converters.

	1:1 Transformer	Inductor 1	Inductor 2	Inductor 3
Core size	34 × 35 × 10.5 mm^3	34 × 35 × 10.5 mm^3	34 × 35 × 10.5 mm^3	40 × 42 × 15 mm^3
N	15	3	15	3
S_a	0.1 mm	0.1 mm	8 mm	0.1 mm
Inductance	5.25 µH	5.25 µH	5.25 µH	5.25 µH
Photographs				

The waveforms of i_L, i_{Lm}, i_p, and i_s for forward boost conversion (Figure 13) were measured at V_a = 48 V, V_b = 60 V, P_b = 50 W or P_b = 500 W. The proposed converter operated in PFM and had $\Delta i_p \approx \Delta i_s \leq$ 4.1 A$_{p\text{-}p}$ for P_b = 50 W (Figure 13a) and ≤16.3 A$_{p\text{-}p}$ for P_b = 500 W (Figure 13b). Δi_{Lm} was 0.25 A$_{p\text{-}p}$ at P_b = 50 W and 0.73 A$_{p\text{-}p}$ at P_b = 500 W, when $i_{Lm} = i_p - i_s$ was calculated using the i_s and i_p measurements. The conventional CBB BDC operated at f_s = 64 kHz and had an inductor current ripple Δi_L = 30.3 A$_{p\text{-}p}$ at P_b = 500 W.

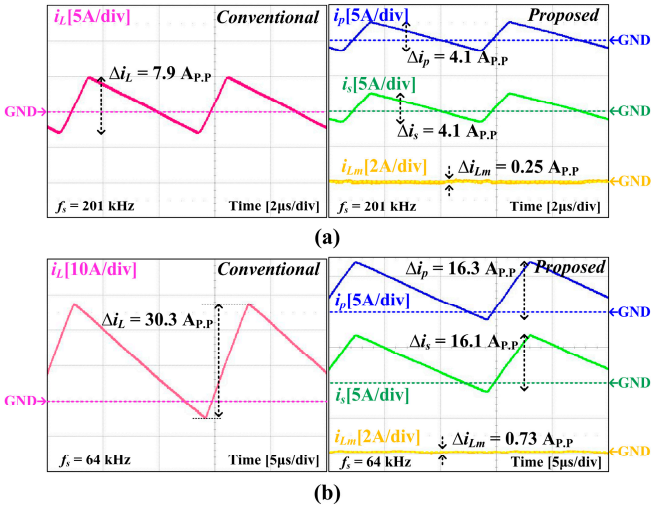


Figure 13. Waveforms for i_L, i_{Lm}, i_p, and i_s at V_a = 48 V, V_b = 60 V, (**a**) P_b = 50 W, and (**b**) P_b = 500 W.

The waveforms of i_{C_b} and ΔV_b (Figure 14) were measured at V_a = 48 V and P_b = 500 W, while the converters were operated at V_b = 60 V (boost conversion, Figure 14a) or V_b = 36 V (buck conversion, Figure 14b). ΔV_b for boost conversion to V_b = 60 V was 3.59 V$_{p.p}$ for the proposed and 6.29 V$_{p.p}$ for

the conventional CBB BDCs. ΔV_b for buck conversion to V_b = 36 V was 1.35 $V_{p.p}$ for the proposed and 1.62 $V_{p.p}$ for the conventional CBB BDCs. Considering that $C_a = C_b = C_B$ = 20 µF in the proposed converter and $C_a = C_b$ = 40 µF in the conventional CBB BDC, the proposed converter reduced the total capacitance by 20 µF for the given ΔV_b, by providing a bypass to i_{Le} through C_B.

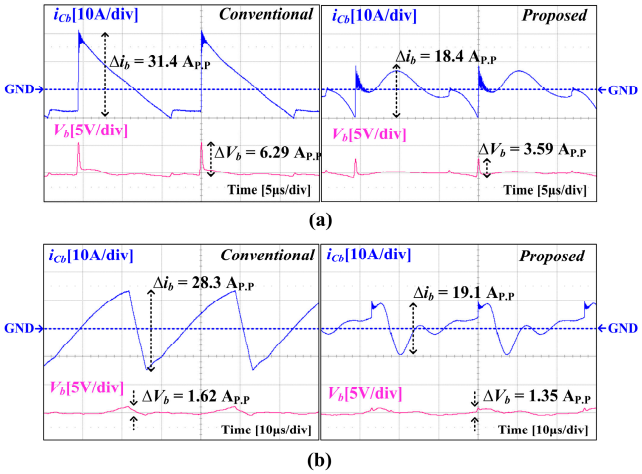


Figure 14. Waveforms of i_{C_b} and ΔV_b at V_a = 48 V, P_b = 500 W, and (**a**) V_b = 60 V or (**b**) V_b = 36 V.

The current and voltage waveforms of switches in the proposed converter for V_a = 48 V (Figure 15) were measured at P_b = 50 W and 500 W, while the converter was operated in either boost (V_b = 60 V, Figure 15a) or buck (V_b = 36 V, Figure 15b) mode. These waveforms show: 1) $i_{SW4} > 0$ when SW_4 was turned off; 2) v_{SW4} increased only up to V_b; 3) 1) and 2) indicate that the body diode of SW_3 was turned on when SW_4 was turned off, so SW_3 had ZVS turn-on; 4) $i_{SW4} < 0$ when SW_3 was turned off; 5) v_{SW3} increased only up to V_b; 6) 4) and 5) indicate that the body diode of SW_4 was turned on when SW_3 was turned off, so SW_4 had ZVS turn-on. The waveforms in Figure 15b show: 7) $i_{SW2} < 0$ when SW_1 was turned off; 8) v_{SW2} increased only up to V_a; 9) points 7) and 8) indicate that the body diode of SW_2 was turned on when SW_1 was turned off, so SW_2 had ZVS turn-on; 10) $i_{SW1} > 0$ when SW_2 was turned off; 11) v_{SW1} increased only up to V_a; 12) points 10) and 11) indicate that the body diode of SW_1 was turned on when SW_2 was turned off, so SW_1 had ZVS turn-on; 13) f_s increased as P_b decreased; this result shows that PFM worked properly and the currents of switches were decreased by the reduced i_p and i_s at the light load; and 14) PWM adjusted D of the main switch so that V_b followed the reference voltage.

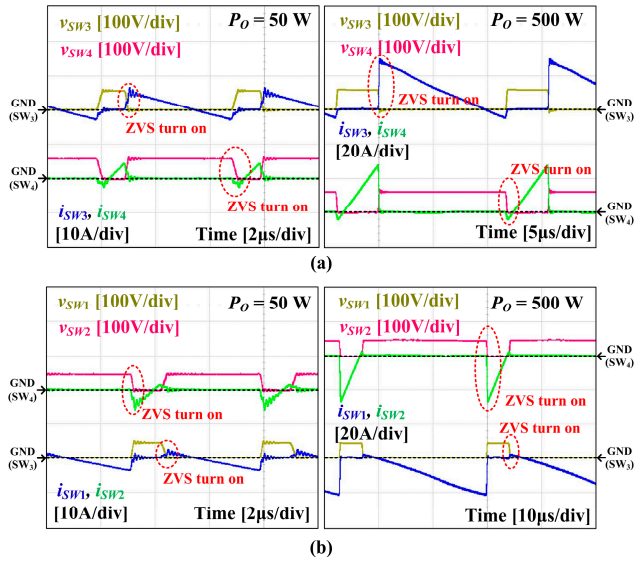
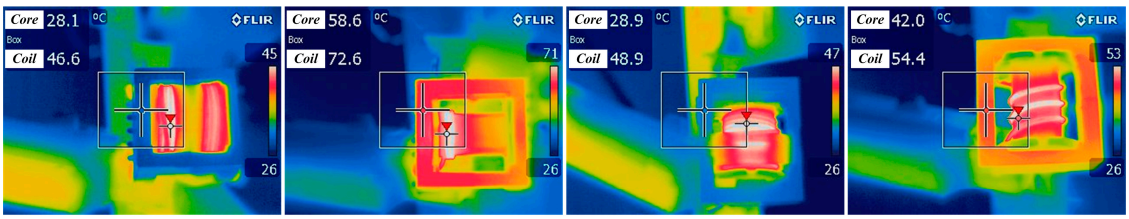


Figure 15. Voltage and current waveforms of switches measured at V_a = 48 V and P_b = 50 W and 500 W: (**a**) V_b = 60 V and (**b**) V_b = 36 V.

The temperatures of cores and windings (Figure 16) were measured at V_a = 48 V, V_b = 60 V, and P_b = 500 W. The proposed converter had small core loss because i_{Lm} was reduced significantly by connecting the windings of the transformer in parallel and in inverse-coupling configuration. As a result, the core temperature T_{core} = 28.1 °C and the winding temperature $T_{winding}$ = 46.6 °C of the proposed converter (Figure 16a) were lower than the other conventional CBB BDCs: T_{core} = 58.6 °C and $T_{winding}$ = 72.6 °C for inductor 1 at P_b = 350 W (Figure 16b), T_{core} = 28.9 °C and $T_{winding}$ = 48.9 °C for inductor 2 at P_b = 500 W (Figure 16c), and T_{core} = 42.0 °C and $T_{winding}$ = 54.4 °C for inductor 3 at P_b = 500 W (Figure 16d). Note that the conventional converter could not operate for P_b > 350 W due to core saturation, so the temperature was measured at 350 W.



(a) **(b)** **(c)** **(d)**

Figure 16. Thermal camera images of inductors: (**a**) 1:1 transformer at P_b = 500 W, (**b**) inductor 1 at P_b = 350 W, (**c**) inductor 2 at P_b = 500 W, and (**d**) inductor 3 at P_b = 500 W.

η_e vs. P_b (Figure 17) for boost conversion were measured at V_a = 48 V and V_b = 60 V, while the converters were operated in PFM mode (64 kHz ≤ f_s ≤ 210 kHz). η_e of the proposed converter was ≥98.3% for P_b > 50 W. The conventional CBB BDC using inductor 1 could not operate at P_b > 350 W due to core saturation; this converter had η_e = 96.1% at P_b = 50 W and η_e = 97.5% at P_b = 350 W when operated in PFM mode. After replacing inductor 1 with inductor 2, the converter had η_e = 98.3% at P_b = 50 W and η_e = 98.1% at P_b = 500 W, which are very close to that for the proposed converter. However, inductor 2 has a large air gap and is difficult to fabricate. Fabrication of the converter using inductor 3 yielded η_e = 97.2% at P_b = 50 W and η_e = 97.6% at P_b = 500 W. The core and switching losses were reduced in the proposed converter, so it had higher η_e than the conventional CBB BDCs. The behaviors of η_e vs. P_b for buck conversion at V_a = 48 V, V_b = 36 V, and 64 kHz ≤ f_s ≤ 201 kHz (Figure 18) were quite similar to those for boost conversion.

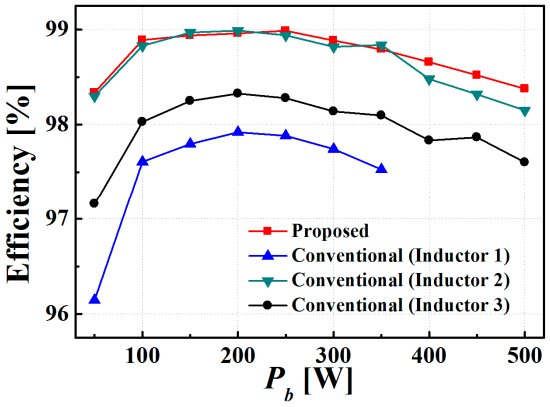


Figure 17. η_e vs. P_b at V_a = 48 V and V_b = 60 V.

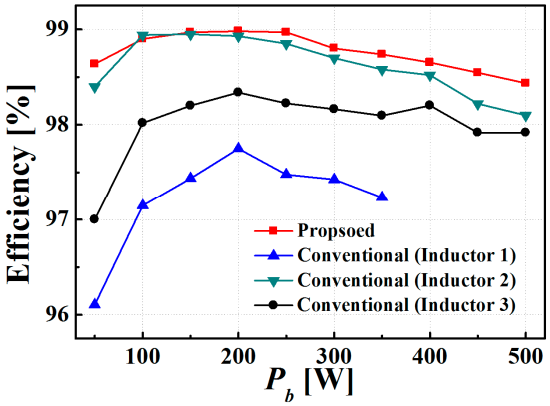


Figure 18. η_e vs. P_b at V_a = 48 V and V_b = 36 V.

η_e vs. V_b (Figure 19) was measured at V_a = 48 V and P_b = 500 W. The proposed converter had $\eta_e \geq 98.3\%$ for 36 V $\leq V_b \leq$ 60 V, whereas the conventional CBB BDC had ~0.76% lower η_e than the proposed converter. The results of loss analyses at V_a = 48 V, V_b = 60 V, and P_b = 500 W show that the total losses were 7.41 W in the proposed circuit and 12.6 W in the conventional CBB BDC (Figure 20). The major losses in the proposed converter were the switching (1.75 W) and winding (5.52 W) losses, and those in the conventional CBB BDC were the core (7.8 W), switching (2.0 W), and winding (2.8 W) losses. In the proposed converter, the switching loss was reduced by using the snubber capacitors C_{s1} and C_{s2}, and the core loss was reduced significantly by connecting the windings of the 1:1 transformer in parallel and in inverse-coupling configuration, but the winding loss was increased because N was increased.

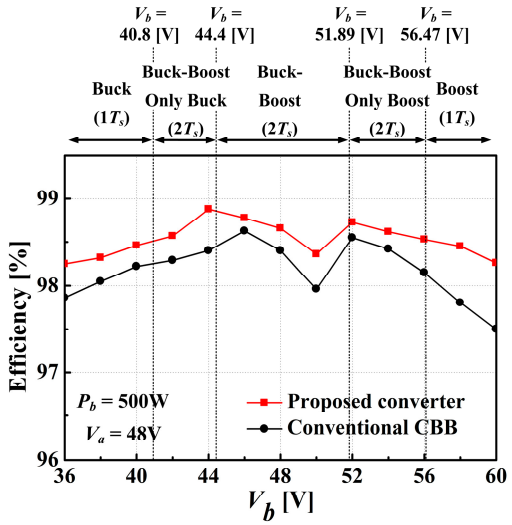


Figure 19. η_e vs. V_b at V_a = 48 V and P_b = 500 W.

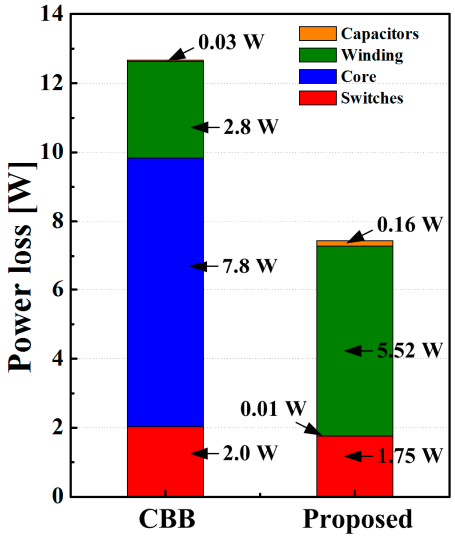


Figure 20. Results of loss analysis for the conventional and proposed CBB BDCs operating at V_a = 48 V, V_b = 60 V, and P_b = 500 W.

The costs of the conventional and proposed CBB BDCs were calculated using the prices on the websites of [23] and [24] (Table 5), assuming that both BDCs use the same switches and ferrite core and have the same input/output voltage ripples. Compared to the conventional converter, the proposed CBB BDC costs $1.93 more because C_B, C_{s1}, C_{s2} and transformer windings are additionally required. However, the proposed CBB BDC can save $14.44 in cost by using small filter capacitors. Therefore, the proposed CBB BDC is $5.29 cheaper than the conventional one.

Table 5. Prices of components for the proposed and conventional CBB BDC.

Components	Part Number	Quantity of Parts		Cost	
		Proposed	Conventional	Proposed	Conventional
Transformer	Core: ETD 34	1 pc.	1 pc.	$1.17	$1.17
	Winding: USTC litz wire	1.74 m	0.18 m	$1.04	$0.11
DC-blocking capacitor (C_B)	ECQ-E2106JF	2 pc.	0 pc.	$7.22	$0
Snubber capacitors (C_{s1}, C_{s2})	ECQ-E6222JF	2 pc.	0 pc.	$1.00	$0
Filter capacitor (C_a)	ECQ-E2106JF	2 pc.	4 pc.	$7.22	$14.44
Filter capacitor (C_b)	ECQ-E2106JF	2 pc.	4 pc.	$7.22	$14.44
Switches (SW_1–SW_4)	IPP200N15N3	4 pc.	4 pc.	$10.96	$10.96
	Total			$35.83	$41.12

5. Conclusions

The circuit structure of a bidirectional converter for a residential energy storage system is proposed. The proposed converter could operate at maximum power point regardless of V_{PV} and V_{bat} because it works well for both $V_{IN} > V_O$ and $V_{IN} \leq V_O$. In addition, this converter increased the power conversion efficiency η_e by using two snubber capacitors to reduce switching loss, and by using a 1:1 transformer with windings connected in parallel and in inverse-coupling configuration to reduce core loss. Ripples of output current and voltage were reduced by modulating the switching frequency, and by placing a blocking capacitor between input and output to reduce the filter size. The conventional CBB BDC could not operate at $P_b > 350$ W due to core saturation, but the proposed converter operated normally up to P_b = 500 W. The efficiency was ≥98.3% for 50 W ≤ P_b ≤ 500 W, which is up to 2.5% higher than that of the conventional CBB BDC. These results show that the proposed converter is suitable for residential energy storage systems that require high η_e in the condition of overlapping input and output range.

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