energies

MDPI

Article

A Hybrid Nine-Arm High-Voltage Inverter with DC-Fault Blocking Capability

Luyun Jiao, Dongyuan Qiu *, Bo Zhang and Yanfeng Chen

School of Electric Power, South China University of Technology, Guangzhou 510640, China; eelyjiao@163.com (L.J.); epbzhang@scut.edu.cn (B.Z.); eeyfchen@scut.edu.cn (Y.C.)
* Correspondence: epdyqiu@scut.edu.cn

Received: 2 September 2019; Accepted: 8 October 2019; Published: 11 October 2019

Abstract: The nine-arm inverter integrates two modular multilevel converters (MMCs) into one compact inverter to diminish the number of power semiconductor devices. It can be used for dual-motor driving or connecting two AC power sources in a multi-terminal high voltage direct current (HVDC) system, etc. Although the half-bridge based modular multilevel converter has the fewest components, it is generally not resistant to the DC-side faults. In order to achieve a DC fault blocking capability with high efficiency and low cost, this paper proposes a hybrid nine-arm high-voltage inverter, which is consists of a full-bridge sub-module (FBSM) and a half-bridge sub-module (HBSM). Firstly, the topology, operation modes, and modulation strategy of the proposed hybrid inverter are presented. Then, by analyzing the potential short-circuit current paths between different ports, the ability of the proposed hybrid inverter to block the DC faults is described and the appropriate ratio of HBSM and FBSM is determined to further reduce the number of devices and the losses of the proposed hybrid inverter. Finally, simulation results based on MATLAB/Simulink are provided to demonstrate the effectiveness and feasibility of the proposed hybrid nine-arm high-voltage inverter under normal operation and DC fault condition.

Keywords: DC fault blocking; modular multilevel converter; half-bridge sub-module; full-bridge sub-module

1. Introduction

In recent years, the power system is gradually comprising more and more power sources, such as renewable energy sources and energy storage systems. Thus, multi-terminal converters have become increasingly attractive, as they can connect multiple distributed power sources instead of using several individual converters [1–4]. For example, a multi-port boost converter can collect multiple low-voltage photovoltaic outputs to achieve high-voltage output and deliver DC current to the inverter station near the load [5,6]. Furthermore, multi-terminal converters will play an important role in the multi-terminal HVDC grid to interconnect multiple energy sources across regions and nations [5,6]. In addition, in order to realize further reductions in complexity and capital cost, multi-terminal inverters with a reduced number of power semiconductor devices have been developed for the multi-motor drive systems over the past two decades [7,8].

Among multi-port inverters, a nine-switch inverter is a typical three-port system that can connect one DC supply to two AC loads and has the advantage of saving 25% of the number power semiconductor devices compared to using two independent inverters [9]. However, it is limited to low and medium power applications. A modular multilevel converter (MMC) is considered the most attractive converter in high voltage applications due to its inherent features of high modularity and scalability [10–13], but it has only one output port.

The nine-arm modular multilevel converter (NA-MMC) combines the advantages of an MMC and a nine-switch inverter [6,10], where each arm consists of sub-modules in series, rather than a single switch. Thus, it can reduce the number of power semiconductor devices, compared to using two separate MMCs, and can operate in high-voltage occasions. In the case shown in Figure 1 [14,15], one NA-MMC is used to connect the DC bus, the AC bus, and an AC load which has different frequency and/or amplitude from the nearby AC bus. Another NA-MMC is used to connect the outputs of two different wind turbines to the DC bus. Thus, an NA-MMC can be applied in many medium/high voltage multi-terminal systems.

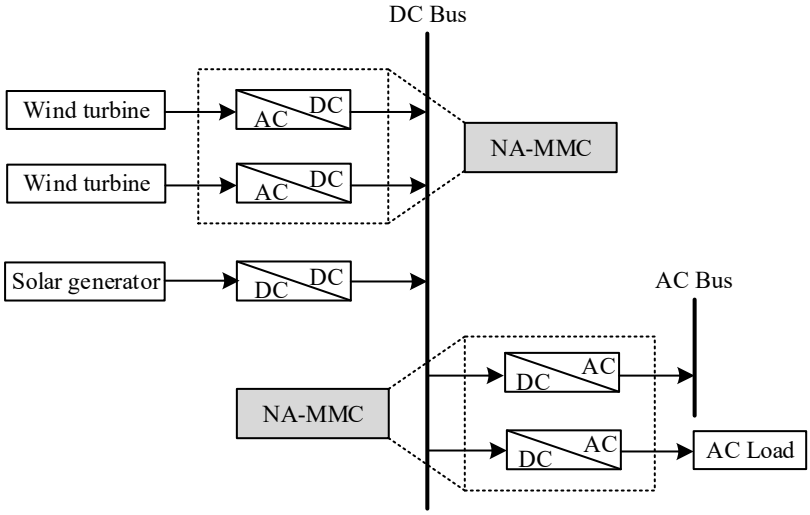


Figure 1. NA-MMC application.

It is known that the pole-to-pole DC fault will impose major restrictions on MMC, especially for overhead transmission lines [16,17]. As a multi-terminal converter has more than two terminals, its DC-side fault phenomena is more complex than that of a traditional MMC. There are usually two main approaches to assist MMCs with handling DC-side faults. One is to employ a DC circuit breaker (CB) with relatively high let-through current to isolate the DC fault current in a short time after the DC side fault occurs. However, the availability of DC CBs are restricted due to their high cost and imperfections [18,19]. The other approach is to use sub-modules with DC fault handling capabilities [19–21]. For example, by replacing the half-bridge sub-module (HBSM) with the full-bridge sub-module (FBSM) in the NA-MMC, a reverse voltage can be generated by the FBSM capacitors to block the short-circuit current subsequent to the DC-side fault. Obviously, if the NA-MMC is composed of FBSM, it will have the a DC-fault blocking capability. Nevertheless, the number of power semiconductor devices in FBSMs is twice that of power semiconductor devices in HBSMs [22]. This not only increases the cost of NA-MMC systems, but also brings larger power losses as the current passes two power semiconductor devices in each FBSM instead of one in each HBSM. Thus, the configuration scheme based on FBSM only manages the fault condition and sacrifices the cost and efficiency. To pursue the optimal design in terms of DC-fault blocking capability, efficiency, and cost, the hybrid design concept making use of HBSM and FBSM has been put forward [23].

Therefore, the contributions of this paper are as follows: (1) To construct a hybrid nine-arm high-voltage inverter with HBSMs and FBSMs, (2) to analyze all types of fault current in the multi-terminal inverter, and (3) to obtain the optimal ratio of HBSM and FBSM in the different arms.

The rest of this paper is organized as follows. Section 2 introduces the topology and operating principle of the proposed hybrid nine-arm high-voltage inverter. Section 3 analyzes all potential short-circuit current paths and the corresponding DC fault blocking scheme of the proposed hybrid inverter. Section 4 provides the simulation results to demonstrate the feasibility and effectiveness of the proposed hybrid inverter. Section 5 draws the conclusions.

2. Topology and Operating Principle

2.1. Basic Configuration

Figure 2 shows one phase of the hybrid nine-arm high-voltage inverter with a DC fault blocking capability. The upper and lower arms are composed of m HBSMs and n FBSMs, but the middle arm is composed of $(m + n)$ FBSMs. Every sub-module (SM) can be considered as a controlled voltage source, for which output voltage is determined by the ON/OFF states of power switches.

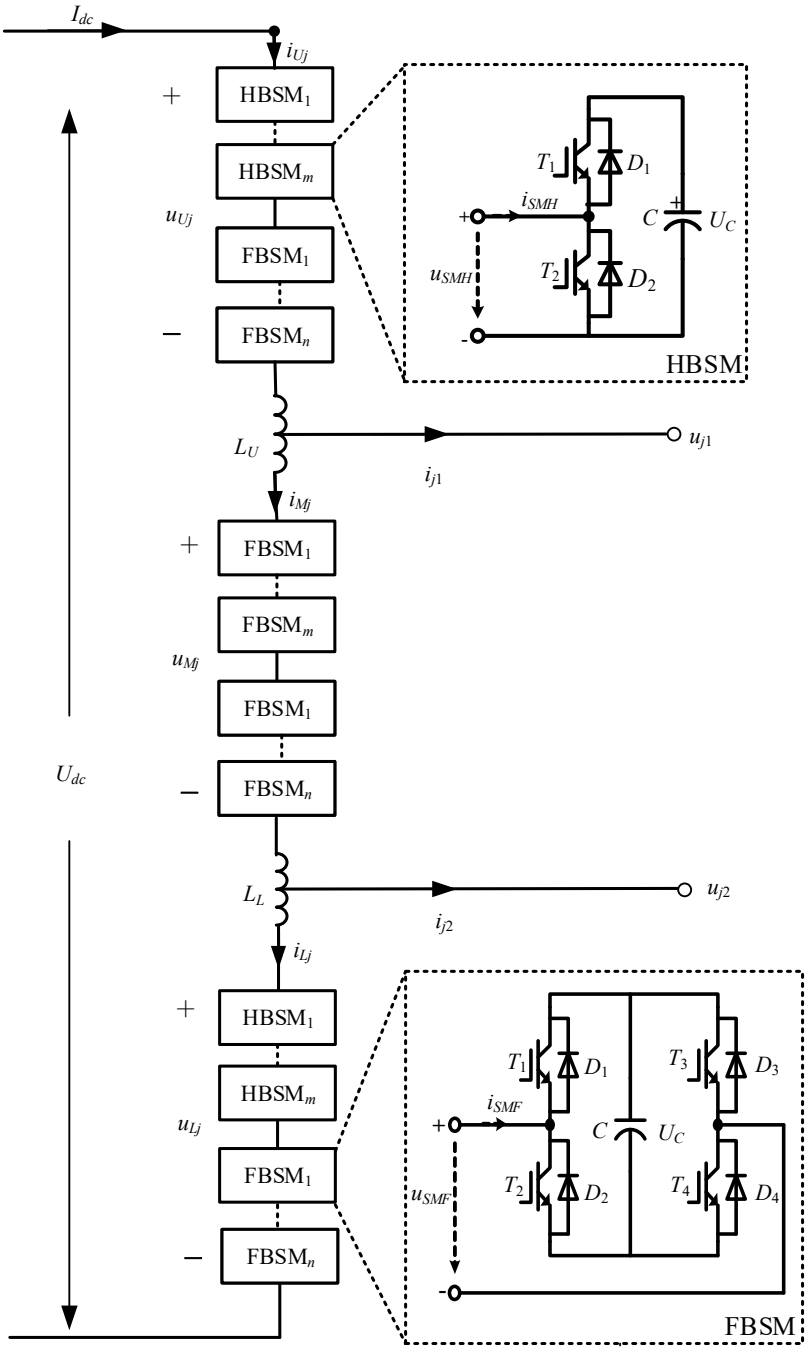


Figure 2. Single phase of the hybrid nine-arm high-voltage inverter.

Inductors L_U and L_L are two buffer inductors, with $L_U = L_L$. The value U_{dc} is the DC-link voltage and I_{dc} is the DC-side current. The value U_C is the capacitor voltage of SM and equals to

$U_c = U_{dc}/(m+n)$. The values i_{Uj}, i_{Mj}, and i_{Lj} are the currents of upper arm, middle arm, and lower arm in phase j ($j = a,\ b,\ c$), respectively. The values u_{Uj}, u_{Mj}, and u_{Lj} are the voltages of upper arm, middle arm, and lower arm in phase j, respectively. The values u_{j1} and u_{j2} are the output voltages of the inverter upper port and lower port of phase j, while i_{j1} and i_{j2} are the corresponding output port currents.

Based on the structure of HBSM shown in Figure 2, the output voltage of HBSM, u_{SMH}, is decided by the ON/OFF states of switches T_1 and T_2, and the driving signals of T_1 and T_2 are complementary. When $T_1(D_1)$ is ON, u_{SMH} is equal to the capacitor voltage U_C. When $T_2(D_2)$ is ON, u_{SMH} is equal to 0. Similarly, the output voltage of FBSM u_{SMF} depends on the ON/OFF states of $T_1(D_1)$ to $T_4(D_4)$, which is U_C, $-U_C$, or 0.

2.2. Modulation Scheme

Like the NA-MMC, the hybrid nine-arm high-voltage inverter can also be controlled by carrier phase-shifted pulse-width modulation (CPS-PWM), in which N triangular carriers C_i ($i = 1,\ 2,\ 3\ldots,\ N$) are compared with two modulating references to obtain the driving signals for SMs. The triangular carriers are shifted in an angle of $360/N$, where N is the total number of SMs in each arm and $N = m + n$.

Assume that the modulating references of dual AC outputs are expressed as follows:

$$\begin{aligned} u_{j1-ref} &= M_1 \sin(\omega_1 t + \psi_1 + \theta) + U_{offset1} \\ u_{j2-ref} &= M_2 \sin(\omega_2 t + \psi_2 + \theta) + U_{offset2} \end{aligned}, \tag{1}$$

where ω_1 and ω_2 are fundamental angular frequencies of dual AC outputs u_{uj} and u_{lj}, M_1 and M_2 are modulation ratios, ψ_1 and ψ_2 are relative phases, $U_{offset1}$ and $U_{offset2}$ are appropriate offsets, and θ is 0 when $j =$ a, $-2\pi/3$ when $j =$ b, and $2\pi/3$ when $j =$ c.

The hybrid nine-arm high-voltage inverter has two operating modes. When $\omega_1 = \omega_2$, the inverter is working in common frequency (CF) mode. In another situation ($\omega_1 \neq \omega_2$), the inverter is working in different frequency (DF) mode. The relationship among the upper reference, u_{j1-ref}, the lower reference, u_{j2-ref}, and carrier signal, C_i, under CF and DF modes are shown in Figure 3. The amplitudes of u_{j1-ref} and u_{j2-ref} cannot exceed the range of the carrier, so then we have $-1 \leq M_1 + U_{offset1},\ M_2 + U_{offset2} \leq 1$. As the upper modulating reference, u_{j1-ref}, should always be greater than the lower modulating reference, u_{j2-ref}, to avoid overlap [10], $M_1 + U_{offset1} \geq M_2 + U_{offset2}$ and $-M_1 + U_{offset1} \geq -M_2 + U_{offset2}$ must be satisfied in CF mode, while $M_1 + M_2 \leq 1$ must be satisfied in DF mode.

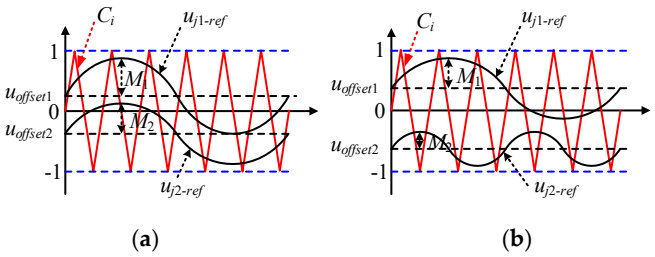


Figure 3. Modulating references under (**a**) CF mode and (**b**) DF mode.

Based on the CPS-PWM method for the NA-MMC [10], the gate signals for the i^{th} SM in upper, middle, and lower arms (S_{Ui}, S_{Mi} and S_{Li}) can be obtained by comparing the i^{th} carrier signal C_i (where $i = 1, 2, \ldots, N$) to the reference signals u_{j1-ref} and u_{j2-ref}, which are shown in Figures 3 and 4. It can be found that S_{Ui} is the positive logic value generated by C_i and u_{j1-ref}, S_{Li} is the negative logic value generated by C_i and u_{j2-ref}, and S_{Mi} is the logical exclusive OR (XOR) value of S_{Ui} and S_{Li}, that is, $S_{Mi} = S_{Ui} \oplus S_{Li}$.

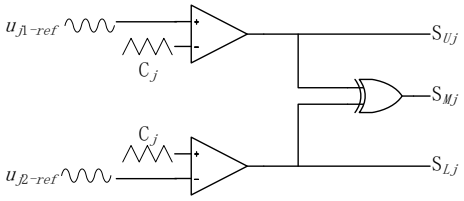


Figure 4. Control method for the hybrid nine-arm high-voltage inverter.

2.3. Basis Operation

According to Reference [10], the upper and lower AC voltages, u_{j1} and u_{j2}, are determined by

$$\begin{aligned} u_{j1} &= \frac{1}{2}\left(u_{Lj} + u_{Mj} - u_{Uj}\right), \\ u_{j2} &= \frac{1}{2}\left(u_{Lj} - u_{Mj} - u_{Uj}\right), \end{aligned} \tag{2}$$

where u_{Uj}, u_{Mj}, and u_{Lj} are the voltages of the upper, middle and lower arm, respectively.

The arm voltage is known to be the sum of SM output voltages on the arm. With the CPS-PWM scheme [24], u_{Uj}, u_{Mj}, and u_{Lj} can be controlled to

$$\begin{aligned} u_{Uj} &= U_{dc} \cdot M_1 sin(\omega_1 + \psi_1 + \theta) + U_{dc} \cdot U_{offset1}, \\ u_{Mj} &= U_{dc} - u_{Uj} - u_{Lj}, \\ u_{Lj} &= U_{dc} \cdot M_2 sin(\omega_2 + \psi_2 + \theta) + U_{dc} \cdot U_{offset2}. \end{aligned} \tag{3}$$

Substituting (3) into (2), u_{j1} and u_{j2} are expressed as

$$\begin{aligned} u_{j1} &= \frac{1}{2}U_{dc} \cdot M_1 sin(\omega_1 t + \psi_1 + \theta) + \frac{1}{2}U_{dc}\left(1 + U_{offset1}\right), \\ u_{j2} &= \frac{1}{2}U_{dc} \cdot M_2 sin(\omega_2 t + \psi_2 + \theta) + \frac{1}{2}U_{dc}\left(1 + U_{offset2}\right). \end{aligned} \tag{4}$$

2.4. Operation Under DC Fault Condition

After a pole-to-pole DC fault occurs, the DC side current is raised rapidly and the load on the AC side will inject energy into the DC side through the hybrid inverter. If the hybrid inverter does not provide a large enough reverse voltage to prevent the injected energy, then an AC side current will flow directly to the DC side fault point due to the freewheeling effect of the anti-parallel diode of the sub-module and the DC fault will turn to an AC fault.

The DC fault blocking capability of the proposed hybrid nine-arm high-voltage inverter is achieved by inhibiting the gate signals to the SMs after the DC fault is detected. Figure 5 shows the equivalent circuits of different arms when all insulated gate bipolar transistors (IGBTs) in SMs are turned off, which turn out to be diodes in series with SM capacitors. If the formed series voltage is larger than the AC side voltage, then the fault current will be interrupted within a very short time.

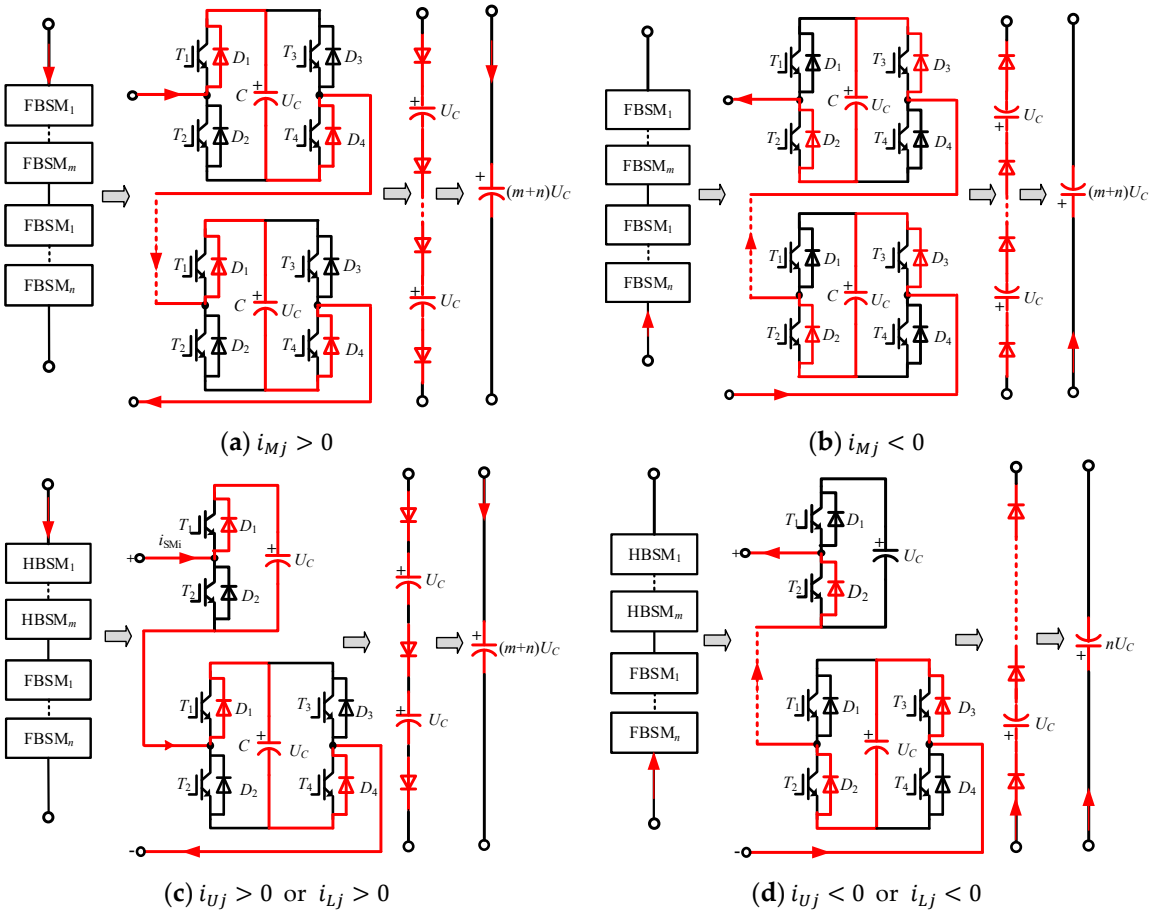


Figure 5. Equivalent circuits when all IGBTs in SMs are turned OFF.

3. DC Fault Blocking Scheme

The hybrid nine-arm high-voltage inverter can connect to two AC loads with different frequencies and amplitudes. When the DC side fault occurs, the AC sides will feed the current to the fault point through arms. The possible fault current paths of the hybrid nine-arm high-voltage inverter are shown in Figure 6, where a_1, b_1, and c_1 are the upper AC ports and a_2, b_2, and c_2 are the lower AC ports.

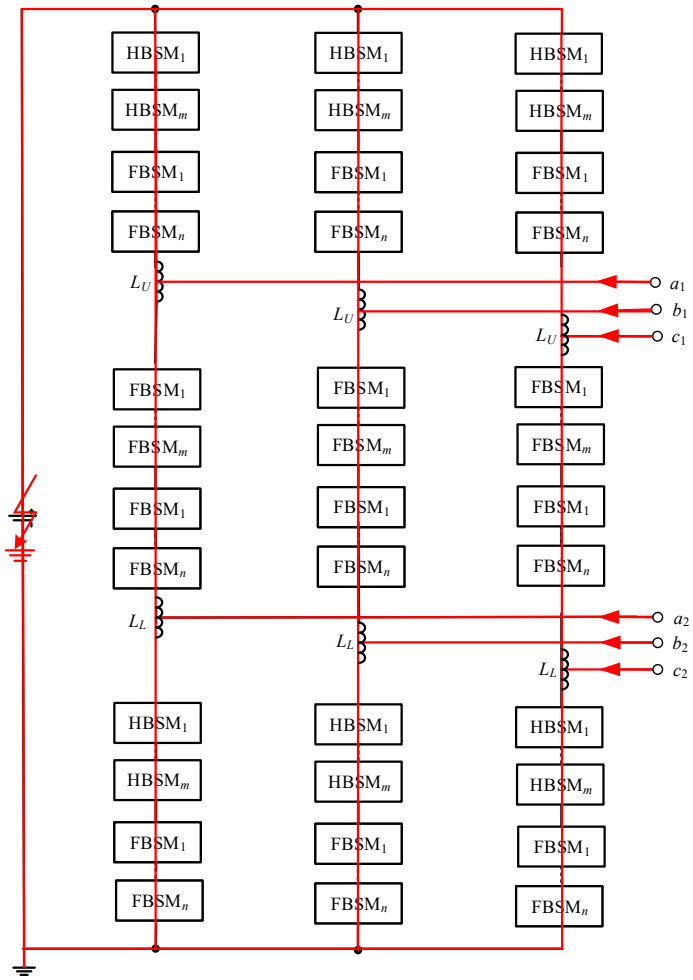


Figure 6. The possible fault current paths of the hybrid nine-arm high-voltage inverter.

After the DC side fault occurs, U_{dc} drops to zero rapidly and I_{dc} increases sharply. When the current is detected to be greater than the current threshold, it can be judged that there is a short circuit fault in the system, then all the IGBTs of the inverter receive the turn-off signals to protect the SMs. After all of the IGBTs are turned off, the short circuit current can be formed between different output ports and the DC side. In order to reduce the fault currents, a sufficiently large reverse voltage must be provided in the fault current flow path. All types of possible current flow paths in the hybrid nine-arm high-voltage inverter are analyzed in order to obtain the total reverse voltage that should be provided.

3.1. Different Ports with the Middle Arm

The fault current path shown in Figure 7 is formed by the middle arm of the inverter. Although this current path does not pass through the DC side when a short-circuit fault occurs on the DC side, a large current will be generated between the different ports through the middle arm of the converter, which may damage the inverter.

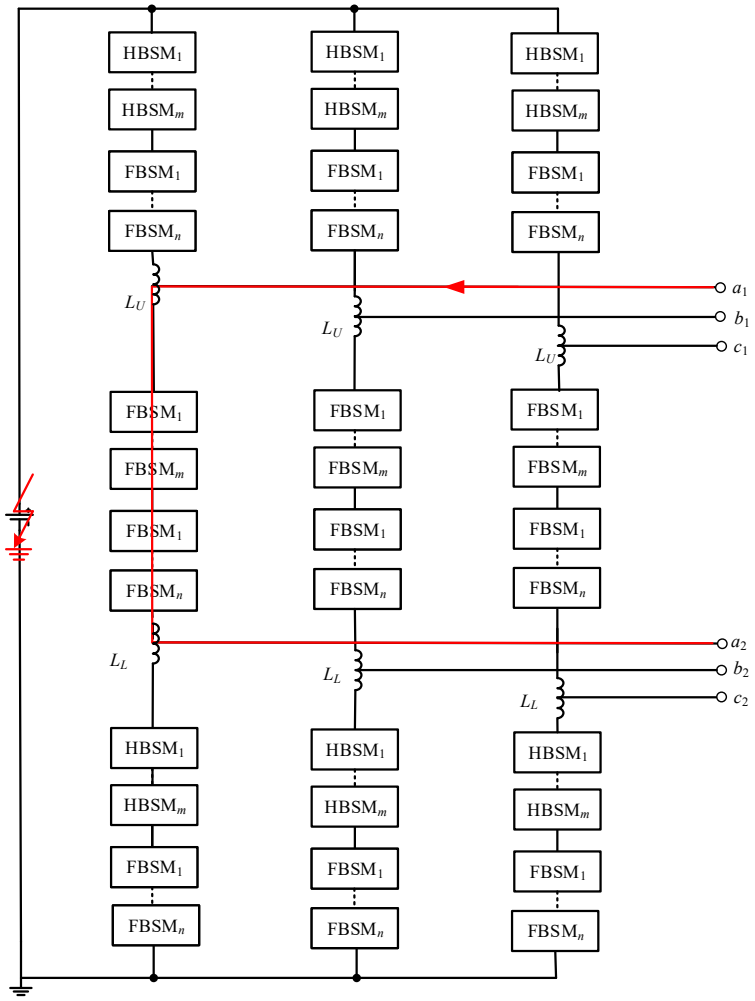


Figure 7. Potential flow path of short-circuit current (a_1–*middle arm*–a_2).

Take the upper output port a_1 and the lower output port a_2 as the example. Assume that $\psi_1 = \psi_2 = 0$ and $\theta_1 = \theta_2 = 0$. The voltage difference between two output ports is

$$u_{a1a2} = u_{a1} - u_{a2} = \frac{1}{2}U_{dc}\left[M_1 sin\omega_1 t + U_{offset1} - (M_2 sin\omega_2 t + U_{offset2})\right]. \quad (5)$$

According to Figure 3, we have

$$\left|M_1 + U_{offset1}\right| \leq 1, \ \left|M_2 + U_{offset2}\right| \leq 1. \quad (6)$$

Then the maximum voltage between the two ports is

$$U_{a1a2(\max)} = \frac{1}{2}U_{dc}\left(M_1 + M_2 + U_{offset1} - U_{offset2}\right) \leq U_{dc}. \quad (7)$$

It is known that the maximum voltage between the output ports a_1 and a_2 is smaller than U_{dc}. Assume that there are m HBSMs and n FBSMs in the middle arm, based on Figure 5, the voltage formed by the capacitors in series will be $(m+n)U_c$ when the fault current flows from a_1 to a_2, or nU_c when the fault current flows from a_2 to a_1. In order to keep the fault current under control in any case, $nU_c \geq U_{dc}$ should be satisfied. Hence, there is no need to use HBSM to meet the requirement of fault current blocking and the middle arm can be composed of FBSMs only. In order to make the number of sub-modules the same as that of the upper and lower arms, there must be $m+n$ FBSMs in the middle

arm. This is the main reason why the ratio of HBSM to FBSM in the middle arm is different from the other two arms in the proposed hybrid nine-arm high-voltage inverter.

3.2. Different Ports with the DC-Side

The fault current path shown in Figure 8 is formed by the upper output port, the DC side, and the lower output port. When a short-circuit fault occurs on the DC side, the AC side inputs energy to the DC side through the different arms of the inverter.

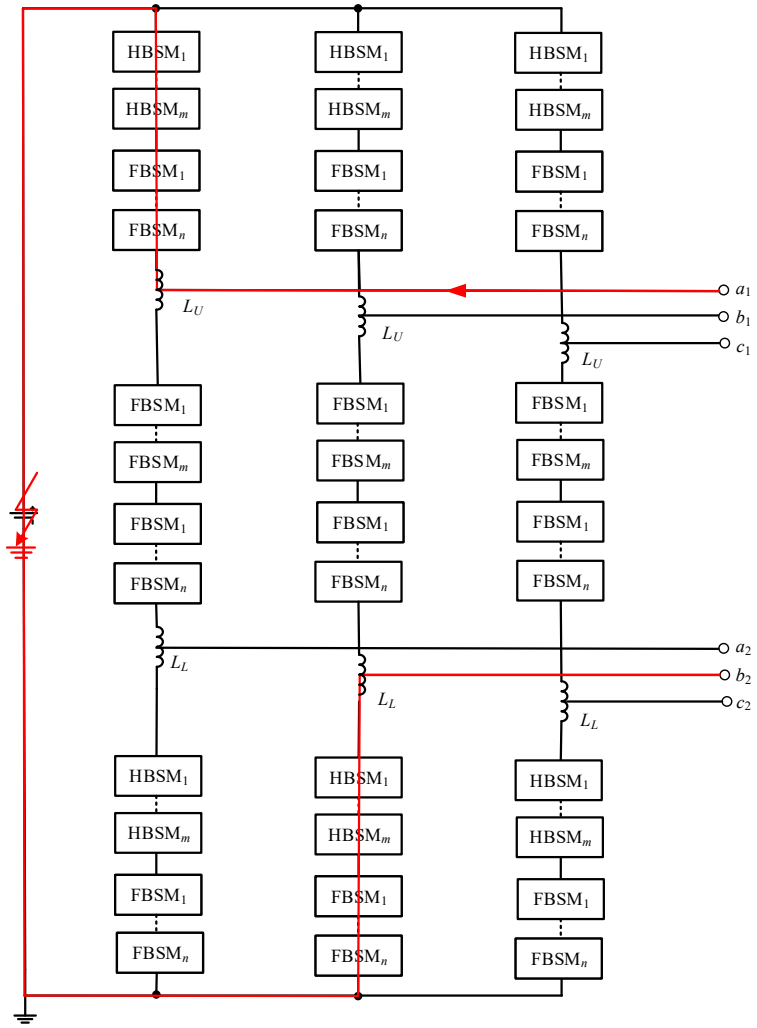


Figure 8. Potential flow path of short-circuit current (a_1–*dc side*–b_2).

Take the upper output port a_1 and the lower output port b_2 as the example. Assume that $\psi_1 = \psi_2 = 0$, $\theta_1 = 0$ and $\theta_2 = 2\pi/3$, the voltage difference between two output ports is

$$u_{a1b2} = u_{a1} - u_{b2} = \frac{1}{2}U_{dc} \cdot \left[M_1 sin\omega_1 t + U_{offset1} - M_2 sin\left(\omega_2 t + \frac{2\pi}{3}\right) - U_{offset2}\right]. \quad (8)$$

No matter if it is in CF mode ($\omega_1 = \omega_2$) or DF mode ($\omega_1 \neq \omega_2$), the maximum magnitude of u_{a1b2} is

$$U_{a1b2(max)} \leq \frac{1}{2}U_{dc} \cdot (M_1 + M_2) = U_{dc}. \quad (9)$$

That is, the maximum voltage between two AC ports of a_1 and b_2 is U_{dc}. As there are $2n$ FBSMs and $2m$ HBSMs in this path, the voltage formed by FBSMs and HBSMs on this path is $(m + 2n)U_c$, according to Figure 5c,d. The total capacitor voltage $(m + 2n)U_c$ is greater than U_{dc}

because $U_c = U_{dc}/(m+n)$. Therefore, any relationship between m and n in this case can keep the possible fault current under control.

3.3. Same Port of the Different Phase

The fault current path shown in Figure 9 is formed by the two upper (lower) output ports and the upper (lower) arm of the different phase. This type of fault current does not pass through the DC side, but a large current can also be generated between the different ports through the upper or lower arms.

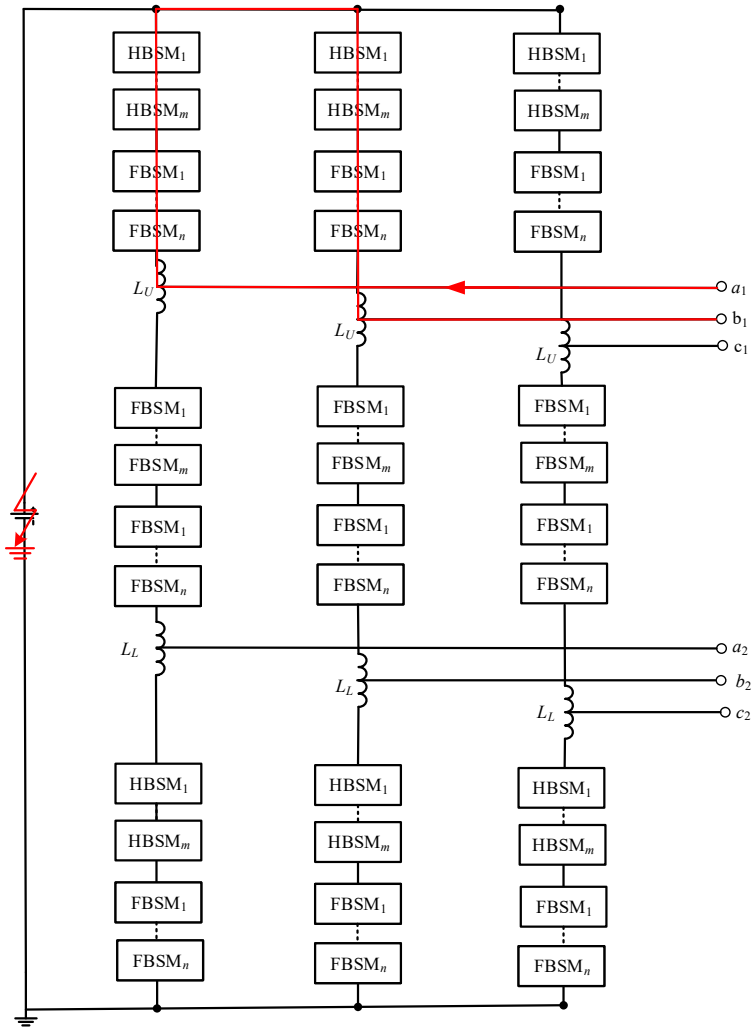


Figure 9. Potential flow path of short-circuit current (a_1–b_1).

Take the upper output port a_1 and the other upper output port b_1 as the example. Assuming that $\psi_1 = \psi_2 = 0$, $\theta_1 = 0$, and $\theta_2 = 2\pi/3$, the voltage difference between these two ports is

$$u_{a1b2} = \frac{1}{2}U_{dc}[M_1 sin\omega_1 t - M_1 sin(\omega_1 t - \frac{2\pi}{3})]. \quad (10)$$

Then the maximum magnitude of u_{a1b1} is

$$U_{a1b2(max)} = \frac{\sqrt{3}}{4}U_{dc}. \quad (11)$$

Based on Figure 5c,d, the voltage formed by SMs in this path is $(m+2n)U_c$, or $(m+2n)U_{dc}/(m+n)$, since the capacitor voltage of each SM is controlled to be $U_c = U_{dc}/(m+n)$,

which is absolutely larger than $U_{a1b2(max)}$. In order to control the cost and to maintain the ability of DC fault self-cleaning, $n/m = 1$ is the most suitable ratio for the upper and lower arms.

The characteristics of the HBSM based nine-arm inverter (HBSM based NA inverter), the FBSM based high-voltage nine-arm inverter (FBSM based NA Inverter), and the proposed hybrid nine-arm inverter (Hybrid NA inverter) are summarized in Table 1.

Table 1. Comparison between HBSM based NA inverter, FBSM based NA inverter, and hybrid NA inverter.

Items	HBSM Based NA Inverter	FBSM Based NA Inverter	Hybrid NA Inverter
Cells per arm	N	N	N (HBSM:FBSM = 1:1)
IGBTs per phase	6 N	12 N	10 N
DC fault blocking	No	Yes	Yes
Conduction loss	Low	High	Medium

4. Simulation Results

To verify the operating scheme and theoretical analysis of the hybrid nine-arm high-voltage inverter presented in this paper, a simulation model of the proposed inverter, which has the same configuration as shown in Figure 2, was set up in MATLAB/SIMULATION. The parameters of the simulation model are listed in Table 2.

Table 2. Simulation parameters.

Items	Values
U_{dc}	1 kV
m	2
n	2
$N = m + n$	4
u_{a1-ref}	$0.9\sin(100\pi t)$
u_{b1-ref}	$0.8\sin(100\pi t) - 0.1$
f_c	2 kHz

Some key waveforms of the proposed hybrid nine-arm high-voltage inverter are shown in Figure 10. Figure 10a,c shows the line-to-line voltages of the upper and lower output ports, respectively. Figure 10b shows the three-phase current of the upper output port and Figure 10d shows the DC side voltage of the proposed inverter.

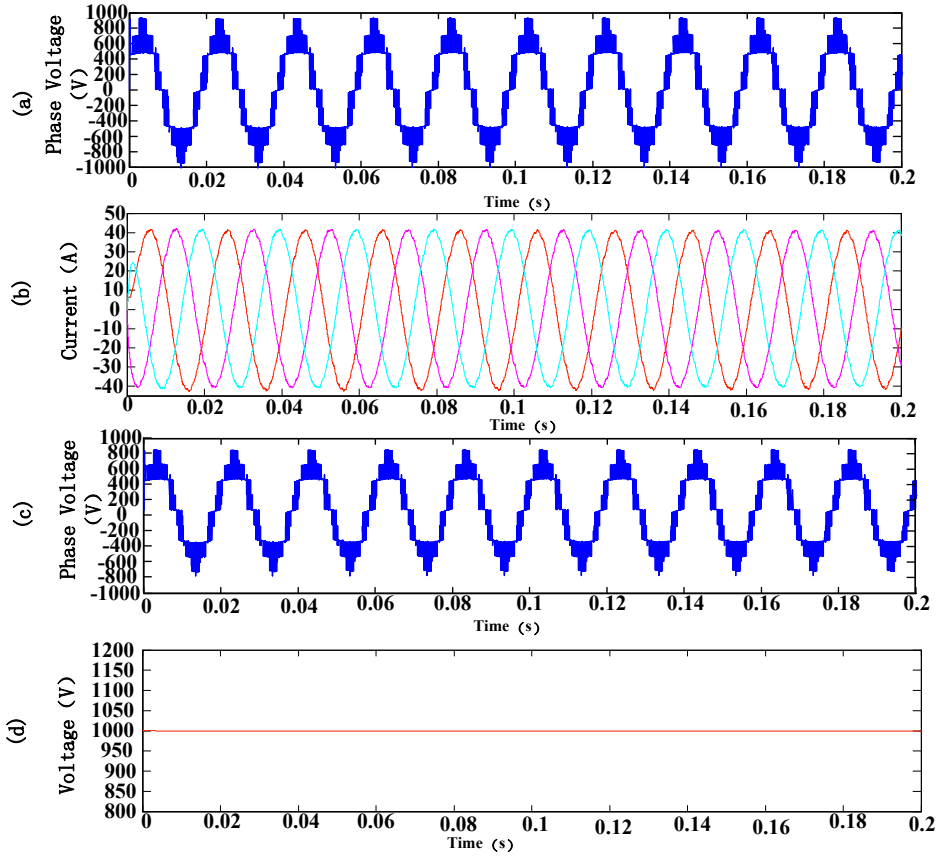


Figure 10. Simulation results of the hybrid nine-arm high-voltage inverter under normal condition. (**a**) Upper line voltage $(u_{a1} - u_{b1})$; (**b**) Upper output current i_{a1}, i_{b1}, i_{c1}; (**c**) Lower line voltage $(u_{a2} - u_{b2})$; and (**d**) DC side voltage U_{dc}.

In order to prove the above three fault current paths and verify the ability to clear DC fault, the hybrid nine-arm high-voltage inverter is tested by momentarily changing the DC-side voltage to zero. After the DC fault occurs, the hybrid nine-arm high-voltage inverter takes no actions and keeps operation as normal state.

Assuming that the hybrid nine-arm high-voltage inverter is in normal operation before 0.1s and the DC fault occurs at 0.1s, Figure 11 shows the current of middle arm, of which the direction is the same as in Figure 7. Figure 12 shows the current waveforms of the upper arm and lower arm when the fault current path in Figure 8 is generated. Figure 13 shows the current waveforms of different upper arms when the fault current flows in the path shown in Figure 9. It can be seen from these figures that the fault current increases at a very high speed after the DC fault occurs and the AC side continuously delivers energy to the inverter. The large fault current will damage the inverter if no protective measures are taken after 0.1 s.

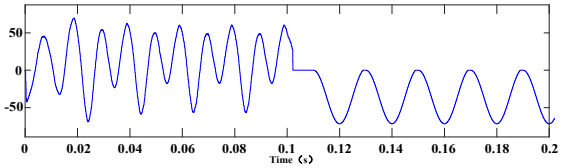
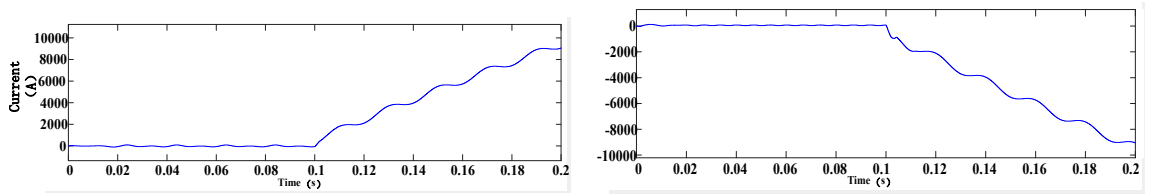
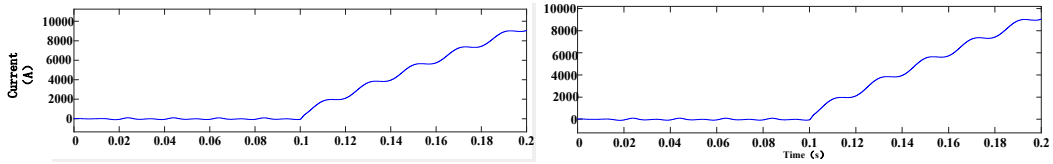


Figure 11. Arm current i_{Ma} without fault blocking.



(**a**) (**b**)

Figure 12. Arm current without fault blocking: (**a**) i_{Ua} and (**b**) i_{Lb}.



(**a**) (**b**)

Figure 13. Arm current without fault blocking (**a**) i_{Ua} (**b**) i_{Ub}.

When the DC fault happens, the DC side voltage U_{dc} drops to 0 immediately, as shown in Figure 14a. The proposed hybrid nine-arm high-voltage inverter still maintains the operating state as before at the first several milliseconds, the energy from the AC side and capacitors feed back to the DC side, then both the DC side and AC side currents increase, as shown in Figure 14b. The fault current flows through the capacitors in the FBSMs and causes its voltage to increase slightly, as seen in Figure 14c. Assume that all the IGBTs of the proposed hybrid inverter are turned off at 0.102 s. Since the total series voltage formed by the SM capacitors in the fault current flow path is greater than the AC voltage, the arm current quickly reduces to zero, then there is no energy exchange between the DC side and the AC side. After the DC fault is cleared, no current flows through the capacitors and the capacitor voltage remains unchanged.

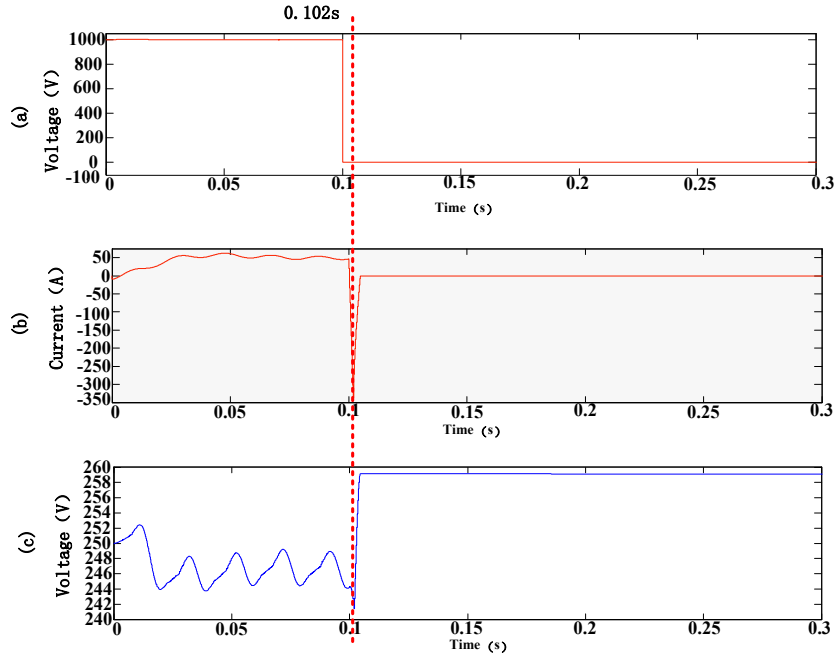


Figure 14. Simulation results of the hybrid nine-arm high-voltage inverter when a DC-side fault occurs 0.1s. (**a**) DC side voltage U_{dc}; (**b**) DC side current I_{dc}; (**c**) Capacitor voltage U_c.

Figure 15 shows the upper arm currents of phase *a* and phase *c* with the peak values 197 A and 157 A, respectively. In fact, the fault current will not exceed the preset current threshold. Obviously, the above simulation results prove that the proposed hybrid nine-arm high-voltage inverter has the DC fault blocking capability.

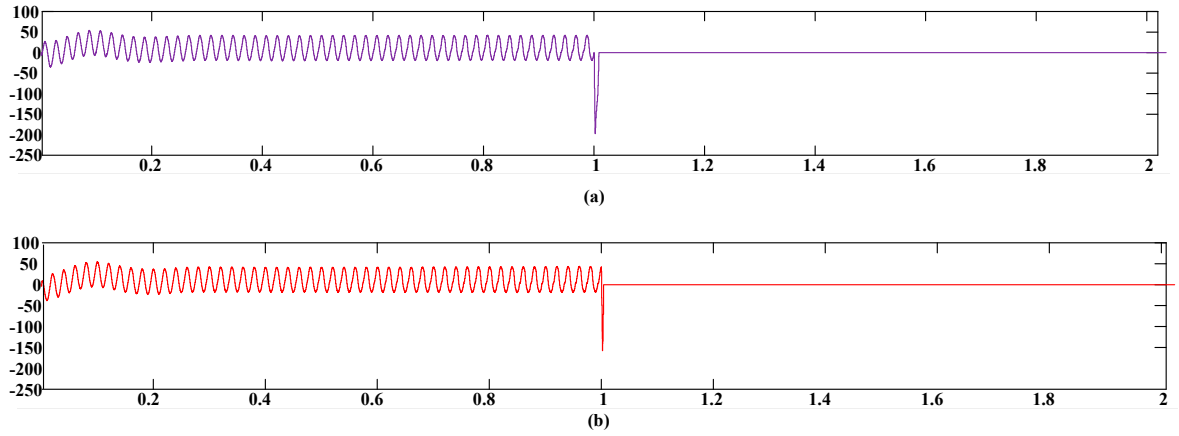


Figure 15. Arm Current with fault blocking: (**a**) i_{Ua} and (**b**) i_{Uc}.

5. Conclusions

This paper proposes a hybrid nine-arm high-voltage inverter configuration consisting of FBSMs and HBSMs, in which FBSM is utilized to suppress the DC fault current and HBSM is used to reduce the device number and power consumption. As a result, the hybrid nine-arm high-voltage inverter has inherent DC fault reverse-blocking capability. By analyzing the magnitude of AC voltage between the different output ports after the DC-side short circuit fault occurs, the most economical ratio between HBSM and FBSM can be obtained. From simulation results, the proposed hybrid inverter can successfully prevent energy transfer from the AC side to the DC side and clear the DC side fault shortly after a fault occurs on the DC side. The fault analysis method of the proposed hybrid nine-arm high-voltage inverter can be extended to multi-port converters with more ports.

Author Contributions: Conceptualization, L.J. and D.Q.; Methodology, D.Q. and L.J.; Writing, L.J. and D.Q.; Revised and guided, B.Z. and Y.C.

Funding: This work was supported in part by the Team Program of Natural Science Foundation of Guangdong Province, China (Grant No. 2017B030312001).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Faraji, R.; Farzanehfard, H. Soft-switched Non-Isolated High Step-up Three-port DC–DC converter for Hybrid Energy Systems. *IEEE Trans. Power Electron.* **2018**, *33*, 10101–10111. [CrossRef]
2. Qian, Z.; Abdelrahman, O.; Alatrash, H.; Batarseh, I. Modeling and Control of Three-Port DC/DC Converter Interface for Satellite Applications. *IEEE Trans. Power Electron.* **2010**, *25*, 637–649. [CrossRef]
3. Sathyan, S.; Suryawanshi, H.; Shitole, A.; Ballal, M.; Borghate, V. Soft-Switched Interleaved DC/DC Converter as Front-End of Multi-Inverter Structure for Micro Grid Applications. *IEEE Trans. Power Electron.* **2018**, *33*, 7645–7655. [CrossRef]
4. Ding, Z.; Yang, C.; Zhang, Z.; Wang, C.; Xie, S. A Novel Soft-Switching Multiport Bidirectional DC–DC Converter for Hybrid Energy Storage System. *IEEE Trans. Power Electron.* **2014**, *29*, 1595–1609. [CrossRef]
5. Xu, L.; Yao, L. DC voltage control and power dispatch of a multi-terminal HVDC system for integrating large offshore wind farms. *IET Renew Power Gen.* **2011**, *5*, 223–233. [CrossRef]
6. Zhang, B.; Qiu, D. *Multiple-Terminal High-Voltage DC-DC Converters*, 1st ed.; Wiley-IEEE Press: Hoboken, NJ, USA, 2019; pp. 10–56.

7. Baruschka, L.; Mertens, A. A New Three-Phase AC/AC Modular Multilevel Converter with Six Branches in Hexagonal Configuration. *IEEE Trans. Ind. Appl.* **2013**, *49*, 1400–1410. [CrossRef]
8. Wang, P.; Liu, F.; Zha, X.; Gong, J.; Zhu, F.; Xiong, X. A Regenerative Hexagonal Cascaded Multilevel Converter for Two-Motor Asynchronous Drive. *IEEE J. Sel. Topics Power Electron.* **2017**, *5*, 1687–1699. [CrossRef]
9. Kominami, T.; Fujimoto, Y. Inverter with Reduced Switching-Device Count for Independent AC Motor Control. In Proceedings of the IECON 2007–33rd Annual Conference of the IEEE Industrial Electronics Society, Taipei, Taiwan, 5–8 November 2007; pp. 1559–1564.
10. Fu, J.; Zhang, B.; Qiu, D. A Novel Nine-Arm Modular Multilevel Converter. In Proceedings of the 2014 40th IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014; pp. 4528–4533.
11. Glinka, M.; Marquardt, R. A new AC/AC multilevel converter family. *IEEE Trans. Ind. Electron.* **2005**, *52*, 662–669. [CrossRef]
12. Wang, Z.; Lin, H.; Ma, Y. A Control Strategy of Modular Multilevel Converter with Integrated Battery Energy Storage System Based on Battery Side Capacitor Voltage Control. *Energies* **2019**, *12*, 2151. [CrossRef]
13. Rohner, S.; Bernet, S.; Hiller, M.; Sommer, R. Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2633–2642. [CrossRef]
14. Perez, M.A.; Bernet, S.; Rodriguez, J.; Kouro, S.; Lizana, R. Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 4–17. [CrossRef]
15. Cai, W.; Yi, F. Topology simplification method based on switch multiplexing technique to deliver DC-DC-AC converters for microgrid applications. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; pp. 6667–6674.
16. Uno, M.; Sugiyama, K. Switched Capacitor Converter-Based Multi-Port Converter Integrating Bidirectional PWM and Series-Resonant Converters for Standalone Photovoltaic Systems. *IEEE Trans. Power Electron.* **2018**, *34*, 1394–1406. [CrossRef]
17. Tang, G.; Xu, Z.; Zhou, Y. Impacts of Three MMC-HVDC Configurations on AC System Stability under DC Line Faults. *IEEE Trans. Power Syst.* **2014**, *29*, 3030–3040. [CrossRef]
18. Li, C.; Gole, A.M.; Zhao, C. A Fast DC Fault Detection Method Using DC Reactor Voltages in HVdc Grids. *IEEE Trans. Power Deliv.* **2018**, 2254–2264. [CrossRef]
19. Zhu, J.; Wei, T.; Huo, Q.; Yin, J. A Full-bridge Director Switches based Multilevel Converter with DC Fault Blocking Capability and Its Predictive Control Strategy. *Energies* **2019**, *12*, 91. [CrossRef]
20. Li, X.; Song, Q.; Liu, W.; Rao, H.; Xu, S.; Li, L. Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems. *IEEE Trans. Power Deliv.* **2012**, *28*, 483–490. [CrossRef]
21. Yu, X.; Wei, Y.; Jiang, Q. STATCOM Operation Scheme of the CDSM-MMC during a Pole-to-pole DC Fault. *IEEE Trans. Power Deliv.* **2016**, *31*, 1150–1159. [CrossRef]
22. Hu, J.; Xu, K.; Lin, L.; Zeng, R. Analysis and Enhanced Control of Hybrid-MMC-Based HVDC Systems During Asymmetrical DC Voltage Faults. *IEEE Trans. Power Deliv.* **2017**, *32*, 1394–1403. [CrossRef]
23. Jung, J.J.; Cui, S.; Lee, J.H.; Sul, S.K. A New Topology of Multilevel VSC Converter for a Hybrid HVDC Transmission System. *IEEE Trans. Power Electron.* **2017**, *32*, 4199–4209. [CrossRef]
24. Cai, X.; Wu, Z.; Li, Q.; Wang, S. Phase-Shifted Carrier Pulse Width Modulation Based on Particle Swarm Optimization for Cascaded H bridge Multilevel Inverters with Unequal DC Voltages. *Energies* **2015**, *8*, 9670–9687. [CrossRef]