

Article

Control for Three-Phase LCL-Filter PWM Rectifier with BESS-Oriented Application

Dante Mora, **Ciro Núñez ***, Nancy Visairo , Juan Segundo and Eugenio Camargo

Faculty of Engineering, University of San Luis Potosí, San Luis Potosí 78290, Mexico; dante.mora32@gmail.com (D.M.); nvisairoc@uaslp.mx (N.V.); juan.segundo@uaslp.mx (J.S.); eugenio_camargo2000@yahoo.com.mx (E.C.)

* Correspondence: calberto@uaslp.mx; Tel.: +52-444-826-2300 (ext. 6264)

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Abstract: This paper deals with a battery energy storage system (BESS) in only one of its multiple operating modes, that is when the BESS is charging the battery bank and with the focus on the control scheme design for the BESS input stage, which is a three-phase LCL-filter PWM rectifier. The rectifier's main requirements comprise output voltage regulation, power factor control, and low input current harmonic distortion, even in the presence of input voltage variations. Typically, these objectives are modeled by using a dq model with its corresponding two-loop controller architecture, including an outer voltage loop and a current internal loop. This paper outlines an alternative approach to tackle the problem by using not only an input–output map linearization controller, with the aim of a single-loop current control, but also by avoiding the dq modeling. In this case, the voltage is indirectly controlled by computing the current references based on the converter power balance. The mathematical model of the three-phase LCL-filter PWM rectifier is defined based on the delta connection of the filter, which accomplishes the requirements of a 100 kW BESS module. Extensive simulation results are included to confirm the performance of the proposed closed-loop control in practical applications.

Keywords: battery energy storage system (BESS); LCL filter; PWM rectifier; nonlinear control; tracking problem

1. Introduction

The three-phase PWM voltage source rectifiers are broadly used in several industrial applications, such as battery energy storage systems (BESSs), which have been firmly increasing in installed power worldwide since 2015 [1–4]. Actually, as a starting background, a BESS must work in current and voltage control modes either for discharging energy to the grid or charging the battery bank [2]. Until now, this implies the use of several control-loops for complying with the battery-tied and the grid-tied requirements, which are typically carried out by two front-end converters (dc–dc and dc–ac) [2]. Concerning the PWM rectifier, the converter is widely used due to its well-known technical features: dc bus voltage regulation, near unity power factor, and sinusoidal currents with low total harmonic distortion (THD) as well [5–8].

To reduce high-frequency harmonic contents, according to the international standards such as IEEE519 and IEC 1000-3-2, the PWM rectifier is connected to the grid through an LCL filter for medium power applications. This type of filter leads not only to better mitigation of switching harmonics with lower inductances but also allows compliance with the voltage and current control modes when the converter delivers energy to the grid [9–12].

Regarding the rectifier mode operation, the most common control architecture found in the literature consists of two control loops (voltage and current) using PI or nonlinear controllers applying abc–dq–abc transformations [13–17]. In contrast, there are other control techniques for three-phase

rectifiers, such as direct power control [18], which is similar to direct torque control [19]. In this control scheme, the switching states are selected based on a table, which avoids the current regulation loop. However, the control architecture relies on two power control loops. Additionally, the indirect power control or voltage oriented control requires two control loops as well [20]: current regulation loop and outer voltage loop [6]. The latter mentioned control algorithm requires Clark–Park transformations, and the computational burden per sampling is high [19].

Additionally, the hysteresis current control is simpler than the previously mentioned controllers [21]. This technique relies on variable switching frequency, which highly depends on the correct choice of the hysteresis band for proper system operation. Once the current reference is obtained, the hysteresis controller block generates the switching pattern, which results in more semiconductor power losses when the frequency rises at the upper band, and the parameter sensitivity is critical if an adaptive control technique is not used [19,21–23].

Up to now, several papers have reported the rectifier control design based on the dq transformation to compute the compensation references [5,7,8,11–13,15,19,23,24]. In these methods, the outer voltage loop generates a current command for the d-axis current and controls the dc bus voltage, while the inner current loop generates a q-axis current to modify the power factor. The relevant reason for using such a transformation is that the tracking problem is turned into a regulation problem in a dq synchronous frame [25]. Although it implies a certain degree of delay due to the transformation itself, it is still a common practice in this type of system [26]. According to the above methods, some controllers have also been proposed in the literature to obtain the main rectifier control objectives with additional features, such as voltage sag ride-through capabilities [27–29]. Additionally, when a controller is tuned in the dq domain, the dq and its inverse conversions should be perfectly synchronized with the grid; otherwise, these could work incorrectly, causing frequency variations.

Identified key features within much of the reviewed literature are the use of the dq transformations on the one hand and the use of two control-loop schemes on the other hand. The hypothesis of this paper is that even excluding these traditional control scheme characteristics, it is still possible to comply with the rectifier requirements and obtain a reduced control concept within a BESS. Therefore, the aim of this research is to analyze, design, and validate an alternative control scheme for a three-phase LCL-filter PWM rectifier that fulfills the requirements of a BESS module.

Unlike the conventional approaches, this paper proposes a straightforward control scheme that directly solves the tracking problem in the time domain, and consequently, it avoids the synchronous dq stages. Additionally, the two-loop control architecture is avoided by using a single-loop current control based on its input-output feedback linearization, where the current references are generated with the power balance concept. In this research work, we considered the BESS requirements when it works as a charger, and we focused the analysis in the control scheme design for the three-phase LCL-filter PWM rectifier stage. We undertook this research to develop a reduced control scheme concept that can be thought and adapted to other BESS power stages, and the traditional overall control concept is reduced.

The methodology chosen for our research is mainly based on the analysis of the line-to-line model to simplify the control design and the extension of it to the three-phase case. In summary, the problem to address is organized in this paper as follows. The second section describes the PWM rectifier and the filter stages within the BESS. The third section is dedicated to the development of the PWM rectifier model with the delta-connected LCL filter. The fourth section analyzes the closed-loop system based on the proposed nonlinear controller. The fifth section presents a set of simulations with the fulfillment of the corresponding BESS requirements. Then, some conclusions are drawn in the final section.

2. PWM Rectifier Topology within the BESS

Among the BESS solutions, the modular options are the most popular in the market owing to the characteristics of mobility and ease of increasing installed power [30]. Whereas the former is useful in placing the BESS as needed in the grid, the latter refers to connecting parallel modules (in a container)

to typically reach a rated power from 1 MW to 2 MW depending on the battery technology [1,2,26]. The modular topology presented in [26,31] (see Figure 1) is a suitable option for a medium power rating. The BESS comprises two main power stages: the dc-dc stage fulfills the battery bank requirements, while the dc-ac stage accomplishes the utility requirements through the LCL filter.

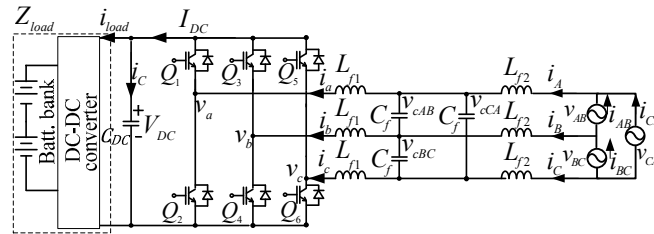


Figure 1. PWM rectifier with delta-LCL filter within the battery energy storage system (BESS) module.

The LCL filter is mainly designed to comply with the harmonic requirements when the BESS works as a load and as a power source, but it also allows the BESS to operate as a current source or as a voltage source. Nonetheless, there are some filter design constraints to consider, such as total impedance, current ripple through inductors, reactive power absorbed by filter capacitors, and resonance [10–12].

Furthermore, when the BESS delivers energy to the grid, the LCL filter is in delta connection because the battery bank voltage reference imposes how the dc bus voltage feeds the dc-ac stage [26]. This power stage works as a three-phase PWM rectifier to feed the dc-dc stage for charging the battery bank. For this purpose, the rectifier boosts the input voltages (v_{AB} , v_{BC} , and v_{CA}) to the dc bus voltage V_{DC} ; besides, the input currents (i_{AB} , i_{BC} , and i_{CA}) are indirectly controlled through the inductor currents (i_A , i_B , and i_C) of each L_{f2} to fulfill the grid requirements. These grid-tied inductors are designed with a slight voltage drop so that the capacitor voltages (v_{cAB} , v_{cBC} , and v_{cCA}) are similar to the input voltages [32]. Finally, the dc bus current I_{DC} is the result of each rectifier-tied inductor current (i_a , i_b , and i_c). As a result, the mentioned characteristics define the converter topology to model.

3. Phase-Phase PWM Rectifier Model

Two considerations are established to analyze the three-phase PWM rectifier of Figure 1:

- Assume that Z_{load} represents the combined battery bank and dc-dc converter dynamics. Hence, Z_{load} is computed with the sensed delivered current i_{load} and the sensed output voltage, as specified in Equation (1). This consideration is valid due to the decoupling capacitor C_{DC} that allows the modeling of each power stage separately.
- Full-bridge converter model, formed by the line-to-line v_{AB} , is obtained. This consideration is given for a considered three-phase balanced system where the converter and its voltage sensors are naturally delta-connected.

The corresponding switching states that generate the output voltage $v_{ab} = v_a - v_b$ are shown in Table 1. The switching states sw_1 and sw_2 , which are, respectively, associated with Q_1 and Q_3 , simplify the model analysis by stating: $v_{AB} = V_{DC}(sw_1 - sw_2)$ and $I_{DC(ab)} = i_{ab}(sw_1 - sw_2)$, where sw_1 , and $sw_2 \in \{1, 0\}$ are the switching functions and the dc bus current $I_{DC(ab)}$ is formed with the corresponding current phases (i_a and i_b).

Table 1. Switching states for the line-to-line v_{AB} circuit.

Mode	Q_1	Q_2	Q_3	Q_4	sw_1	sw_2	v_{ab}	$I_{DC(ab)}$
I	0	1	0	1	1	1	0	0
II	0	1	1	0	0	1	$-V_{DC}$	$-i_{ab}$
III	1	0	0	1	1	0	V_{DC}	i_{ab}
IV	1	0	1	0	0	0	0	0

$$Z_{load} = \frac{V_{DC}}{i_{load}} \tag{1}$$

Besides, the input current i_{AB} in the delta connected source is computed with Equation (2), based on the sensed current at each inductor L_{f2} .

$$i_{AB} = \frac{1}{3}(i_A - i_B) \tag{2}$$

The previous considerations lead to the equivalent phase–phase circuit model of Figure 2, where $d_1, d_2 \in (0,1)$ are the averaged functions of sw_1 and sw_2 , respectively, and $d_{12} = d_1 - d_2 \in (-1, 1)$. Current $i_{AB} = (i_A - i_B)/3$, and the dc bus current is given by the function $d_{12}i_{ab}$ where $i_{ab} = i_a - i_b$.

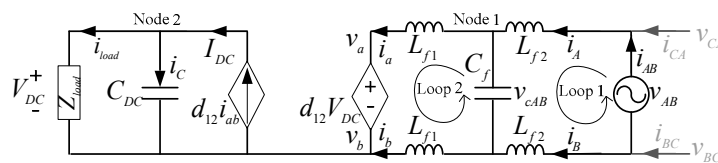


Figure 2. Equivalent line-to-line v_{AB} PWM rectifier circuit.

By analyzing the bold circuit with Kirchhoff’s voltage and current laws (KVL and KCL, respectively), the mathematical model is expressed in Equation (3). The first and the second expressions describe the KVL for loops one and two, where the source current i_{AB} and the current through inductors L_{f2} are obtained as state variables, respectively. Similarly, the third and the fourth expressions describe the KCL at nodes one and two, where the capacitor voltage v_{cAB} and the dc bus voltage V_{DC} are obtained as state variables, respectively.

$$\frac{di_{AB}}{dt} = \frac{v_{AB}}{3L_{f2}} - \frac{v_{cAB}}{3L_{f2}} \frac{di_{ab}}{dt} = \frac{v_{cAB}}{3L_{f1}} - \frac{V_{DC}}{3L_{f1}} d_{12} \frac{dv_{cAB}}{dt} = \frac{3i_{AB}}{C_f} - \frac{3i_{ab}}{C_f} \frac{dV_{DC}}{dt} = \frac{i_{ab}}{C_{DC}} d_{12} - \frac{V_{DC}}{Z_{load}C_{DC}} \tag{3}$$

Defining $\tilde{x} = (\tilde{x}_1 \tilde{x}_2 \tilde{x}_3 \tilde{x}_4)'$ as the state variables of $(i_{AB} i_{ab} v_{cAB} V_{DC})'$, respectively and the line-to-line control as $d_{12} = u_{ab}$; then, the corresponding state-space system in matrix form is shown in Equation (4).

$$\begin{bmatrix} \dot{\tilde{x}}_1 \\ \dot{\tilde{x}}_2 \\ \dot{\tilde{x}}_3 \\ \dot{\tilde{x}}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{3L_{f2}} & 0 \\ 0 & 0 & \frac{1}{3L_{f1}} & \frac{-u_{ab}}{3L_{f1}} \\ \frac{3}{C_f} & \frac{-3}{C_f} & 0 & 0 \\ 0 & \frac{u_{ab}}{C_{DC}} & 0 & \frac{-1}{Z_{load}C_{DC}} \end{bmatrix} \begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \\ \tilde{x}_3 \\ \tilde{x}_4 \end{bmatrix} + \begin{bmatrix} \frac{v_{AB}}{3L_{f2}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4}$$

The state-space system can be expressed in its input-affine nonlinear form $\dot{\tilde{x}} = f(\tilde{x}) + g(\tilde{x})u_{ab}$, which is described in Equation (5).

$$\dot{\tilde{x}} = \begin{bmatrix} \frac{-\tilde{x}_3 + v_{AB}}{3L_{f2}} \\ \tilde{x}_3 \\ \frac{3(\tilde{x}_1 - \tilde{x}_2)}{C_f} \\ \frac{-\tilde{x}_4}{Z_{load}C_{DC}} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{-\tilde{x}_4}{3L_{f1}} \\ 0 \\ \frac{\tilde{x}_2}{C_{DC}} \end{bmatrix} u_{ab} \tag{5}$$

In this research paper, all sensors are considered available to obtain the physical variables for the control loop, since these sensors are typically used in a power converter. Besides, the sinusoidal PWM (SPWM) technique is considered due to its simplicity to prove the proposed control.

4. Nonlinear Control Design Based on Input-Output Map Linearization

The control scheme is developed using the line-to-line model. Its merit lies in the opportunity to avoid abc–dq–abc transformations and double control loops. Hence, to pinpoint the control design, the control objectives should be considered:

- To regulate the dc bus voltage for a given duty cycle, even with input voltage variations.
- To produce a low-harmonic distortion of the input current signal. In this case, the THD should be lower than 5%.
- To accomplish a near unity input power factor. For this task the current i_{AB} must track the input voltage v_{AB} .

The first objective, which is naturally the main function of the rectifier itself, is a sufficient task because the converter acts as a voltage source for the dc-dc stage that should be designed to withstand input voltage disturbances. In contrast, the other two control objectives are needed to comply with the power quality requirements described in IEEE-519. These control objectives are achieved with the proposed control scheme of Figure 3. It mainly consists of a single-loop nonlinear controller and a current reference generator.

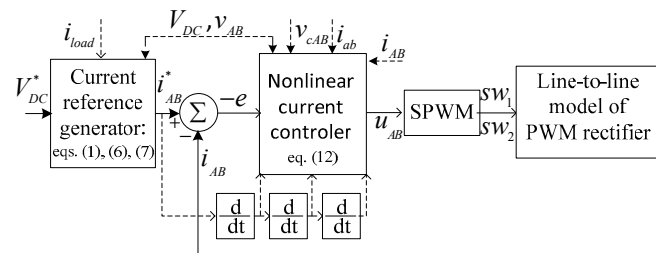


Figure 3. The proposed control scheme for the line-to-line v_{AB} circuit.

To compute the current reference, the power balance between the ac side and the dc side is considered. Then, by matching the input power P_{AC} described by Equation (6) to the output power P_{DC} described by Equation (7), the peak current I_p^* can be obtained, as shown in Equation (8), where V_p is the peak grid voltage, V_{DC}^* is the desired dc bus voltage, and i_{load}^* is the load current computed with Z_{load} from Equation (1) as $i_{load}^* = V_{DC}^* / Z_{load}$.

$$P_{AC} = \frac{3V_p I_p^*}{2} \tag{6}$$

$$P_{DC} = V_{DC}^* i_{load}^* \tag{7}$$

$$I_p^* = \frac{2V_{DC}^{*2}}{3V_p Z_{load}} \tag{8}$$

Given I_p^* , the instantaneous current reference i_{AB}^* is computed with Equation (9), where the reference must be in phase (ϕ) with the line-to-line voltage v_{AB} to approach a unitary power factor.

$$i_{AB}^* = r_{AB} = I_p^* \sin(2\pi ft + \phi) \tag{9}$$

The tracking problem is solved with the control law u_{ab} by using the input-output map linearization of Equation (4) to simplify the analysis. The bilinear system has a relative degree of $\rho = 3$ with $h(\tilde{x}) = \tilde{x}_1$, so that its diffeomorphism $\tilde{T}_{AB}(\tilde{x})$ is defined in Equation (10), where $L_f^i h(\tilde{x})$ is the i -th derivative of Lie and $\phi(\tilde{x})$ satisfies $L_\phi g(\tilde{x}) = 0$ and $g(0) = 0$. The normal form is given in Equation (11), which is obtained with Equation (10), where $\eta \in \mathbb{R}$ and $\xi \in \mathbb{R}^3$.

$$\tilde{T}_{AB}(\tilde{x}) = \begin{bmatrix} \eta \\ \xi_1 \\ \xi_2 \\ \xi_3 \end{bmatrix} = \begin{bmatrix} \phi(\tilde{x}) \\ h(\tilde{x}) \\ L_f h(\tilde{x}) \\ L_f^2 h(\tilde{x}) \end{bmatrix} = \begin{bmatrix} \frac{C_{DC}\tilde{x}_4^2 + 3L_{f1}\tilde{x}_2^2}{C_{DC}} \\ \tilde{x}_1 \\ \frac{-\tilde{x}_3}{3L_{f2}} + \frac{v_{AB}}{3L_{f2}} \\ \frac{-1}{3L_{f2}C_f}(\tilde{x}_1 - \tilde{x}_2) \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} \dot{\eta} \\ \dot{\xi}_1 \\ \dot{\xi}_2 \\ \dot{\xi}_3 \end{bmatrix} = \begin{bmatrix} \frac{2(L_{f2}C_f\xi_3 + \xi_1)(v_{AB} - 3L_{f2}\xi_2)}{C_{DC}} - \frac{2(\eta C_{DC} - 3L_{f1}(L_{f2}C_f\xi_3 + \xi_1)^2)}{Z_{load}C_{DC}^2} \\ \xi_2 \\ \xi_3 \\ \frac{-1}{3L_{f1}L_{f2}C_f} \left[\sqrt{\frac{\eta C_{DC} - 3L_{f1}(L_{f2}C_f\xi_3 + \xi_1)^2}{C_{DC}}} u_{AB} - v_{AB} + 3L_{f1}L_{f2}\xi_2 \right] \end{bmatrix} \quad (11)$$

The internal dynamics is restricted to $z^* = \{\tilde{x} \in \mathbb{R}^4 \mid h(\tilde{x}) = L_f h(\tilde{x}) = L_f^2 h(\tilde{x}) = 0\} = \{\tilde{x} \in \mathbb{R}^4 \mid \tilde{x}_1 = 0, \tilde{x}_3 = v_{AB}, \tilde{x}_2 = 0\}$. As a result, the zero dynamics is described by Equation (12), which is asymptotically stable for $Z_{load} > 0$ and $C_{DC} > 0$.

$$\dot{\tilde{\eta}} = f_0(\tilde{\eta}, 0) = \frac{-2}{C_{DC}Z_{load}}\tilde{\eta} \quad (12)$$

By defining $e = h(x) - r_{AB}$ and assuming that:

- The current reference r_{AB} and its derivatives up to \ddot{r}_{AB} are bounded for all $t \geq 0$ and \ddot{r}_{AB} is a piecewise continuous function of t , and
- The signals $r_{AB}, \dots, \ddot{r}_{AB}$ are available online,

the external dynamics can be linearized by using the control law (Equation (13)).

$$\tilde{u}_{AB} = \tilde{\alpha}_{AB}(\tilde{x}) + \tilde{\beta}(\tilde{x})\{-\tilde{K}[\tilde{T}_{AB}^{\rho}(\tilde{x}) - \tilde{R}_{AB}] + \ddot{r}_{AB}\} \quad (13)$$

where

$$\begin{aligned} \tilde{\alpha}_{AB}(\tilde{x}) &= \frac{-L_f^3 h(\tilde{x})}{L_g L_f^2 h(\tilde{x})} = \frac{L_{f1}}{\tilde{x}_4} \left[\frac{\tilde{x}_3}{L_{f1}} + \frac{\tilde{x}_3}{L_{f2}} - \frac{v_{AB}}{L_{f2}} \right] \\ \tilde{\beta}(\tilde{x}) &= \frac{1}{\gamma(\tilde{x})} = \frac{L_{f1}}{L_g L_f^2 h(\tilde{x})} = \frac{-3L_{f1}L_{f2}C_f}{\tilde{x}_4} \\ \tilde{K} &= [k_1 \ k_2 \ k_3], \quad \tilde{R}_{AB} = [r_{AB} \ \dot{r}_{AB} \ \ddot{r}_{AB}]' \end{aligned}$$

\tilde{T}_{AB}^{ρ} the last ρ components of the diffeomorphism.

5. Modeling and Control for Three-Phase PWM Rectifier

The strategy of using the line-to-line model to tune the nonlinear control gains leads to computing vector $\tilde{K}_{1 \times 3}$, for solving the tracking problem, instead of computing a matrix $K_{3 \times 9}$ for the three-phase model. For analyzing the three-phase rectifier, the following model based on the extension of (4) is considered:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \vdots \\ \dot{x}_{10} \end{bmatrix} = \begin{bmatrix} 0_{3 \times 3} & 0_{3 \times 3} & \mathbf{M}_1 & 0_{3 \times 1} \\ 0_{3 \times 3} & 0_{3 \times 3} & \mathbf{M}_2 & \mathbf{M}_3 \\ \mathbf{M}_4 & -\mathbf{M}_4 & 0_{3 \times 3} & 0_{3 \times 1} \\ 0_{1 \times 3} & \mathbf{M}_5 & 0_{1 \times 3} & \frac{-1}{Z_{load}C_{DC}} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_{10} \end{bmatrix} + \begin{bmatrix} \frac{v_{AB}}{3L_{f2}} \\ \frac{v_{BC}}{3L_{f2}} \\ \frac{v_{CA}}{3L_{f2}} \\ 0_{7 \times 1} \end{bmatrix} \quad (14)$$

where $(x_1 \ x_2 \ x_3 \ x_4 \ x_5 \ x_6 \ x_7 \ x_8 \ x_9 \ x_{10})'$ are defined as the state variables of $(i_{AB} \ i_{BC} \ i_{CA} \ i_{ab} \ i_{bc} \ i_{ca} \ v_{cAB} \ v_{cBC} \ v_{cCA} \ V_{DC})'$ respectively, and:

$$M_1 = \begin{bmatrix} \frac{-1}{3L_{f2}} & 0 & 0 \\ 0 & \frac{-1}{3L_{f2}} & 0 \\ 0 & 0 & \frac{-1}{3L_{f2}} \end{bmatrix}, M_2 = \begin{bmatrix} \frac{-1}{3L_{f1}} & 0 & 0 \\ 0 & \frac{-1}{3L_{f1}} & 0 \\ 0 & 0 & \frac{-1}{3L_{f1}} \end{bmatrix}, M_3 = \begin{bmatrix} \frac{-u_{AB}}{3L_{f1}} \\ \frac{-u_{BC}}{3L_{f1}} \\ \frac{-u_{CA}}{3L_{f1}} \end{bmatrix}, M_4 = \begin{bmatrix} \frac{3}{C_f} & 0 & 0 \\ 0 & \frac{3}{C_f} & 0 \\ 0 & 0 & \frac{3}{C_f} \end{bmatrix}, M_5 = \begin{bmatrix} \frac{u_{AB}}{C_{DC}} & \frac{u_{BC}}{C_{DC}} & \frac{u_{CA}}{C_{DC}} \end{bmatrix}.$$

For the three-phase rectifier control, consider $(h_1(x) \ h_2(x) \ h_3(x))' = (x_1 \ x_2 \ x_3)'$ and its relative grade vector as $\rho = (3 \ 3 \ 3)$, let T_{AB}^ρ , T_{BC}^ρ , and T_{CA}^ρ be the last ρ components of the diffeomorphism for each line-to-line voltage sub-circuit described as:

$$T_{AB}^\rho(x) = \begin{bmatrix} x_1 \\ \frac{-x_7}{3L_{f2}} + \frac{v_{AB}}{3L_{f2}} \\ \frac{-1}{3L_{f2}C_f}(x_1 - x_4) \end{bmatrix}, T_{BC}^\rho(x) = \begin{bmatrix} x_2 \\ \frac{-x_8}{3L_{f2}} + \frac{v_{BC}}{3L_{f2}} \\ \frac{-1}{3L_{f2}C_f}(x_2 - x_5) \end{bmatrix}, T_{CA}^\rho(x) = \begin{bmatrix} x_3 \\ \frac{-x_9}{3L_{f2}} + \frac{v_{CA}}{3L_{f2}} \\ \frac{-1}{3L_{f2}C_f}(x_3 - x_6) \end{bmatrix}$$

Then, the diffeomorphism of the three-phase PWM rectifier is described in Equation (15).

$$T(x) = \begin{bmatrix} \frac{C_{DC}x_{10}^2 + 3L_{f1}(x_4^2 + x_5^2 + x_6^2)}{C_{DC}} \\ T_{AB}^\rho(x) \\ T_{BC}^\rho(x) \\ T_{CA}^\rho(x) \end{bmatrix} \tag{15}$$

The internal dynamics is restricted to $z^* = \{x \in \mathbb{R}^{10} \mid x_1, x_2, x_3 = 0; x_4, x_5, x_6 = 0; x_7 = v_{AB}; x_8 = v_{BC}; x_9 = v_{CA}\}$. As a result, the zero dynamics is described by Equation (16), which is asymptotically stable for $Z_{load} > 0$ and $C_{DC} > 0$.

$$\dot{\eta} = f_0(\eta, 0) = \frac{-2}{C_{DC}Z_{load}}\eta \tag{16}$$

Therefore, the line-to-line control can be computed with Equations (17)–(19) for the three-phase rectifier by considering the corresponding voltages and current references.

$$u_{AB} = \frac{L_{f1}}{x_{10}} \left[\frac{x_7}{L_{f1}} + \frac{x_7 - v_{AB}}{L_{f2}} \right] + \beta(x) \left\{ -K \left[T_{AB}^\rho(x) - R_{AB} \right] + \ddot{r}_{AB} \right\} \tag{17}$$

$$u_{BC} = \frac{L_{f1}}{x_{10}} \left[\frac{x_8}{L_{f1}} + \frac{x_8 - v_{BC}}{L_{f2}} \right] + \beta(x) \left\{ -K \left[T_{BC}^\rho(x) - R_{BC} \right] + \ddot{r}_{BC} \right\} \tag{18}$$

$$u_{CA} = \frac{L_{f1}}{x_{10}} \left[\frac{x_9}{L_{f1}} + \frac{x_9 - v_{CA}}{L_{f2}} \right] + \beta(x) \left\{ -K \left[T_{CA}^\rho(x) - R_{CA} \right] + \ddot{r}_{CA} \right\} \tag{19}$$

where

$$\beta(x) = \frac{-3L_{f1}L_{f2}C_f}{x_{10}}, K = [k_1 \ k_2 \ k_3], R_{AB} = [r_{AB} \ \dot{r}_{AB} \ \ddot{r}_{AB}]', R_{BC} = [r_{BC} \ \dot{r}_{BC} \ \ddot{r}_{BC}]', R_{CA} = [r_{CA} \ \dot{r}_{CA} \ \ddot{r}_{CA}]'$$

An integral controller is included, in the nonlinear control block of Figure 3, to provide robustness to the system concerning constant parametric uncertainties that could be in the converter itself, such as parasitics and disturbances in the grid, such as voltage variations. Then, the control laws result in:

$$u_{AB} = \frac{L_{f1}}{x_{10}} \left[\frac{x_7}{L_{f1}} + \frac{x_7 - v_{AB}}{L_{f2}} \right] + \beta(x) \left\{ -K e_{AB} - k_i \int (x_1 - r_{AB}) dt + \ddot{r}_{AB} \right\} \tag{20}$$

$$u_{BC} = \frac{L_{f1}}{x_{10}} \left[\frac{x_8}{L_{f1}} + \frac{x_8 - v_{BC}}{L_{f2}} \right] + \beta(x) \left[-K e_{BC} - k_i \int (x_2 - r_{BC}) dt + \ddot{r}_{BC} \right] \tag{21}$$

$$u_{CA} = \frac{L_{f1}}{x_{10}} \left[\frac{x_9}{L_{f1}} + \frac{x_9 - v_{CA}}{L_{f2}} \right] + \beta(x) \left[-K e_{CA} - k_i \int (x_3 - r_{CA}) dt + \ddot{r}_{CA} \right] \tag{22}$$

The control objective can be met by the design of the gain values $(K k_i) = \mathcal{K}$ for the extended system, such that the matrix $\mathcal{A} - \mathcal{B}\mathcal{K}$ is Hurwitz (or stable) where \mathcal{A} and \mathcal{B} are defined in Equation (23) with A_c and B_c as the canonical representation of the ρ integrators. The tracking control problem, now converted into a stabilization one, is reduced to a problem of designing the \mathcal{K} values to assign every eigenvalue with a strictly negative real part and place them in the open left-half complex plane [33].

$$\mathcal{A} = \begin{bmatrix} A_c & 0 \\ 0 & 0 \end{bmatrix}, \mathcal{B} = \begin{bmatrix} B_c \\ 0 \end{bmatrix} \tag{23}$$

For the gain selection, the topology physical limitations should be considered given that, even with nonlinear controllers, the established objectives cannot be achieved if these limitations are exceeded. In summary, the procedure of the control design is described in Figures 4 and 5.

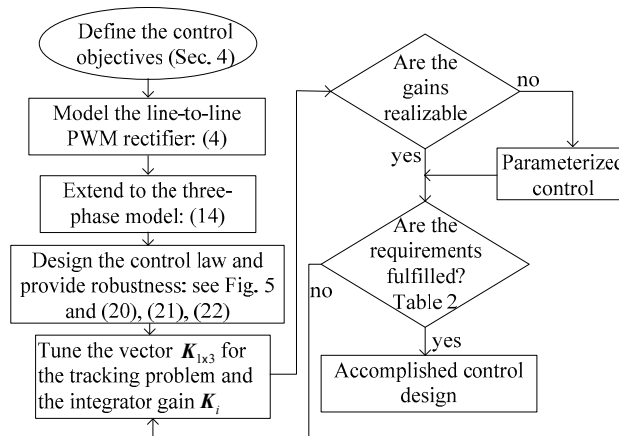


Figure 4. Procedure flowchart for the control scheme design.

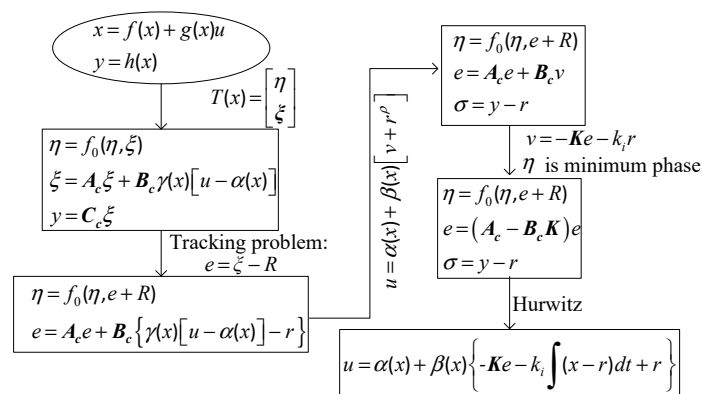


Figure 5. Procedure flowchart for the control law design.

6. Simulation Results

In this section, the main simulation results are presented to point out the control effectiveness in complying with the rectifier requirements, which are shown in Table 2 [34]. Additionally, the passive devices are sized for a 100 kW module, which is a common power rating for BESS applications [1]. The simulated system is shown in Figure 6 where the required sensed signals, according to variables of

Figure 1, are pointed out for computing the current references and the nonlinear control. According to Figure 4, a parameterization with respect to the highest value of \mathcal{K} is considered, as described in Equation (24), for u_{AB} , and a similar consideration is done for the other control laws.

$$u_{AB} = \frac{L_{f1}}{x_{10}} \left[\frac{x_7}{L_{f1}} + \frac{x_7 - v_{AB}}{L_{f2}} \right] + \bar{\beta}(x) \left\{ -\bar{K}e_{AB} - \bar{k}_i \int (x_1 - r_{AB}) dt + \ddot{r}_{AB} \right\} \quad (24)$$

where

$$\bar{\beta}(x) = (1 \times 10^{17})\beta(x), \bar{K} = \frac{K}{1 \times 10^{17}},$$

Table 2. Three-phase PWM rectifier requirements and parameters [34].

Parameter	Value
Grid voltage (ac: L-L, RMS)	480 V
Grid voltage regulation	±10%
Rated power	100 kW
Power factor	Near to unity
Output voltage (dc bus voltage)	920 V (±3%)
THD of current (i_{AB}, i_{BC}, i_{CA})	<5%
THD of voltage (v_{AB}, v_{BC}, v_{CA})	<5%
dc bus capacitor	6 mF
Duty class	1.1 p.u. for 1 h, 1.25 p.u. for 2 min, and 1.5 p.u. for 10 s
Response time in transient load	<40 ms
Delta – LCL filter : L_{f1}, L_{f2}, C_f	387 μH, 231.5 μH, 9.8 μF
Parasitic resistances of L_{f1}, L_{f2}, C_f	1.9 mΩ, 2.6 mΩ, and 3.8 mΩ, respectively
Switching frequency (it is chosen as a prime number multiple of three to eliminate triplen harmonics)	12,060 Hz
Battery model parameters (equivalent values for a vented lead-acid battery bank)	$R_0 = 0.45 \Omega, R_1 = 0.13 \Omega, R_2 = 0.15 \Omega, C_1 = 765 \text{ F}, C_2 = 4081 \text{ F},$ and $v_{oc} = 816 \text{ V}$
Parameterized gain values: ($k_1 k_2 k_3 k_i$)	$(5.1 \times 10^{-2}, 270 \times 10^{-8}, 8.93 \times 10^{-12}, 5.2)$

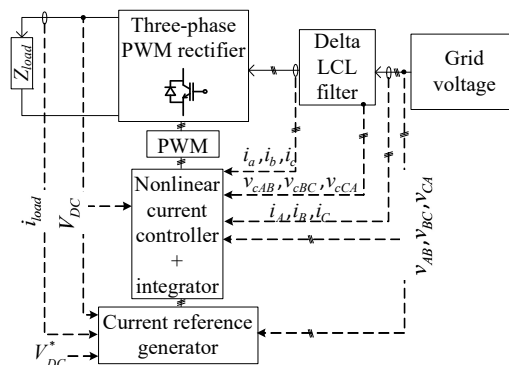


Figure 6. Simulation diagram of three-phase PWM rectifier.

For designing the control law, the three-phase LCL PWM rectifier model (Equation (14)) was validated with the specialized simulators: PSCAD[®] and SimPowerSystems-Simulink[®]. Figure 7 shows the validation with Simulink in open-loop mode showing currents i_A, i_B, i_C , voltages $v_{cAB}, v_{cBC}, v_{cCA}$, and the dc voltage V_{DC} . However, for the simulation, the defined libraries with semiconductors were used for the power converter stage. Concerning the battery model, the equivalent electrical circuit (EEC) of Figure 8, was used. The elements of the EEC model represent the internal battery dynamics where R_0 is the internal/ohmic resistance, C_1 and R_1 represent capacitor and resistor for the distribution of reactivity and the local property of electrodes, C_2 and R_2 represent the interfacial impedance of the cell, v_{oc} represents the battery open circuit voltage, and v_{bat} is the battery voltage [35–37].

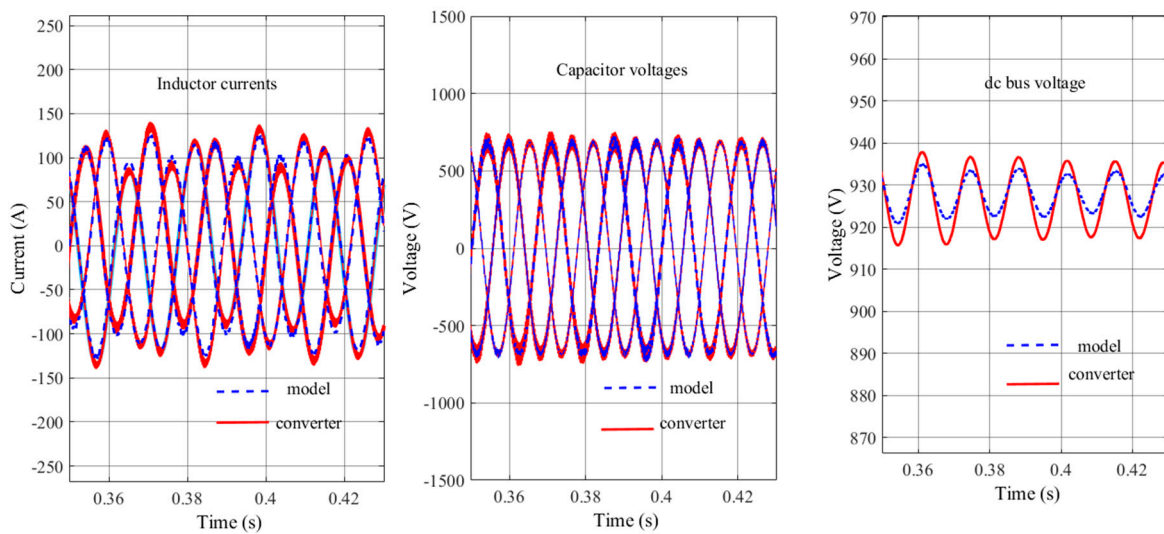


Figure 7. The contrast of the three-phase rectifier model and converter signals in open-loop mode. From left to right: i_A , i_B , i_C , v_{cAB} , v_{cBC} , v_{cCA} , and V_{DC} .

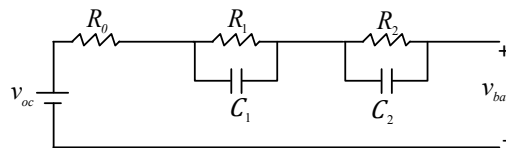


Figure 8. Equivalent electrical circuit (EEC) model of the battery. The parameter values, which represent the battery bank, were obtained for the vented Lead-acid technology.

To assess the three-phase PWM rectifier performance with the proposed control scheme, a load current i_{load} depicted in Figure 9 was used. It represents the current with load steps of the dc-dc stage for charging the battery bank in accordance with the duty class.

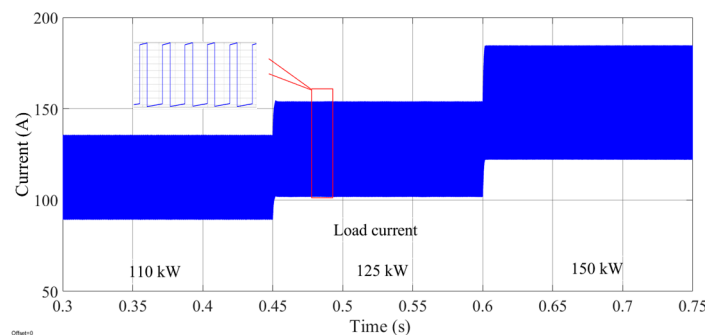


Figure 9. Load current i_{load} demanded by Z_{load} .

6.1. Performance with the Duty Class

The tracking problem is achieved as it is depicted in Figure 10, with the corresponding duty class, where the input currents i_{AB} , i_{BC} , and i_{CA} track their corresponding references and are in phase with the voltages v_{AB} , v_{BC} , and v_{CA} with a power factor of 0.99. It can be observed in Figure 11 that the error is kept close to zero, even at the highest load condition.

Concerning the THD of current, the requirement is achieved with the proposed control along with the inductor L_{f1} and L_{f2} values of the LCL filter. The criteria for selecting the filter values were considering the converter operation as an inverter. Nevertheless, this paper only addresses the process of working as a PWM rectifier; hence, the THD = 0.95% for 110 kW as shown in Figure 12.

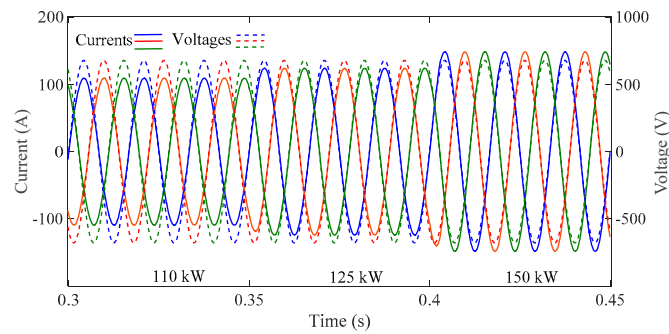


Figure 10. Input currents (i_{AB}, i_{BC}, i_{CA}) and input voltages (v_{AB}, v_{BC}, v_{CA}).

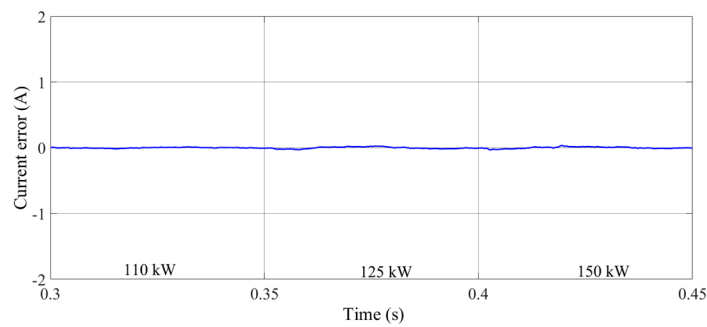


Figure 11. Current error ($x_1 - r_{AB}$).

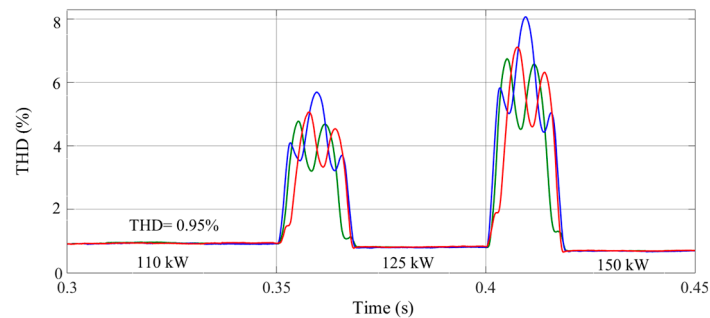


Figure 12. THD of currents i_{AB}, i_{BC} , and i_{CA} .

The dc bus voltage regulation, which is indirectly controlled by the input current, as shown in Figure 13. An error of 0.5% can be observed by using the integral action in contrast to the 2.9% of error without using it.

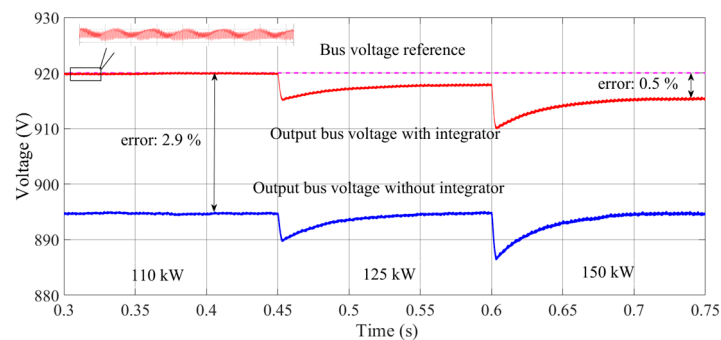


Figure 13. Output voltage V_{DC} during the duty class.

6.2. Performance with Input Voltage Variations and Uncertainties

Additionally, to reveal the effectiveness of the integral action, the control robustness is tested for input voltage variations; the indirectly regulated output voltage V_{DC} remains within the established 3% requirement despite the grid voltage varies $\pm 10\%$ based on rated power, as it can be seen in Figure 14.

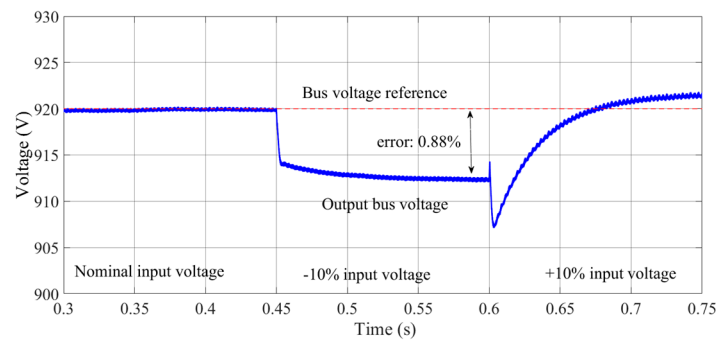


Figure 14. Output voltage V_{DC} during a grid voltage variation ($\pm 10\%$).

Concerning the parametric variation, the tolerance values of $\pm 10\%$ in each passive device, the increase of 100% in its parasitic series resistance, and a 100% increase in the on-resistance of power semiconductors are evaluated. For the 10% case, the currents i_{AB} , i_{BC} , and i_{CA} track the corresponding references (with an error near to zero) and are in phase with the voltages v_{AB} , v_{BC} , and v_{CA} , respectively (see Figure 15). As a consequence, the indirectly regulated voltage behaves as shown in Figure 16, where the highest voltage error is 1.4% when the converter delivers 150 kW.

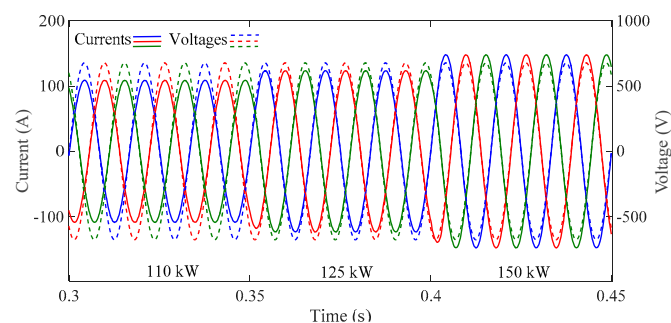


Figure 15. Currents (i_{AB} , i_{BC} , i_{CA}) and voltages (v_{AB} , v_{BC} , v_{CA}) for 10% of tolerance in passive devices and an increase of parasitic resistances.

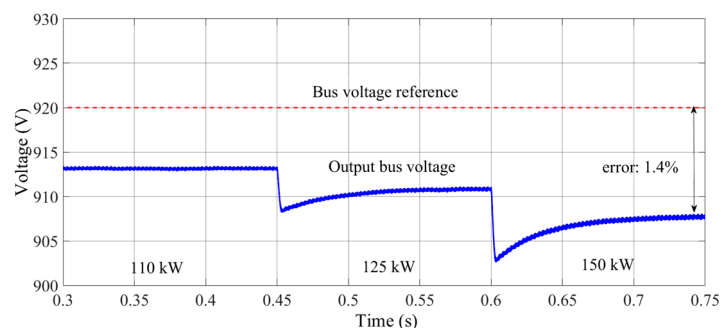


Figure 16. Output voltage V_{DC} with 10% of tolerance value in passive devices and an increase of resistance in passive and active devices.

Similarly, the control performance for the -10% tolerance in passive devices is shown next. The current tracking problem is solved as well, as can be seen in Figure 17, where the currents track the references with an error near to zero. In this case, the indirectly controlled voltage has an error of 1.2%

for 150 kW (Figure 18), which is slightly less than the +10% tolerance. However, in both circumstances, the voltage is within the defined tolerance of 3%.

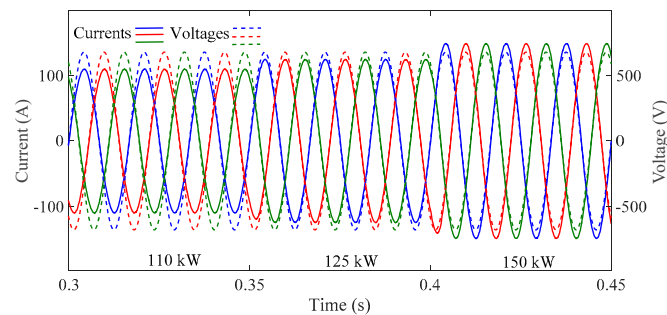


Figure 17. Currents (i_{AB} , i_{BC} , i_{CA}) and voltages (v_{AB} , v_{BC} , v_{CA}) for -10% of tolerance in passive devices and an increase in parasitic resistances.

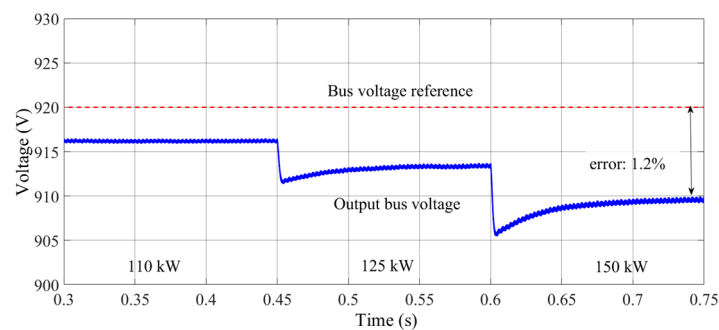


Figure 18. Output voltage V_{DC} with -10% of tolerance value in passive devices and an increase of resistance in passive and active devices.

For the duty class shown in previous figures, the control signal u_{AB} is shown in Figure 19. It can be seen the saturated control is not presented in steady-state even in the 150 kW case, which shows the suitability of the proposed control scheme in achieving the requirements.

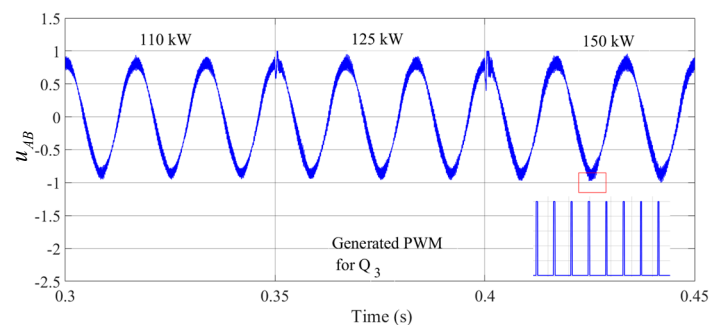


Figure 19. Control signal u_{AB} and a portion of the generated PWM.

7. Discussion: Proposed Alternative Control Scheme vs. Traditional Control Scheme

To evaluate the effectiveness of the proposed alternative control scheme, load step changes, input voltage variations, and parametric uncertainties considering the specified duty class were addressed. Besides, the three main objectives dc bus voltage regulation, THD current requirement, and power factor were accomplished. Remarkably, the dc bus voltage regulation objective is within the $\pm 3\%$ requirement despite having only indirect current-loop control. The proposed control technique shows similar performance to the traditional control scheme.

Concerning the THD and the power factor requirements, the findings confirm the usefulness of the tracking control law. The results show the THD and power factor levels are always satisfactorily

accomplished; however, it is fundamental to notice that these requirements are not only fulfilled with the control law but also with a correct LCL filter design (which is not the purpose of this paper).

In our view, the simulation results emphasize the validation of the proposed controller whose signal evolves in the -1 to 1 interval, which reveals the feasibility of considering the proposed control scheme for a PWM rectifier used into a BESS application.

Additionally, in Table 3, a contrast of the main control characteristics for the proposed control scheme and the reviewed control techniques are summarized. The evaluated items reveal that the Park transformation is avoided in three control approaches including the proposed approach. Nonetheless, the direct power control requires a computing power stage instead. Besides, all the controllers required the internal current control loop, since the system is minimum phase when the current is the output. In contrast to the voltage loop that is included in the reported approaches, it is substituted by the online power balance in the proposed scheme. Also, the delays due to the Park transformations and its inverse are avoided. However, the nonlinear controller requires three derivatives, which adds complexity.

Table 3. The contrast of the proposed control scheme and other reported approaches [6,16,20,23,38–43].

Items/Control Scheme	Traditional Approach	Direct Power Control	Voltage Oriented Control	Hysteresis Current Control	Proposed Schemewith Input-Output Map Linearization
Park transformation	Required	Required/Not required (computing power stage)	Required	Not required	Not required
Internal current control loop (CCL)	Required	Required (two power loops)	Required (two power loops)	Hysteresis command	Required
Outer voltage control loop (VCL)	Required	Required	Required	Required	Not required (power balance is used instead)
Robustness	√	√	√	√	√
Analysis complexity	Medium	Medium	Medium	Medium	High
Control law	PI (CCL) + PI (VCL) or PI (CCL) + PI (VCL)	PI	PI + PI	PI	Nonlinear control
Derivatives	None	None	None	None	3

8. Conclusions

In this paper, we have proposed the use of a single current loop to solve the input current tracking problem and a current reference generator based on the ac–dc power balance to indirectly regulate the dc bus voltage of a three-phase LCL PWM rectifier, avoiding the abc–dq–abc transformations.

Unlike most reported papers where a single-phase L-filter or an LCL-filter wye-connected model is used for control purposes, this work has considered a line-to-line LCL-filter model, since the rectifier is always delta-connected. Due to the fact of considering the delta-connected LCL filter for control purposes, the first three reference derivatives must be included, and this means that the control must be parametrized. It is convenient to mention that the gain tuning process is carried out by using the line-to-line model and then the same gains are used for the other phases. Doing this, the process implies the tuning of three gains instead of twenty-seven gains.

Taking into consideration a BESS application, simulations were performed using a typical current demanded by a dc–dc converter charging a battery bank as the load. Owing to the integral action, the system was provided with robustness and evaluations with load step changes, input voltage

variations, and parametric uncertainties considering the specified duty class has been addressed. Simulation results have shown robustness against simultaneous variations in series parasitic resistance, passive storage devices, and input voltage disturbances of $\pm 100\%$, $\pm 20\%$, and $\pm 10\%$, respectively. Under these stress conditions, the control signals remained within the -1 to 1 interval without saturation. In addition, the system still operated with a power factor of 0.99 and THD around 1% in a steady state.

This research might evolve to tackle unbalanced voltage conditions, or even fault conditions by taking advantage of the decoupled controllers designed for each phase of the system, which could be feasible to implement in a droop control scheme.

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