Double-Layer E-Structure Equalization Circuit for Series Connected Battery Strings

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Abstract: In order to eliminate the voltage imbalance among battery cells when they are connected in series, the paper proposes a double-layer E-structure (DLE) equalizer based on bidirectional buck–boost converters, which has the advantage of quick equalization speed and can be applied to arbitrary number batteries. Furthermore, a novel two-stage equalization control strategy is proposed for the DLE equalizer to decrease maximum voltage gap between the maximum and minimum voltage cells. The paper analyses the working principle of proposed equalizer in detail and describes the detailed design of the control strategy and implement process. Simulation and experiment results show that the proposed equalizer can improve equalization performance of battery cells compared with adjacent cell-to-cell (AC2C) equalizer.

Keywords: series-connected battery string; buck–boost converter; voltage gap; equalizers

1. Introduction

Nowadays, lithium-ion batteries are more and more widely used in the field of electric vehicles (EVs). Since EVs require higher voltage than what a single storage cell can output, large number of cells are needed to be connected in series [1,2]. However, cell voltage imbalance among series-connected batteries will occur due to manufacturing and environmental differences among them. This imbalance will lead to the decay of available battery capacity and lifetime of batteries. Therefore, battery equalizers are needed to eliminate the voltage imbalance among battery cells and to improve system performance.

In order to equalize the energy among the mismatch cells connected in series, many battery equalizers have been developed [3,4]. These equalizers can be classified into two categories: passive and active battery equalizers. Passive battery equalizers have the advantages of low cost and small size, because they just need a resistor and a switch for each cell [5,6]. However, the energy dissipation of resistor degrades the efficiency and might cause thermal issue. In order to overcome the drawback of the passive equalizers, many active battery equalizers have been proposed. These equalizers transfer excessive energy from the higher voltage cells to the lower voltage cells by using capacitors or inductors. Typical active battery equalizers include switched capacitor equalizers [7–9], equalizers based on bidirectional buck–boost converters [10–16], and transformer equalizers [17–19]. Among them, switched capacitor equalizers have advantages of small volume and simple control strategy, such as single-tiered switched capacitor [7], and improved switched capacitor [8,9], but their equalization speeds are slow. Transformer equalizers have advantages of flexible equalization path and quick equalization speed, such as single-winding transformer equalizer [18], and multi-winding transformer equalizers [17,19], but leakage inductor of transform lead to the appearance of equalization deviation. Equalizers based on the bidirectional buck–boost converters have the advantages of the bidirectional energy flow, easy modularization, and simple structure. Literature [10] proposes an adjacent cell-to-cell (AC2C) equalizer based on bidirectional buck–boost converters. The AC2C equalizer is featured with

arbitrary battery number and simple control, but the redundant energy of higher voltage cell can only be transferred between two adjacent cells. When an AC2C equalizer is applied to a large battery string, it has many shortcomings, such as slow equalization speed, low equalization efficiency, and huge voltage gap between maximum and minimum voltage cells in the battery string. Literature [11] improves the equalization speed by exchanging the positions of switches and inductors, but the equalizer control strategy is complicated. Studies [12,13] have improved the equalization speed by changing the connection of equalizer unit, but their cost are increased. Studies [14,15] introduce two methods to improve equalization speed and efficiency, but the huge voltage gap after equalization is still existed. Reference [16] proposes a parallel architecture equalizer based on buck–boost converter. It has fast equalization speed and high equalization efficiency compared to the AC2C equalizer. However, it is worth mentioning that the parallel structure is difficult to extend. In other words, the number of batteries is restricted. Figure 1 shows AC2C equalizer and parallel structure equalizer, which are commonly used in battery equalization mentioned above. Figure 1a shows the AC2C equalizer. Figure 1b shows the parallel architecture equalizer.
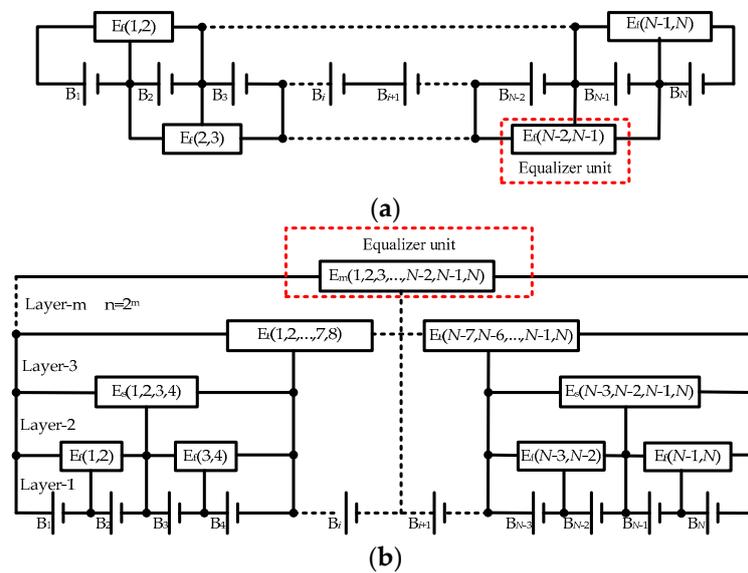

Figure 1. AC2C equalizer and parallel structure equalizer. (**a**) AC2C equalizer; (**b**) parallel structure equalizer.

A double-layer E-structure (DLE) battery equalizer is proposed in this paper. The proposed equalizer has the advantage of quick equalization speed and can be applied to arbitrary number batteries. In addition, a novel two-stage control strategy is proposed to decrease the maximum voltage gap after equalization. The structures of proposed equalizer are described in Section 2. The equalization principle is described in Section 3. The equalization control strategy is described in Section 4. The simulation results are described in Section 5. The experimental results are described in Section 6, followed by the conclusion in Section 7.

2. Structures of Proposed Equalizer

The structures of proposed equalizer are shown in Figure 2. Figure 2a,b show the odd structure and even structure of proposed equalizer, respectively. The proposed equalizer is composed of the inner-layer equalizer units and the outer-layer equalizer units. E_f $(i, i + 1)$ represents the inner-layer equalizer unit and it equalizes the cells B_i and B_{i+1}. E_s $(j, j + 1, j + 2, j + 3)$ represents outer-layer equalizer unit and it equalizes the cell substrings (B_i, B_{i+1}) and (B_{i+2}, B_{i+3}).

When cell number N is odd, the inner-layer equalizer units of proposed equalizer include E_f (1, 2), E_f (3, 4), ... , E_f $(i, i + 1)$, ... , E_f $(N − 2, N − 1)$, E_f $(N − 1, N)$ and its outer-layer equalizer units include

E_s (1, 2, 3, 4), E_s (3, 4, 5, 6), ... , E_s (j, j + 1, j + 2, j + 3), ... , E_s (N − 4, N − 3, N − 2, N − 1). The number of equalizer units can be expressed as

$$\begin{cases} \text{Inner-layer}: N_f = \frac{N+1}{2} \\ \text{Outer-layer}: N_s = \frac{N-3}{2} \end{cases} \tag{1}$$

where N_f and N_s are the number of inner-layer and outer-layer equalizer units, respectively.

When N is even, the inner-equalizer units of proposed equalizer include E_f (1, 2), E_f (3, 4), ... , E_f (i, i + 1), ... , E_f (N − 1, N), and its outer-layer equalizer units include E_s (1, 2, 3, 4), E_s (3, 4, 5, 6), ... , E_s (j, j + 1, j + 2, j + 3), ... , E_s (N − 3, N − 2, N − 1, N). The number of equalizer units can be expressed as

$$\begin{cases} \text{Inner-layer}: N_f = \frac{N}{2} \\ \text{Outer-layer}: N_s = \frac{N-2}{2} \end{cases} \tag{2}$$

Each equalizer unit of proposed equalizer is a bidirectional buck–boost converter, as shown in Figure 3. Figure 3a shows an inner-layer equalizer unit that equalizes two adjacent cells; Figure 3b shows an outer-layer equalizer unit that equalizers two adjacent cell substrings. The proposed equalizer is composed of ($2N$ − 2) switches (inner-layer switches: S_1–S_N, outer-layer switches: S_{N+1}–S_{2N-2}) and (N − 1) inductors, as many as the traditional AC2C equalizer. In addition, similar to the parallel structure equalizer, the proposed equalizer provides flexible equalization paths, which reduces equalization time and improves equalization efficiency.
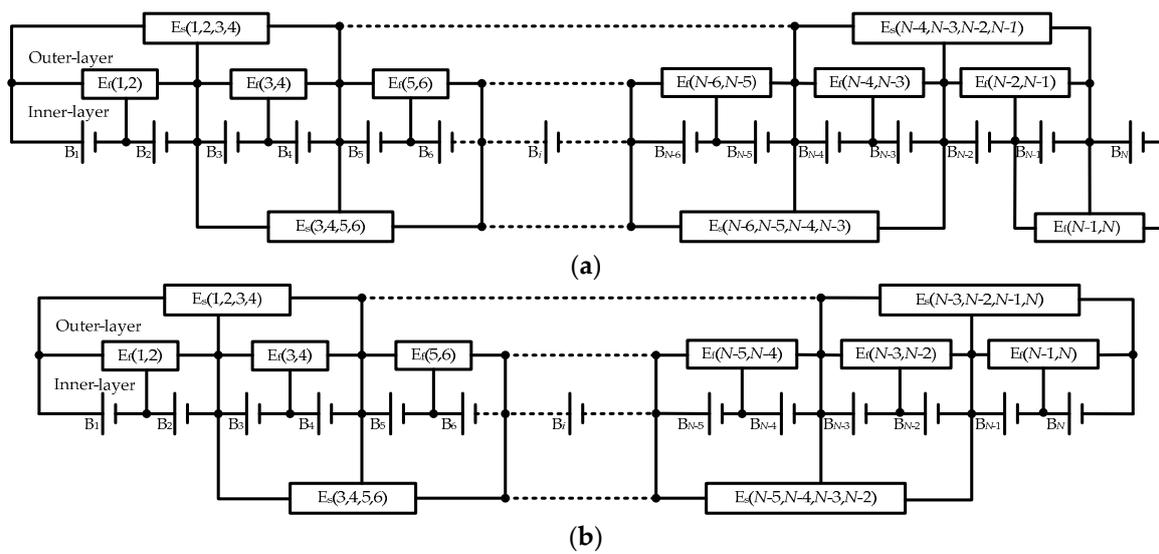

(a)

(b)

Figure 2. Structures of proposed equalizer. (**a**) Odd structure of proposed equalizer. (**b**) Even structure of proposed equalizer.
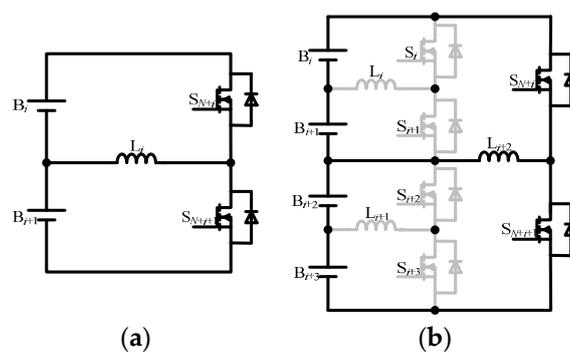

(a)   (b)

Figure 3. Equalizer unit. (**a**) Inner-layer equalizer unit. (**b**) Outer-layer equalizer unit.

To facilitate the analysis, several assumptions are made as follows:

1. All diodes, switches, and inductors employed in proposed equalizer are ideal;
2. Each inductor has the identical parameter, i.e., $L = L_1 = L_2 = L_3 = \ldots = L_{2N-2}$;
3. Cell voltages are constant during one switching period;
4. All of the buck–boost converters are operated in discontinuous conduction mode (DCM)

3. Equalization Principles

The equalization process of the proposed equalizer consists of two stages. In the first stage, the energy is transferred among adjacent cell substrings and between two cells in a substring by corresponding outer-layer and inner-layer equalizer units, respectively. It is noted that, when N is odd, the energy can also be transferred between cells B_N and B_{N-1}, which are adjacent cells but belong to different substrings. In the second stage, the energy is transferred from the maximum voltage cell to the minimum voltage cell, which is implemented by multiple inner-layer and outer-layer equalizer units. By the first stage equalization process, adjacent cell substrings and two cells in a substring are equalized, but the imbalance among cells in the whole battery string is still large. The second stage equalization can realize the equalization of the battery string with small maximum voltage gap among cells, but its equalization speed is slower. Thus, the proposed equalization control strategy combines the first with second stage equalization, which has advantages of both the first and second stage equalization.

3.1. First Stage Equalization

In the first stage equalization, the inner-layer equalizer and outer-layer equalizer work independently. The operation of the equalizer is based on the voltage gap between two adjacent cells or cell substrings. The equalizer has two predefined equalization thresholds; one predefined threshold ΔV for the inner-layer equalizer unit and one predefined threshold $2\Delta V$ for out-layer equalizer unit. If the voltage gap is less than the predefined equalization threshold, the corresponding equalizer unit stops working. The working condition of inner-layer equalizer unit can be expressed as

$$\left| V_{Bi} - V_{Bi+1} \right| > \Delta V \begin{cases} N \text{ is odd}: \ i = 1,3,5,\ldots,N-2, \text{ and } i = N-1 \\ N \text{ is even}: \ i = 1,3,5,\ldots,N-1 \end{cases} \tag{3}$$

where V_{Bi} is the voltage of cell B_i. The working condition of outer-layer equalizer unit can be expressed as

$$\left| (V_{Bi} + V_{Bi+1}) - (V_{Bi+2} + V_{Bi+3}) \right| > 2\Delta V \begin{cases} N \text{ is odd}: \ i = 1,3,5,\ldots,N-4 \\ N \text{ is even}: \ i = 1,3,5,\ldots,N-3 \end{cases} \tag{4}$$

When both the inner-equalizer unit and outer-layer equalizer unit stop working, the equalization process ends. During this stage, the operation principles of inner-layer and outer-layer equalizer units are similar. For the sake of simplification, take inner-equalizer unit as an example to analyze the working process. Assuming that cell voltage V_{Bi} is higher than cell voltage V_{Bi+1}. The equalization process of this stage includes two modes, i.e., Mode 1 and Mode 2. The current paths of the first stage equalization during different modes are shown in Figure 4.

Mode 1 [t_0–t_1]: B_i discharges.

Figure 4a presents the inductor current path of Mode 1. Mode 1 starts when the switch S_i is turned on and the switch S_{i+1} is turned off. Then, V_{Bi} is directly applied to the terminal of the inductor L_i, and the inductor current i_{Li} is built up. During this mode, L_i is charged by cell B_i and i_{Li} increases linearly. Therefore, i_{Li} can be expressed as

$$i_{Li} = \frac{V_{Bi}}{L_i}(t - t_0), t_0 < t < t_1 \tag{5}$$

The energy W_i is transferred from cell B_i to L_i, and it can be expressed as

$$W_i = V_{Bi} \int_0^{D_i T_s} (\frac{V_{Bi}}{L_i} t) dt = \frac{V_{Bi}^2}{2L_i} D_i^2 T_s^2 \tag{6}$$

In the Formula (6), D_i is the duty cycle of the switch S_i, and T_s is the switching period.

Mode 2 [t_1–t_2]: B_{i+1} charges.

Figure 4b presents the inductor current path of Mode 2. Mode 2 begins when the switches S_i and S_{i+1} are turned off. The inductor current is commutated from S_i to the parasitic diode of S_{i+1}, and it decreases linearly due to the cell voltage is applied to the inductor in the opposite direction. During this mode, the energy is transferred into cell B_{i+1} and V_{Bi+1} increases slowly. i_{Li} can be expressed as

$$i_L = \frac{V_{Bi}}{L}(t_1 - t_0) - \frac{V_{Bi+1}}{L}(t - t_1), t_1 < t < t_2 \tag{7}$$

When i_L reduces to zero, the energy transportation will be stopped by the parasitic diode of S_{i+1}. The freewheeling time T_d of i_L can be expressed as

$$T_d = \frac{V_{Bi}}{V_{Bi+1}}(t_1 - t_0) \tag{8}$$

In order to avoid magnetic saturation of inductors, the duty cycle of all switches should be designed to satisfy the following expression

$$D_i = \frac{t_1 - t_0}{T_s} < \frac{t_1 - t_0}{T_d + t_1 - t_0} = \frac{V_{Bi}}{V_{Bi} + V_{Bi+1}} \tag{9}$$

The normal voltage range of lithium-ion battery is 2.8–4.2 V, so the duty cycle of all switches must be less than 0.4 to avoid magnetic saturation.
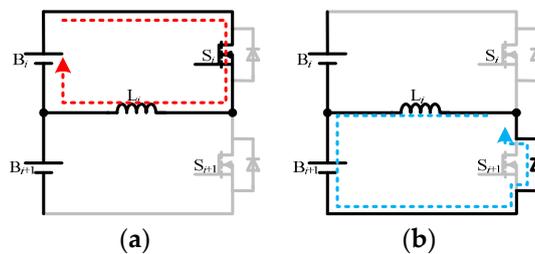

Figure 4. Current paths of the first stage equalization during different modes. (**a**) Mode 1, B_i discharges; (**b**) Mode 2, B_{i+1} charges.

3.2. Second Stage Equalization

The second stage equalization forms an equivalent equalization path by controlling the conduction of the switches and regulating specific duty cycle to achieve equalization between the maximum voltage cell and minimum voltage cell. The second stage equalization includes three modes: Mode 1, the energy transfers from the maximum voltage cell to outer-layer inductor; Mode 2, the energy flows among outer-layer inductors; Mode 3, the energy transfers from outer-layer inductor to the minimum voltage cell. The paper takes even structure of proposed equalizer as an example to elaborate the operation process of the second stage equalization. It is supposed that the voltage of cell B_i is maximum and the voltage of cell B_j is minimum.

Mode 1: the energy transfers from the maximum voltage cell to outer-layer inductor.

Whether switches work or not in equalization process is related to the position of maximum voltage cell B_i in Mode 1, and the corresponding relationship is shown in Table 1. The energy transfer

process consists of two parts in Mode 1: (a) the maximum voltage cell B$_i$ discharges; (b) the outer-layer inductor L$_{i+2}$ charges. The two parts are presented in Figure 5.

Table 1. Switches working in Mode 1

Layer \ i	Odd Number	Even Number
Inner-layer	S$_i$	S$_i$
Outer-layer	S$_{N+i}$	S$_{N+i-1}$

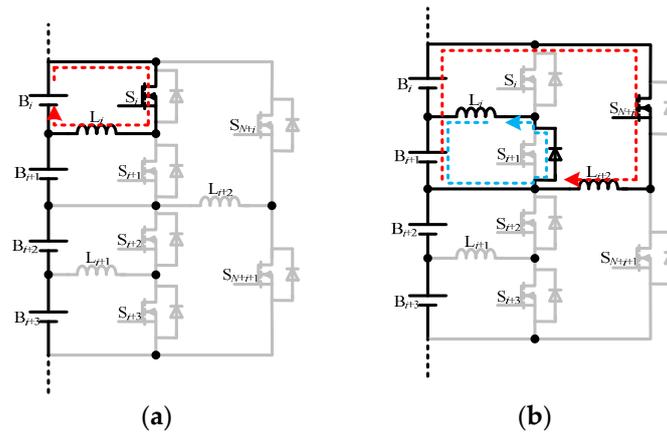(**a**)   (**b**)

Figure 5. Current paths of second stage equalization in Mode 1. (**a**) The maximum voltage cell B$_i$ discharges. (**b**) The out-layer inductor L$_{i+2}$ charges.

As shown in Figure 5a, when the inner-layer switch S$_i$ is turned on, the analysis process is the same as the first stage equalization, the energy that stored in L$_i$ can be obtained from Formula (6). When S$_i$ is turned off, the inductor current i_{Li} flows from the parasitic diode of S$_{i+1}$ to the adjacent cell B$_{i+1}$. The equalizer unit transfers the excess energy from the highest voltage cell B$_i$ to the adjacent cell B$_{i+1}$. On the other hand, as shown in Figure 5b, when the outer-layer switches S$_{N+i}$ is turned on, the cell B$_{i+1}$ charges the outer-layer inductor L$_{i+2}$. The energy W_{ri+1} transfers from cell B$_{i+1}$ to L$_{i+2}$ can be expressed as

$$W_{ri+1} = V_{Bi+1} \int_0^{D_{n+i}T_s} \left(\frac{V_{Bi} + V_{Bi+1}}{2L} t \right) dt = \frac{(V_{Bi} + V_{Bi+1})V_{Bi+1}}{2L} D_{N+i}^2 T_s^2 \tag{10}$$

If the energy of cell B$_{i+1}$ maintains dynamic balance in the process of charging and discharging, the process transfers excess energy from cell B$_i$ to L$_{i+2}$, and the energy of cell B$_{i+1}$ is unchanged. The corresponding energy relationship can be expressed as

$$W_i = W_{ri+1} \tag{11}$$

From Formula (11), the duty cycle D_{N+i} of S$_{N+i}$ can be obtained as

$$D_{N+i} = D_i V_{Bi} \sqrt{\frac{1}{(V_{Bi} + V_{Bi+1})V_{Bi+1}}} \tag{12}$$

In addition, the energy W_{Li+2} transferred from the cell substring (B$_i$, B$_{i+1}$) to L$_{i+2}$ during this process can be expressed as

$$W_{Li+2} = (V_{Bi} + V_{Bi+1}) \int_0^{D_{i+6}T_s} \frac{(V_{Bi} + V_{Bi+1})}{L} t dt = \frac{(V_{Bi} + V_{Bi+1})^2}{2L} D_{N+i}^2 T_s^2 \tag{13}$$

Mode 2: the energy flows among outer-layer inductors.

Whether switches work or not in equalization process is related to the position of maximum voltage cell B$_i$ and minimum voltage cell B$_j$ in Mode 2, and the corresponding relationship is shown in Table 2. In addition, the energy transfer process consists of three parts in Mode 2: (a) the outer-layer inductor L_{i+2} discharges; (b) the outer-layer inductor L_{i+3} charges; (c) the outer-layer inductor L_{j+1} charges. The three parts are presented in Figure 6.

Table 2. Switches working in Mode 2.

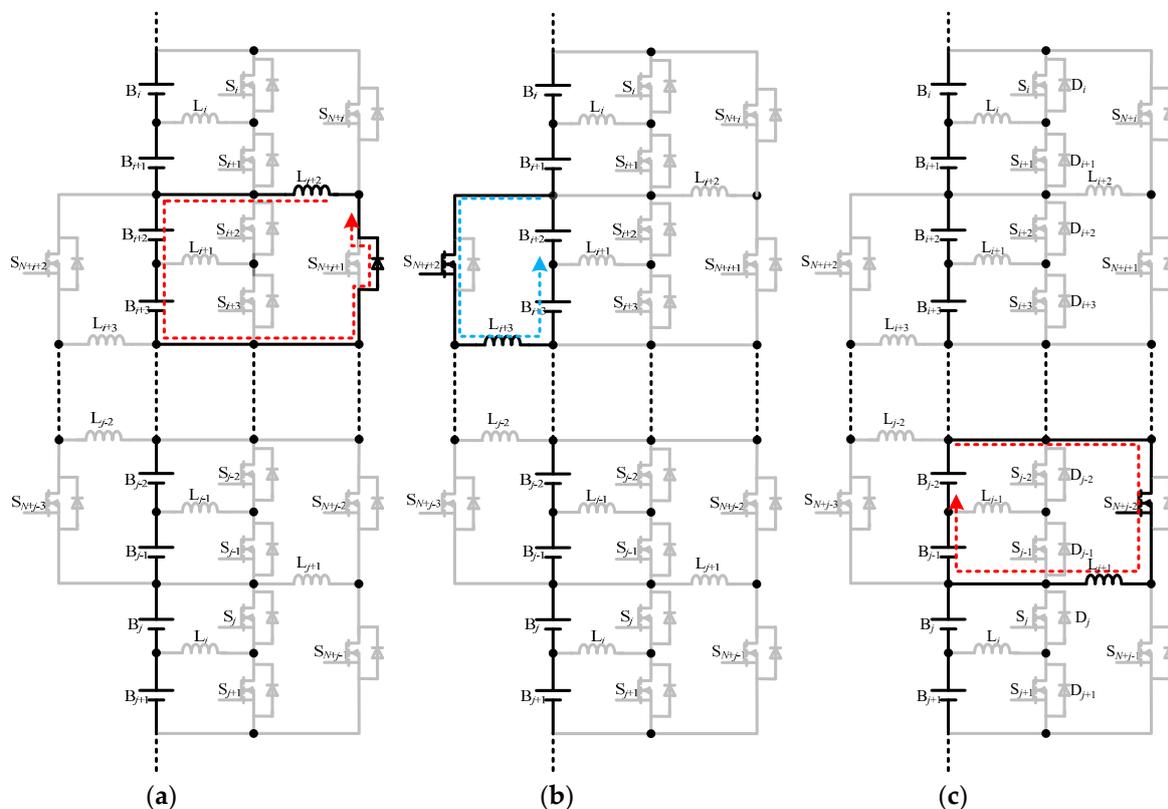| j \ i	Odd Number	Even Number
Odd number	$S_{N+i+2}, S_{N+i+4}, \ldots, S_{N+j-4}, S_{N+j-2}$	$S_{N+i+1}, S_{N+i+3}, \ldots, S_{N+j-4}, S_{N+j-2}$
Even number	$S_{N+i+2}, S_{N+i+4}, \ldots, S_{N+j-3}, S_{N+j-1}$	$S_{N+i+1}, S_{N+i+3}, \ldots, S_{N+j-3}, S_{N+j-1}$

(a) (b) (c)

Figure 6. Current paths of the second stage equalization in Mode 2. (**a**) Outer-layer inductor L_{i+2} discharges. (**b**) Outer-layer inductor L_{i+3} charges. (**c**) Outer-layer inductor L_{j+1} charges.

As shown in Figure 6a, when the switch S$_{N+i}$ is turned off, L_{i+2} charges the adjacent cell substrings through the parasitic diode of switch S$_{N+i+1}$ to realize the energy transfer from L_{i+2} to the cell substring (B$_{i+2}$, B$_{i+3}$). Then, as shown in Figure 6b, when the outer-layer switch S$_{N+i+2}$ is turned on, the cell substring (B$_{i+2}$, B$_{i+3}$) charges the outer-layer inductor L_{i+3}. In this process, the energy W_{Li+3} transfers from the cell substring (B$_{i+2}$, B$_{i+3}$) to L_{i+3}, which can be expressed as

$$W_{Li+3} = (V_{\mathrm{B}i+2} + V_{\mathrm{B}i+3}) \int_0^{D_{i+8}T_s} \frac{(V_{\mathrm{B}i+2} + V_{\mathrm{B}i+3})}{L} t \, dt = \frac{(V_{\mathrm{B}i+2} + V_{\mathrm{B}i+3})^2}{2L} D_{N+i+2}^2 T_s^2 \qquad (14)$$

If the energy of cell substring (B_{i+2}, B_{i+3}) maintains dynamic balance in the process of charging and discharging, the mode transfers excess energy from cell B_i to L_{i+3}, and the energy of cell substring (B_{i+2}, B_{i+3}) is unchanged in this process. The corresponding energy relationship can be expressed as

$$W_{Li+2} = W_{Li+3} \tag{15}$$

From Formula (15), the duty cycle D_{N+i+2} of S_{N+i+2} can be expressed as

$$D_{N+i+2} = \frac{V_{Bi} + V_{Bi+1}}{V_{Bi+2} + V_{Bi+3}} D_{N+i} \tag{16}$$

Similarly, owing to the unchanged energy of intermediate cell substrings in this mode, it means that the duty cycle of the corresponding switches can be solved. Meanwhile, the energy that stored in the inductor L_{j-2} can be obtained from Formula (6). When the outer-layer switch S_{N+j-4} is turned off, the inductor L_{j-2} charges the cell substring (B_{j-2}, B_{j-1}) through the parasitic diode of switch S_{N+j-3}. Then, as shown in Figure 6c, when the switch S_{N+j-2} is turned on, the cell substring (B_{j-2}, B_{j-1}) charges the outer-layer inductor L_{j+1}. Similar to the above Formulas (13), (14), (15), duty cycle D_{N+j-2} of S_{N+j-2} can be expressed as

$$D_{N+j-2} = \frac{V_{Bi} + V_{Bi+1}}{V_{Bj-2} + V_{Bj-1}} D_{N+i} \tag{17}$$

Mode 3: the energy transfers from outer-layer inductor to the minimum voltage cell.

Whether switches work or not in equalization process is related to the position of maximum voltage cell B_i in Mode 3, and the corresponding relationship is shown in Table 3. In addition, the energy transfer process consists of two parts in Mode 3: (a) the outer-layer inductor L_{j+1} discharges; (b) the minimum voltage cell B_j charges. The two parts are presented in Figure 7.

Table 3. Switches working in Mode 3

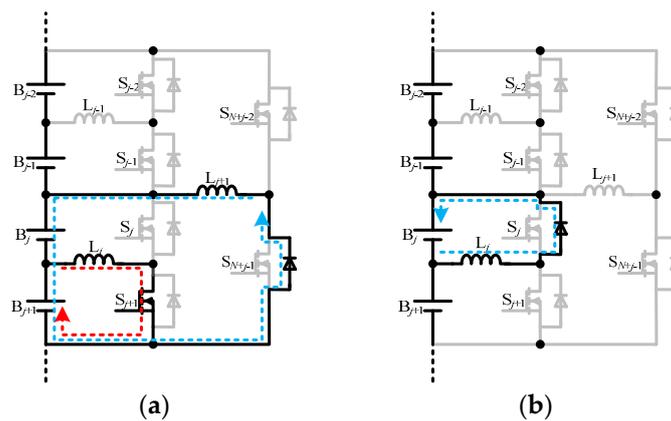| Layer \ j	Odd Number	Even Number
Inner-layer	S_{j+1}	S_{j-1}

(a) (b)

Figure 7. Current paths of the second stage equalization in Mode 3. (**a**) Outer-layer inductor L_{j+1} discharges. (**b**) Minimum voltage cell B_j charges.

To simplify the analysis, it is assuming that all components is ideal, then the energy loss of the whole equalization process can be ignored. The energy transfers from the cell B_i to the inductor L_{j+1} can be obtained from the Formula (13). As shown in Figure 7a, when S_{N+j-2} is turned off, the inductor current i_{Lj+1} commutated from S_{N+j-2} to parasitic diode of outer-layer switch S_{N+j-1}, and the outer-layer

equalizer unit transfers energy from L_{j+1} to the cell substring (B_j, B_{j+1}). According to voltage-divider theorem, the energy W_{sj+1} transferred from L_{j+1} to the cell B_{j+1} can be expressed as

$$W_{sj+1} = \frac{V_{Bj+1}}{(V_{Bj} + V_{Bj+1})} W_{Li+2} \tag{18}$$

On the other hand, when the inner-layer switch S_{j+1} is turned on, cell B_{j+1} charges the inner-layer inductor L_j. The energy W_{rj+1} transferred from the cell B_{j+1} to L_j can be expressed as

$$W_{rj+1} = V_{Bj+1} \int_0^{D_{j+1}T_s} \frac{V_{Bj+1}}{L} t dt = \frac{V_{Bj+1}^2}{2L} D_{j+1}^2 T_s^2 \tag{19}$$

If the energy of cell B_{j+1} maintains dynamic balance in the process of charging and discharging, the mode transfers excess energy from the maximum voltage cell B_i to L_j, and the energy of cell B_{j+1} is unchanged in this process. The corresponding energy relationship can be expressed as

$$W_{sj+1} = W_{rj+1} \tag{20}$$

From Formulas (18), (19), and (20), the duty cycle D_{j+1} of S_{j+1} can be expressed as

$$D_{j+1} = D_{N+i}(V_{Bi} + V_{Bi+1}) \sqrt{\frac{1}{(V_{Bj} + V_{Bj+1})V_{Bj+1}}} \tag{21}$$

As shown in Figure 7b, when S_{j+1} is turned off, L_j charges the cell B_j through the parasitic diode of inner-layer switch S_j to realize the energy transfer from L_j to cell B_j.

In fact, the energy transfers from the maximum voltage cell B_i to the minimum voltage cell B_j by the second stage equalization, and the energy of other cells are unchanged. Thus, the second stage equalization decreases the maximum voltage gap between maximum voltage and minimum voltage in the battery string.

4. Equalization Control Strategy

The paper proposes a two stages equalization control strategy. The first stage equalization is widely used in traditional equalizers, it has the advantages of fast equalization speed and simply control, but it has the disadvantage of repeated flow of energy. Meanwhile, the maximum voltage gap after balancing among cells is increased with the increase of N due to the accumulation of threshold voltage gap of equalizers. Especially for AC2C equalizer, if the voltage gap of two adjacent cells is less than the predefined threshold, then in the worst case, the maximum voltage gap between maximum voltage and minimum voltage in the battery string can be expressed as

$$V_{gap} = (N-1)\Delta V \tag{22}$$

The increase of maximum voltage gap after balancing among cells affects the equalization performance, which will decrease the total storage capacity and battery lifecycle. Meanwhile, if the given threshold is reduced, although the maximum voltage gap will also decrease, the corresponding equalization time will be greatly increased. Therefore, the second stage equalization is proposed to decrease the maximum voltage gap.

The flow chart of the proposed equalization control strategy used in simulations and experiments is show in Figure 8. When the arbitrary equalizer unit detects that two adjacent cells or cell substrings voltage gap is greater than the predefined threshold, the first stage equalization starts working. On the contrary, when all equalization units detect that the adjacent voltage gap is less than the given threshold, the first stage equalization stops working. Unfortunately, the maximum voltage gap is still large after

finishing the first stage equalization, the equalizer begins the second stage equalization, and it stops working until the maximum voltage gap is less than the predefined threshold. Thus, the proposed control strategy can improve equalization performance.
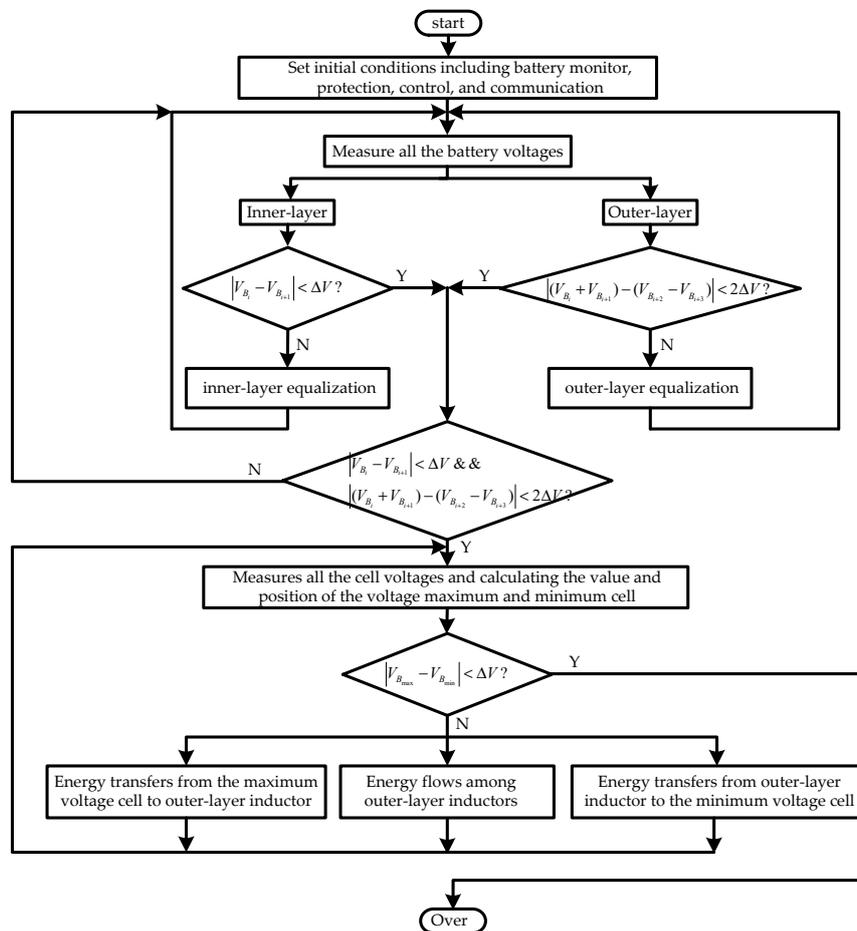

Figure 8. Flow chart of proposed equalization control strategy used in simulations and experiments.

5. Simulation

In order to compare the equalization performance of proposed equalizer with AC2C equalizer, the simulations for six cells at six different initial voltage distributions were carried out using PSIM software. Table 4 shows the initial voltage distributions of six cells.

Table 4. Initial voltage distributions for simulation

	B_1 (V)	B_2 (V)	B_3 (V)	B_4 (V)	B_5 (V)	B_6 (V)
Case 1	3.21	3.47	3.35	3.72	3.13	3.64
Case 2	3.21	3.47	3.13	3.64	3.35	3.72
Case 3	3.35	3.72	3.21	3.47	3.13	3.64
Case 4	3.35	3.72	3.13	3.64	3.21	3.47
Case 5	3.13	3.64	3.21	3.47	3.35	3.72
Case 6	3.13	3.64	3.35	3.72	3.21	3.47

As shown in Table 4, at different cases, the maximum voltage gaps among cells are 0.59 V. In simulation, the switching frequency was set as 10 kHz, and the value of each inductor is 100 μH

and duty cycle was set as 0.4. In addition, energy storage cells B_1–B_6 were replaced by capacitors (0.1F). The paper compares three equalizers by simulation: AC2C equalizer, DLE equalizer with first stage equalization (DLE1 equalizer), and DLE equalizer with the proposed two-stage equalization (DLE2 equalizer). For the AC2C equalizer, simulation and experimental voltage thresholds are set to 10 mV. For DLE1 equalizer, the inner-layer voltage threshold was set as 10 mV and outer-layer voltage threshold was set as 20 mV. Furthermore, for DLE2 equalizer, the maximum voltage gap of the whole battery pack was set as 10 mV.

The three equalizers are simulated using identical voltage distribution and parameters. Under the condition of six cells, the number of different initial voltage distribution sequences is $A_6^6 = 720$. It is almost impossible to simulate those distributions one by one. However, for DLE equalizer, six cells can be divided into three substrings that include two adjacent cells, so the paper compares six different voltage distributions due to $A_3^3 = 6$.

The simulation results are shown in Figure 9. From the simulation results, at six different initial voltage distributions, DLE2 equalizer has controllable maximum voltage gap compared to the other equalizers. Furthermore, the DLE equalizer has a relatively stable equalization time than AC2C equalizer in different distribution sequences of the cell voltage, it means that DLE equalizer has more stable equalization performance.

The paper also defines voltage variance and maximum voltage gap as extra index for further evaluate the equalization performance.

The variance σ^2 is defined as

$$\sigma^2 = \frac{1}{N}\sum_{i=1}^{n}\left(V_{\text{B}i} - \overline{V}\right)^2 \tag{23}$$

where $\overline{V}$ is the average voltage of cells in the battery string. The smaller σ^2 is, the better equalization performance is.

The maximum voltage gap V_{gap} in the battery string is defined as

$$V_{gap} = V_{B\max} - V_{B\min} \tag{24}$$

where V_{Bmax} is maximum voltage in the battery string and V_{Bmin} is minimum voltage in the battery string. Similarly, the smaller V_{gap} is, the better equalization performance is.

Table 5 shows the average equalization performance of six simulation results. The DLE1 and DLE2 equalizers have shorter average equalization time, smaller voltage variance, and smaller maximum voltage gap compare with AC2C equalizer, which further proves that DLE1 and DLE2 equalizers have superior equalization performance. As N grows, the advantages of DLE1 and DLE2 equalizers will become more and more obvious. In addition, although the average equalization time of DLE2 equalizer increases slightly compared with DLE1 equalizer, the voltage variance and the maximum voltage gap is significant declined.

Table 5. Average equalization performance of six simulation results

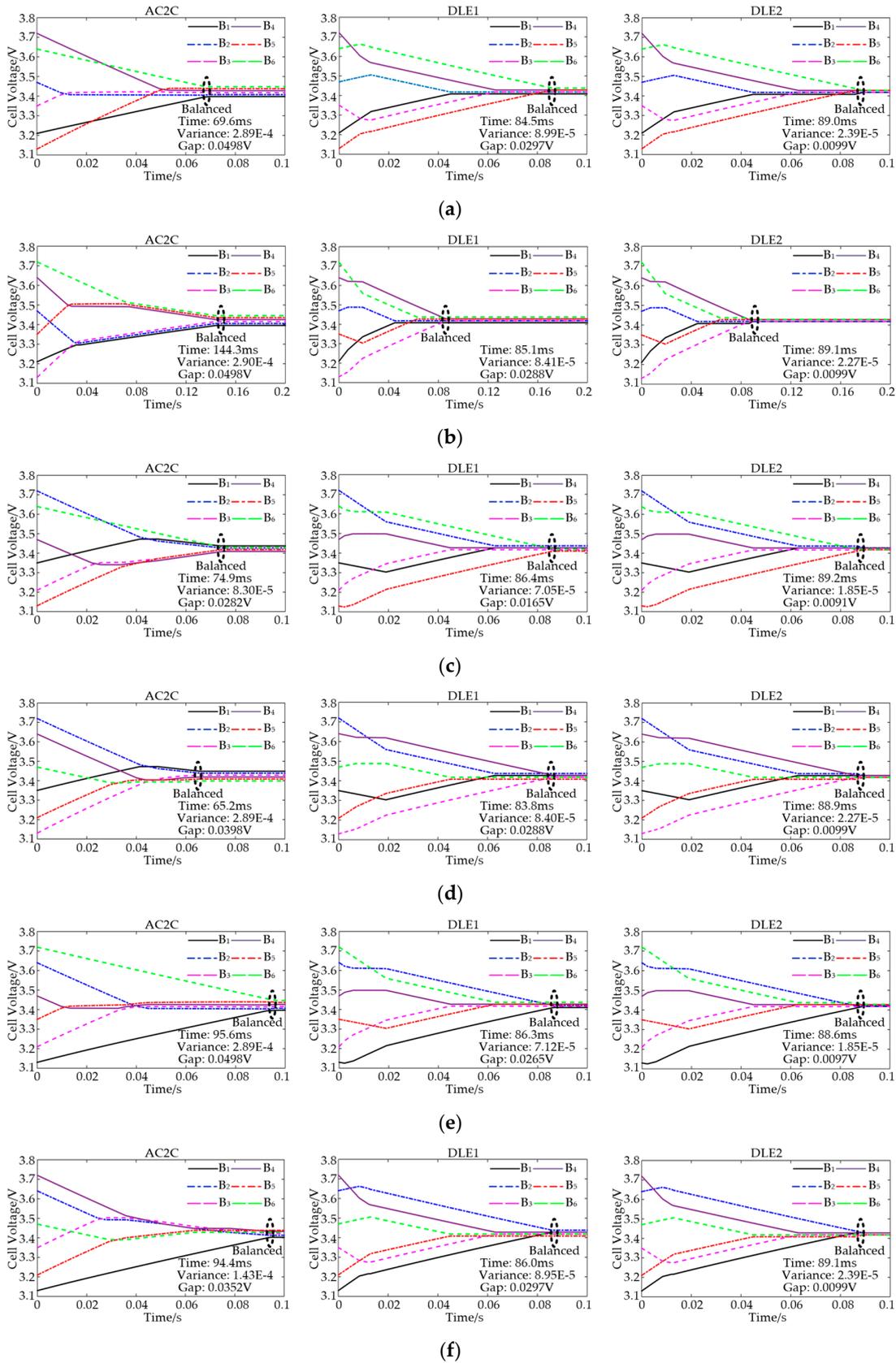|	AC2C	DLE1	DLE2
Equalization time (ms)	90.67	85.42	88.97
Variance	2.3×10^{-4}	8.16×10^{-5}	2.17×10^{-5}
Voltage gap (V)	0.0421	0.0267	0.0097

Figure 9. Simulation results of different initial voltage distribution. (**a**) Case 1; (**b**) Case 2; (**c**) Case 3; (**d**) Case 4; (**e**) Case 5; (**f**) Case 6.

6. Experimental Results

In order to verify the analysis and simulation results in above sections, experiments were carried out by using lithium-ion battery string containing six cells connected in series. Figure 10 shows a photograph of the experimental circuit. The acquisition chip is the sensor to make measurement on the status of the battery cell. The monitoring IC reads the voltage value of the cells and communication with the microcontroller. The microcontroller collects data and sends it to upper computer. The microcontroller comparers the result with the threshold value set, detects the unbalanced cell and generates pulse width modulation (PWM) signals to drive the corresponding MOSFET according to the proposed algorithm. Figure 10 shows a photograph of the experimental circuit and Table 6 shows the specification of component used for experiments.
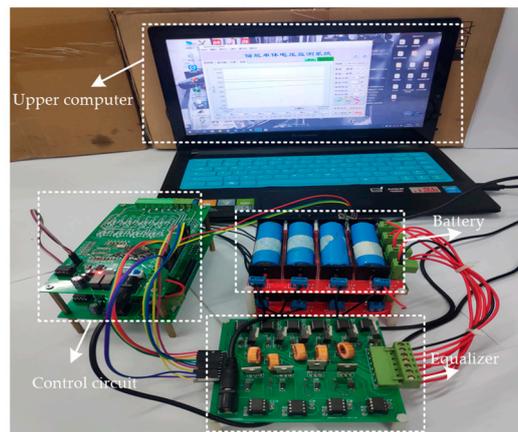
Figure 10. Photograph of the experimental circuit.

Table 6. Specification of component for experiments

Parameters		Value
Cell balancing circuit	MOSFET	IRF540NPBF
	Gate driver	HCPL-3120
	Switching frequency	10 KHz
	Inductor	100 μH
	Microcontroller	STM32F103RCT6
	Acquisition chip	LTC6803
Lithium-ion battery	Nominal capacity	2 Ah
	Cell voltage variation	2.8–4.2 V

Figure 11 shows the experimental results for six cells under the condition of Case 2 of Table 4. The operating conditions of AC2C equalizer and the proposed equalizers are the same as the simulation. As shown in Figure 11, three equalizers can realize the equalization of battery string, but their balancing time is different. The AC2C equalizer takes 440 min. However, the proposed equalizers require only 280 min and 290 min. Thus, the equalization speed of the proposed equalizers is better than that of the conventional AC2C equalizer. In addition, the maximum voltage gap of conventional AC2C equalizer is 0.045 V after the total equalization process. The maximum voltage gap of DLE1 equalizer is 0.025 V after balancing, and it is reduced by 55.6% compared with AC2C equalizer. For the DLE2 equalizer, although the equalization time equalizer increases slightly compared with DLE1 equalizer, the maximum voltage gap is reduced from 0.025 V to 0.009 V, which is the minimum among three equalizers. Meanwhile, the voltage variance of the proposed equalizers is smaller than the AC2C equalizer.
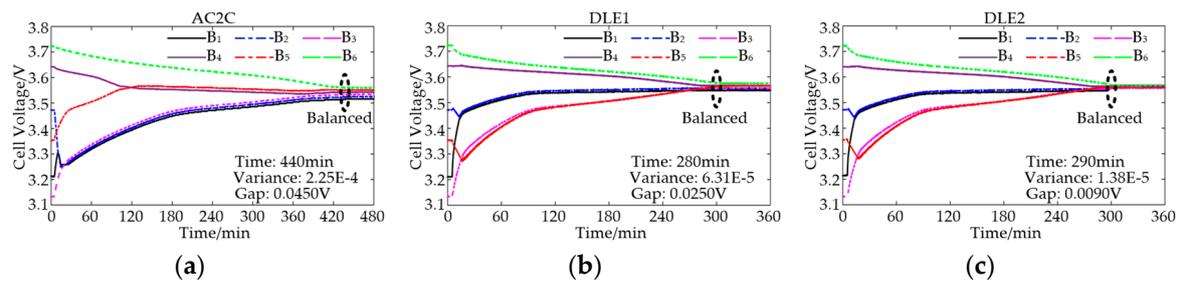
Figure 11. Experimental results of three equalizers for six cells under the condition of Case 2 of Table 4. (**a**) AC2C; (**b**) DLE1; (**c**) DLE2.

Figure 12 shows the cell voltage distributions of three equalizers after balancing. Among them, the maximum voltage gap of the DLE2 equalizer is minimum, followed by DLE1 equalizer, and the maximum voltage gap of the AC2C equalizer is maximum. Thus, it is further demonstrated that the proposed equalizers can achieve better equalization performance.
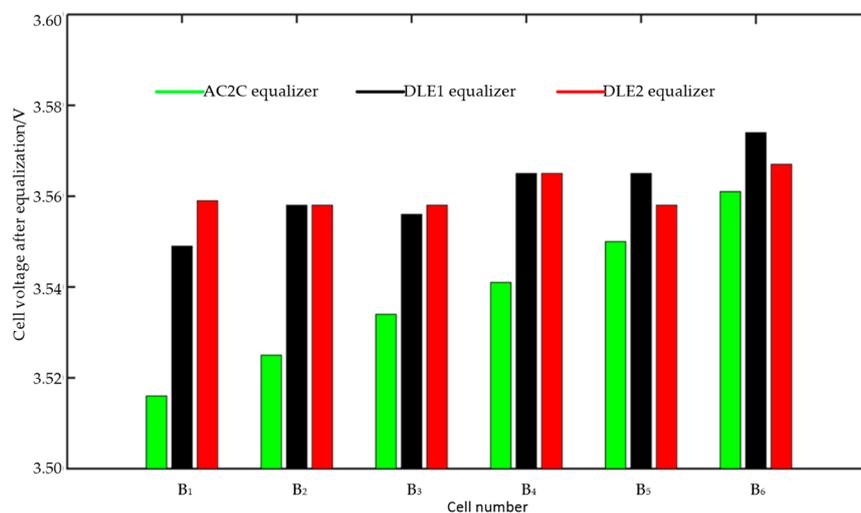

Figure 12. Cell voltage distributions of three equalizers after balancing.

In summary, DLE1 and DLE2 equalizers realize better equalization performance compared with AC2C equalizer. In addition, the DLE2 equalizer decreases efficiency and speed a little compared with the DLE1 equalizer due to adding second stage equalization, but the maximum voltage gap and variance are minimum of the DLE2 equalizer among three equalizers. Furthermore, the maximum voltage gap of the DLE2 equalizer is controllable and does not increase as N increases. It means that the DLE2 equalizer can better prolong battery lifecycle and available capacity compared with the AC2C equalizer and the DLE1 equalizer. However, as in any engineering problem, the DLE2 equalizer exists as a tradeoff. The DLE2 equalizer increases equalization performance, but it also increases complexity of the control strategy compared with the AC2C equalizer and DLE1 equalizer.

7. Conclusions

This paper proposes a new double-layer E-structure (DLE) equalizer for battery voltage equalization, in which the equalization time can be decreased compared with AC2C equalizer. In addition, a novel two-stage control strategy is proposed to decrease the maximum voltage gap. The novel control strategy is very useful to meet higher cell voltage consistency. Furthermore, simulations and experiments are used to verify the validity of the proposed equalizer and control strategy. Thus, it is anticipated that the proposed equalizer and control strategy will allow important improvements in the performance of energy storage systems.

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