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A Power Loss Decrease Method Based on Finite Set Model Predictive Control for a Motor Emulator with Reduced Switch Count

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Abstract: This paper presents a power loss decrease method based on finite set model predictive control (FSMPC) with delay compensation for a motor emulator with reduced switch count. Specifically, the topology and mathematical model of the proposed motor emulator with reduced switch count are firstly built. Secondly, in light of given instructions, the normal or fault reference current of the motor emulator is set by a reference current setter. Then delay compensation is applied for the predictive current model to calculate the current residual generated by each switch control signal, and the current tracking performance under actions of two adjacent switch control signals is evaluated for each sector. Finally, a switch power loss objective function is defined, then the two adjacent switch control signals that generate the lowest switch power loss are selected for the next second instant, which minimizes the power loss of the motor emulator with ensuring satisfied current tracking performance. Simulation and experimental results show the feasibility and effectiveness of the proposed method.

Keywords: motor emulator; power loss; current tracking; finite set model predictive control

1. Introduction

As key power equipment, motors are widely used in various applications such as defense military, industrial production, and rail transit [1–3]. In the past few decades, the research about motor operating on fault state and condition suddenly alteration have become hot topics in high voltage and power applications [4,5]. The physical motors in the experiments of motor faults are usually damaged, which are not beneficial for performing experiments repeatedly and the cost of the experiments is high. Moreover, the drive shafts of the two physical motors in the experiments of speed with sudden alteration are connected together by adopting the output torque of one motor drive system as the load torque of another motor drive system. The speed of physical motors in the experiments is difficult to sudden change. Stator current of a motor is one of the most reliable electrical signals that reflecting specific features of motor operating on fault state and condition suddenly alteration [6,7]. Motor emulator was proposed by the British scholar H.J. Slater for the first time [8,9], in which the port characteristics of load current are the same as that of stator current of physical motor by controlling power electronic components. So various experiments that motor operating on fault state and condition sudden alteration could be conducted by motor emulator instead of physical motor. It is more secure and economical to perform these experiments by motor emulator compared with a physical motor.

The core of the motor emulator is the load current tracking stator current of motor [10,11]. During several years, motor emulators with plenty of electronic components are employed to simulate port characteristics of stator current [12,13]. In [14,15], the three-level converter of motor emulator

is constituted by twelve Insulated Gate Bipolar Translators (IGBTs) and eighteen antiparallel diodes. Other motor emulators can be found in [16,17], in which the two-level converter is composed of six IGBTs and six antiparallel diodes. In [18], linear inverter structure is applied to reduce the harmonics of load current in the motor emulator, but the cost is double the number of electronic components compare with traditional two-level inverter. The load model of motor emulator proposed in [19] is an inductor-capacitor-inductor (LCL) filter, which improves current ripple induced by high-frequency switch, but increase reactive power consumption. There are many electronic components are used in these above motor emulators, which increase volume, weight, cost and directly incur excessive switch power loss [20]. Therefore, the power loss of the motor emulator caused by electronic components has become an important issue to be considered.

The load current tracking control of the motor emulator is mostly realized by PI modulation in the present motor emulators. In [21], the dynamic mathematical model of asynchronous motor is established to realize real-time calculation of stator current and tracking control of load current. A wind generator emulator is proposed in [22], which simulates static characteristics of stator current at different wind speeds by controlling a converter. But the steady-state error between stator current and load current is hardly eliminated by PI modulation. A current tracking method based on FSMPC is presented in [23], which improves the accuracy and rapidity of current tracking when compare to PI modulation. In [24], an optimized current control method with delay compensation is proposed to overcome harmonic current in distributed generation converters, and reference current at the next instant is tracked by controlling one switch control signal to generate one basic space voltage vector during every sampling period. However, these presented motor emulators only pursuit current tracking performance as the control object, while power loss of motor emulators is severely neglected. For motor emulators, especially applying to high voltage and power systems, various crucial factors such as on-off time and frequency of switch, can affect switch power loss, which directly linked with service behavior and life of switch. To the best of our knowledge, there is a lack of work about the power loss control method of motor emulator.

Motivated by the above discussion, a power loss decrease method for a reduced switch count motor emulator is proposed in this paper, which is realized by FSMPC with delay compensation. At the first, a topology of the motor emulator is proposed, in which the switch count of converter is reduced. Secondly, a power loss decrease method based on FSMPC is presented, an objective function is designed to select two adjacent switch control signals that generating lowest switch power loss on the premise of ensuring current tracking performance. Finally, the delay compensation is applied to improve current tracking accuracy, which is realized by calculating the current residual between predicted load current and reference current at the next second instant.

The rest of the paper is organized as follows. The topology and modeling of the motor emulator with reduced switch count are illustrated in Section 2. The power loss decrease method based on FSMPC with delay compensation is elaborated upon in Section 3. Section 4 is dedicated to present experimental results and discussion of switch power loss and performance of current tracking of motor emulator. Finally, the conclusions of this paper are reviewed in Section 5.

2. Motor Emulator with Reduced Switch Count

2.1. Topology of Motor Emulator

The topology of the motor emulator with reduced switch count is presented in Figure 1. It consists of the three-phase four-switch converter, coupled load network, motor model, the reference current setter and predictive controller. In three-phase four-switch converter, *b* and *c* phase are constructed of four active switches and four antiparallel diodes, and *a* phase is composed of two dc-link capacitors. The coupled load network consists of three-phase resistance-inductance load, where each phase includes a coupled resistance R and a coupled inductance L. The left and right ports of coupled load networks are connected to three-phase midpoint of three-phase four-switch converter and voltage

source. The motor model is a squirrel cage asynchronous motor model, which provides a normal three-phase stator current signal. According to given instruction, reference current is generated by reference current setter. When normal instruction is given, a three-phase stator current is adopted directly as reference current signal. When fault instruction is given, fault reference current signal is generated by conditioning three-phase stator current signal and specific fault signal, which is detailed in [25]. By calculating the current residual between reference current signal and predictive value of load current, the best applicable switch control signal is selected by predictive controller as switch control signal of three-phase four-switch converter for the next second instant.

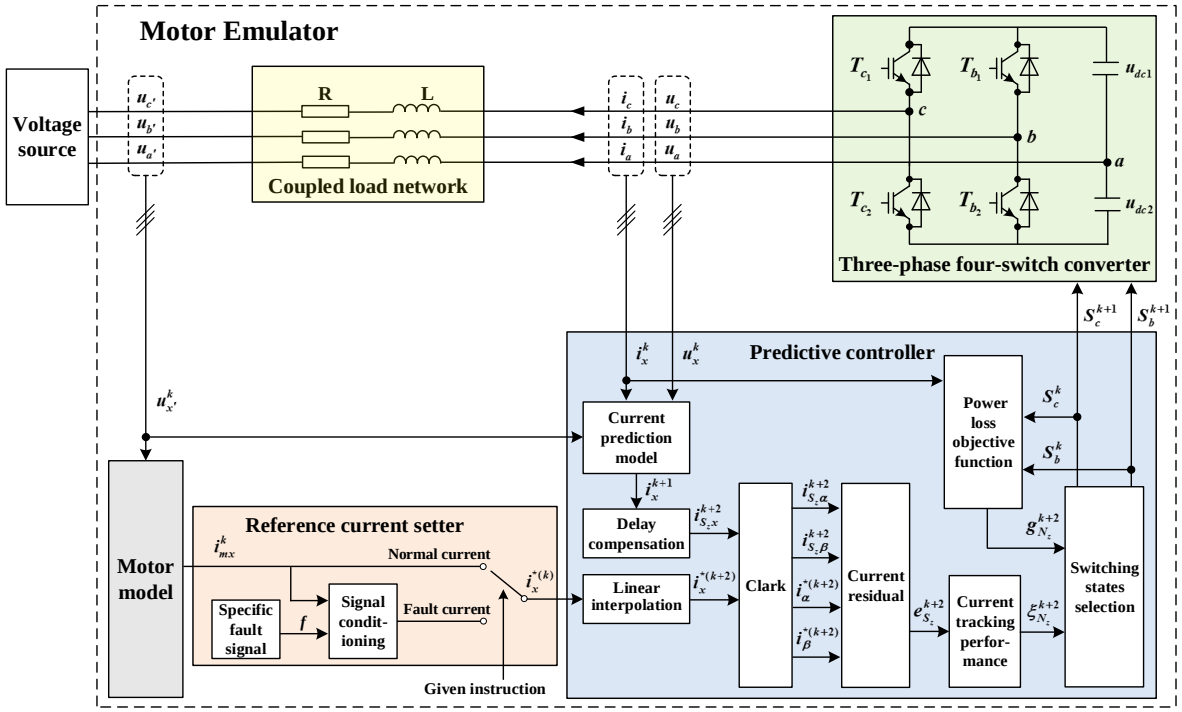


Figure 1. The topology of motor emulator with reduced switch count.

2.2. Modeling of Motor Emulator

Three-phase output voltages of three-phase four-switch converter can be expressed by switching state as:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = u_{dc} \begin{bmatrix} 0.5 \\ S_b \\ S_c \end{bmatrix} \tag{1}$$

where u_a, u_b and u_c are output voltage values of a, b and c phases of three-phase four-switch converter, u_{dc} is input voltage of three-phase four-switch converter, which is the sum of voltages of split capacitors u_{dc1} and u_{dc2} at the dc side. S_b and S_c are switching states of b and c phases in the three-phase four-switch converter, each of them has two logical states 0 and 1 [26,27]. When $S_X = 0$, T_{X_1} is off and T_{X_2} is on. When $S_X = 1$, T_{X_1} is on and T_{X_2} is off , $X = b, c$.

In addition, the switch control signal of three-phase four-switch converter can be defined as S_z, which can be given by $S_z = S_b S_c$, and z represents the selected number of S_z. The basic space voltage vector corresponding to switch control signal S_z is defined as $\boldsymbol{V}_z$, which is synthesized by three-phase output voltages $\boldsymbol{u_a}$, $\boldsymbol{u_b}$ and $\boldsymbol{u_c}$ in three-phase *abc* static coordinate frame. The basic space voltage vector $\boldsymbol{V}_z$ is described as (2) and the spatial distribution on the *abc* static coordinate frame is shown Figure 2.The relationship of switch control signal S_z, three-phase output voltages $\boldsymbol{u_a}$, $\boldsymbol{u_b}$ and $\boldsymbol{u_c}$, and basic space voltage vectors $\boldsymbol{V}_z$ are listed in Table 1.

$$\boldsymbol{V}_z = \boldsymbol{u}_a + \boldsymbol{u}_b + \boldsymbol{u}_c \tag{2}$$

Table 1. Switch control signals, three-phase output voltages and basic space voltage vectors.

Selected Number	Switch Control Signals	Three-Phase Output Voltages			Basic Space Voltage Vectors
z	$S_z = S_b S_c$	$\boldsymbol{u}_a$	$\boldsymbol{u}_b$	$\boldsymbol{u}_c$	$\boldsymbol{V}_z$
1	00	$\frac{1}{2}u_{dc}e^{j0}$	0	0	$\frac{1}{2}u_{dc}e^{j0}$
2	01	$\frac{1}{2}u_{dc}e^{j0}$	0	$u_{dc}e^{j\frac{4\pi}{3}}$	$\frac{\sqrt{3}}{2}u_{dc}e^{j\frac{3\pi}{2}}$
3	11	$\frac{1}{2}u_{dc}e^{j0}$	$u_{dc}e^{j\frac{2\pi}{3}}$	$u_{dc}e^{j\frac{4\pi}{3}}$	$\frac{1}{2}u_{dc}e^{j\pi}$
4	10	$\frac{1}{2}u_{dc}e^{j0}$	$u_{dc}e^{j\frac{2\pi}{3}}$	0	$\frac{\sqrt{3}}{2}u_{dc}e^{j\frac{\pi}{2}}$

In *abc* static coordinate frame, every work period of the three-phase four-switch converter is divided into four sectors by four basic space voltage vectors. The sector formed by two adjacent basic space voltage vectors $\boldsymbol{V}_z$ and $\boldsymbol{V}_{z+1}$ is named as N_z, where $(z, z+1)$ can be $(1,2)$, $(2,3)$, $(3,4)$ and $(4,1)$, as shown in Figure 2.

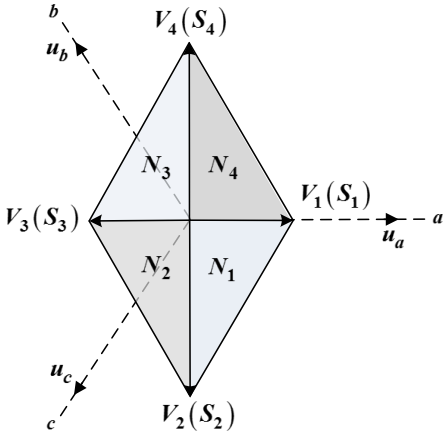


Figure 2. Spatial distribution diagram of basic space voltage vectors and sectors.

The voltage state equation of the motor emulator can be expressed as:

$$u_x = u_{x'} + Ri_x + L\frac{di_x}{dt}, \qquad x = a, b, c;\ x' = a', b', c'. \tag{3}$$

where u_x is output voltage of x phase of three-phase four-switch converter, $u_{x'}$ is output voltage of x' phase of voltage source. i_x is load current of x phase of coupled load network. R and L are the resistance and inductance of coupled load network respectively.

Then, predictive current at the (k + 1)-th instant can be obtained by discretizing Equation (3):

$$i_x^{k+1} = (1 - \frac{RT_s}{L})i_x^k + \frac{T_s}{L}(u_x^k - u_{x'}^k) \tag{4}$$

where k is sampling instant and k = 1, 2, 3 $\cdots$. T_s is the sampling period. i_x^{k+1} is predictive current at the (k + 1)-th instant. i_x^k is sampling of i_x at the k-th instant. u_x^k and $u_{x'}^k$ are samplings of u_x and $u_{x'}$ at the k-th instant respectively.

3. Power Loss Decrease Method Based on FSMPC with Delay Compensation

3.1. Current Tracking Performance

The theory of ideal FSMPC is shown in Figure 3a. Reference stator current i_x^* is obtained and actual load current i_x^k are sampled at the k-th instant, and the optimal switch control signal is determined

during the k-th sampling period and applied to the system at the k-th instant, then load current will reach the expected value at the $(k+1)$-th instant. However, digital process system needs time to perform algorithm, as shown in Figure 3b. The sampling is accomplished at the k-th instant, but the optimal switch control signal is applied to system after t_d delay, which results in error between actual load current and expected value at the $(k+1)$-th instant. Thus, the accuracy and rapidity of current tracking is partly decreased, especially for motor operating on fault state and condition suddenly alteration. Therefore, the delay compensation is adopted to regulate action time of the optimal switch control signal, as shown in Figure 3c. Sampling is completed at the k-th instant and calculating the optimal switch control signal during the the k-th sampling period, and applied to the system at the $(k+1)$-th instant, then load current will reach the expected value at the $(k+2)$-th instant. The delay compensation not only makes up for computation time of the algorithm, but also effectively raises the performance of current tracking for motor operating on fault state and condition suddenly alteration.

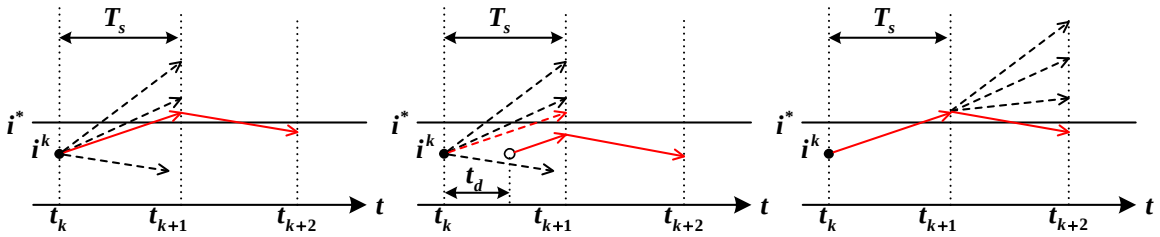


Figure 3. Principle of delay compensation.

According to principle of delay compensation [24], all switch control signals are used to calculate the predictive current at the $(k+2)$-th instant:

$$i_{S_z x}^{k+2} = (1 - \tfrac{RT_s}{L}) i_x^{k+1} + \tfrac{T_s}{L}(u_{S_z x}^{k+1} - u_{x'}^{k}), \qquad z = 1,2,3,4. \tag{5}$$

where $i_{S_z x}^{k+2}$ is predictive current at the $(k+2)$-th instant corresponding to switch control signal S_z. $u_{S_z x}^{k+1}$ predictive voltage at the $(k+1)$-th instant corresponding to switch control signal S_z. Considering that the change of voltage source during one sampling period is not obvious, the sampling of $u_{x'}$ at the $(k+1)$th instant is approximatively equal to $u_{x'}^{k}$.

After Clark coordinate transformation, $i_{S_z x}^{k+2}$ can be converted as:

$$\begin{bmatrix} i_{S_z\alpha}^{k+2} \\ i_{S_z\beta}^{k+2} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{S_z a}^{k+2} \\ i_{S_z b}^{k+2} \\ i_{S_z c}^{k+2} \end{bmatrix} \tag{6}$$

where $i_{S_z\alpha}^{k+2}$ and $i_{S_z\beta}^{k+2}$ are the values of predictive current $i_{S_z x}^{k+2}$ in $\alpha\beta$ stationary frame.

Then, the current residual function at the $(k+2)$-th instant can be defined as:

$$e_{S_z}^{k+2} = |i_{S_z\alpha}^{k+2} - i_{\alpha}^{*(k+2)}|^2 + |i_{S_z\beta}^{k+2} - i_{\beta}^{*(k+2)}|^2 \tag{7}$$

where $e_{S_z}^{k+2}$ is current residual at the $(k+2)$-th instant corresponding to switch control signal S_z. $i_{\alpha}^{*(k+2)}$ and $i_{\beta}^{*(k+2)}$ are the reference currents at the $(k+2)$-th instant in $\alpha\beta$ stationary frame. The $i_{\alpha}^{*(k+2)}$ and $i_{\beta}^{*(k+2)}$ can be constructed by the reference currents at the $(k-1)$-th, the k-th and the $(k+1)$-th instants according to linear interpolation theorem:

$$\begin{cases} i_{\alpha}^{*(k+2)} = 3i_{\alpha}^{*(k+1)} - 3i_{\alpha}^{*(k)} + i_{\alpha}^{*(k-1)} \\ i_{\beta}^{*(k+2)} = 3i_{\beta}^{*(k+1)} - 3i_{\beta}^{*(k)} + i_{\beta}^{*(k-1)} \end{cases} \tag{8}$$

where, when k is equal to 1, the values of $i_\alpha^{*(0)}$ and $i_\beta^{*(0)}$ are set to equal the values of $i_\alpha^{*(1)}$ and $i_\beta^{*(1)}$ respectively.

In the traditional method of current tracking, only one basic space voltage vector $\boldsymbol{V}_z$ is generated by controlling a switch control signal S_z during every sampling period. When the traditional strategy is adopted for the current tracking control of the motor emulator, the error between load current and stator current is larger and current tracking accuracy is lower because of the finiteness and space distribution fixity of basic space voltage vectors. In the method of current tracking in this paper, there are two adjacent basic space voltage vectors $\boldsymbol{V}_z$ and $\boldsymbol{V}_{z+1}$ are generated by controlling two adjacent switch control signals S_z and S_{z+1} during every sampling period. By allocating the action time proportion of the two space voltage vectors during one period, the error between load current and stator current can be minimized.

Since the sum of action time of two adjacent switch control signals S_z and S_{z+1} is constant T_s, and the action time of each switch control signal is inversely proportional to the current residual generated by it, larger current residual leads to smaller action time. Thus the action time of two adjacent switch control signals S_z and S_{z+1} for the sector N_z are derived as:

$$\begin{cases} d_{N_zS_z}^{k+2} = \frac{e_{S_{z+1}}^{k+2}}{e_{S_z}^{k+2}+e_{S_{z+1}}^{k+2}} T_s \\ d_{N_zS_{z+1}}^{k+2} = \frac{e_{S_z}^{k+2}}{e_{S_z}^{k+2}+e_{S_{z+1}}^{k+2}} T_s \\ T_s = d_{N_zS_z}^{k+2} + d_{N_zS_{z+1}}^{k+2} \end{cases} \tag{9}$$

where $d_{N_zS_z}^{k+2}$ and $d_{N_zS_{z+1}}^{k+2}$ are action times two switch control signals S_z and S_{z+1} of sector N_z for the (k + 2)-th instant.

The current tracking performance function for the sector N_z at the (k + 2)-th instant can be designed as:

$$\xi_{N_z}^{k+2} = 1 - \frac{T_s}{4I_{mx}^*}\left(\frac{e_{S_{z+1}}^{k+2}}{d_{N_zS_z}^{k+2}} + \frac{e_{S_z}^{k+2}}{d_{N_zS_{z+1}}^{k+2}}\right) \tag{10}$$

where $\xi_{N_z}^{k+2}$ expresses current tracking performance at the (k + 2)-th instant under the action of the two switch control signals S_z and S_{z+1} for sector N_z. I_{mx}^* is peak value of three-phase reference current i_x^*. The value of $\xi_{N_z}^{k+2}$ is between 0 to 1. When $\xi_{N_z}^{k+2}$ = 1, current tracking performance is optimal, $\xi_{N_z}^{k+2}$ is dropping gradually as the current tracking performance decreases.

3.2. Power Loss Minimization

The switch power loss generated by switch control signal S_z at the (k + 2)-th instant is defined as $P_{S_z}^{k+2}$, which can be given by:

$$P_{S_z}^{k+2} = P_{S_zb_1}^{k+2} + P_{S_zb_2}^{k+2} + P_{S_zc_1}^{k+2} + P_{S_zc_2}^{k+2} \tag{11}$$

where, $P_{S_zb_1}^{k+2}$, $P_{S_zb_2}^{k+2}$, $P_{S_zc_1}^{k+2}$ and $P_{S_zc_2}^{k+2}$ are switch power losses of switches T_{b_1}, T_{b_2}, T_{c_1} and T_{c_2} at the (k + 2)-th instant under the action of switch control signal S_z, they can be expressed as follows:

$$\begin{cases} P_{S_zX_1}^{k+2} = \bar{\delta_X^k}[S_{X_1}^k(|i_X^k| \times u_{S_zX_1}^{k+1} \times T_s) + L_{S_zX_1}^{k+1}] \\ P_{S_zX_2}^{k+2} = \delta_X^k[S_{X_2}^k(|i_X^k| \times u_{S_zX_2}^{k+1} \times T_s) + L_{S_zX_2}^{k+1}] \end{cases}, \quad X = b, c. \tag{12}$$

where, i_X^k is sampling of i_X at the k-th instant. δ_X^k is flag of i_X^k, if $i_X^k \geqslant 0$, $\delta_X^k = 1$; if $i_X^k < 0$, $\delta_X^k = 0$. $S_{X_1}^k$ and $S_{X_2}^k$ are pulse signals of T_{X_1} and T_{X_2} at the k-th instant, $S_{X_1}^k$ = 1 when T_{X_1} on, and $S_{X_1}^k$ = 0 when T_{X_1} off, which also beseem to $S_{X_2}^k$ and T_{X_2}. $u_{S_zX_1}^{k+1}$ and $u_{S_zX_2}^{k+1}$ are on-state voltage drops of T_{X_1} and T_{X_2}

at the $(k+1)$-th instant corresponding to switch control signal S_z, they are assumed to be constant values, which can be found in [25]. $L_{S_zX_1}^{k+1}$ and $L_{S_zX_2}^{k+1}$ are on-off losses of T_{X_1} and T_{X_2} at the $(k+1)$-th instant corresponding to switch control signal S_z, they can be given by:

$$L_{S_zX_m}^{k+1} = \begin{cases} E_{on}, & S_{zX_m}^{k+1} - S_{X_m}^{k} = 1 \\ 0, & S_{zX_m}^{k+1} - S_{X_m}^{k} = 0 \\ E_{off}, & S_{zX_m}^{k+1} - S_{X_m}^{k} = -1 \end{cases}, \quad X = b, c;\ m = 1, 2. \tag{13}$$

where, E_{on} and E_{off} are on and off power loss of switch, they are assumed to be constant values, which can be found in [25]. $S_{zX_m}^{k+1}$ is pulse signal of T_{X_m} at the $(k+1)$-th instant corresponding to switch control signal S_z.

The switch power loss objective function is designed as:

$$g_{N_z}^{k+2} = \frac{P_{S_z}^{k+2} + P_{S_{z+1}}^{k+2}}{8} \tag{14}$$

where, $g_{N_z}^{k+2}$ is average switch power loss at the $(k+2)$-th instant under the action of the two adjacent switch control signals S_z and S_{z+1} for sector N_z. During the the k-th sampling period, two adjacent switch control signals of each sectors are orderly used to calculate value of switch power loss objective function $g_{N_z}^{k+2}$.

The switching states of b and c phases can be obtained according to Equation (15):

$$g[S_b^{k+1}, S_c^{k+1}] = \min_{\substack{\xi_{N_z}^{k+2} \in (0.95, 1] \\ z = 1,2,3,4}} \{g_{N_z}^{k+2}\} \tag{15}$$

where, S_b^{k+1} and S_c^{k+1} are switching states of b and c phases in the three-phase four-switch converter at the $(k+1)$-th instant. On the condition that current tracking performance greater than 95%, the switches that generating lowest switch power loss are selected to operate during every sampling period, then switch power loss can be reduced.

The flowchart of proposed power loss decrease method based on FSMPC with delay compensation is shown in Figure 4.

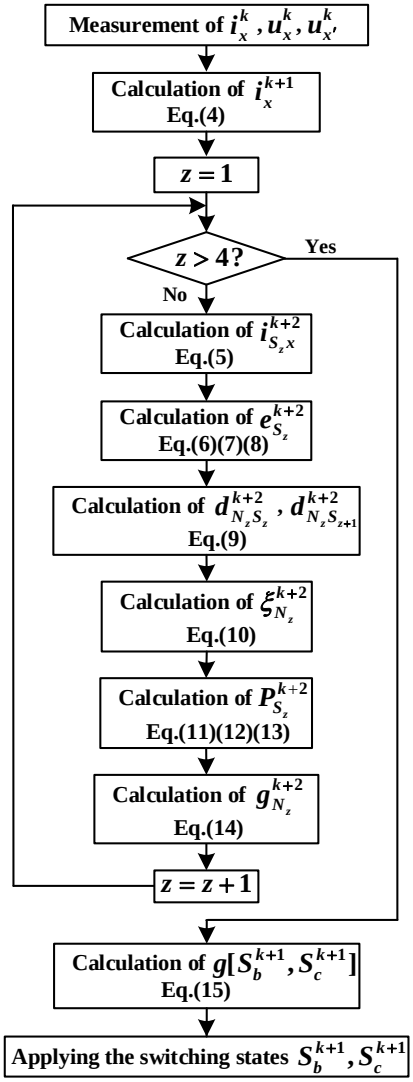


Figure 4. Flowchart of the FSMPC with delay compensation.

4. Experimental Results

In this section, the power loss decrease method for motor emulator based on reducing switch count and FSMPC with delay compensation is verified on a hardware-in-the-loop platform as shown in Figure 5. The corresponding component parameters are indicated in Table 2. The platform consists of a physical controller, real-time simulator, and PC. Physical controller adopts TMS320F28335 control chip with high processing capacity and rich interface resources to realize real-time control of voltage source. The real-time simulator includes DS1007CPU board and DS5203FPGA board, the former is used for real-time calculation of reference current setter and predictive controller, and the latter is used for real-time simulation of motor model, coupled load network and three-phase four-switch converter. The PC collects real-time data from model by real-time simulation software, and monitors running state of observation point.

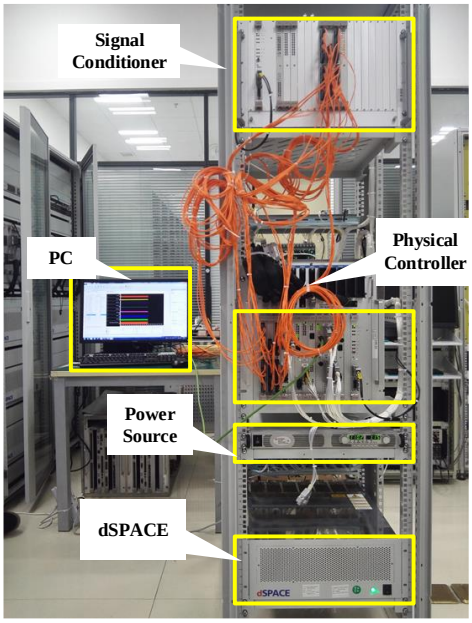


Figure 5. Experimental platform.

Table 2. Parameters of the experimental platform.

	Parameters	High Power Motor	Low Power Motor
Motor model	Rated power	300 kW	100 W
	Stator inductance	0.142 H	0.021 H
	Rotor inductance	0.130 H	0.018 H
	Stator resistor	0.144 Ω	0.014 Ω
	Rotor resistor	0.142 HΩ	0.012 Ω
Coupled load network	Load resistor	1 Ω	0.05 Ω
	Load inductance	0.004 H	0.00013 H
Frequency	Sampling frequency	20 kHz	20 kHz
	Switching frequency	10 kHz	10 kHz

4.1. Motor Emulators with Different Switch Counts

On the condition that high power motor is operating with reference load current set 60 A/20 Hz and low power motor is operating with reference load current set 7 A/30 Hz, respectively. The comparison of current tracking performance and switch power loss for traditional six-switch motor emulator and proposed four-switch motor emulator without power loss minimization control are displayed in this section.

For the high power motor, the experimental waveforms of *a*-phase reference current, *a*-phase load current of six-switch motor emulator, and *a*-phase load current of four-switch motor emulator are shown in Figure 6a. Based on these conditions, the experimental waveforms of average three-phase current residual of between reference current and load current of six-switch and four-switch motor emulator are shown in Figure 6b, respectively. The experimental waveforms of average three-phase current THD (total harmonic distortion) of reference current, load current of six-switch and four-switch motor emulator are shown in Figure 6c, respectively. The switch power loss during entire simulation period of six-switch and four-switch motor emulator are shown in Table 3. Similarly, the experimental waveforms for the low power motor are shown in Figure 7a–c and Table 4.

Table 3. Switch power losses of traditional six-switch and proposed four-switch motor emulator for high power motor.

	Switch Power Loss (KJ)								σ (%)
	p_{a1}	p_{a2}	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
Traditional six-switch	21.09	18.62	19.16	20.43	20.27	19.75	119.32	19.89	23.8
Proposed four-switch	—	—	22.40	23.36	23.25	21.83	90.84	22.71	

Table 4. Switch power losses of traditional six-switch and proposed four-switch motor emulator for low power motor.

	Switch Power Loss (J)								σ (%)
	p_{a1}	p_{a2}	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
Traditional six-switch	34.74	35.22	35.46	34.87	35.91	34.05	210.25	35.04	20.7
Proposed four-switch	—	—	41.75	42.16	41.84	40.97	166.72	41.68	

As shown in Figure 6a, comparing to the zero-crossing time of reference current, the zero-crossing time of six-switch motor emulator is delayed by about 30 us, which is expressed as t_n^T, and the zero-crossing time of four-switch motor emulator is delayed by about 35 us, which is denoted as t_n^P. From Figure 6b, average three-phase current residual of six-switch motor emulator is about 1.1A, current tracking accuracy is 98.2% according to (16). Average three-phase current residual of four-switch motor emulator is about 1.3 A, current tracking accuracy is 97.8% according to (17). In Figure 6c, the average THD of three-phase reference current is 1.30%, and average THD of three-phase load current of six-switch and four-switch motor emulator are about 1.7% and 1.80%, respectively. From Table 3, comparing to a traditional six-switch motor emulator, although the average switch power loss has increased, the sum of switch power loss decreases 23.81%, according to (18).

$$\varepsilon^T = \frac{i^R - \Delta i^{RT}}{i^R} \times 100\% \tag{16}$$

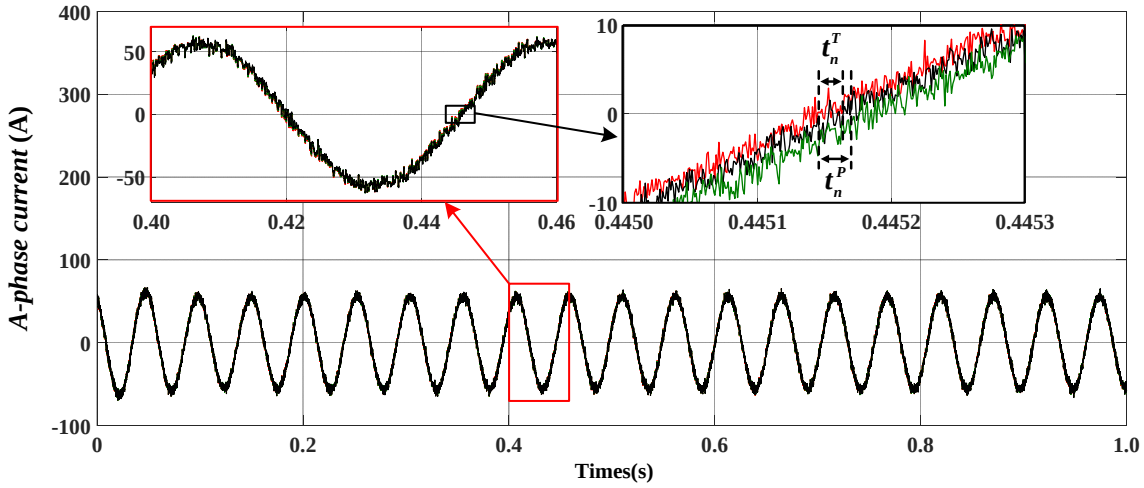
where ε^T is current tracking accuracy of traditional six-switch motor emulator, i^R is reference current, Δi^{RT} is average three-phase current residual between reference current and load current of traditional six-switch motor emulator.

$$\varepsilon^P = \frac{i^R - \Delta i^{RP}}{i^R} \times 100\% \tag{17}$$

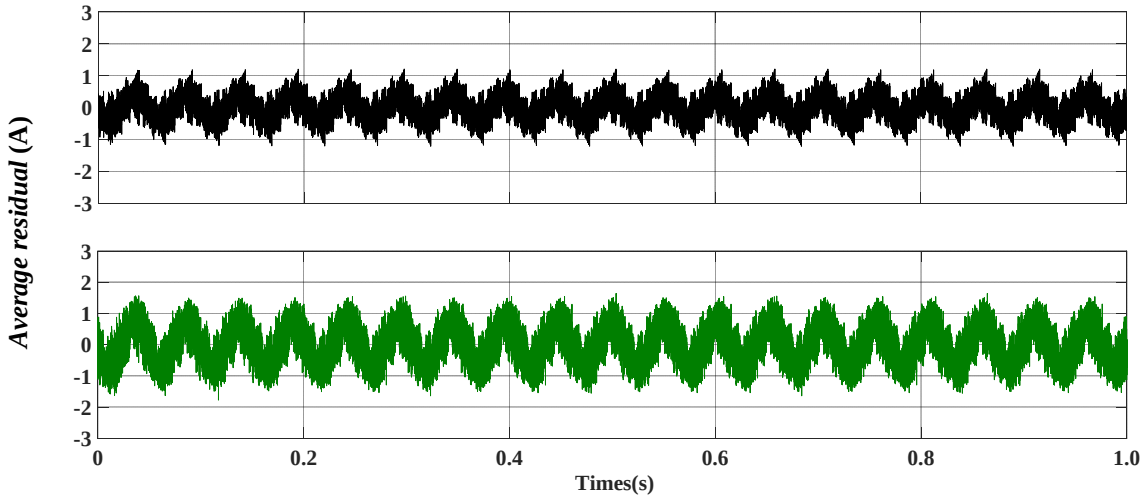
where ε^P is current tracking accuracy of proposed four-switch motor emulator, i^R is reference current, Δi^{RP} is average three-phase current residual between reference current and load current of proposed four-switch motor emulator.

$$\sigma = \frac{P_{sum}^T - P_{sum}^P}{P_{sum}^T} \times 100\% \tag{18}$$

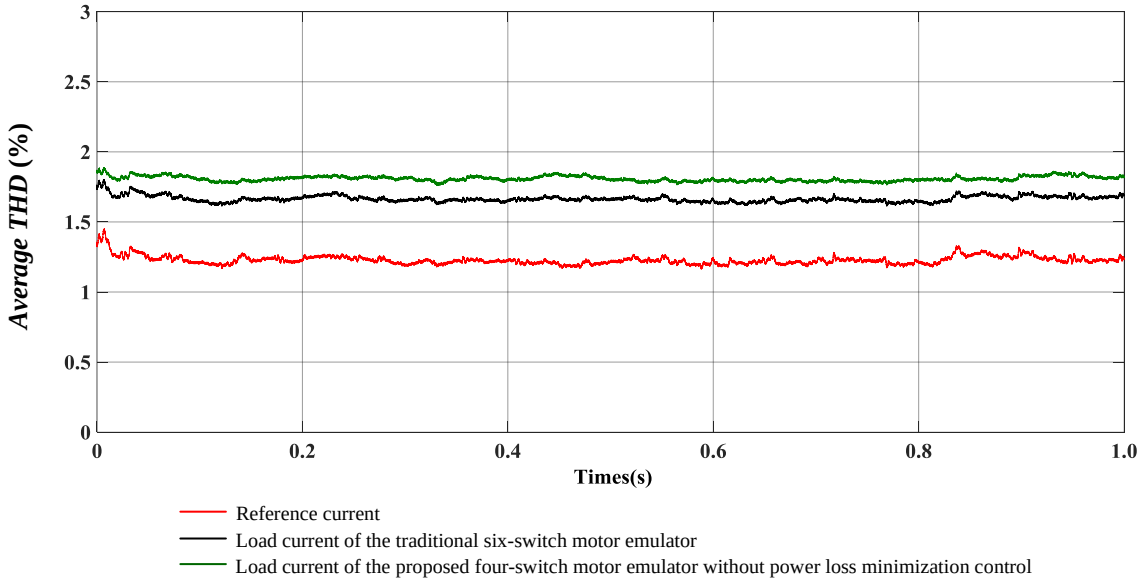
where σ is decrease percent of total switch power loss, P_{sum}^T is sum of switch power loss of traditional six-switch motor emulator, P_{sum}^P is sum of switch power loss of proposed four-switch motor emulator.



(**a**)A-phase currents

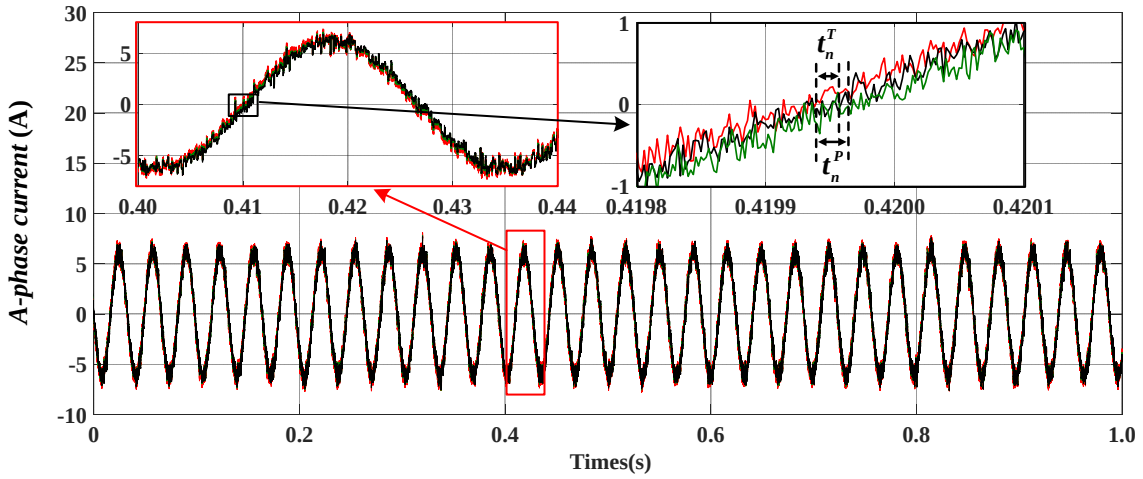


(**b**)Average residual of three-phase currents

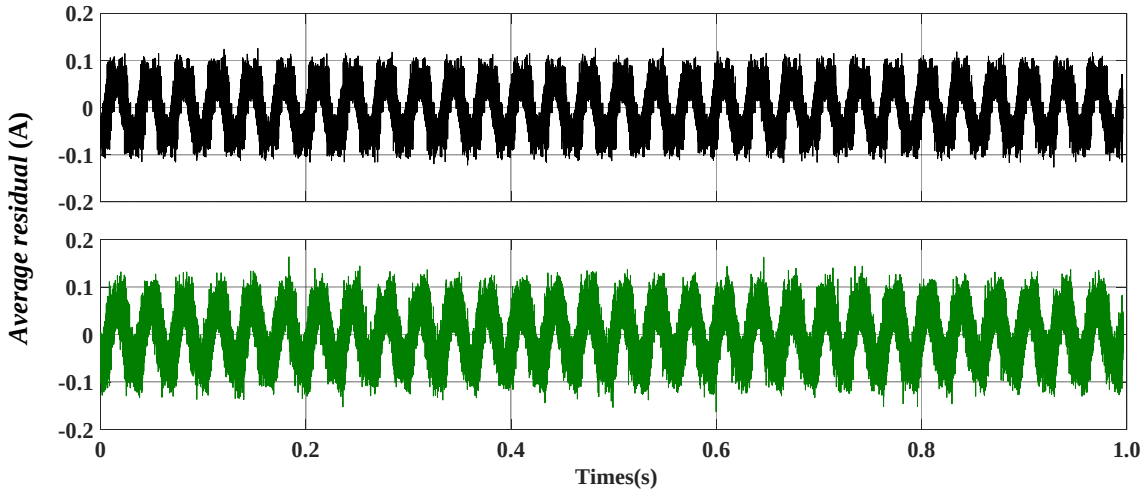


(**c**)Average THD of three-phase currents

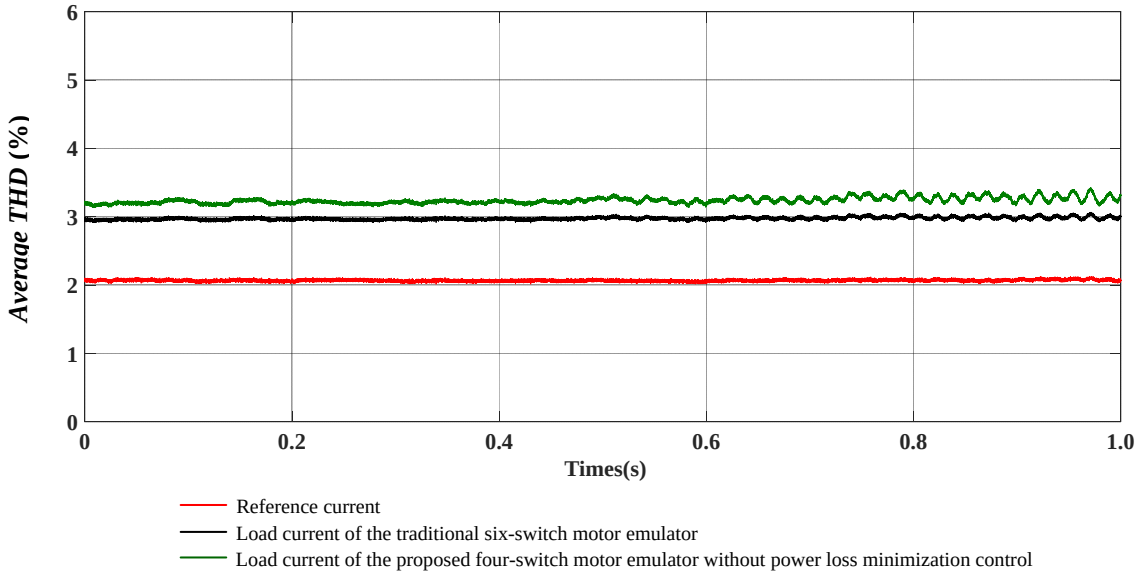
Figure 6. Waveforms of traditional six-switch and proposed four-switch motor emulator for high power motor.



(**a**)A-phase currents



(**b**)Average residual of three-phase currents



(**c**)Average THD of three-phase currents

Figure 7. Waveforms of traditional six-switch and proposed four-switch motor emulator for low power motor.

As shown in Figure 7a, comparing to the zero-crossing time of reference current, the zero-crossing time of six-switch motor emulator is delayed by about 30 us, which is expressed as t_n^T, and the zero-crossing time of four-switch motor emulator is delayed by about 35 us, which is denoted as t_n^P. From Figure 7b, average three-phase current residual of six-switch motor emulator is about 0.1 A, current tracking accuracy is 98.6%. Average three-phase current residual of four-switch motor emulator is about 0.12 A, current tracking accuracy is 98.3%. In Figure 7c, the average THD of three-phase reference current is 2.1%, and average THD of three-phase load current of six-switch and four-switch motor emulator are about 2.9% and 3.3%, respectively. From Table 4, comparing to traditional six-switch motor emulator, although the average switch power loss has increased, the sum of switch power loss decreases 20.7%. The experimental results have shown that the proposed four-switch motor emulator decrease effectively switch power loss on the premise of ensuring current tracking effect of motor emulator for the high and low power motor.

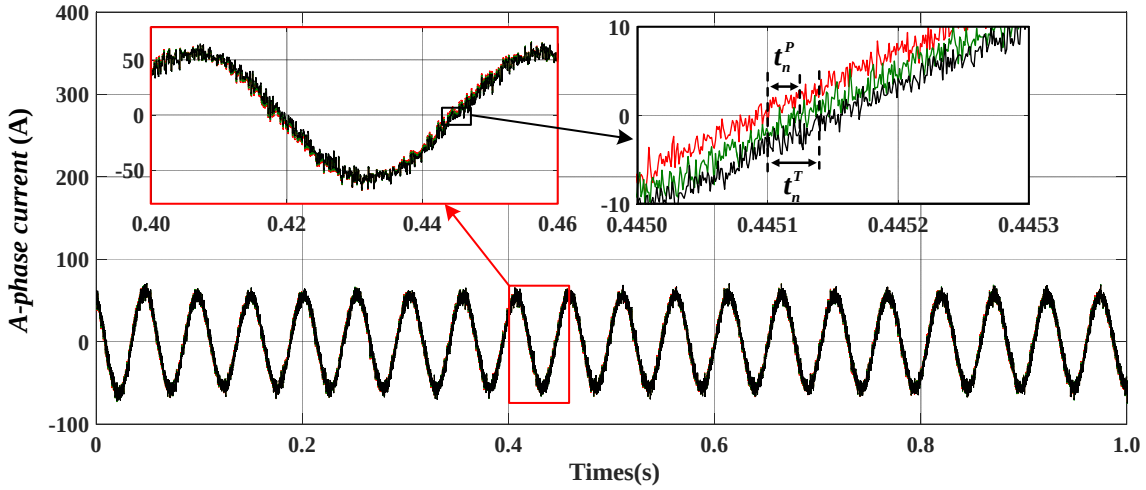
4.2. Current Tracking Performance Based on FSMPC and FSMPC with Delay Compensation

On the condition that high power motor is operating with reference load current set 60 A/20 Hz and low power motor is operating with reference load current set 7 A/30 Hz, respectively. The comparison of current tracking performance and switch power loss based on FSMPC and FSMPC with delay compensation on the condition without power loss minimization control are displayed in this section.

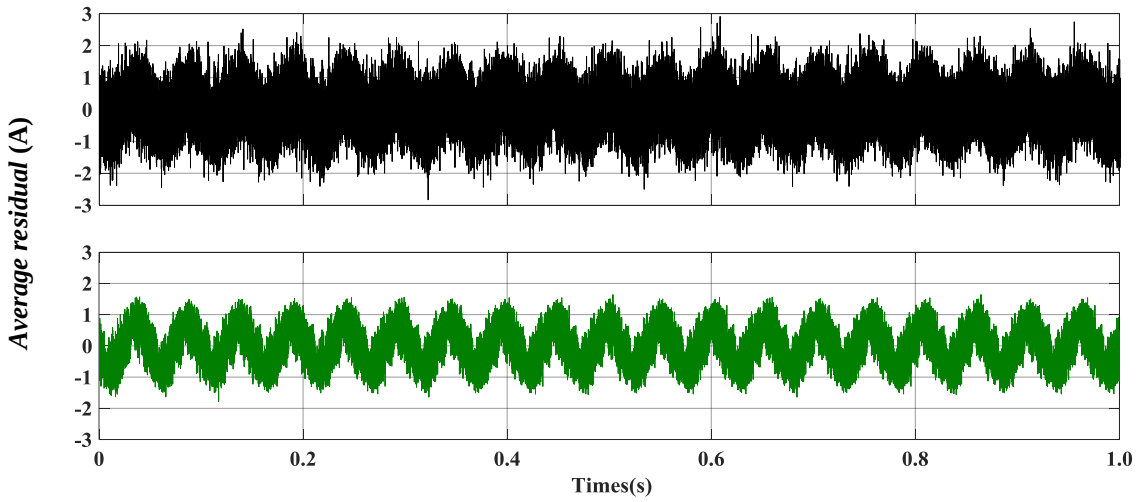
For the high power motor, the experimental waveforms of *a*-phase reference current, *a*-phase load current based on FSMPC, and *a*-phase load current based on FSMPC with delay compensation are shown in Figure 8a. With these conditions, the experimental waveforms of average three-phase current residual of between reference current and load current based on FSMPC and FSMPC with delay compensation are shown in Figure 8b, respectively. The experimental waveforms of average three-phase current THD of reference current, load current based on FSMPC and FSMPC with delay compensation are shown in Figure 8c, respectively. The switch power loss results during entire simulation period based on FSMPC and FSMPC with delay compensation are shown in Table 5. Similarly, the experimental waveforms for the low power motor are shown in Figure 9a–c and Table 6. Comparison of based on FSMPC and FSMPC with delay compensation for high and low power motor are shown in Table 7.

Table 5. Switch power losses based on FSMPC and FSMPC with delay compensation for high power motor.

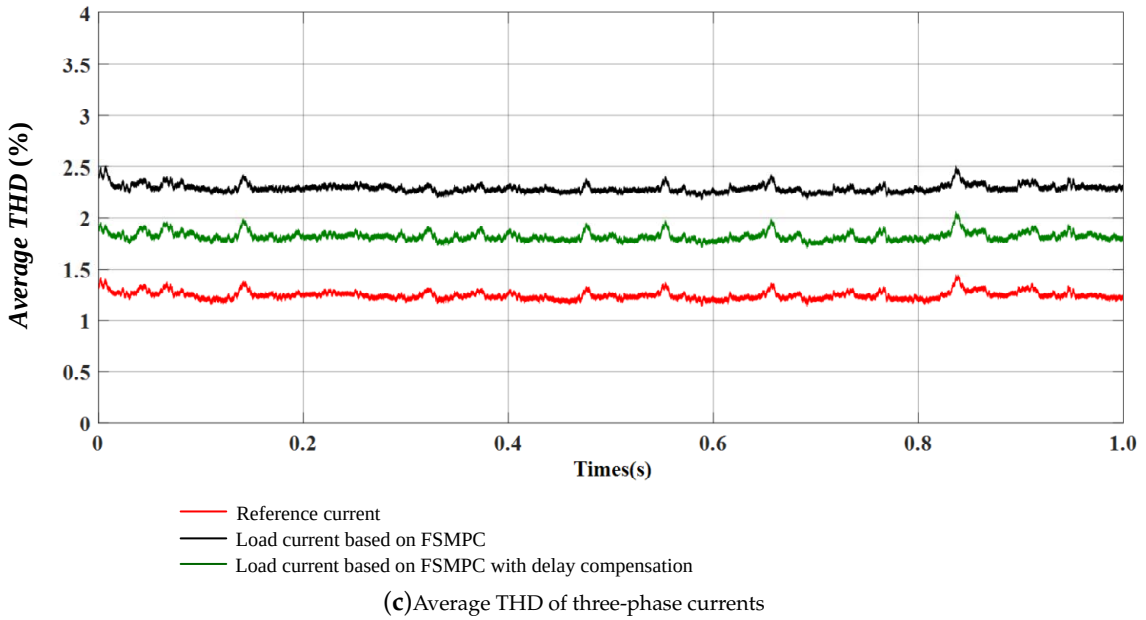
	Switch Power Loss (KJ)						σ **(%)**
	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
FSMPC	22.40	23.36	23.25	21.83	90.84	22.71	0.13
FSMPC with delay compensation	21.84	23.47	23.69	21.72	90.72	22.68	



(**a**)A-phase currents

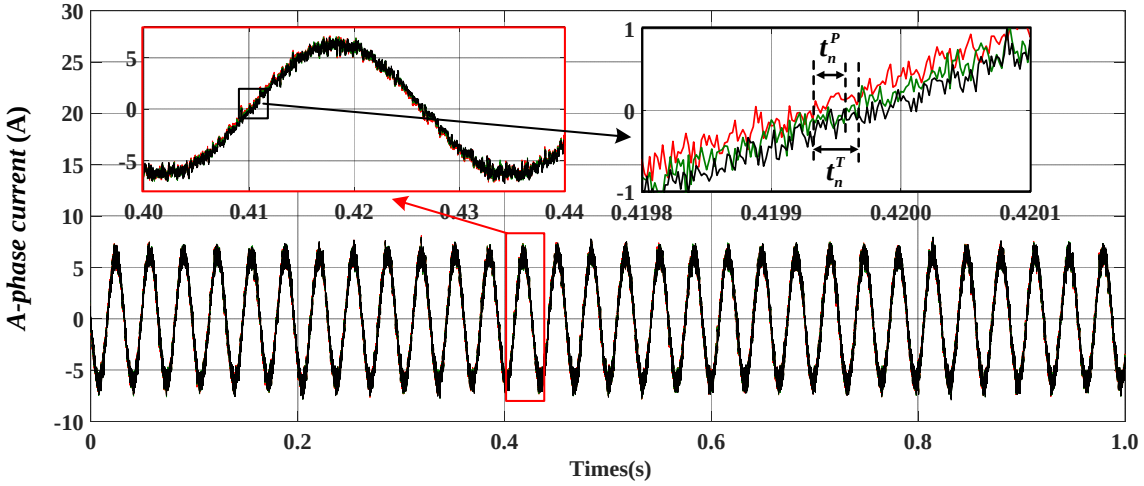


(**b**)Average residual of three-phase currents

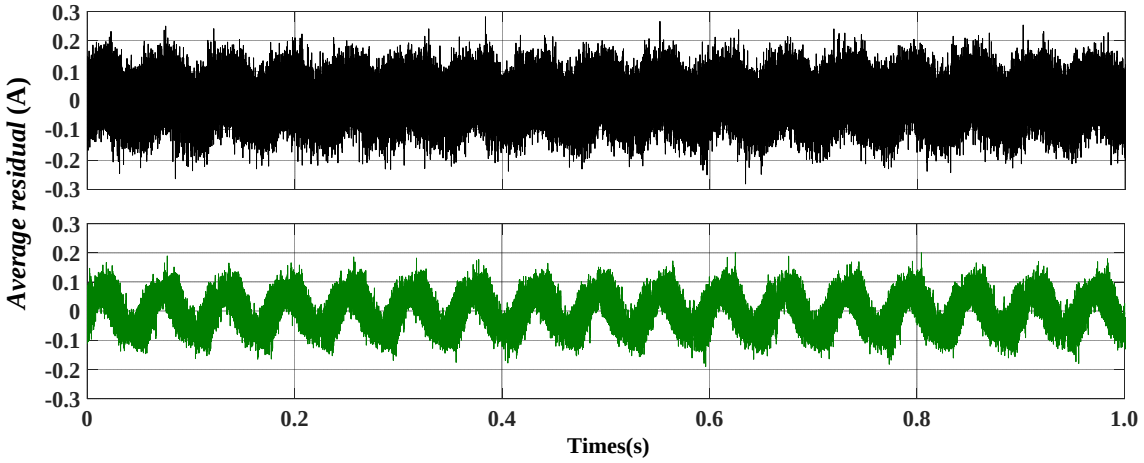


(**c**)Average THD of three-phase currents

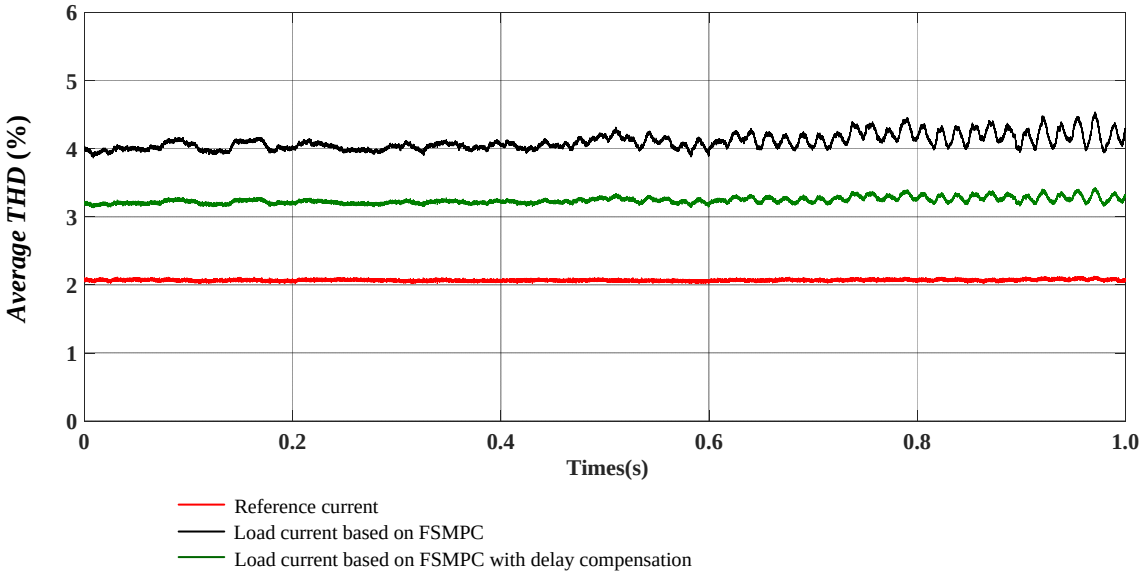
Figure 8. Waveforms based on FSMPC and FSMPC with delay compensation for high power motor.



(**a**)A-phase currents



(**b**)Average residual of three-phase currents



(**c**)Average THD of three-phase currents

Figure 9. Waveforms based on FSMPC and FSMPC with delay compensation for low power motor.

As shown in Figure 8a, comparing to the zero-crossing time of reference current, the zero-crossing time of load current based on FSMPC is delayed by about 45 us, which is expressed as t_n^T, and the zero-crossing time of load current based on FSMPC with delay compensation is delayed by about 35 us, which is denoted as t_n^P. From Figure 8b, average three-phase current residual based on FSMPC is about 1.9 A, current tracking accuracy is 96.8%. Average three-phase current residual based on FSMPC with delay compensation is about 1.3 A, current tracking accuracy is 97.8%. In Figure 8c, the average THD of three-phase reference current is 1.30%, and average THD of three-phase load current based on FSMPC and FSMPC with delay compensation are about 2.4% and 1.80%, respectively. From the Table 5, the sum and average switch power loss based on FSMPC and FSMPC with delay compensation are almost equal.

Table 6. Switch power losses based on FSMPC and FSMPC with delay compensation for low power motor.

	Switch Power Loss (J)						σ **(%)**
	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
FSMPC	41.75	42.16	41.84	40.97	166.72	41.68	0.22
FSMPC with delay compensation	41.80	41.94	41.57	41.06	163.37	41.59	

As shown in Figure 9a, comparing to the zero-crossing time of reference current, the zero-crossing time of load current based on FSMPC is delayed by about 45 us, which is expressed as t_n^T, and the zero-crossing time of load current based on FSMPC with delay compensation is delayed by about 35 us, which is denoted as t_n^P. From Figure 9b, average three-phase current residual based on FSMPC is about 0.17 A, current tracking accuracy is 97.5%. Average three-phase current residual based on FSMPC with delay compensation is about 0.12 A, current tracking accuracy is 98.3%. In Figure 9c, the average THD of three-phase reference current is 2.1%, and average THD of three-phase load current based on FSMPC and FSMPC with delay compensation are about 3.2% and 4.3%, respectively. From the Table 6, the sum and average switch power loss based on FSMPC and FSMPC with delay compensation are almost equal. The experimental results have shown that, for the high and low power motor, the residual between load current and reference current is reduced and current tracking accuracy is improved by applying FSMPC with delay compensation, when compared with FSMPC.

Table 7. Comparison of based on FSMPC and FSMPC with delay compensation for high and low power motor.

	High Power Motor		**Low Power Motor**	
	FSMPC	**FSMPC with Delay Compensation**	**FSMPC**	**FSMPC with Delay Compensation**
Tracking accuracy of load current	96.8%	97.8%	97.5%	98.3%
Zero-crossing delay time	45 us	35 us	45 us	35 us
THD	2.4%	1.8%	4.3%	3.2%
Decrease percent of switch power loss	0.13%		0.22%	
Load inductance	4 mH		0.13 mH	
Switching frequency	10 kHz			
Sampling frequency	20 kHz			

4.3. Motor Rotor Broken Bar Fault

When the motor is operating under rotor broken bar fault with the reference current for high power motor set 60 A/20 Hz and low power motor set 7 A/30 Hz respectively, and fault level set 20%. The comparison of current tracking performance and switch power loss for proposed motor emulator without and with power loss minimum control are displayed in this section.

For the high power motor, the experimental waveforms of *a*-phase reference current, *a*-phase load current of proposed motor emulator without and with power loss minimization control are shown in Figure 10a. Based on these conditions, the experimental waveforms of average three-phase current residual of between reference current and load current of without and with power loss minimization control are shown in Figure 10b, respectively. The experimental waveforms of average three-phase current THD of reference current, load current with or without power loss minimization control are shown in Figure 10c, respectively. The switch power loss results during entire simulation period of proposed motor emulator without and with power loss minimization control are shown in Table 8. Similarly, the experimental waveforms for the low power motor are shown in Figure 11a–c and Table 9.

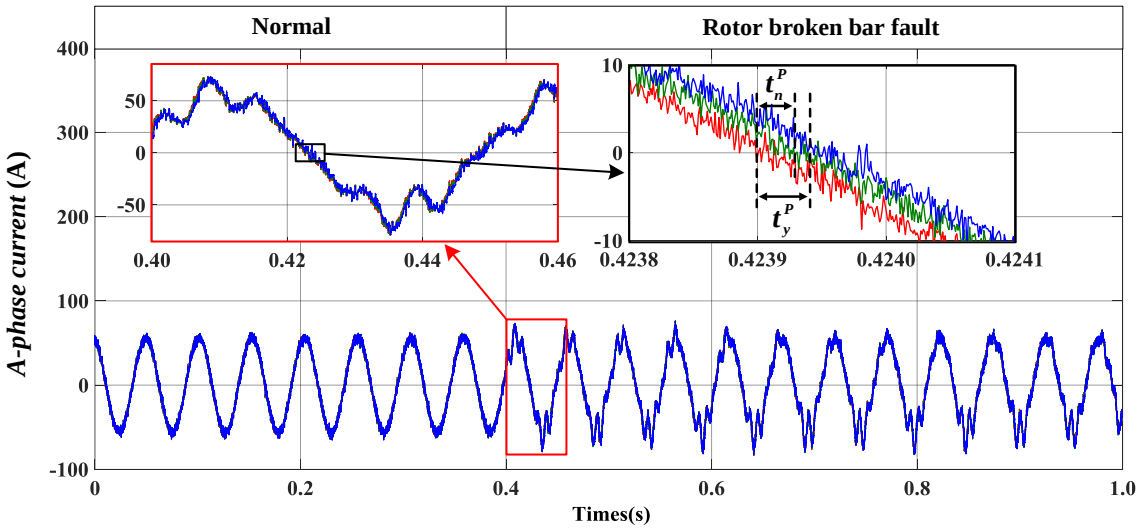
Table 8. Switch power losses of motor rotor broken bar fault for high power motor.

	Switch Power Loss (KJ)						σ **(%)**
	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
Without	22.91	23.84	23.75	22.36	92.86	23.22	22.74
With	17.52	18.37	18.65	17.22	71.76	17.94	

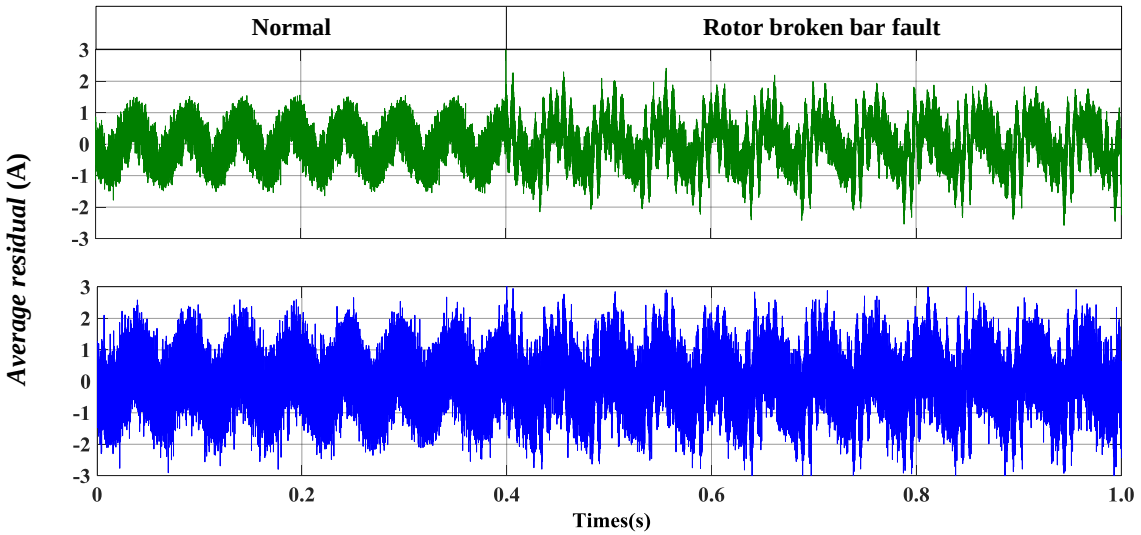
As shown in Figure 10a, when the motor is operating under rotor broken bar fault, comparing to the zero-crossing time of reference current, the zero-crossing time of load current without power loss minimization control is delayed by about 40 us, which is expressed as t_n^P, and the zero-crossing time of load current with power loss minimization control is delayed by about 50 us, which is denoted as t_y^P. From Figure 10b, average three-phase current residual of without and with power loss minimization control are about 2.0 A and 2.2 A, and current tracking accuracy are 96.6% and 96.3%. In Figure 10c, the average THD of three-phase reference current is 19%, and average THD of three-phase load current of without and with power loss minimization control is 22% and 24%, respectively. From Table 8, consideration of power loss, the sum and average switch power loss of the latter have both decreased by 22.74% than the former.

Table 9. Switch power losses of motor rotor broken bar fault for low power motor.

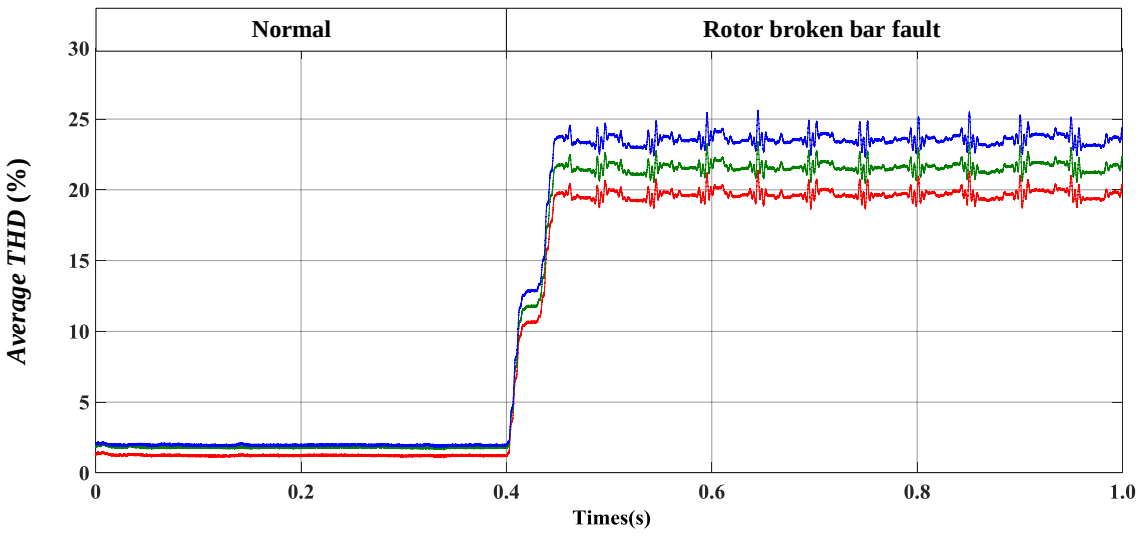
	Switch Power Loss (J)						σ **(%)**
	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
Without	42.29	42.61	41.77	42.85	169.52	42.38	21.47
With	32.96	33.72	33.36	33.04	133.08	33.27	



(**a**)A-phase currents

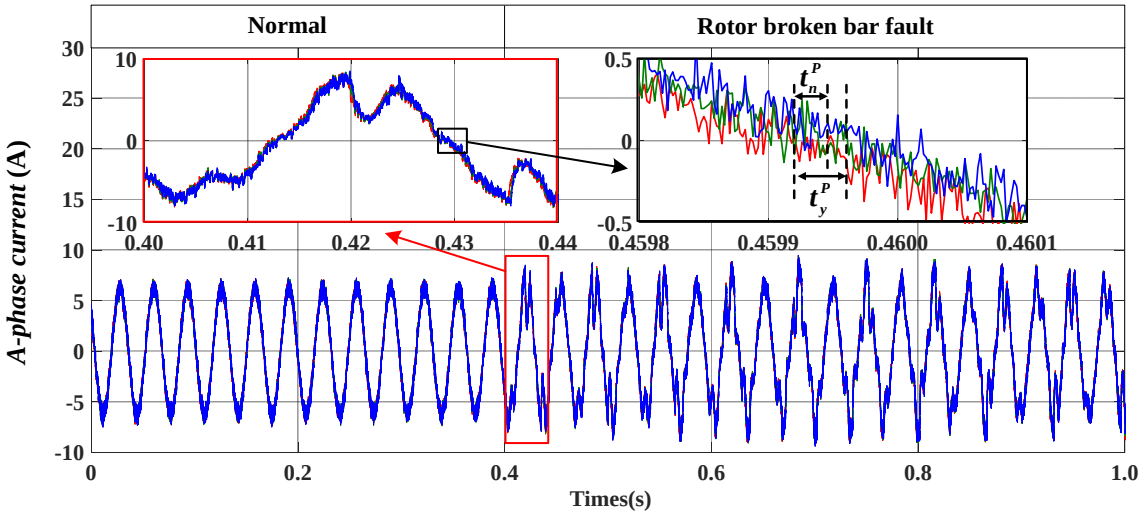


(**b**)Average residual of three-phase currents

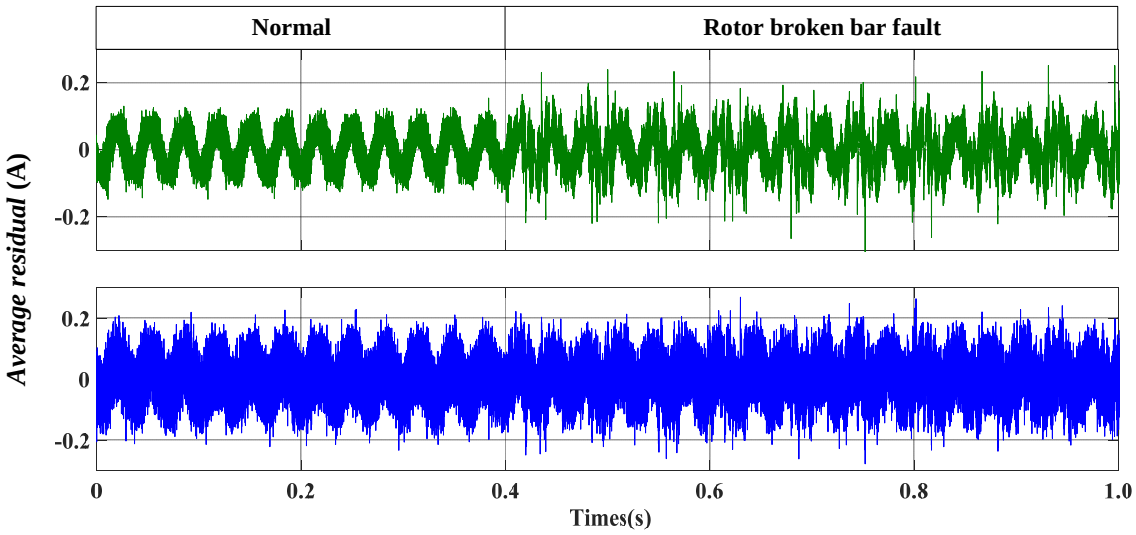


(**c**)Average THD of three-phase currents

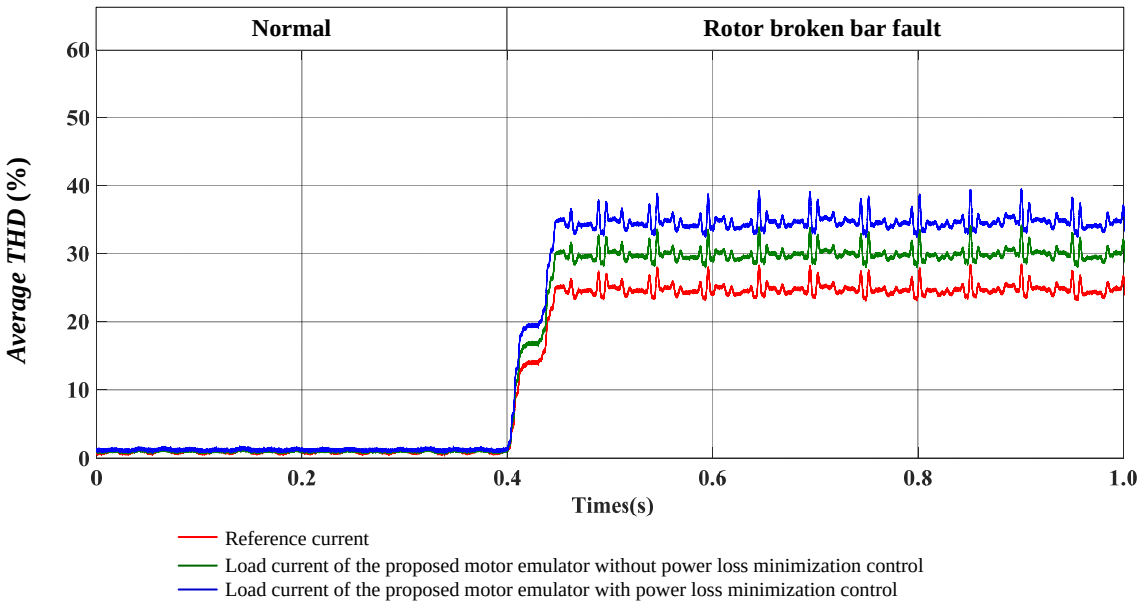
Figure 10. Waveforms of rotor broken bar fault for high power motor.



(**a**)A-phase currents



(**b**)Average residual of three-phase currents



(**c**)Average THD of three-phase currents

Figure 11. Waveforms of rotor broken bar fault for low power motor.

As shown in Figure 11a, when the motor is operating under rotor broken bar fault, comparing to the zero-crossing time of reference current, the zero-crossing time of load current without power loss minimization control is delayed by about 40 us, which is expressed as t_n^P, and the zero-crossing time of load current with power loss minimization control is delayed by about 50 us, which is denoted as t_y^P. From Figure 11b, average three-phase current residual of without and with power loss minimization control are about 0.15 A and 0.18 A, and current tracking accuracy are 97.8% and 97.4%. In Figure 11c, the average THD of three-phase reference current is 25%, and average THD of three-phase load current of without and with power loss minimization control is 30% and 35%, respectively. From Table 9, consideration of power loss, the sum and average switch power loss of the latter have both decreased by 21.47% than the former, respectively. The experimental results have shown that, for the high and low power motor, the proposed power loss decrease method can reduce effectively switch power loss on the premise of ensuring the current tracking effect of the motor emulator when the motor is operating under rotor broken bar fault.

4.4. Motor Speed Suddenly Alteration

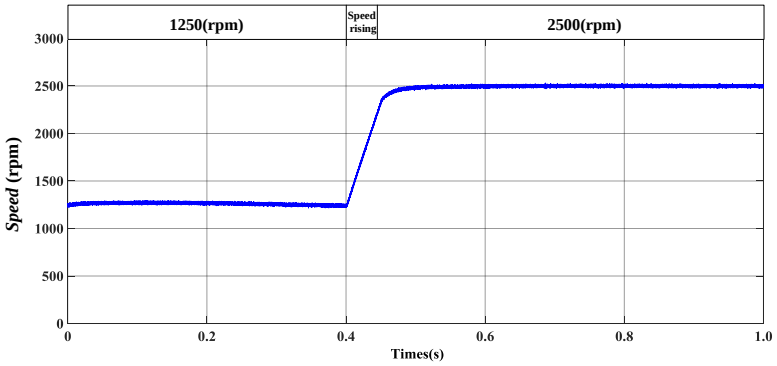
When the motor is operating under speed suddenly alteration with speed set 1250 rpm to 2500 rpm for high power motor and speed set 1000 rpm to 1800 rpm for low power motor respectively, as show in Figures 12a and 13a. The comparison of current tracking performance and switch power loss for proposed motor emulator without and with power loss minimization control are displayed in this section.

For the high power motor, the experimental waveforms of *a*-phase reference current, *a*-phase load current of proposed motor emulator without and with power loss minimization control are shown in Figure 12b. Based on these conditions, the experimental waveforms of average three-phase current residual of between reference current and load current of without and with power loss minimization control are shown in Figure 12c, respectively. The experimental waveforms of average three-phase current THD of reference current, load current of proposed motor emulator without and with power loss minimization control are shown in Figure 12d, respectively. The switch power loss results during the entire simulation period of the proposed motor emulator without and with power loss minimization control are shown in Table 10. Similarly, the experimental waveforms for the low power motor are shown in Figure 13b–d and Table 11.

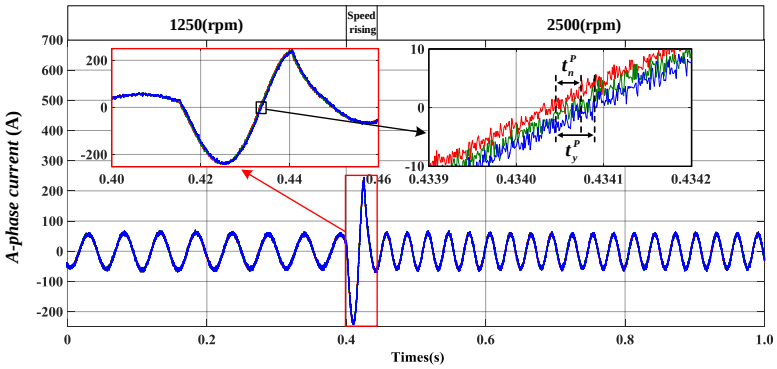
Table 10. Switch power losses of speed suddenly alteration for high power motor.

	Switch Power Loss (KJ)						σ **(%)**
	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
Without	22.76	23.95	23.47	22.36	92.54	23.13	20.83
With	17.72	18.96	18.75	17.83	73.26	18.32	

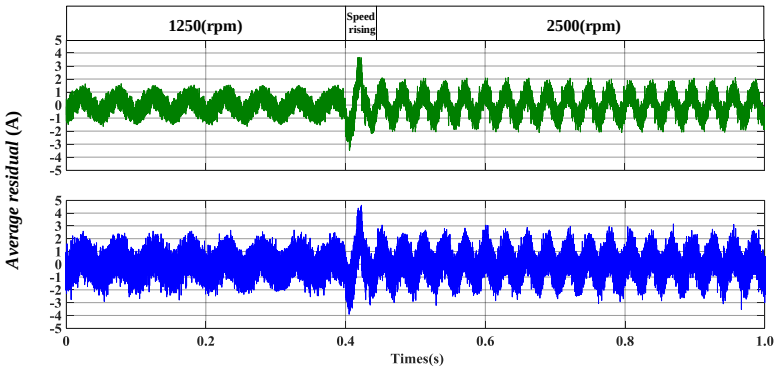
As shown in Figure 12b, when the motor is operating under speed sudden alteration, comparing to the zero-crossing time of reference current, the zero-crossing time of load current without power loss minimization control is delayed by about 40 us, which is expressed as t_n^P, and the zero-crossing time of load current with power loss minimization control is delayed by about 60 us, which is denoted as t_y^P. From Figure 12c, average three-phase current residual of without and with power loss minimization control are about 2.0 A and 2.2 A, and current tracking accuracy are 96.6% and 96.3%. In Figure 12d, the average THD of three-phase reference current is 1.7%, and average THD of three-phase load current of without and with power loss minimization control is 1.9% and 2.0%, respectively. From Table 10, consideration of power loss, the sum and average switch power loss of the latter have both decreased by 20.83% than the former.



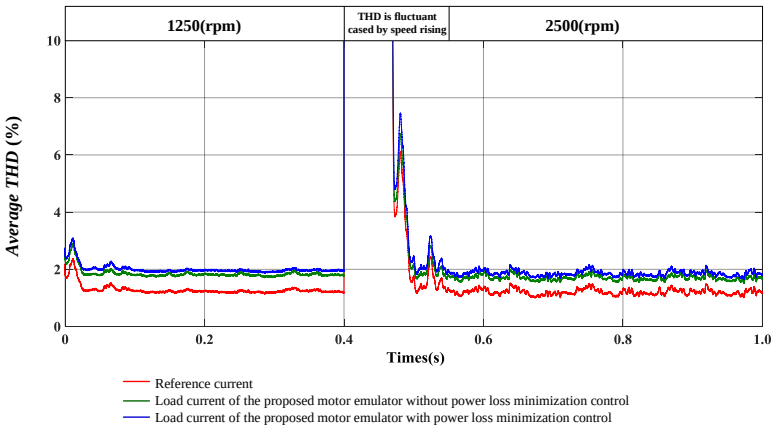
(**a**)Speed



(**b**)A-phase currents

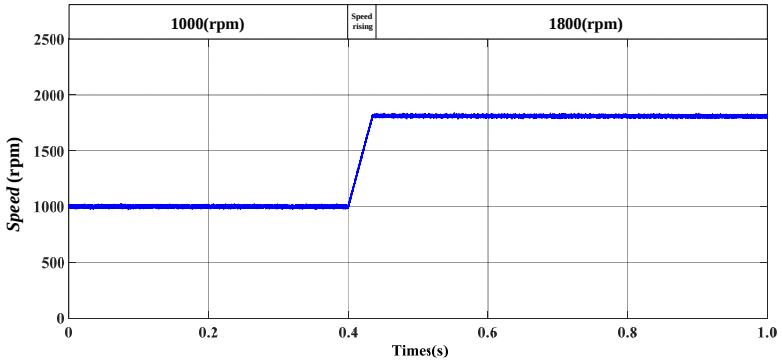


(**c**)Average residual of three-phase currents

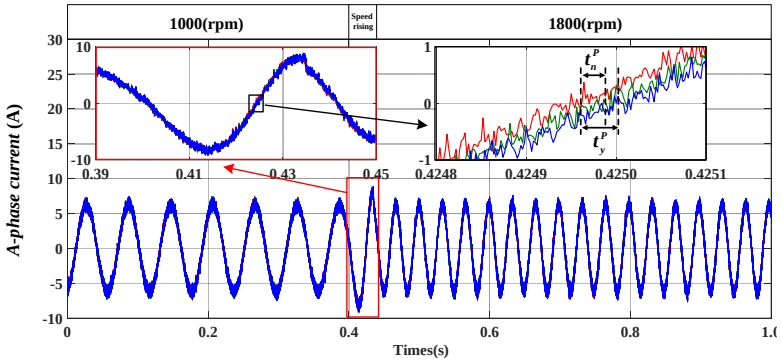


(**d**)Average THD of three-phase currents

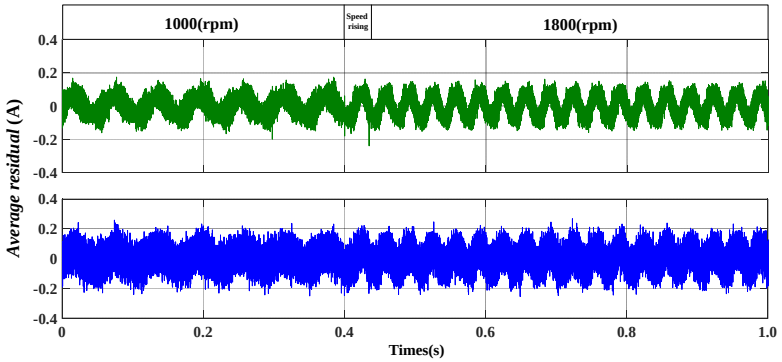
Figure 12. Waveforms of speed suddenly alteration for high power motor.



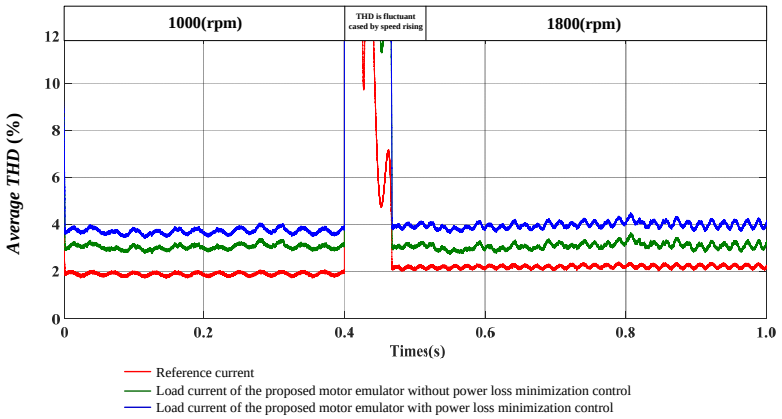
(**a**)Speed



(**b**)A-phase currents



(**c**)Average residual of three-phase currents



(**d**)Average THD of three-phase currents

Figure 13. Waveforms of speed suddenly alteration for low power motor.

Table 11. Switch power losses of speed suddenly alteration for low power motor.

	Switch Power Loss (J)						σ (%)
	p_{b1}	p_{b2}	p_{c1}	p_{c2}	p_{sum}	p_{ave}	
Without	45.64	46.32	45.27	45.70	182.94	45.73	20.88
With	36.31	35.97	35.86	36.58	144.72	36.18	

As shown in Figure 13b, when the motor is operating under speed suddenly alteration, comparing to the zero-crossing time of reference current, the zero-crossing time of load current without power loss minimization control is delayed by about 40 us, which is expressed as t_n^P, and the zero-crossing time of load current with power loss minimization control is delayed by about 60 us, which is denoted as t_y^P. From Figure 13c, average three-phase current residual of without and with power loss minimization control are about 0.16 A and 0.19 A, and current tracking accuracy are 97.7% and 97.3%. In Figure 13d, the average THD of three-phase reference current is 2.0%, and average THD of three-phase load current of without and with power loss minimization control is 3.2% and 4.0%, respectively. From Table 11, consideration of power loss, the sum and average switch power loss of the latter have both decreased by 20.88% than the former, respectively. The experimental results show that, for the high and low power motor, the proposed power loss decrease method can reduce effectively switch power loss on the premise of ensuring the current tracking effect of the motor emulator, when the motor is operating under speed suddenly alteration.

5. Conclusions

A power loss decrease method based on FSMPC with delay compensation for a reduced switch count motor emulator is proposed in this paper. In the proposed motor emulator topology, converter consists of four active switches and two capacitors. Within the power loss decrease method based on FSMPC with delay compensation, an objective function is designed to select the two adjacent switch control signals that generating lowest switch power loss while keeping satisfied current tracking performance. The simulation and experiment results show the feasibility and effectiveness of the proposed method which achieving minimum power loss and ensuring current tracking performance greater than 95%. Besides, they also testify that the current can track stator current accurately and rapidly when the motor operating on the cases, namely in the normal state, or the fault state or the speed suddenly alteration. A real-time platform of a motor emulator for the presented method has been built to provide a reliable environment and offers more authentic data for motor fault injection, diagnosis, and tolerance research.

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References

1. Chen, Z.; Li, X.; Yang, C.; Peng, T.; Yang, C.; Karimi, H.R.; Gui, W. A data-driven ground fault detection and isolation method for main circuit in railway electrical traction system. *ISA Trans.* **2019**, *87*, 264–271. [CrossRef] [PubMed]
2. Yang, X.; Yang, C.; Peng, T.; Chen, Z.; Liu, B.; Gui, W. Hardware-in-the-Loop Fault Injection for Traction Control System. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 696–706. [CrossRef]
3. Chen, Z.; Ding, S.; Peng, T. Fault Detection for Non-Gaussian Processes Using Generalized Canonical Correlation Analysis and Randomized Algorithms. *IEEE Trans. Ind. Electron.* **2018**, *65*, 1559–1567. [CrossRef]
4. Chen, Z.; Yang, C.; Peng, T.; Dan H.; Li, C.; Gui, W. A Cumulative Canonical Correlation Analysis-Based Sensor Precision Degradation Detection Method. *IEEE Trans. Ind. Electron.* **2019**, *66*, 6321–6330. [CrossRef]
5. Glowacz, A. Acoustic-Based Fault Diagnosis of Commutator Motor. *Electronics* **2018**, *7*, 299. [CrossRef]
6. Primavera, S.; Rella, G.; Maddaleno, F. One-cycle controlled three-phase electronic load. *IET Power Electron.* **2012**, *5*, 827–832. [CrossRef]
7. Tsang, K.M.; Chan, W.L. Fast Acting Regenerative DC Electronic Load Based on a SEPIC Converter. *IEEE Trans. Power Electron.* **2012**, *27*, 269–275. [CrossRef]
8. Jack, A.G.; Atkinson, D.J.; Slater, H.J. Real-time emulation for power equipment development. Part 1: Real-time simulation. *IEE Proc.-Electr. Power Appl.* **1998**, *145*, 92–97. [CrossRef]
9. Slater, H.J.; Atkinson, D.J.; Jack, A.G. Real-time emulation for power equipment development. Part 2: The virtual machine. *IEE Proc.-Electr. Power Appl.* **1998**, *145*, 153–158. [CrossRef]
10. Roodsari, B.N.; Nowicki, E.P. Analysis and Experimental Investigation of the Improved Distributed Electronic Load Controller. *IEEE Trans. Energy Convers.* **2018**, *33*, 905–914. [CrossRef]
11. Singh, B; Murthy, S.; Gupta, S. Transient analysis of self-excited induction generator with electronic load controller (ELC) supplying static and dynamic loads *IEEE Trans. Ind. Appl.* **2005**, *41*, 1194–1204. [CrossRef]
12. Wang, J.; Yang, L.; Ma, Y. Static and Dynamic Power System Load Emulation in a Converter-Based Reconfigurable Power Grid Emulator. *IEEE Trans. Power Electron.* **2016**, *31*, 3239–3251. [CrossRef]
13. Geng, Z.; Gu, D.; Hong, T. Programmable Electronic AC Load Based on a Hybrid Multilevel Voltage Source Inverter. *IEEE Trans. Ind. Appl.* **2018**, *54*, 5512–5522. [CrossRef]
14. Heerdt, J.A.; Coutinho, D.F.; Mussa, S.A. Control Strategy for Current Harmonic Programmed AC Active Electronic Power Loads. *IEEE Trans. Ind. Electron.* **2014**, *61*, 3810–3822. [CrossRef]
15. Kesler, M.; Ozdemir, E.; Kisacikoglu, M.C. Power Converter-Based Three-Phase Nonlinear Load Emulator for a Hardware Testbed System. *IEEE Trans. Power Electron.* **2014**, *29*, 5806–5812. [CrossRef]
16. Grubic, S.; Amlang, B.; Schumacher, W. A High-Performance Electronic Hardware-in-the-Loop Drive-Load Simulation Using a Linear Inverter (LinVerter). *IEEE Trans. Ind. Electron.* **2010**, *57*, 1208–1216. [CrossRef]
17. Rao, Y.S.; Chandorkar, M.C. Real-Time Electrical Load Emulator Using Optimal Feedback Control Technique. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1217–1225.
18. Marguc, J.; Truntic, M.; Rodic, M. FPGA Based Real-Time Emulation System for Power Electronics Converters. *Energies* **2019**, *12*, 969. [CrossRef]
19. Moussa, I.; Khedher, A.; Bouallegue, A. Design of a Low-Cost PV Emulator Applied for PVECS. *Electronics* **2019**, *8*, 232. [CrossRef]
20. Sadigh, A.; Dargahi, V.; Corzine, K. Investigation of Conduction and Switching Power Losses in Modified Stacked Multicell Converters. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7780–7791. [CrossRef]
21. Chen, P.; Hu, K.; Lin, Y. Development of a Prime Mover Emulator Using a Permanent-Magnet Synchronous Motor Drive. *IEEE Trans. Power Electron.* **2018**, *33*, 6114–6125. [CrossRef]
22. Kojabadi, H.M.; Chang, L.C.; Boutot, T. Development of a Novel Wind Turbine Simulator for Wind Energy Conversion Systems Using an Inverter-Controlled Induction Motor. *IEEE Trans. Energy Convers.* **2004**, *19*, 547–552. [CrossRef]
23. Peng, T.; Liu, B.; Yang, C.; Qin, R.; Yang, C. Fault current tracking method of motor simulator based on finite set model prediction. *J. Cent. South Univ.* **2019**, *50*, 1098–1104.
24. Naderi, Y.; Hosseini, S.; Zadeh, S.; Mohammadi, B.; Savaghebi, M.; Guerrero, J. An optimized direct control method applied to multilevel inverter for microgrid power quality enhancement. *Int. J. Electr. Power Energy Syst.* **2018**, *170*, 496–506. [CrossRef]

25. Yang, C.; Yang, C.; Peng, T.; Yang X.; Gui, W. A Fault-Injection Strategy for Traction Drive Control System. *IEEE Trans. Ind. Electron.* **2017**, *64*, 5719–5727. [CrossRef]
26. Chen, X.; Wu, W.; Gao, N.; Liu, J.; Henry S.; Frede B. Finite Control Set Model Predictive Control for an LCL-Filtered Grid-Tied Inverter with Full Status Estimations under Unbalanced Grid Voltage. *Energies* **2019**, *12*, 2691. [CrossRef]
27. Hu, S.; Liu, G.; Jin, N.; Guo, L. Constant-Frequency Model Predictive Direct Power Control for Fault-Tolerant Bidirectional Voltage-Source Converter with Balanced Capacitor Voltage. *Energies* **2018**, *11*, 2692.