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FPGA Based Real-Time Emulation System for Power Electronics Converters

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Abstract: This paper deals with an emulation system for Power Electronics Converters (PEC). The emulation of PECs is performed on a Field-Programmable Gate Array (FPGA) capable of hard real-time operation. To obtain such a system, the converter operation is described using a differential equations-based model designed with the graph theory. Differential equation coefficients are changed according to the type of converter and pulse-width modulation (PWM) signals. The tie-set and incidence matrix approach for the converter modelling is performed to describe the converter operation in a general way. Such approach enables that any type of PECs can be described appropriately. The emulator was verified experimentally by synchronous operation with a real DC-AC converter built for this purposes.

Keywords: power electronics; modelling; network theory; emulation; FPGA

1. Introduction

In recent years, demand for utilization of power electronic converters in industrial, commercial and household applications has increased significantly. It is critical for engineers to design these converters very quickly. Considering the time constraints on engineers, it is not surprising that rapid prototyping tools, different Hardware-in-the-Loop (HiL) systems and fault diagnosis techniques have become the key issue in Power Electronics System (PES) applications. For these applications, the modelling techniques process enables faster developing of the PESs. Off-line simulation using different tools is used widely to predict the behaviour of PESs in a time domain. Some ideas of simulation are exploited to some extent for real-time application as estimators and observers in different control processes.

HiL emulation techniques are used extensively in the control of electrical motors and generators designs as reported in [1–5], where the authors used the HiL emulator approach for rapid prototyping issues and studying fault tolerant operation of the observing systems. The research in [1] deals with the design and application of a new ultra-high speed real-time emulation platform for HiL testing and design of high-power PESs. The real-time HiL emulation is performed with a reconfigurable, heterogeneous, multi-core processor architecture that emulates power electronics and includes a circuit compiler that translates graphic system models into processor executable machine code. The authors of [2] developed a synchronous generator emulator by using a three-phase voltage source converter for transmission level power system testing. The research is concentrated to study the different interface algorithms in order to select the ideal voltage type transformer model by considering accuracy and stability. By means of decreasing the emulation error, a closed-loop voltage control is proposed with current feed-forward. The usage of the emulation system for study of the operation of DC-DC converters in a fuel-cell vehicle power-train application is studied in [3]. The bidirectional buck-boost type DC-DC converter is considered as a basic element, which is used as a device under test, and the

rest of the system is emulated. Fault tolerant methods are described in [4,5]. Experimental tools for the development of fault-tolerant machines designed for aerospace motor drives are described in [4], where the authors studied safety critical systems that should be able to overcome hardware or software faults and, therefore, need to be fault tolerant. For safety purposes, the multi-phase machine is chosen to improve the fault-tolerance. The fault tolerant principle for a five-phase permanent-magnet motor operated with an appropriate PEC is described in [5]. The authors improved the motor operation under the open-circuit fault condition and proposed a new, remedial field-oriented control strategy. A review of literature on HiL systems yields several existing methods based on process modelling for the given systems [6–10]. These methods start by process modelling mainly for the high power systems, where it is suitable to study all modes of operation by developed models to avoid costs for real-time experimentation.

The complex power-transmission networks are usually modelled by using graph-theory because of its complexity. To study different operation modes, the incidence matrix approach is recognised as the most useful one. The usage of the network graph theory in this role is reviewed in [11–17]. In [11], the authors demonstrated the consequence of the calculated nodal voltages and branch currents to the eigenvalues and eigenvectors of the Laplacian matrix, which describes the connectivity of the electrical network. The authors of [12] exploited the benefits of systematic analyses by using the complex network theory in order to study the impact of the wind power system to the power grid. The reason why grid-connected wind power should be mitigated is interpreted based on the complex network theory. In the work presented in [13], the authors demonstrated how a simple model of an AC network for three-phase unbalanced power flow with embedded transformers can be obtained, conjugating the use of a complex vector based model in a stationary reference frame and the node incidence matrix based formulation. Zhang [14] proposed a numerical method, which identifies all the single and double edges of the network cut-sets in order to address these vulnerabilities. The described method is based on the factorization of reduced incidence matrix. Reliability Evaluation of the power system also relies on the fault incidence matrix approach. The authors of [15] proposed such an algorithm. Saleh [16] provided a review of the research conducted on complex network analysis in electric power systems. This work presents the finding of the optimal locations for micro-grids in electric distribution systems utilising complex network analysis. In [17], the authors researched the energy flow, material flow and information flow, considering the inherent dynamism and uncertainty of material, energy and information flows, by using the static and dynamic incidence matrices. The modelling approaches for different PECs are described in [18,19], where the authors described the connections of algebraic graph theory, the design and analysis of electric circuits for different network systems.

The emulation of the physical systems is recognised as a modern approach for rapid prototyping of different PESs in order to develop fast and cheap motor drives for different applications. However, all the above described approaches extract the power converter system from the emulators, and the PES is considered as HiL and the rest of the system is emulated due to the cost. The work described here deals with a software/hardware FPGA platform for emulation and verification of PES. The DC-AC converter is chosen to verify the thesis that any PEC can be described by mathematical models, which enables the detailed real-time emulation. The verification system consists of a real DC-AC converter and emulator, which is operating inside the FPGA in real-time, as shown in Figure 1. The paper is organised into five sections. The principle of system operation, method for developing the differential equations for a DC-AC converter model, and features the necessary mathematical background for modelling purposes are described in Section 2. The tie-set and incidence-matrix approach is also introduced for PEC modelling. Section 3 deals with the hardware system necessary in order to solve the developed differential equations by using the FPGA platform. The verification of the method is described in Section 4 as a description and discussion of the obtained experimental results. The main contribution of the paper is the proof of the thesis that it is possible to perform the emulation in real-time, synchronised with the operation of a real DC-AC converter. In general, by using the

incidence matrix approach, any PEC can be described. Finally, the conclusion and contributions of this paper are outlined in Section 5 together with suggestions for future research topics.

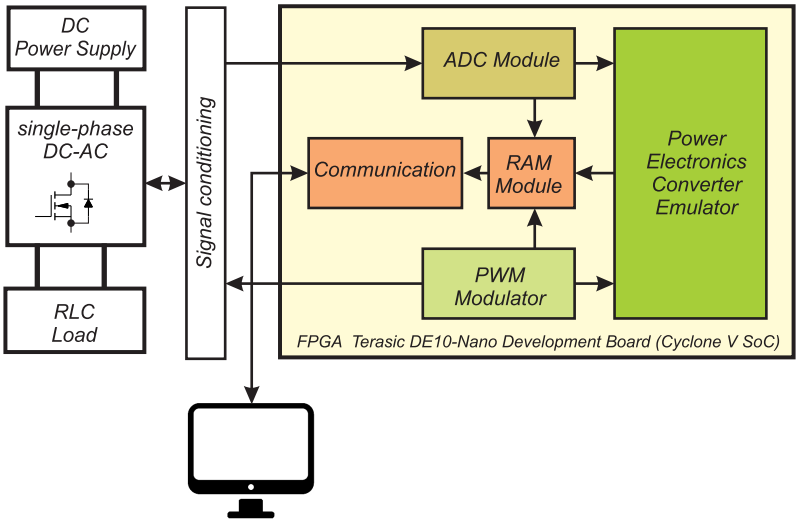
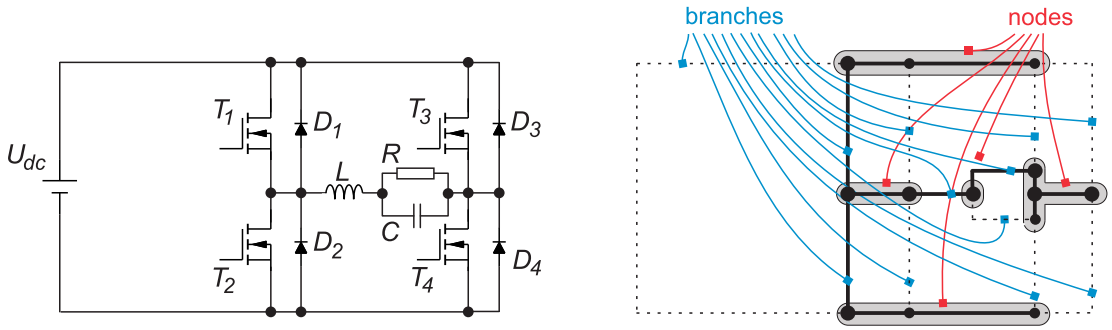


Figure 1. The emulator and real DC-AC system architecture appropriate for testing and verification.

2. Modelling Method Description

To develop the PEC model, the network topology based on Kirchhoff's laws can be used. The network topology analysis is based on graphical representation of the electric circuits. This method is useful for analysing the complex electric circuits by converting them into network graphs. More precisely, the theory of network topology analyses can be found in [20]. The network representing the single-phase DC-AC converter shown in Figure 2a was chosen for describing the modelling method.



(**a**) (**b**)

Figure 2. (**a**) Electrical circuit DC-AC converter; and (**b**) circuit graph.

2.1. Basic Terminology for the Graph Theory

Any electric circuit or network (Figure 2a) can be transformed into a so-called equivalent graph, as shown in Figure 2b. Thus, an equivalent graph is obtained by replacing the passive elements (R, L, C, diodes or transistors) and voltage sources by short circuits, and the current sources by open circuits. A network graph could be connected, unconnected, directed or undirected. A graph is said to be directed (or oriented) when all the nodes and branches are numbered, and direction is assigned to the branches by arrow. The branch represents the line segment, indicated by Arabic numbers, that connects two nodes indicated by Arabic numbers in the circle. In electric circuits, the arrows can indicate the

direction of current flow in each branch. For modelling purposes, the connected and directed graph is considered and the definitions of two sub-graphs, so-called tree and co-tree, need to be explained.

- **Tree** is a connected sub-graph of a given graph, where branches only connect graph nodes. Tree is shown in Figure 2b indicated by bold lines. The branches of a tree are called twigs. A tree consists of only branches that do not form loops. The number of tree branches (b_T) that form a graph tree can be calculated:

$$b_T = n - 1 \tag{1}$$

  where n represents the number of nodes.
- **Co-Tree** is a sub-graph, which is formed with the branches that are removed while forming a tree. It is indicated in Figure 2b by dashed lines. If branches from the co-tree are connected to the tree, loops are formed. Hence, it is called a complement of a tree. For every tree, there will be a corresponding co-tree, and its branches are called links or chords.
- **Incidence matrix** is description of any oriented graph in a compact matrix form. The incident matrix translates the graphical data of a network into algebraic form. For a graph with n nodes and b branches, the complete incidence matrix $\mathbf{A_i}$ is an $n \times b$ matrix with elements defined by:

$$a_{ji} = \begin{cases} 1; & \text{if branch } i \text{ leaves node } j \\ -1; & \text{if branch } i \text{ enters node } j \\ 0; & \text{if branch } i \text{ is not incident with node } j \end{cases}$$

  Using Kirchhoff's Current Law (KCL), the rules can be obtained for an incidence matrix. For the chosen circuit graph shown in Figure 2a, it follows:

$$\begin{aligned} -i_1 - i_2 + i_4 - i_6 + i_{11} &= 0 \\ i_2 - i_3 + i_9 + i_{10} - i_{11} &= 0 \\ i_1 + i_3 - i_5 + i_7 - i_9 &= 0 \\ i_8 - i_{10} + i_{12} &= 0 \\ -i_4 + i_5 + i_6 - i_7 - i_8 - i_{12} &= 0 \end{aligned} \tag{2}$$

  where i_1–i_{12} represent the branch currents, which are depicted in Figure 3a. Equation (2) can be expressed in the matrix form as follows:

$$\begin{array}{l} \text{n\textbackslash b} \rightarrow \\ \downarrow \\ \textcircled{1} \\ \textcircled{2} \\ \textcircled{3} \\ \textcircled{4} \\ \textcircled{5} \end{array} \underbrace{\begin{bmatrix} -1 & -1 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & -1 & 0 \\ 1 & 0 & 1 & 0 & -1 & 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & -1 & 1 & 1 & -1 & -1 & 0 & 0 & 0 & -1 \end{bmatrix}}_{\mathbf{A_i}} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \\ i_9 \\ i_{10} \\ i_{11} \\ i_{12} \end{bmatrix}}_{\mathbf{i_b}} = \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{0}} \tag{3}$$

  where $\mathbf{A_i}$ represents the incidence matrix. If one complete row is removed from an incidence matrix, it results in a reduced incidence matrix, which is appropriate for further calculations.

By choosing the node (5) as a reference node, and according to the graph shown in Figure 3a, the reduced incidence matrix is:

$$\underbrace{\begin{matrix}(1)\\(2)\\(3)\\(4)\end{matrix}\begin{bmatrix} -1 & -1 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & -1 & 0 \\ 1 & 0 & 1 & 0 & -1 & 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 1 \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \\ i_9 \\ i_{10} \\ i_{11} \\ i_{12} \end{bmatrix}}_{\mathbf{i_b}} = \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{0}} \tag{4}$$

and using the matrix notations, it follows:

$$\mathbf{A}\mathbf{i_b} = \mathbf{0} \tag{5}$$

where $\mathbf{A}$ represents the reduced incidence matrix and $\mathbf{i_b}$ is the branch current vector. Equation (5) also gives the maximum possible number of linearly-independent KCL equations for a connected circuit. The numbers of rows (N) in the reduced incidence matrix is:

$$N = n - 1 \tag{6}$$

where n is number of all graph nodes. To calculate the nodes voltages, Kirchhoff's Voltage Law (KVL) can be used to connect branch and nodes voltages as follows:

$$\begin{aligned} v_1 &= -V_1 + V_3 \\ v_2 &= -V_1 + V_2 \\ v_3 &= -V_2 + V_3 \\ v_4 &= V_1 \\ v_5 &= -V_3 \\ v_6 &= -V_1 \\ v_7 &= V_3 \\ v_8 &= V_4 \\ v_9 &= V_2 - V_3 \\ v_{10} &= V_2 - V_4 \\ v_{11} &= V_1 - V_2 \\ v_{12} &= V_4 \end{aligned} \tag{7}$$

which leads to:

$$\underbrace{\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \\ v_9 \\ v_{10} \\ v_{11} \\ v_{12} \end{bmatrix}}_{\mathbf{v_b}} = \underbrace{\begin{bmatrix} -1 & 0 & 1 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & -1 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}}_{\mathbf{A^T}} \underbrace{\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}}_{\mathbf{V_N}} \tag{8}$$

and in the matrix form

$$\mathbf{v_b} = \mathbf{A^T V_N} \tag{9}$$

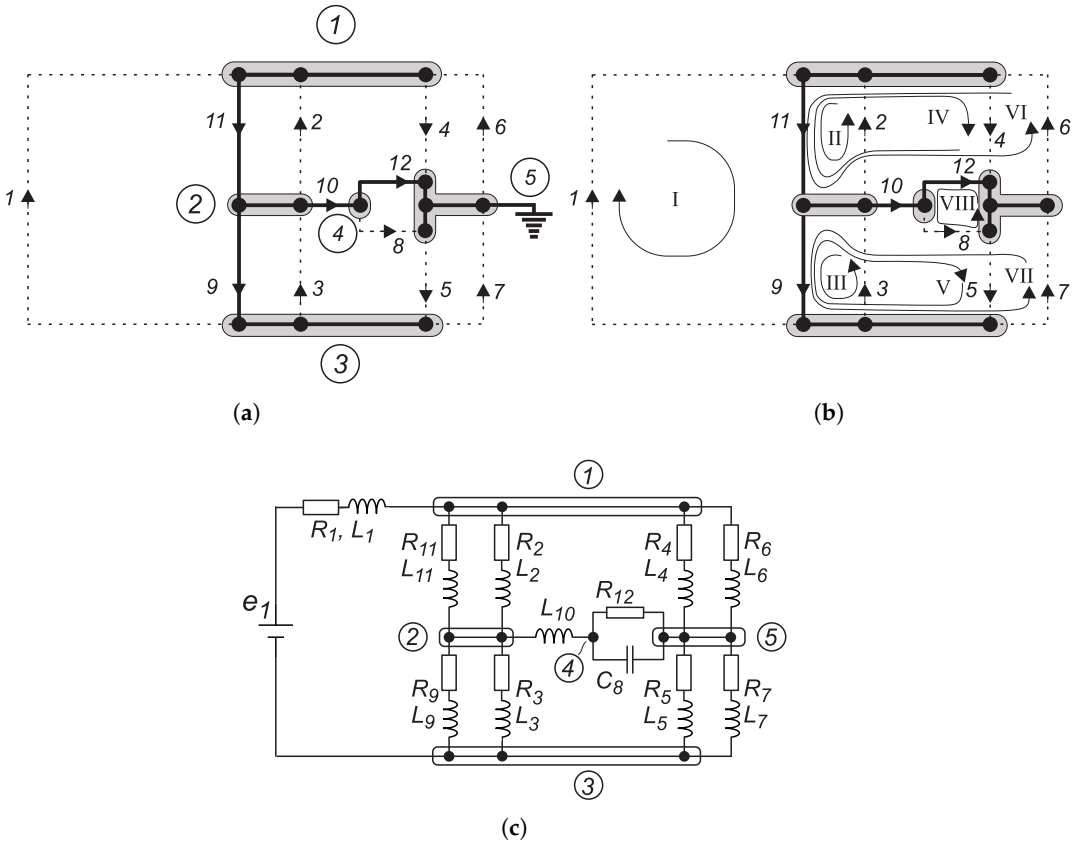


Figure 3. (**a**) Oriented graph; (**b**) Tie-set matrix graph; and (**c**) Circuit elements.

- **Tie-set matrix**

  For a given tree of a graph, the addition of each link between any two nodes forms a loop called the fundamental loop. In a loop, there exists a closed path and a circulating current, which is called the link current. The fundamental loop formed by one link has a unique path in the tree joining the two nodes of the link. This loop is also called a f-loop or a tie-set. The current in any branch of a graph can be found by using link currents. Consider the connected graph

shown in Figure 3a, which has five nodes and twelve branches. In general, the tree branches are chosen arbitrarily, and are indicated by a bold line, as shown in Figure 3a. The twigs of this tree are branches 9–12. The links corresponding to this tree are branches 1–8. Every link defines a fundamental loop of the network. The number of graph links (or f-loops) b_ℓ can be calculated as follows:

$$b_\ell = b - n + 1 \tag{10}$$

Thus, for a given oriented graph (Figure 3), the next set of parameters are defined: the number of nodes ($n = 5$), number of branches ($b = 12$), number of tree branches or twigs ($b_T = n - 1 = 4$), and number of link branches ($b_\ell = b - n + 1 = 8$). KVL can be applied to the f-loops to get a set of linearly independent equations. Consider Figure 3b, where there are eight fundamental loops i_I–i_{VIII} corresponding to the link branches 1–8, respectively. If $v_1, v_2, \ldots v_{12}$ are the branch voltages, the KVL equations for the tree f-loops can be written as:

$$\begin{aligned} v_1 + v_9 + v_{11} &= 0 \\ v_2 + v_{11} &= 0 \\ v_3 + v_9 &= 0 \\ v_4 - v_{10} - v_{11} - v_{12} &= 0 \\ v_5 - v_9 + v_{10} + v_{12} &= 0 \\ v_6 + v_{10} + v_{11} + v_{12} &= 0 \\ v_7 + v_9 - v_{10} + v_{12} &= 0 \\ v_8 - v_{12} &= 0 \end{aligned} \tag{11}$$

and in matrix form, Equation (11) becomes:

$$\begin{array}{l} b_\ell \backslash b \rightarrow \\ \downarrow \\ \\ \text{I} \\ \text{II} \\ \text{III} \\ \text{VI} \\ \text{V} \\ \text{VI} \\ \text{VII} \\ \text{VIII} \end{array} \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & -1 & -1 & -1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & -1 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \end{bmatrix}}_{\mathbf{B}} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \\ v_9 \\ v_{10} \\ v_{11} \\ v_{12} \end{bmatrix}}_{\mathbf{v_b}} = \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{0}} \tag{12}$$

or

$$\mathbf{B}\mathbf{v_b} = \mathbf{0} \tag{13}$$

where **B** is a so-called tie-set matrix or fundamental loop matrix, and $\mathbf{v_b}$ is a column vector of the branch voltages.

- **Tie-set matrix and branch currents**

  Let $i_1, i_2, \ldots, i_{12}$ be the branch currents with directions as shown in Figure 3a. Then, add the links in their proper places to the tree, as shown in Figure 3b. It can be seen that the loops currents are formed by the tree branches 9–12. There is a formation of link currents indicated in Figure 3b by Roman numbers $i_I, i_{II}, \ldots, i_{VII}$. By convention, the f-loops currents are given the same orientation as their defining links currents, i.e., the link current i_I coincides with the branch

current direction i_1, the link current i_{II} coincides with the branch current direction i_2, and so on until the link current i_{VII} coincides with the branch current direction i_7, and, according to tree branches, the branches currents are combinations of f-loops currents. Thus, based on these assumptions, branches currents related with the loops currents can be expressed as:

$$\begin{aligned}
i_1 &= i_I \\
i_2 &= i_{II} \\
i_3 &= i_{III} \\
i_4 &= i_{IV} \\
i_5 &= i_V \\
i_6 &= i_{VI} \\
i_7 &= i_{VII} \\
i_8 &= i_{VIII} \\
i_9 &= i_I + i_{III} - i_V + i_{VII} \\
i_{10} &= -i_{IV} + i_V + i_{VI} - i_{VII} \\
i_{11} &= i_I + i_{II} - i_{IV} + i_{VI} \\
i_{12} &= -i_{IV} + i_V + i_{VI} - i_{VII} - i_{VIII}
\end{aligned} \tag{14}$$

Equation (14) can be written in matrix form as:

$$\underbrace{\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \\ i_9 \\ i_{10} \\ i_{11} \\ i_{12} \end{bmatrix}}_{\mathbf{i_b}} = \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 1 & 1 & -1 & 0 \\ 1 & 1 & 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 1 & -1 & -1 \end{bmatrix}}_{\mathbf{B^T}} \underbrace{\begin{bmatrix} i_I \\ i_{II} \\ i_{III} \\ i_{IV} \\ i_V \\ i_{VI} \\ i_{VII} \\ i_{VIII} \end{bmatrix}}_{\mathbf{i_\ell}} \tag{15}$$

which leads to:

$$\mathbf{i_b} = \mathbf{B^T} \mathbf{i}_\ell \tag{16}$$

2.2. General "Construction" of Circuit Differential Equations

The basic KVL and KCL used by the graph are explained above, which enables two different approaches for power converters modelling. In general, the node voltage or loop current calculation approach can be used.

Loop Current Differential Equations

According to the circuit and its graph, shown in Figure 2a,b, and to apply the above mentioned tie-set matrix developed facts, one branch can be extracted from the circuit. In general, between two arbitrary nodes x and y, there is a branch where the voltage source (e), the resistor (R), inductor (L) and the capacitor (C) can be present, as shown in Figure 4.

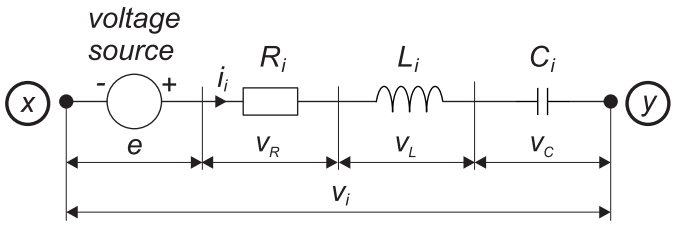


Figure 4. General branch model.

For every branches voltages in the circuit, the KVL gives:

$$v_i = -e_i + R_i i_i + L_i \frac{di_i}{dt} + S_i q_i \tag{17}$$

where e_i is the voltage source present in the branch, i_i is the branch current, q_i is the charge present in the branch, and R_i, L_i and S_i $(S_i = 1/C_i)$ are branch resistance, inductance and elastance respectively (elastance $S = 1/C$). Using the known connection between capacitor charge and currents yields:

$$\frac{dq_i}{dt} = i_i \tag{18}$$

where $i = 1, 2, 3, \cdots b$. Thus, for every graph branch, it is possible to write down its own equation, as follows:

$$\begin{aligned} v_1 &= -e_1 + R_1 i_1 + L_1 \frac{di_1}{dt} + S_1 q_1 \\ v_2 &= -e_2 + R_2 i_2 + L_2 \frac{di_2}{dt} + S_2 q_2 \\ &\vdots \\ v_b &= -e_b + R_b i_b + L_b \frac{di_b}{dt} + S_b q_b \end{aligned} \tag{19}$$

Equation (19) can be expressed in a matrix form as follows:

$$\begin{aligned} \mathbf{v_b} &= -\mathbf{e_b} + \mathbf{R_b i_b} + \mathbf{L_b} \frac{d\mathbf{i_b}}{dt} + \mathbf{S_b q_b} \\ \frac{d\mathbf{q_b}}{dt} &= \mathbf{i_b} \end{aligned} \tag{20}$$

where

$$\mathbf{v_b} = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_b \end{bmatrix}, \ \mathbf{e_b} = \begin{bmatrix} e_1 \\ e_2 \\ \vdots \\ e_b \end{bmatrix}, \ \mathbf{i_b} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_b \end{bmatrix}, \quad \mathbf{q_b} = \begin{bmatrix} q_1 \\ q_2 \\ \vdots \\ q_b \end{bmatrix}, \tag{21}$$

$$\mathbf{R_b} = \begin{bmatrix} R_1 & 0 & \cdots & 0 \\ 0 & R_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & R_b \end{bmatrix}, \ \mathbf{L_b} = \begin{bmatrix} L_1 & 0 & \cdots & 0 \\ 0 & L_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & L_b \end{bmatrix}, \ \mathbf{S_n} = \begin{bmatrix} S_1 & 0 & \cdots & 0 \\ 0 & S_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & S_b \end{bmatrix} \tag{22}$$

where $\mathbf{v_b}$ represents the voltage vector with the elements $v_1, v_2, ..., v_b$; $\mathbf{e_b}$ represents the voltage sources vector with the components $e_1, e_2, ..., e_b$; $\mathbf{i_b}$ represents the current branch vector with the elements $i_1, i_2, ...i_b$; $\mathbf{q_b}$ represents the branch charges vector (i.e., capacitor voltages vector) with the components

$q_1, q_2, ..., q_b$; $\mathbf{R_b}$ represents the resistance branch matrix with the elements $R_1, R_2, ..., R_b$; $\mathbf{L_b}$ represents the inductance branch matrix with the components $L_1, L_2, ..., L_b$; and $\mathbf{S_b}$ represents the elastance branch matrix with the elements $S_1, S_2, ...S_b$. The system in Equation (20) represents the voltage drop on every circuit branch. With the KVL applied, which means that every equation member must be multiplied on the left side by tie-set matrix $\mathbf{B}$, Equation (20) is modified as follows:

$$\begin{array}{l} \mathbf{B v_b} = -\mathbf{B e_b} + \mathbf{B R_b i_b} + \mathbf{B L_b} \frac{d\mathbf{i_b}}{dt} + \mathbf{B S_b q_b} \\ \frac{d\mathbf{q_b}}{dt} = \mathbf{i_b} \end{array} \tag{23}$$

According to Equation (13) term $\mathbf{B v_b} = \mathbf{0}$, substituting Equation (16) into Equation (23), and considering that $\mathbf{q_b} = \mathbf{B^T q}_\ell$, yields:

$$\begin{array}{l} 0 = -\mathbf{e}_\ell + \mathbf{B R_b B^T i}_\ell + \mathbf{B L_b B^T} \frac{d\mathbf{i}_\ell}{dt} + \mathbf{B S_b B^T q}_\ell \\ \frac{d\mathbf{q}_\ell}{dt} = \mathbf{i}_\ell \end{array} \tag{24}$$

where $\mathbf{e}_\ell$ ($\mathbf{e}_\ell = \mathbf{B e_b}$) represents the transformation of branch voltage sources into the loops. After rearranging Equation (24), it follows:

$$\begin{array}{l} \frac{d\mathbf{i}_\ell}{dt} = \mathbf{L}_\ell^{-1} \left(\mathbf{e}_\ell - \mathbf{R}_\ell \mathbf{i}_\ell - \mathbf{S}_\ell \mathbf{q}_\ell \right) \\ \frac{d\mathbf{q}_\ell}{dt} = \mathbf{i}_\ell \end{array} \tag{25}$$

where $\mathbf{R}_\ell = \mathbf{B R_b B^T}$, $\mathbf{S}_\ell = \mathbf{B S_b B^T}$ and $\mathbf{L}_\ell = \mathbf{B L_b B^T}$.

The matrices $\mathbf{R}_\ell$, $\mathbf{S}_\ell$ and $\mathbf{L}_\ell$ are called the loops matrices, and have the dimension $\ell \times \ell$.

$$\mathbf{R}_\ell = \begin{bmatrix} b_{11} & b_{12} & \cdots & \cdots & \cdots & b_{1b} \\ b_{21} & b_{22} & \cdots & \cdots & \cdots & b_{2b} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ b_{\ell 1} & b_{\ell 2} & \cdots & b_{\ell\ell} & \cdots & b_{\ell b} \end{bmatrix} \begin{bmatrix} R_1 & 0 & \cdots & \cdots & 0 \\ 0 & R_2 & 0 & \cdots & 0 \\ 0 & 0 & \ddots & \cdots & 0 \\ 0 & \vdots & \vdots & \ddots & 0 \\ 0 & 0 & 0 & 0 & R_b \end{bmatrix} \begin{bmatrix} b_{11} & b_{21} & \cdots & b_{\ell 1} \\ b_{12} & b_{22} & \cdots & b_{\ell 2} \\ \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & \vdots & b_{\ell\ell} \\ \vdots & \vdots & \vdots & \vdots \\ b_{1b} & b_{2b} & \vdots & b_{\ell b} \end{bmatrix} \tag{26}$$

$$\mathbf{L}_\ell = \begin{bmatrix} b_{11} & b_{12} & \cdots & \cdots & \cdots & b_{1b} \\ b_{21} & b_{22} & \cdots & \cdots & \cdots & b_{2b} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ b_{\ell 1} & b_{\ell 2} & \cdots & b_{\ell\ell} & \cdots & b_{\ell b} \end{bmatrix} \begin{bmatrix} L_1 & 0 & \cdots & \cdots & 0 \\ 0 & L_2 & 0 & \cdots & 0 \\ 0 & 0 & \ddots & \cdots & 0 \\ 0 & \vdots & \vdots & \ddots & 0 \\ 0 & 0 & 0 & 0 & L_b \end{bmatrix} \begin{bmatrix} b_{11} & b_{21} & \cdots & b_{\ell 1} \\ b_{12} & b_{22} & \cdots & b_{\ell 2} \\ \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & \vdots & b_{\ell\ell} \\ \vdots & \vdots & \vdots & \vdots \\ b_{1b} & b_{2b} & \vdots & b_{\ell b} \end{bmatrix} \tag{27}$$

$$\mathbf{S}_\ell = \begin{bmatrix} b_{11} & b_{12} & \cdots & \cdots & \cdots & b_{1b} \\ b_{21} & b_{22} & \cdots & \cdots & \cdots & b_{2b} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ b_{\ell 1} & b_{\ell 2} & \cdots & b_{\ell\ell} & \cdots & b_{\ell b} \end{bmatrix} \begin{bmatrix} S_1 & 0 & \cdots & \cdots & 0 \\ 0 & S_2 & 0 & \cdots & 0 \\ 0 & 0 & \ddots & \cdots & 0 \\ 0 & \vdots & \vdots & \ddots & 0 \\ 0 & 0 & 0 & 0 & S_b \end{bmatrix} \begin{bmatrix} b_{11} & b_{21} & \cdots & b_{\ell 1} \\ b_{12} & b_{22} & \cdots & b_{\ell 2} \\ \vdots & \vdots & \ddots & \vdots \\ \vdots & \vdots & \vdots & b_{\ell\ell} \\ \vdots & \vdots & \vdots & \vdots \\ b_{1b} & b_{2b} & \vdots & b_{\ell b} \end{bmatrix} \tag{28}$$

The obtained system in Equation (25) describes the circuit by using the state variables, i.e., the inductor currents and capacitor voltages, and enables the modelling of the converter circuit.

2.3. Consideration of Circuit Loops Matrices

For converter emulation purposes, it is necessary to define the branches where the semiconductors switches and diodes are present. According to the DC-AC converter scheme (Figure 2a) and established graph (Figure 3a), the transistors are present in branches 4, 5, 9 and 11, and diodes in branches 2, 3, 6 and 7. For MOSFETs and diodes, the ON resistance and inductance are chosen to be $R_{on} = 20$ mΩ, $L_{on} = 20$ nH, and for OFF state $R_{off} = 100$ kΩ, $L_{off} = 100$ mH respectively. In this example, MOSFETs are used but there are also possibilities of other semiconductor switches (IGBT, GaN, SiC, etc.), where the correct equivalent resistances, inductances and applicable PWM technique should be used.

2.3.1. Control of Branches Containing Transistors

The emulation of switching the transistor is performed by changing the modelled equivalent resistance and inductance in the branches with semiconductors according to the used modulation signal and voltage polarity. Thus, by defining the branches with transistors, and by including the triggering pulses in order to select correct equivalent resistances R_i (R_{on} or R_{off}) and inductances L_i (L_{on} or L_{off}) in appropriate branches of Equations (26) and (27), respectively, the obtained loops matrices can be used for converter emulation. To control the emulation variables, it is necessary for the circuit loops matrices to be connected with pulse width modulation (PWM) signals [21].

Based on the chosen graph (Figure 3) and using Table 1, the appropriate R_{on}, L_{on} and R_{off}, L_{off} values should be used in the branches containing the transistors. To produce the three-level voltage on the converter output, the necessary gate signals are shown in Figure 5. When gate signals Q_{T1}–Q_{T4} are equal to logic value 1, the matrices $\mathbf{R_b}$ and $\mathbf{L_b}$ contain R_{on} and L_{on} in appropriate branches, and, when these are equal to logic value 0, the matrices contain R_{off} and L_{off} in appropriate branches.

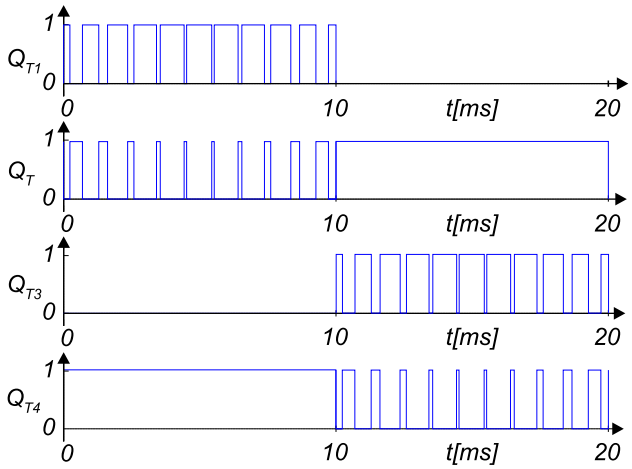


Figure 5. Gate signals: Q_{T1}–Q_{T4}.

Table 1. Matrix elements for transistors controlled by PWM.

Gate Signals	T_1	T_2	T_3	T_4
$Q_{Ti} = 1$ $i = 1,2,3,4$	$R_{11} = R_{on}$ $L_{11} = L_{on}$	$R_9 = R_{on}$ $L_9 = L_{on}$	$R_4 = R_{on}$ $L_4 = L_{on}$	$R_5 = R_{on}$ $L_5 = L_{on}$
$Q_{Ti} = 0$ $i = 1,2,3,4$	$R_{11} = R_{off}$ $L_{11} = L_{off}$	$R_9 = R_{off}$ $L_9 = L_{off}$	$R_4 = R_{off}$ $L_4 = L_{off}$	$R_5 = R_{off}$ $L_5 = L_{off}$

2.3.2. Control of Branches Containing Diodes

The emulation of switching the diodes is performed by changing the resistance and inductance in the branches with diodes according to the voltage polarity. To make the diode forward or reverse biased, the branch voltages where diodes are present can be evaluated by Equations (7) and (19) with the help of Equation (25). During the integration process (solving the differential equation system), it is necessary to calculate the exact voltage transient through zero, which is almost impossible. For simulation purposes, it is possible by introducing the iteration approach and changing the simulation step in order to obtain exactly the diode voltage transient-zero point [22], but for emulation purposes such approach is not appropriate. On the other hand, the exact time when diodes must be active is known by generated gate signals Q_{T1}–Q_{T4} for transistors T_1–T_4. To obtain the three-level output voltage between the nodes (2) and (5), the dead-time intervals between transistors in the converter leg must be generated (first leg transistors T_1 and T_2 and second leg T_3 and T_4). During these intervals, the diodes must be activated, as shown in Figure 6a,b, respectively. The appropriate time sequences when diodes are active are shown in Figure 7a,b. Based on this, the decision table (Table 2) can be established, and the boolean logic function can be developed by using Karnaugh Maps minimization as follows:

$$\begin{array}{rcl} Q_{D2} & = & \overline{Q}_{T1} \,\&\, \overline{Q}_{T2} \\ Q_{D4} & = & \overline{Q}_{T3} \,\&\, \overline{Q}_{T1} \end{array} \tag{29}$$

where Q_{D2} and Q_{D4} represent the logic signals with values 1 or 0. They are controlling branches 3 and 7, where the diodes are present, by putting in the branches the values R_{on}, L_{on} or R_{off}, L_{off}. Thus, the diode states ON or OFF are controlled indirectly by the PWM generator, which is summarised in Table 3. Diodes D_1 and D_3 are not active in any of the possible states of the converter by applied modulation, which can be seen in Figure 6. That is why branches 2 and 6 always have the values R_{off} and L_{off}, respectively.

Some combinations of the gate signals should never appear (Table 2), and can be used for FPGA logic cells configuration error identification (for safety reasons). Thus, if any of these combinations appear, it can be decoded as an error, which is indicated in the last column of Table 2. Boolean logic function for modulation error is also developed by Karnaugh Maps as follows:

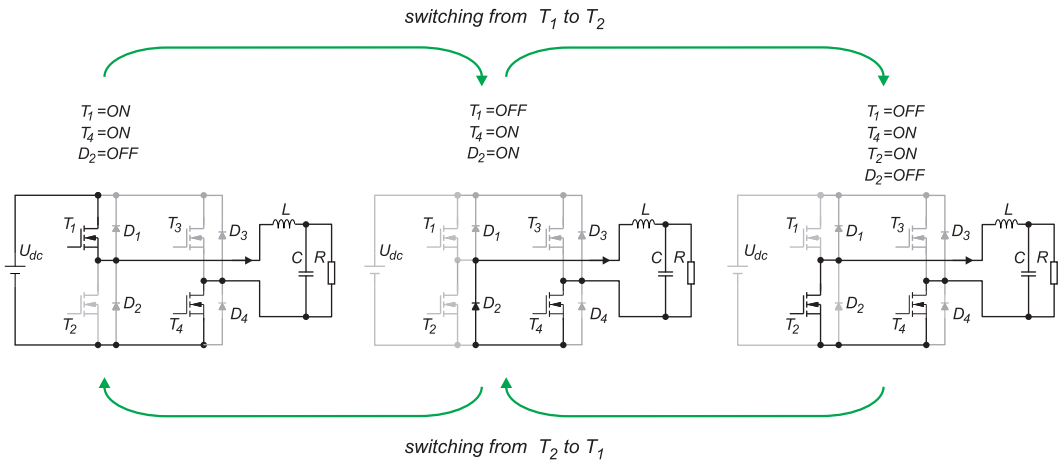
$$Error = (Q_{T1} \,\&\, Q_{T2}) \,\mathrm{OR}\, (Q_{T3} \,\&\, Q_{T4}) \,\mathrm{OR}\, \left(\overline{Q}_{T2} \,\&\, Q_{T3}\right) \mathrm{OR}\, \left(Q_{T1} \,\&\, \overline{Q}_{T4}\right) \tag{30}$$

To evaluate the voltages appearing on the transistors placed in the branches 4, 5, 9 and 11 and the voltages appearing on the diodes in the branches 2, 3, 6 and 7, the following procedure should be carried out. Loops currents can be calculated using Equation (25) and then converted to branches currents by Equation (16). Finally, using Equation (19), the voltages on every branch (v_1 to v_{12}) can be evaluated. Using some expressions coming from Equation (7), the nodes voltages can be calculated as follows:

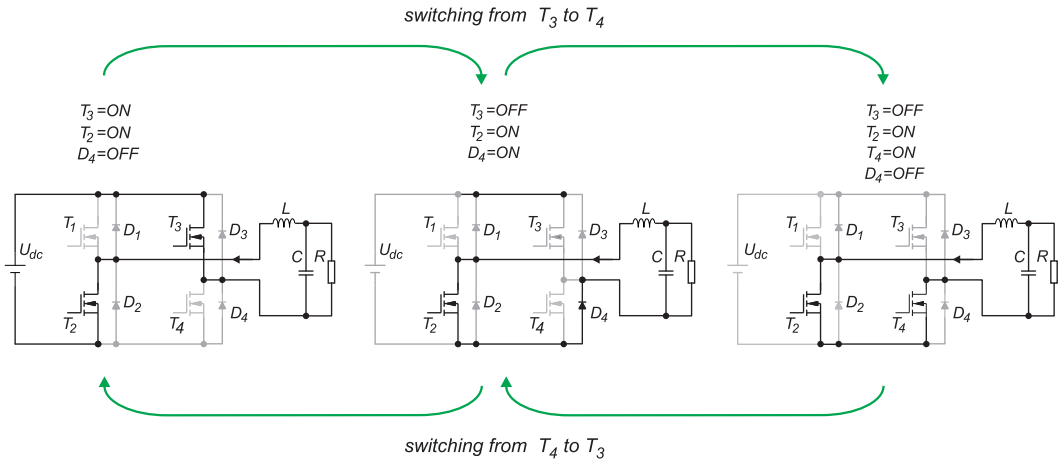
$$\begin{array}{l} V_1 = v_4 = -v_6 \\ V_2 = v_{10} + v_{12} \\ V_3 = v_7 = -v_5 \\ V_4 = v_{12} = v_8 \\ V_5 = 0 \end{array} \tag{31}$$

Table 2. PWM generator error detection.

#	Q_{T1}	Q_{T2}	Q_{T3}	Q_{T4}	Q_{D2}	Q_{D4}	Error
0	0	0	0	0	x	x	0
1	0	0	0	1	1	x	0
2	0	0	1	0	x	x	1
3	0	0	1	1	x	x	1
4	0	1	0	0	x	1	0
5	0	1	0	1	0	0	0
6	0	1	1	0	x	0	0
7	0	1	1	1	x	x	1
8	1	0	0	0	x	x	1
9	1	0	0	1	0	x	0
10	1	0	1	0	x	x	1
11	1	0	1	1	x	x	1
12	1	1	0	0	x	x	1
13	1	1	0	1	x	x	1
14	1	1	1	0	x	x	1
15	1	1	1	1	x	x	1



(**a**)



(**b**)

Figure 6. (**a**) Switch sequences when first leg transistors of DC-AC are switching from T_1 to T_2; and (**b**) switch sequences when second leg transistors of DC-AC are switching from T_3 to T_4.

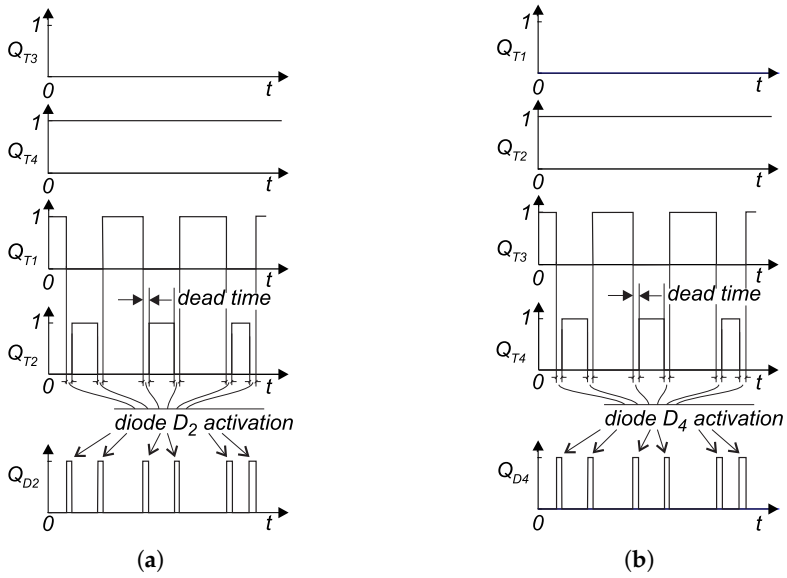


Figure 7. Gate signals when: (**a**) positive half-period output voltage is required; and (**b**) negative half-period output voltage is required.

Table 3. Matrix elements for diodes controlled by gate signals Q_{D2} and Q_{D4}.

Gate Signals	D_2	D_4
$Q_{Di} = 1$ $i = 2, 4$	$R_3 = R_{on}$ $L_3 = L_{on}$	$R_7 = R_{on}$ $L_7 = L_{on}$
$Q_{Di} = 0$ $i = 2, 4$	$R_3 = R_{off}$ $L_3 = L_{off}$	$R_7 = R_{off}$ $L_7 = L_{off}$

By evaluating all nodes voltages as follows from Equation (31), the voltage drops can also be calculated on every element in the DC-AC converter. To verify the proposed modelling method for emulator purposes, the experimental test-bench system was built. It consists of three main units: A 500 W single-phase DC-AC converter, a Terasic DE10-Nano Cyclone V evaluation board (FPGA), and off-line data preparation (calculation), as can be seen in Figure 8. The performed tasks and necessary signals and data flow are evident from the block scheme shown in Figure 9.

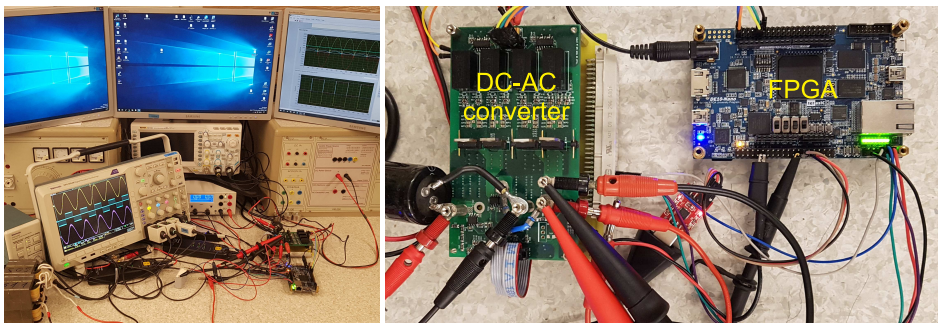


Figure 8. Experimental test-bench system.

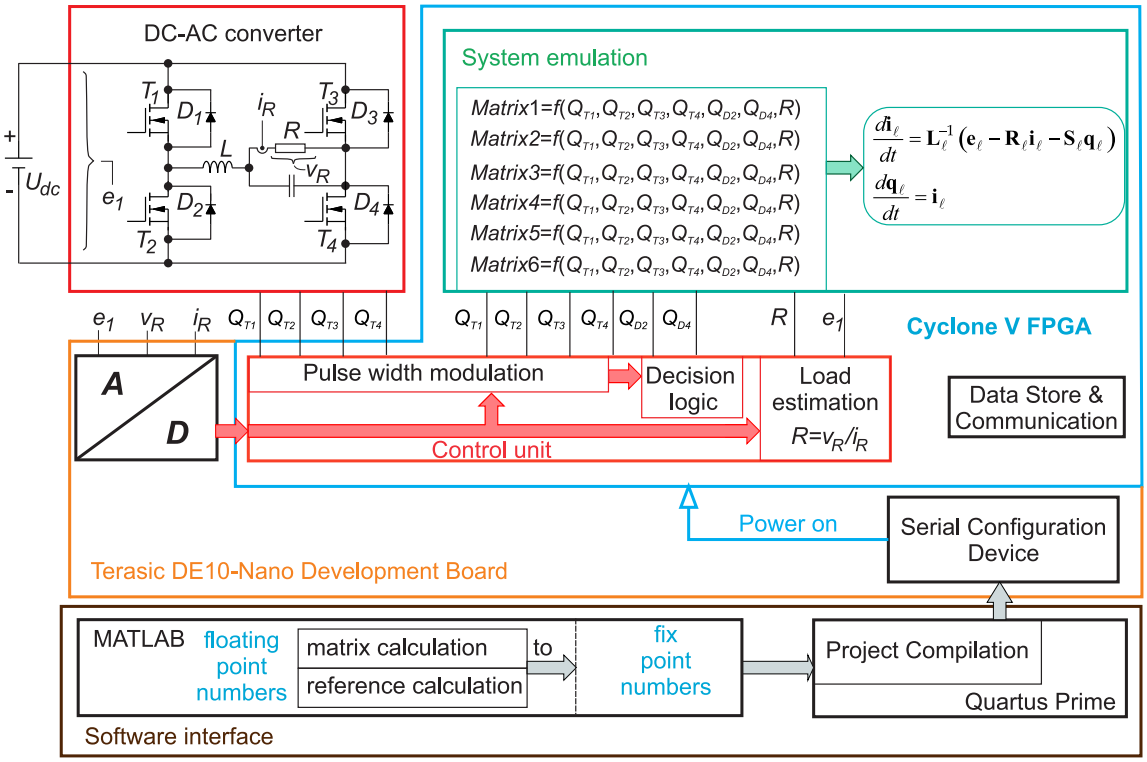


Figure 9. Block scheme, signal-flows, branch elements.

2.4. Off-Line Data Calculation

For faster execution of the FPGA programme, two LUTs (Look Up Tables) were built off-line with a similar method as that presented in [23,24]. Difference to the compared method is in generation process of the possible scenarios, which here are derived from feasible converter power switches combinations, and different data calculation. Firstly, reference voltage signal calculation was performed, and, as result, reference LUT with modulation signal for PWM was designed by Equation (32):

$$m_i(t) = \frac{\hat{U}}{U_{dc}} \sin(\omega_0 t) = m_I \sin(\omega_0 t) \tag{32}$$

and discretized to a 16-bit fix-point vector with 500 points. Thus, for every PWM period ($T_s = 40$ µs), there is different modulation signal value, defined as follows:

$$m_i(nT_s) = \frac{\hat{U}}{U_{dc}} \sin(\omega_0 nT_s) = m_I \sin(\omega_0 nT_s);\ n = 1:500 \tag{33}$$

where $\hat{U}$ is the peak value of output sine voltage, U_{dc} is the constant power source (DC) voltage, and $\omega_0 = 2\pi 50$ rad/s. Further explanation of PWM follows in the next subsection. Secondly, LUT was designed for loops matrices. As shown in Table 2 and Figure 6, there are six possible states of converter, which means there are six different loops matrices calculated from Equations (26)–(28) by considering Tables 1 and 3. The inverse of each loops inductance matrices $\mathbf{L_1}, \mathbf{L_2}, ..., \mathbf{L_6}$ is calculated before conversion to a fix-point. Loops matrices LUT, shown as Matrix1–Matrix6 in Figure 9, were designed after conversion to fix-point. When all data were prepared in fix-point format, two separate Verilog modules were written automatically in Matlab. These modules can be imported in a Quartus Prime FPGA Design Software project, where main FPGA compilation and programming was performed.

3. Setup for Algorithm Verification

3.1. FPGA Unit

A PWM generator module programmed on FPGA uses an up–down counter with 2000 steps counting at $f = 100$ MHz, which yields PWM switching frequency $f_s = 25$ kHz. The counter is forming a triangle carrier signal. Gate signal Q_{T1} is formed by comparing the modulation signal to the triangle carrier signal as follows:

$$Q_{T1} = \begin{cases} 1; \ counter \leq m_i \ and \ m_i > 0 \\ 0; \ counter > m_i \ \ or \ \ m_i \leq 0 \end{cases}$$

Gate signal Q_{T3} is formed by comparing the modulation signal to the triangle carrier signal as follows:

$$Q_{T3} = \begin{cases} 1; \ counter \leq |m_i| \ \ and \ m_i < 0 \\ 0; \ counter > |m_i| \ \ \ or \ \ m_i \geq 0 \end{cases}$$

Gate signals Q_{T2} and Q_{T4} are negations of their complementary pairs as follows: $Q_{T2} = \overline{Q}_{T1}$ and $Q_{T4} = \overline{Q}_{T3}$. Each gate signal also has on-delay for 300 ns as a dead time generator. Diodes switching signals Q_{D2} and Q_{D4} are formed as defined in Equation (29).

An Analog to Digital Converter (ADC) was used to measure DC-link voltage, load current and load voltage. ADC measurements are triggered when the PWM generator counter is at value 0. The measurement of these three signals and serial communication to FPGA were taking 6 µs, hence maximum sampling rate was 166 ksps. Due to synchronised measurement to centre of PWM pulse, update of measured values was taking place every 40 µs. Measured values are used for load estimation (for updating load resistance in loops matrices LUT), emulator input (gate signals Q_x for correct loops matrices LUT values selection and adapting $\mathbf{e}_\ell$ vector of emulator to actual DC-link voltage), or further regulation and fault detection purposes that will be implemented.

The system emulation module was designed as a Euler differential equation solver, as follows from Equation (25):

$$\begin{aligned} \mathbf{i}_{\ell(k+1)} &= \mathbf{i}_{\ell(k)} + h\, \mathbf{L}^{-1}_{\ell(k)} \left(\mathbf{e}_{\ell(k)} - \mathbf{R}_{\ell(k)} \mathbf{i}_\ell(k) - \mathbf{S}_{\ell(k)} \mathbf{q}_{\ell(k)} \right) \\ \mathbf{q}_{\ell(k+1)} &= \mathbf{q}_{\ell(k)} + h\, \mathbf{i}_{\ell(k)} \end{aligned} \tag{34}$$

where $h = 1 \times 10^{-7}$ s is an integration step. This module state diagram can be seen in Figure 10. Values in loops matrices are being updated from corresponding LUTs at every gate signal or load change. Because a great number of parallel and serial calculations have to be done, clocked pipelining was used for the complete emulation system module. The right side of Equation (34) is calculated every FPGA clock cycle (f = 100 MHz) with the loops matrices values that are provided considering input control signals. Then, loop currents and loop charges are converted to branches currents and branches charges using Equation (16). Results are then used in Equation (19), by which branches voltages are obtained. Nodes voltages are calculated with usage of Equation (31).

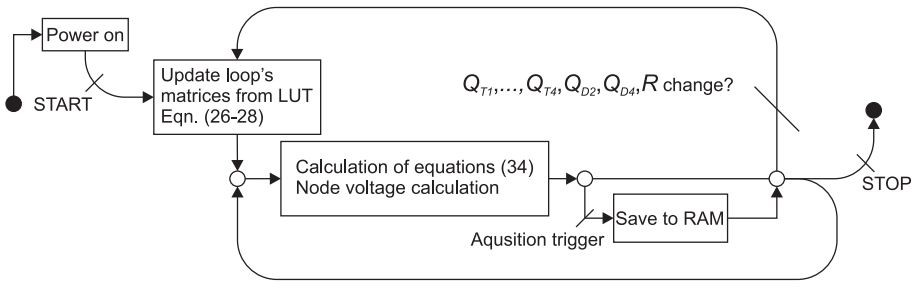


Figure 10. System emulator state diagram.

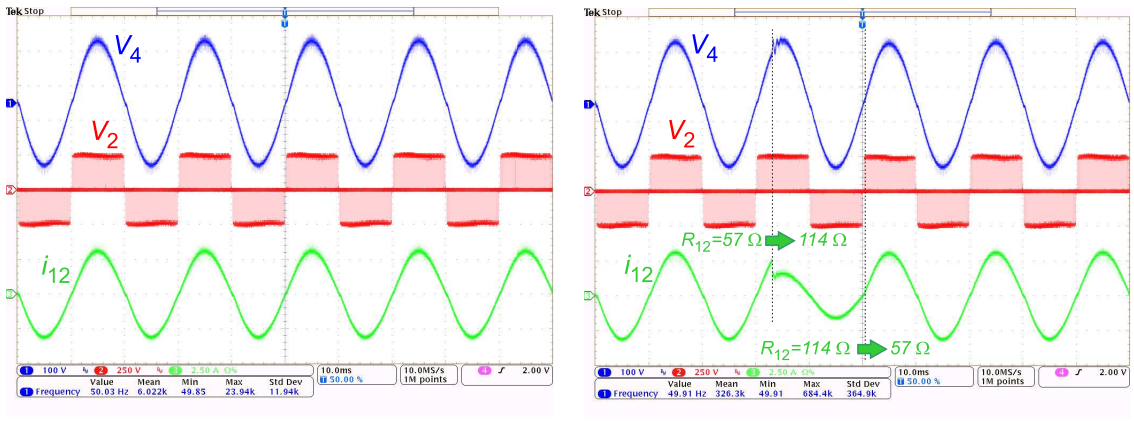
A data store module was used for very high speed sampling of calculated data by the System emulation module and sending them to the host PC for verification purposes. Acquisition timing and synchronization was done via the FPGA clock post-scaler, which is scalable from a user interface on the Host PC, and triggers for positioning of data store start. Acquisition length is also settable from user interface within the limits of the RAM size synthesised on the FPGA.

3.2. Single-Phase DC-AC Converter

A single phase H-bridge structure, also known as a full-bridge structure, represents one of the fundamental converter topologies in power electronics. It can support bidirectional power flow between an alternating and a constant power source. In terms of power conversion capabilities, it provides a voltage step down feature for transferring power from a constant power source (DC) to an alternating power source (AC), and a voltage step up feature for transferring power in the opposite direction (rectifier or boost operating mode). A single-phase DC-AC converter operating in step-down mode was used for verification of the emulation system. The MOSFET single-phase DC-AC converter was equipped with drivers and appropriate measurement circuits.

4. Results and Discussion

For verification of the described modelling based on the system in Equation (25), the experimental test-bench system was built, as shown in Figures 8 and 9. Based on the block scheme shown in Figure 1, the real DC-AC converter and Emulation block were built for experimental purposes. The frequency of 25 kHz (end application of household UPS—above audible range) for the PWM triangle carrier was chosen for both the Emulator and real DC-AC converter. Power supply source of $U_{dc} = 250$ V and the reference voltage (desired output) of $u_{ref} = 0.75 \cdot U_{dc} \cdot \sin(2\pi 50 \cdot t)$ V were chosen. The algorithm was tested under two cases: The first one in the steady state, where load resistance was a constant $R = 57\ \Omega$ (R_{12} in network topology representation), and the second one, where the load resistance was changed from $R = 57\ \Omega$ to $R = 114\ \Omega$ and vice versa. The results of these experiments are shown in Figure 11. To compare the experimental results with the emulated ones, synchronous calculation was performed according to triggering signals. The emulated and real DC-AC converter were exited with the same gate signals Q_{T1}–Q_{T4}. The measured results from the oscilloscope are written to "comma separated values; CSV" file, and, during the emulation, the results were written into the available RAM module. Afterwards, the waveforms were extracted and displayed, as shown in Figures 12–14.



(**a**) (**b**)

Figure 11. Load measurements (x-axis 10 ms/div): (**a**) constant load resistance, voltages; blue curve V_4, y-axis 100 V/div; red curve V_2, y-axis 250 V/div; current, green curve i_{12}, y-axis 2.5 A/div; and (**b**) step change into load resistance, voltages; blue curve V_4, y-axis 100 V/div; red curve V_2, y-axis 250 V/div; current, green curve i_{12}, y-axis 2.5 A/div.

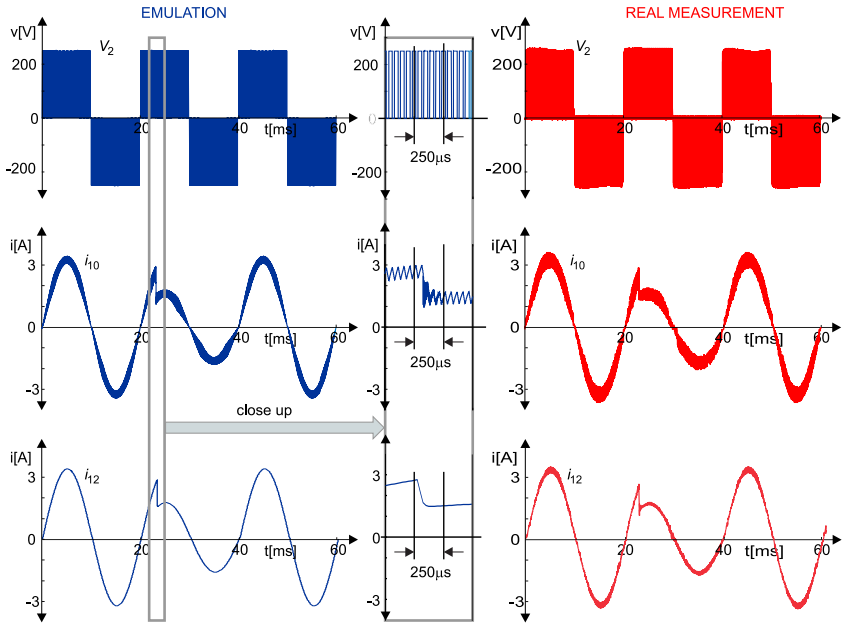


Figure 12. Emulation results and its close-up (blue curves) and measured results (red curves).

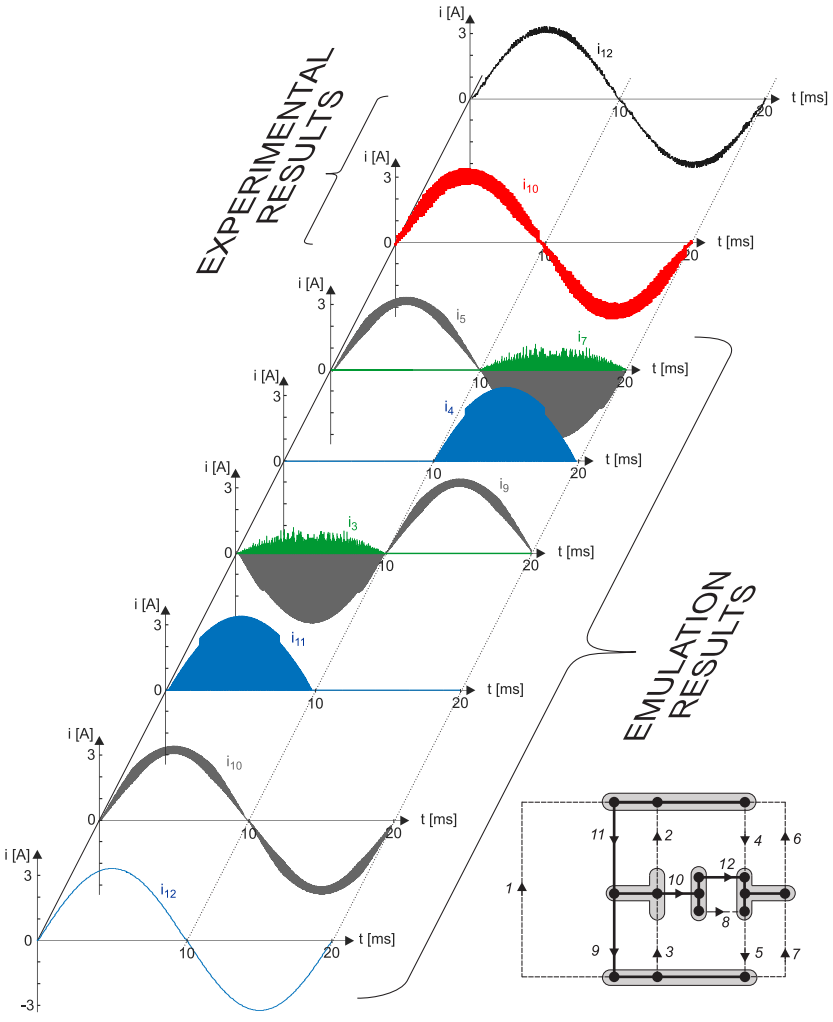


Figure 13. Results of emulation and measurement currents.

Figure 12 shows the emulated and measured voltages on the converter output indicated by V_2, inductor currents i_{10} and resistor currents i_{12}. The obtained results are in a good accordance between emulation and experimentation during the load change. The emulation system enables the observation of any converter variable, component voltages and/or component currents. The emulation system is based on Equation (34), so the loops currents have been calculated. By using the developed tie-set matrix, the branch currents were evaluated as linear transformation of loops currents as follows from Equation (15). Figure 13 shows all of the calculated currents in every converter branch. Emulation and experimental results are marked. All current waveforms directions are indicated according to the graph branches orientation. The emulation system also enables the study of variables in close-up, which is shown in Figure 14. The parts of the positive and negative inductor currents (branch i_{10}) are shown as close-up. The currents can also be seen through semiconductors (transistors and diodes). These are almost impossible to measure on the real converters. These variables can be used for evaluation of possible malfunctions of the semiconductors in fault-tolerant circuits. According to the applied PWM procedure, it is also possible to see the diodes in operation. Diodes are active during the dead-time, which is applied to gate signals (Q_{T1} to Q_{T4}) in order to avoid short circuits in both converter legs.

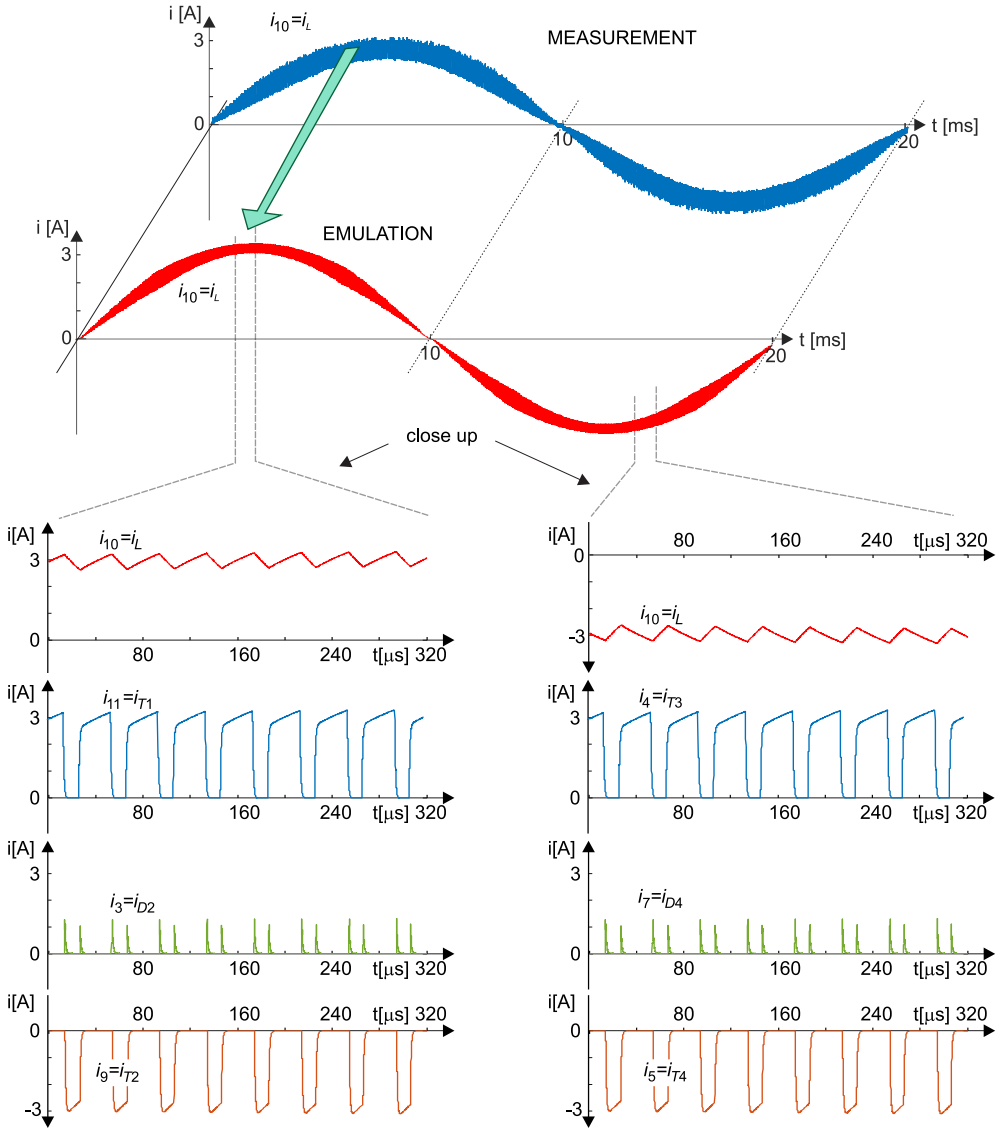


Figure 14. Emulation and measurement results of inductor current and close up of emulated: inductor current (i_{10}), MOSFETs currents (i_4, i_5, i_9 and i_{11}) and diodes currents (i_3 and i_7).

Figure 15 shows all the calculated voltages on every node in the DC-AC converter. The emulation results are in good accordance with the measured ones. To evaluate the voltages, firstly, Equation (19) was calculated, and then, by using these results with Equation (31), the voltages were evaluated on all nodes. The signs of all calculated voltages are in accordance with the voltage drops indicated by arrows in the converter graph.

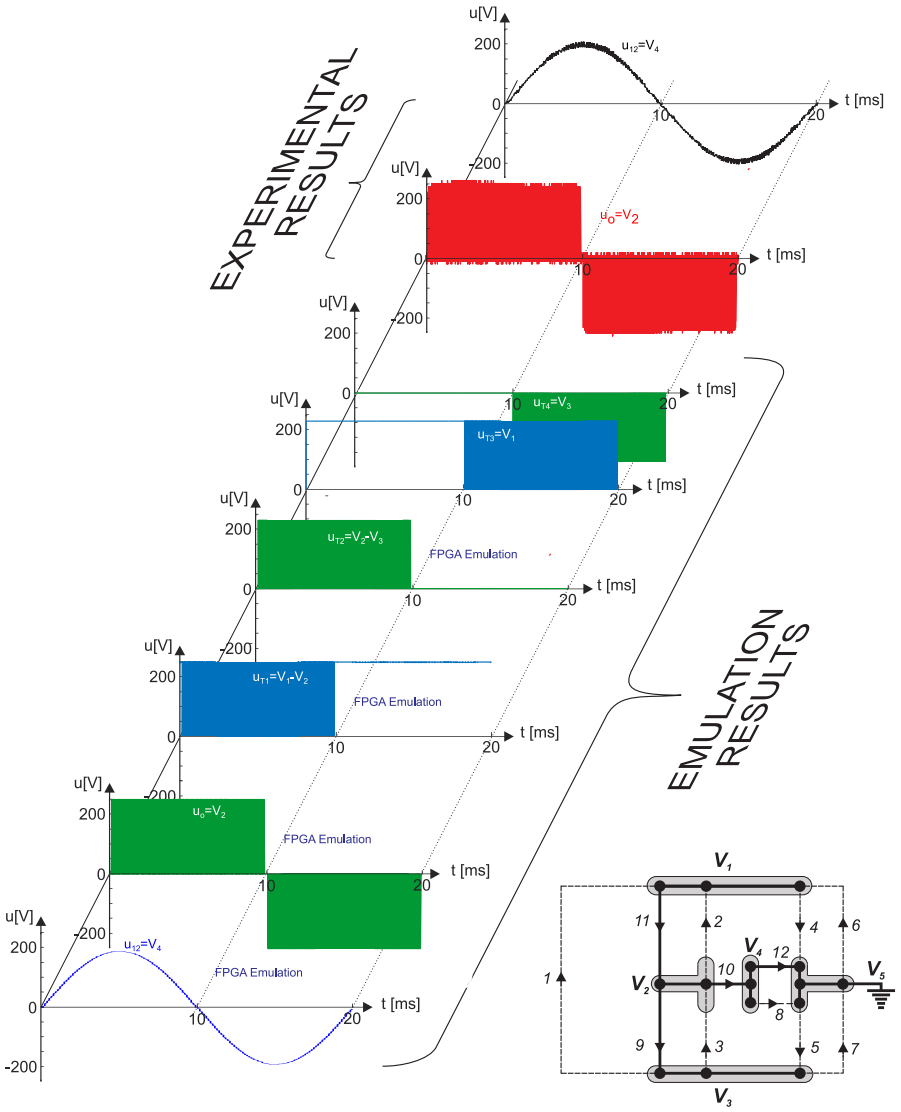


Figure 15. Results of emulation and measurement voltages.

5. Conclusions

An emulator for a DC-AC converter is described in this paper. Using the graph network theory with the proposed approach enables organising the converter mathematical model with the differential equations system. With the help of the tie-set and reduced incidence matrices, all converter currents and voltages can be calculated. Using PWM signals in the converter loops matrices ($\mathbf{R}_\ell$, $\mathbf{S}_\ell$ and $\mathbf{L}_\ell$), the branch values, where semiconductors are placed, were changed to introduce the switching behaviour of the MOSFETs and diodes of the DC-AC converters. As follows from the algorithm, the loops inductance inverse matrix $\mathbf{L}_\ell^{-1}$ should always be calculated when switching actions occur. Due to the requirement that the emulation process must be performed synchronously with the real converter operation, this task is impossible to solve in real-time. This problem was solved by studying

the converter operations, and six inverse matrices were pre-calculated and written in LUT, which were available during the used integration method, and, used correctly, when switching action occurs.

In future work, the focus will be on using the described algorithm for fault tolerant DC-AC converters systems to improve the safety integration level. In addition, the authors would like to extend the used algorithm to other PECs circuits, especially for three-phase systems. The comparison will be done between real and emulated converter total harmonic distortion to check the influence of emulator model parameters and tweak them for better analogy.

Author Contributions: J.M. and M.M. conceived, designed and performed the algorithm necessary for emulation of the PECs, J.M. and M.T. designed the hardware, including the DC-AC converter and test-bench system. M.R. helped in off-line Matlab tasks and communication protocols for the experimental set-up. All authors contributed analysis tools, analysed the data and wrote the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

PEC	Power Electronics Converter
FPGA	Field-Programmable Gate Array
PWM	Pulse-Width Modulation
FD	Fault Diagnosis
HiL	Hardware in the loop
LUT	Look-Up Table
PES	Power Electronics System
DSP	Digital-Signal-Processor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
ADC	Analog to Digital Converter
U_{DC}	Constant Power Source (DC) Voltage
T_1, T_2, T_3, T_4	Converter MOSFET switches
D_1, D_2, D_3, D_4	MOSFETs body diodes
L, R, C	Converter output filter and load
b_T	number of tree branches (or twigs)
n	number of graph nodes
b	number of graph branches
$\mathbf{A_i}$	Incidence matrix
$\mathbf{A}$	Reduced incidence matrix
$\mathbf{A^T}$	Transpose of reduced incidence matrix
N	Number of rows in reduced incidence matrix
a_{ji}	Incidence matrix element ($j \in 1...n$, $i \in 1...b$)
$\mathbf{i_b}$	Branch current vector
v_i	Graph branch voltages
V_j	Graph nodes voltages
$\mathbf{v_b}$	Branch voltage vector
$\mathbf{V_N}$	Node voltage vector
b_ℓ	Number of graph links (or f-loops)
$\mathbf{B}$	Tie-set matrix or fundamental loop matrix
$\mathbf{B^T}$	Transpose of tie-set matrix or fundamental loop matrix
i_i	Graph branch currents
i_j	Graph link (or f-loops) currents (j in Roman numbers)
$\mathbf{i}_\ell$	Link (or f-loops) current vector
e_i	Branch voltage sources

R_i	Branch resistances
L_i	Branch inductances
S_i	Branch elastances ($S_i = \frac{1}{C_i}$)
q_i	Branch charges (i.e., branch capacitor voltages)
$\mathbf{e_b}$	Branch voltage sources vector
$\mathbf{R_b}$	Branch resistances diagonal matrix
$\mathbf{L_b}$	Branch inductances diagonal matrix
$\mathbf{S_b}$	Branch elastances diagonal matrix
$\mathbf{q_b}$	Branch charges vector (i.e., capacitor voltages vector)
$\mathbf{e}_\ell$	Loops voltage sources vector
$\mathbf{R}_\ell$	Loops resistances matrix
$\mathbf{L}_\ell$	Loops inductances matrix
$\mathbf{S}_\ell$	Loops elastances matrix
$\mathbf{q}_\ell$	Loops charges vector (i.e., capacitor voltages vector)
Q_{T1}, Q_{T2}, Q_{T3}, Q_{T4}, Q_{D2}, and Q_{D4}	Transistor gate signals and diode switching signals, respectively
R_{on}, L_{on}	Conducting model value of resistance and inductance for MOSFETs and diodes
R_{off}, L_{off}	Non-conducting model value of resistance and inductance for MOSFETs and diodes
f_s	PWM Frequency
T_s	PWM period
u_{ref}	Modulation reference voltage function
$\hat{U}$	Peak value of reference output sine voltage
ω_0	Sine reference output signal angular frequency
f	FPGA clock frequency
h	Integration step
PC	Personal Computer
RAM	Random-Access Memory
CSV	Comma-Separated Values

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