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SiC-Based Bidirectional Multilevel High-Voltage Gain Switched-Capacitor Resonant Converter with Improved Efficiency

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Abstract: This paper presents the research results of the bidirectional multilevel resonant switched capacitor converter (MRSCC). The converter can achieve a high voltage ratio in multilevel topology, which limits the voltage stress on switches and is able to operate with high power efficiency. The converter can be applied as an interconnector between DC voltage systems used for various applications. This paper presents a method that significantly improves the efficiency of the MSRCC through topology modification. Furthermore, the feasibility of the converter was demonstrated with the use of SiC and Si MOSFET switches, together with suitable passive components. It was demonstrated that the proposed modification of the topology makes the converter very efficient in SiC-based ones and can significantly improve the efficiency of Si MOSFET converters. The series of test results of the SiC-based converter is a novel aspect presented in this paper and shows promising achievements of efficiency. The results were obtained from the laboratory setup of 5 kW and 0.5/2 kV MRSCC. To demonstrate the bidirectional operation of the converter, a back-to-back setup (0.5/2/0.5 kV) was used. It also demonstrates that such a high-voltage gain converter can be accurately tested with the use of laboratory equipment with a typical voltage range.

1. Introduction

The multilevel topology of the converter is favorable for high-voltage circuits due to the reduction of voltage stress on switches. Aside from typical multilevel converters, such as the flying capacitor, neutral point clamped, and cascade bridges, various concepts of switched capacitor-based converters have been proposed recently. The switched capacitor (SC) technique is suitable for high-voltage gain converters and can be effectively used in power converters, which was proven in [1,2]. On the basis of the SC technique, such multilevel topologies include MRSCC (multilevel mesonant switched capacitor converter) [3–5], modular capacitor clamped [6,7], resonant Ladder [8], MMCCC (multilevel modular capacitor clamped converter), 6X [9], converter with coupled inductors in various levels [10], and converters presented in [11–16], where the topologies include a similar concept to MRSCC.

Another important quality of a power electronic converter is its bidirectional operation capability. It is required in a vast range of applications, which incorporates battery management. The analyzed MRSCC is made up of a basic SC structure, which makes it possible to transfer energy in both directions, similar to the converters presented in [3–5,13–17].

The four-level MRSCC converter analyzed in this study (Figure 1a) is a very favorable solution when compared to well-established topologies. It comprises features of a bidirectional and multilevel

topology. In MRSCC, voltage stress on the switches is equal to the voltage of a single cell; therefore, the benefit of switch voltage stress reduction is achieved. In comparison to the other concepts of SC converters, such as SCVMs (switched capacitor voltage multipliers) presented in [18,19], MRSCC is a multilevel concept that can be more favorable for high-voltage applications. Voltage stresses on some switches of SCVMs can reach the output voltage (the highest value). Due to the high voltage gain, low stress on switches, and bidirectional conversion ability, MRSCC can be a beneficial solution for the interconnection between DC voltage systems. Depending on applications, numerous DC voltage systems are often used nowadays [20], and the required DC voltage reaches 1500 V [17]. The microgrid connection is another prospective application of such a converter as well. Furthermore, in MRSCC, the energy is transferred via capacitors, which makes it possible to reduce the weight of the converter in comparison to solutions based on inductive components. In some applications, a low weight can be an important feature due to the requirements related to the assembling system components.

The basic concepts of three-level and four-level MRSCCs are presented in [3], in which a detailed analysis of losses and selection of inductance can be found. In [4], the four-level SC converter with loads connected asymmetrically was analyzed. In [5], the first harmonic approximation analysis and basic experimental results of four-level 1.2 kV MRSCC based on SiC are presented. In [13], as well as [14], the basic structure of a multilevel SC converter is used in cascaded systems. However, the problems of topology modification and efficiency improvement in ZVS conditions were not investigated.

Recently, a lot of research has focused on the elimination or limitation of C_{oss} losses in different types of converters. However, very few of them present a solution for switched capacitor converters and especially multilevel ones. In [15,17], the C_{oss} losses were identified as an important factor in the power efficiency limitation of the voltage doubler based on the MRSCC concept. The solution for C_{oss} elimination is reported in [15] for a MOSFET converter as well as in [16] for GaN and in [17] for SiC. Therefore, the methods for achieving ZVS (zero-voltage switching) in such a converter are demonstrated in those papers, but all of them are similar and limited to two-level (voltage doubler) MRSCC. The methods rely on the application of the special control pattern to switches in higher and lower voltage levels, for additional energy delivery to the resonant inductor before dead time intervals. The energy stored in the resonant inductor is then utilized for the C_{oss} voltage transition in dead time intervals. As reported in [16], this technique is problematic in light load operations, due to significant switching frequency increases. Special control with cycle skipping is required for light load operation, which itself brings some power loss and is problematic due to parasitic oscillations [21]. To mitigate this challenge, the authors in [16,17,21] proposed to move the resonant inductor to the DC side of the converter. It eliminates most disadvantages; however, it still cannot be applied to converters with a number of levels higher than 2, since in higher levels of the converter, the resonant operation could not be achieved. In this paper, the solution with an additional small inductor further referenced as the commutation supporting inductor (L_{SC}) and small (commutation) capacitors connected across resonant branches is presented. This solution is free from the abovementioned limitations. It operates well at any load level, including an idle state, and can be applied for a converter with any number of voltage levels; however, it requires additional components.

C_{oss} losses have an important impact on the efficiency of a high-frequency converter. A model of this type of loss in an SiC-based converter is analyzed in detail in [22]. In the case of SC converters, which contain large numbers of switches, such as SCVM [18,19], and do not operate in ZVS mode, C_{oss} losses can become significant. The method for ZVS operation in SC converters with resonant inductors is an important research subject. It can be introduced to other SC topologies than MRSCC and the results of ZVS operation in an SiC-based converter presented in this paper can have even more general importance. In [23–28], SC converters with ZVS operation are presented. The presented approach for the ZVS problem solution is similar there and the converters use resonant inductors, which makes it possible to apply a phase shift switching or an operation above the resonant frequency for a charge reduction of the switch before it is turned on. The C_{oss} voltage transition method and ZVS operation is accomplished in this paper for four-level MRSCC and can be extended to a higher

number of voltage levels, which is the main difference from previously presented solutions. Therefore, this paper confirms the merit of the MRSCC topology with introduced improvements. Furthermore, numerous new experimental results of Si and SiC MOSFETs based on bidirectional four-level MRSCC, such as the efficiency, voltage ratio measurements, and resonant circuit operation, are presented and compared in this paper. In essence, the main goal of this paper was to verify the concept of the topology modification towards efficiency improvement of four-level SiC-based and Si-based MRSCC converters with the major contributions of this paper being as follows:

- A presentation of a modification of the MRSCC topology to achieve ZVS with no restrictions in terms of the number of voltage levels. A significant increase of the efficiency and significant decrease of idle power losses are achieved in comparison to the base topology by (almost) elimination of the C_{oss} losses.

- A comparison the SiC-based and Si-based MRSCC performance based on experimental results. It is demonstrated that the proposed method makes it possible to achieve a performance of the Si MOSFET design close to the outstanding SiC-based one.

- The demonstration of MRSCC operation in a boost mode as well as in buck mode. It is accomplished in a test setup with two cascaded converters with a common high-voltage DC link (2 kV in the tested case). However, the load and the output voltage sensors operate on a low voltage (<1 kV), which is appropriate for precise voltage registration and efficiency measurement, and MRSCC is a bi-directional converter and such concept of a test setup configuration is justified. A similar approach can be found in [15], which presents the regenerative test setup, composed of two resonant SC converters for efficiency. A single DC-DC converter with a high voltage ratio can be used in photovoltaic systems [17] with a common DC link or DC grid on the output. The application of such converters as an interconnector between DC grids is their prospective application as well, especially as SiC-based solutions.

The paper is organized as follows. In Section 2, the basics of operation of the MRSCC and simulation results are presented. In Section 3, the problem of C_{oss} loss is addressed and a modification of base topology is proposed. Section 4 includes a description of the back-to-back experimental setup and experimental results of MRSCC operation.
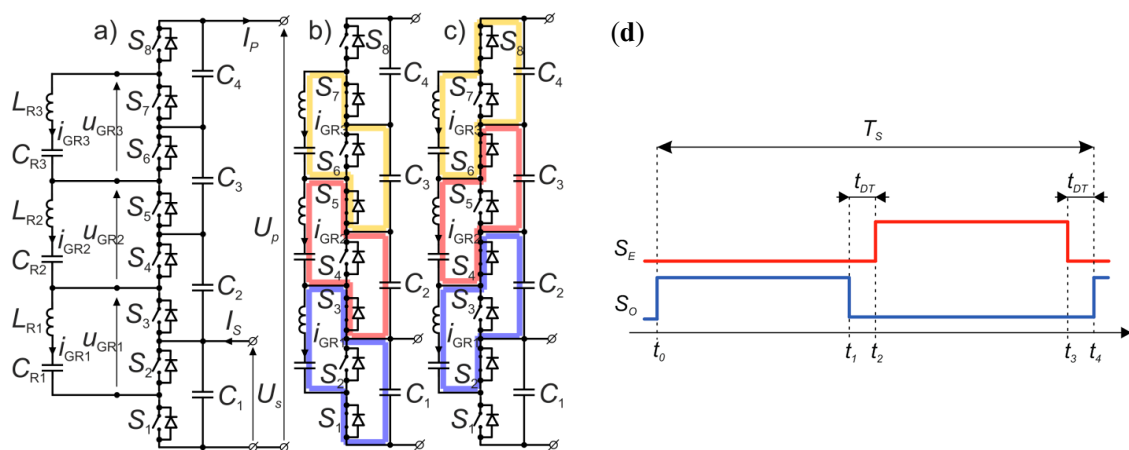
Figure 1. The bidirectional four-level switched capacitor resonant DC-DC converter (**a**) the concept, (**b**,**c**) the modes of operation, (**d**) the control signals of the switches; S_E—control signal of the even switches; S_O—control signal of the even switches.

2. Principle of Operation of the Multilevel Resonant Switched Capacitor Converter (MRSCC)

Figure 1 presents the topology of the MRSCC. The principle of operation assumes charging and discharging of switched capacitors (C_R) in resonant circuits and energy exchange between DC capacitors C_1–C_4. Each voltage level contains two transistors in HB (half bridge) configuration, with

appropriate driving circuits. All the resonant branches $C_{R1}L_{R1}$-$C_{R3}L_{R3}$ are tuned to the same resonant frequency. The control of the converter, in the general concept, requires alternating the switching of odd and even switches with a 50% duty ratio with the resonant frequency of the branches $C_{R1}L_{R1}$-$C_{R3}L_{R3}$. As a result, each resonant branch ($C_{Rk}L_{Rk}$) is switched between two adjacent voltage level capacitors C_k and $C_{(k+1)}$ (Figure 1b,c). The control signals are presented in Figure 1d.

Voltages of the capacitors C_1-C_4 of MRSCC are nearly equalized. As a result, the voltage gain of the idealized converter in the boost-type interpretation is as follows:

$$k_{UTE} = \frac{U_P}{U_s} = n, \tag{1}$$

where U_P-higher side voltage value, U_s-lower side voltage value, and n- number of levels.

During the t_0-t_1 and t_2-t_3 time intervals, the current oscillations occur in resonant branches. During the dead time intervals, the oscillations are stopped, and in the idealized and tuned circuit, the currents of resonant branches are zero during dead time. The current peak stresses of the resonant branches are given by the following relationship:

$$\begin{cases} I_{GR(k)DTmax} = \frac{\pi}{G_{DT}}(n-k)I_P \\ I_S = nI_P \end{cases} \tag{2}$$

where $k = 1, 2, 3, 4, \ldots, (n-1)$; $G_{DT} = 1 - \frac{2t_{DT}}{T_s} \leq 1$; and I_p, I_s-current value of lower and higher voltage side.

The current stresses of the switches are given by:

$$I_{S(2k)RMS}(t) = I_{S(2k-1)RMS}(t) = \frac{\pi}{2}\frac{1}{\sqrt{G_{DT}}}I_P, \tag{3}$$

$$I_{S2RMS}(t) = I_{S1RMS}(t) = \frac{\pi}{2}\frac{1}{\sqrt{G_{DT}}}(n-1)I_P, \tag{4}$$

where $k = 2, 3, 4, \ldots, n$, $\varphi = \varphi_{k-1} = \varphi_k$.

From Equations (3) and (4), it follows that the current stress of switches S1 and S2 is greater than others for $n > 2$. The higher the number of n, the bigger the difference between the current stresses of switches observed in the converter, which is an important conclusion from the switches' selection standpoint. The dead time increases the current stresses of the resonant branches and switches. It corresponds with the G_{DT} coefficient variation in Equations (2)–(4). The example simulation waveforms of the 5 kW and 500 V/2 kV MRSCC are presented in Figures 2 and 3. The results were carried out from two different models and software tools. In the waveforms presented in Figure 2, during the dead time intervals, the oscillations are halted and the current of the resonant branches equals zero. In this simulation, which was performed in MATLAB/SIMULINK software, all parasitic capacitances of the switches were omitted. In a real circuit (Figure 7a), or precise behavioral simulation model designed for PSpice (Figure 3), the distortions can be observed in the dead time intervals. The distortions are caused by an interaction of resonant branches and C_{oss} capacitances of the switches as can be anticipated by comparing the simulation results. Therefore, the distortions in dead time intervals are natural for this topology and are not caused by an improper design of the real converter. For PSpice simulation, the precise models of power transistors provided by the manufactures were used. The simulations parameters are consistent with the experimental setup (Tables 1 and 2) described in Section 4.

Table 1. Parameters for SiC and Si designs for the base configuration.

Number of Voltage Levels	n	4
Switching frequency	f_s	285 kHz
Lower side nominal voltage	V_S	500 V
Higher side nominal voltage	V_P	2000V
Design max power	P_N	5 kW
Capacitance of levels capacitors	$C_4 = C_3 = C_2 = C_1 = 4.7\ \mu F$	
	$C_{1a} = C_{1b} = = 0.47\ \mu F$	
Resonant branches	$L_{R3} = 3.0\ \mu H$ $L_{R2} = 2.0\ \mu H$ $L_{R1} = 0.9\ \mu H$	
	$C_{R3} = 100\ nF$ $C_{R2} = 147\ nF$ $C_{R1} = 320\ nF$	
Commutation branches	$C_{C3} = 22\ nF$ $C_{C2} = 22\ nF$ $C_{C1} = 47\ nF$	
	$R_{C3} = 1\ \Omega$ $R_{C2} = 1\ \Omega$ $R_{C1} = 0.5\ \Omega$	
Switching supporting inductor	$L_{SC} = 54\ \mu H$ ETD29	

Table 2. The measured idle power of a single HB for different transistors used for the SiC and Si setup.

No	Part			Measurement		
	Type	V_{DS} (V)	R_{DSon} (mΩ)	U_{DS} (V)	f (kHz)	ΔP_{CO} (W)
1,2	SCT3030AL	650	30			42
3–8	C3M012090D	900	120	500	285	15
1,2	SiHG33N65EF	650	95			93
3–8	SiHG21N65EF	650	150			60
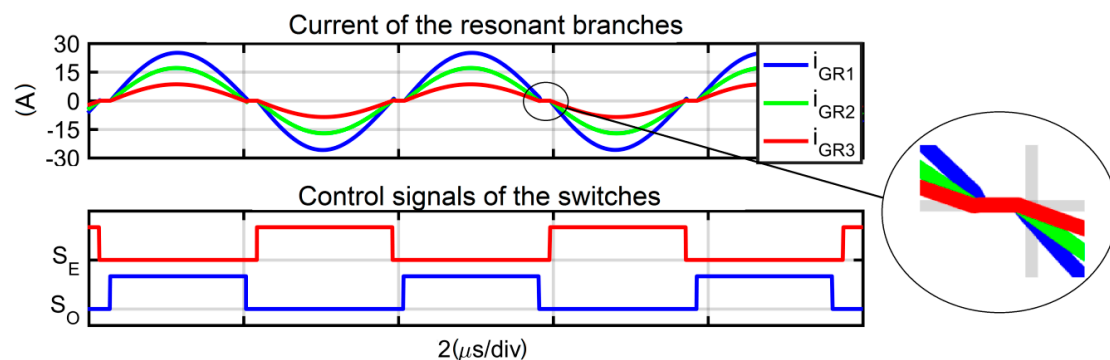
Figure 2. Simulation result of the 5 kW 500V/2 kV MRSCC (Multilevel Resonant Switched Capacitor Converter) in the base configuration in MATLAB/Simulink without C_{oss}.
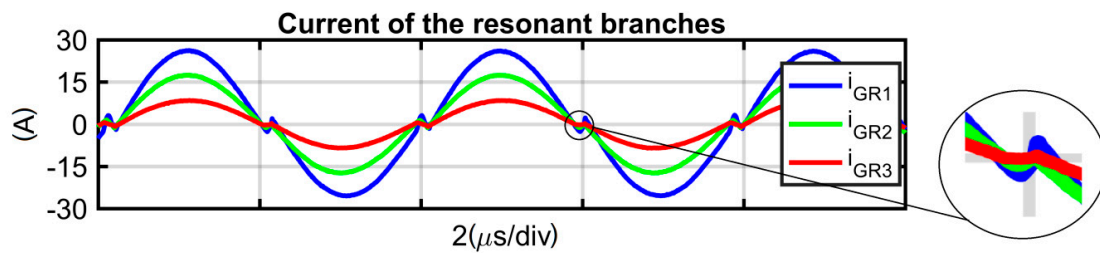
Figure 3. Simulation result of the 5 kW 500 V/2 kV MRSCC in the base configuration in PSpice (plotted in MATLAB) with C_{oss} and other parasitics.

The transition between the boost and buck mode of operation of MRSCC does not require any special control. It depends on the relationships between voltages U_p/U_S. The resonant legs should be tuned to achieve the best possible performance of the converter, and only this case is analyzed in the paper. In [5], the analysis for the general case can be found. For a cost reduction, selected switches can be replaced by diodes, but only unidirectional operation is possible in this case. For example, as presented in the literature [8], a diode-based ladder resonant switched capacitor converter operates in boost mode only.

3. C_{oss} Losses and Its Reduction by Application of the Commutation Supporting Inductor

The converter operates in ZCS (zero current switch) conditions, but switching losses still occur due to charging and discharging of the output capacitances of the switches. The converter consists of a relatively large number of switches; thus, the switching losses may seriously deteriorate its efficiency, especially under the light load operation. C_{oss} losses are also the subject of the research presented in [15,16], where it is eliminated by the special control of the switches. However, a solution for a converter composed of the number of voltage levels above 2 is not presented.

C_{oss} losses are associated with the energy dispersion from C_{oss} by the switch that is turned on as well as the power losses during C_{oss} charging caused by the current flow and commutation in the corresponding switch. In an MOSFET switch, the capacitance C_{oss} is strongly nonlinear and the charge transferred to C_{oss} is (from the DC source U_{HB}, during the lower switch turn on in a half-bridge operating with ZCS):

$$Q_{oss}(U_{HB}) = \int_0^{U_{HB}} C_{oss\_low}(u_{DS\_low})\, du_{DS\_low}. \tag{5}$$

Typically, both switches in HB are the same type and have the same parameters. Therefore, the high side switch will result in the same charge transfer from a DC source. As a result, the charge Q_{oss} is transferred twice in the switching period. Thus, the average value of the C_{oss} losses in a half-bridge of the converter is:

$$\Delta P_{HB\_loss} = 2f_s U_{HB} Q_{oss}(U_{HB}) = 2f_s U_{HB} \int_0^{U_{HB}} C_{oss\_low}(u_{DS\_low})\, du_{DS\_low}. \tag{6}$$

If C_{oss} capacitances are charged to the certain voltage value in the dead time by the external circuit, the start value in the integral in Equation (6) is a nonzero value. Therefore, the losses (Equation (6)) are lower in such a case, and can even be zero (in idealized analysis). The detailed analysis of C_{oss}-related energies and losses in HB can found in [29,30]. The MRSCC converter consists of n number of HBs composed with two various types of switches, resulting from their current stresses described by Equations (3) and (4). The total C_{oss} power loss of the converter is the sum of the C_{oss} losses of all HBs.

For the analysis and optimization of losses in MOSFET power transistors in MRSCC, the following FOM (figure of merit) [31] can be used:

$$F_M = r_{DSon} Q_{oss}, \tag{7}$$

where r_{DSon}-turn on resistance of MOSFET, Q_{oss}-charge calculated as in (5) with $U_{HB} = U_S$.

Based on Equations (3) and (4), the conduction loss in power transistors of the lower HB (S1, S2) and all the higher HBs (S3-S8) can be the following:

$$\Delta P_{Rds\_L} = I_P^2 \frac{\pi^2}{2} r_{DSon\_L}(n-1)^2, \tag{8}$$

$$\Delta P_{Rds\_H} = I_P^2 \frac{\pi^2}{2} r_{DSon\_H}(n-1), \tag{9}$$

where r_{DSon_L}-on-state resistance of the S1-S2 switches, r_{DSon_H}-on-state resistance of the S3–S8 switches.

Utilizing Equations (7) and (6), the C_{oss} loss in power transistors of the lower HB (S1, S2) ΔP_{Coss_L} and all the higher HBs (S3–S8) ΔP_{Coss_H} can be found:

$$\Delta P_{Coss\_L} = 2 f_s F_{ML} U_S \frac{1}{r_{DSon\_L}}, \tag{10}$$

$$\Delta P_{Coss\_H} = 2 f_s F_{MH} U_S (n-1) \frac{1}{r_{DSon\_H}}, \tag{11}$$

where r_{DSon_L}—on resistance of the S1–S2, r_{DSon_H}—on resistance of the S3–S8, f_s—switching frequency, F_{ML}—figure of merit (7) for S1 and S2, F_{MH}—figure of merit (7) for S3–S8.

The total power loss for a given group of switches is the sum of the conduction loss and C_{oss}-related loss. The selection of transistors with higher on-state resistance leads to a higher conduction loss. However, the C_{oss} loss is lower in such a case, if the figure of merit (Equation (7)) is considered constant. Using the above Equations (8)–(11), it is possible to find the optimal value of r_{DSon_L} and r_{DSon_L} for which the total power loss of a transistor is minimal for a given figure of merit. Obviously, the selection of transistors is a discrete problem since only several types of devices with specific parameters are manufactured. The presented solution is continuous, but in spite of this fact, it can be used for the selection of the transistors nearest to the calculated optimal parameters. The optimal on-state resistances of transistors are given by the following relationship:

$$r_{DSon\_L\_opt} = \frac{2 n U_S \sqrt{U_N f_s F_{ML}}}{\pi P_S (n-1)}, \tag{12}$$

$$r_{DSon\_H\_opt} = \frac{2 n U_S \sqrt{U_N f_s F_{MH}}}{\pi P_S}, \tag{13}$$

where $r_{DSon\_L\_opt}$—optimal on resistance of the S1–S2, $r_{DSon\_H\_opt}$—optimal on resistance of the S3–S8, f_s—switching frequency, F_{ML}—figure of merit (7) for S1–S2, F_{MH}—figure of merit (7) for S3–S8, P_S—power of lower voltage side, for which value the minimum losses should occur.

The above Equations (8)–(13) were evaluated for the real setup parameters, which are presented in Section 4, especially in Tables 1 and 2. The figure of merit was calculated based on Equations (5) and (7) and the C_{oss} curves from the data sheets for the two transistors selected in the initial design step: SCT3030AL as S1, S2; F_{ML} = 4 nVs and C3M012090D as S3–S8; F_{MH} = 5.9 nVs. The results are presented in Figure 4.

As can be observed in Figure 4, the initially selected transistors are not optimal. However, there is no significant improvement possible since it is about 20% of the total power loss in the switches. A significant improvement of efficiency may be achieved by the introduction of further modifications as described in Section 4, which nearly eliminates the total C_{oss} power loss. In case of the initially selected transistors, the C_{oss} loss accounts for nearly 87% of the total loss in the switches, and in the case of hypothetical optimal switches, 52%. After the introduced modification of the topology, only conduction losses are relevant. The conduction losses are lower for the initially selected transistors (SCT3030AL, C3M012090D) than in the case of any hypothetical optimal ones. Therefore, the initially

selected transistors were accepted as the final selection. After the modification, the optimization problem must be defined in another way since there is no longer a tradeoff needed between C_{oss} and the on-state resistance.
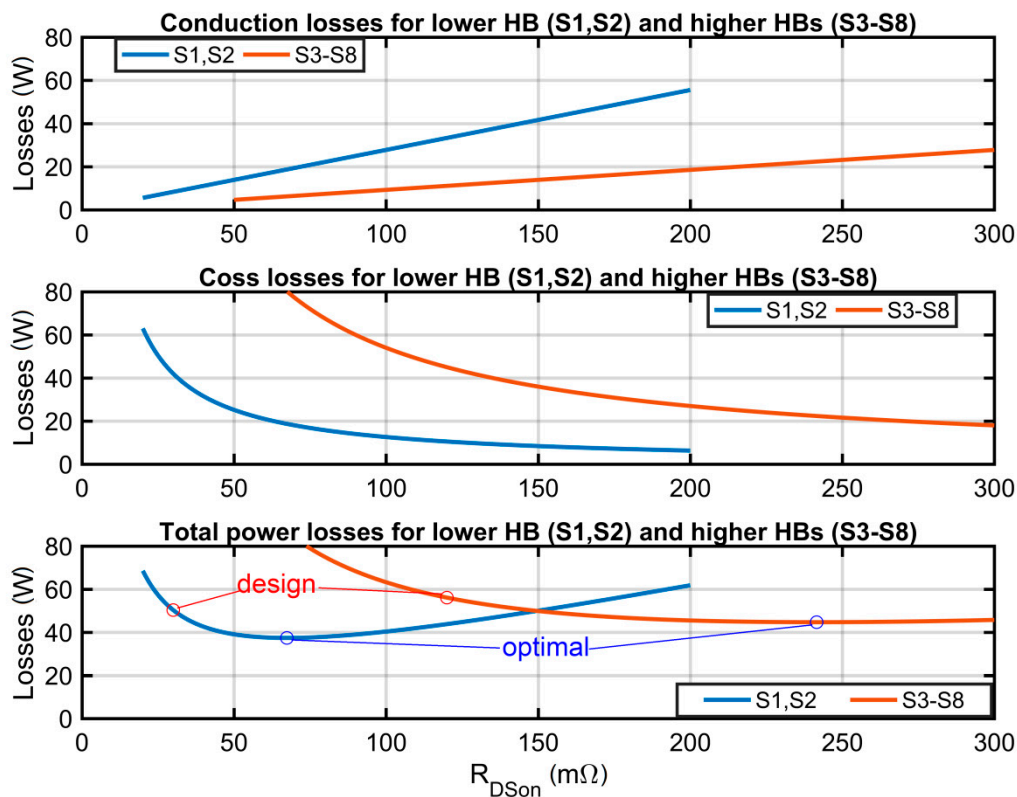

Figure 4. Results of the optimization of losses in power switches in terms of r_{DSon} selection.

3.1. Concept of MRSCC with Commutation Inductor

To reduce the idle power losses, the topology modification is proposed based on the application of the additional commutation inductor L_{SC}, which brings a significant reduction to the switching losses. The proposed concept and commutation sequence from odd to even switches is presented in Figure 5a–c. The inductor L_{SC} is connected between the output of the lowest HB and the output of the voltage divider created in the lowest voltage level. Due to the fact that all HBs are switched with a 50% duty ratio, the waveform of the current in L_{SC} is symmetrically triangular with the positive and negative peaks that occur during the commutation. This current charges and discharges the output capacitances of all switches during the commutation, causing ZVS operation.

When all the HBs are turned into *DT* mode (Figure 5b), the output capacitance of all HBs is charged by the current of inductor L_{SC} (HB1 directly, and the rest via C_{Ck} capacitors). The transition is finished after a certain time, which depends on the peak current of the L_{SC} and the values of the output capacitances of the switches. To finish the switching sequence, all the even switches are turned on (Figure 5c). Because the output capacitances of the switches are charged and discharged by an inductor, their switching losses are significantly reduced (in theory it is lossless).
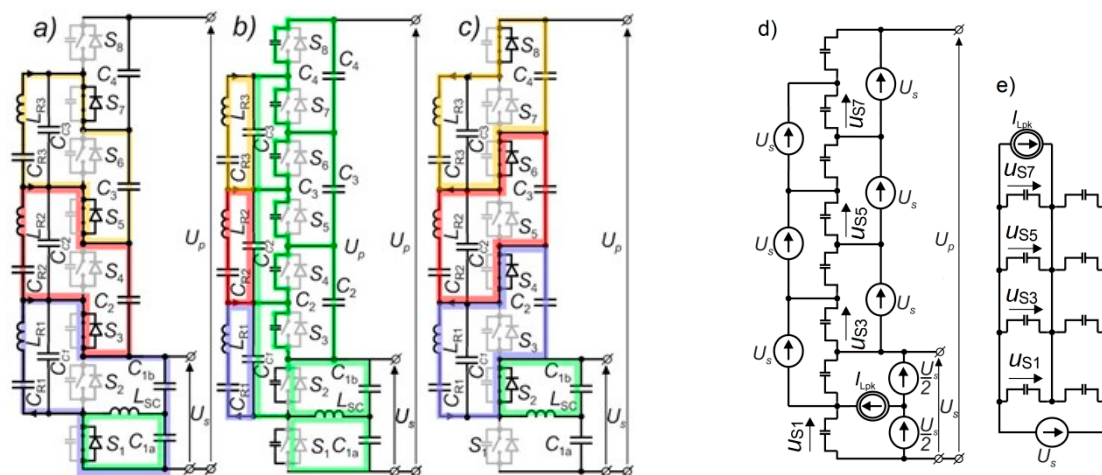
Figure 5. (**a–c**) The sequence of modes for commutation from odd to even switches in MRSCC with the commutation capacitors C_{Cn} and the supporting inductor L_{SC}; (**d**) Simplified equivalent circuit for charging the C_{oss} by L_{CS} current during dead time (mode b); (**e**) further simplification.

3.2. Application of Communication Capacitors in MRSCC Branches

The resonant branches contain series inductors and therefore, for very short commutation processes, they can be considered as the current sources. The values of those current sources can be assumed equal to the instantaneous current of the resonant branches at the beginning of the commutation. In the precisely tuned circuit, those values are close to zero, which means that the resonant branches have almost no effect on the commutation process. For this reason, the commutation capacitors (relatively small) are applied to the circuit, in parallel to the resonant branches. The commutation capacitors C_{Ck} can be considered as the voltage sources with the value of U_S (as well as the all C_k capacitors). They allow the output capacitances of higher-level HBs to be charged and discharged by the current of the L_{SC} inductor flow. The inductor L_{SC} can be considered as the current source with a positive (odd to even switches commutation) or negative (even to odd switches commutation) peak value. The equivalent circuit representing such conditions is shown in Figure 5d. The circuit can be further simplified, to the circuit where all C_{oss} are charged in parallel and supplied by one U_S voltage source, as shown in Figure 5e. The application of the commutation capacitors has an additional effect. In the base circuit, during the dead time, the current oscillations in the resonant branches are stopped, thus the resonant frequency of the converter is lower than the resonant frequency of the branches. The commutation capacitors clamp the resonant branches during the dead time, which allows the oscillation to continue. As a result, the resonant frequency of the converter is equal to the resonant frequency of the resonant branches. Furthermore, an additional benefit is the resonant current is a smooth sinusoidal (Figure 6b), while in the base circuit, some distortion (fast oscillation) can be observed in dead time intervals (Figures 4 and 6a). Such distortions reduce the balancing capability of the resonant branches and increase the series-equivalent output resistance of the converter, which will be presented in Section 4. The application of the L_{SC} inductor and C_{Ck} capacitors has no direct influence on the voltage gain of the converter. However, it improves the power efficiency and eliminates distortions of the oscillations, resulting in a reduction of the series-equivalent resistance of the converter.

Idle mode losses depend on the peak value of the current of L_{SC}, which will be demonstrated in Section 4 together with the research results related to the impact of the I_{LSCpk} on the switch voltage during commutation. The overall efficiency of the MRSCC is also affected by the remaining switching losses and conduction losses, which are out of the scope of this paper.
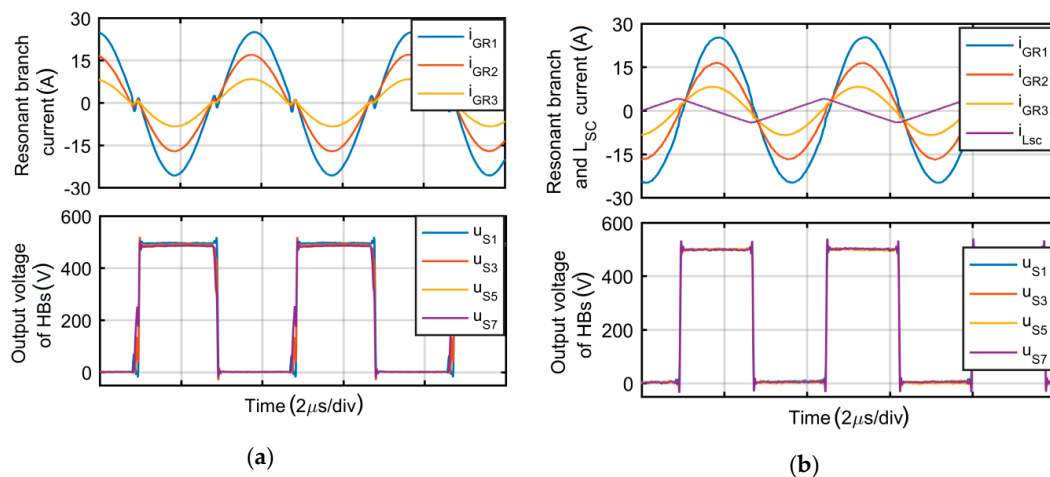
Figure 6. Waveforms of HB (Half Bridge) voltages and resonant branches currents for step-up steady-state operation of: (**a**) base MRSCC at 258 kHz, (**b**) modified MRSCC at 285 kHz. Experimental results of SiC-based converter 5 kW load (oscilloscope data exported and to MATLAB and plotted).

3.3. Selection of L_{SC} and C_{Ck} Values

Firstly, the required peak current of the L_{SC} should be determined. According to Figure 5e, the total charge Q_{ossT} that must be provided by the L_{SC} inductor during the dead time equals the sum of the $Q_{oss}(U_s)$ determined for every transistor. The charge must be transferred during the dead time interval t_{DT}, thus the required peak current of L_{SC} is given as:

$$I_{LSCpk} = \frac{1}{t_{DT}} \sum_{m=1}^{2n} Q_{oss(m)}(U_S), \tag{14}$$

where $Q_{oss(m)}(U_S)$—charge determined based on Equation (6) for the m-th transistor for voltage U_S.

The required inductance L_{SC} could be approximated as:

$$L_{SC} = \frac{U_S}{8 f_s I_{LSCpk}}. \tag{15}$$

The values of the C_{Ck} capacitors should be large enough so that the voltage across does not change significantly in the dead time interval, when the I_{LSC} flows through them, charging the C_{oss} of the transistors. The values of the C_{Ck} capacitors are given by:

$$C_{Ck} = \frac{1}{\Delta U_{CC(k)}} \sum_{m=2k+1}^{2n} Q_{oss(m)}(U_S), \tag{16}$$

where $\Delta U_{CC(k)}$—change of voltage across k-th capacitor in the dead time interval.

The selection of the values of the capacitor according to Equation (16) is therefore dependent on the permitted change of the voltage across in the dead time interval ΔU_{CCk} and C_{oss} of the used transistors. Too high ΔU_{CCk} values (too low capacitance of C_{Ck} capacitors) cause inefficient charging and discharging of C_{oss} of higher-level transistors and stimulation of resonance branches by voltage glitches during the dead time intervals. Too low ΔU_{CCk} values (too high capacitances) are unfavorable not only in terms of size and cost but also due to the increased participation of these capacitors in energy transport between level voltages, which cause unwanted inrush currents. From the conducted experimental research, it follows that the values of ΔU_{CCk} in the range of few volts (for SiC-based devices between 10 and 100 nF) bring suspected favorable effects. From Equation (16), it follows that the higher the index of the capacitor, the lower the capacitance demanded. To dampen very fast

oscillation caused by hard switching of C_{Ck} and parasitic inductances, resistors R_{Ck} should be added in series with C_{Ck}. Typically, values in the range 0.1–1 Ω are optimal.

4. Experimental Results

### 4.1. The laboraTory Setup and Operation of MRSCC

The laboratory setup was designed for performing tests and measurements of a 2 kV four-level MRSCC converter in a comparative manner. To mitigate the problem of high-voltage measurements, the special laboratory setup was designed. Because the topology is bidirectional, twin converters can be connected back-to-back, creating a cascade with the common high-voltage link. The input and output voltage value of the cascade was 500 V, and this allowed for utilization of the low-voltage laboratory equipment.

Figure 7 presents the schematic of the experimental setup. Tables 1 and 2 contain the crucial parameters of the experimental system. Figure 8a presents the picture of the experimental system. The setup consists of two identical converters designed as a PCB module, which contains all the power and auxiliary components. Every voltage level was equipped with two channel gate driver ICs (UCC21520, Texas Instruments, Dallas, USA). The driver incorporates DT logic and a timer, thus only one control signal was sufficient for each voltage level. The fiber wires were used for signal delivery because of the great isolation that they provide. The controller was designed with an FPGA device and provided control for both converters, with eight control signals in total. The control algorithm included simple pattern generation in open loop mode. The resonant branches were designed to achieve a unified voltage ripple across all the resonant capacitors (about 100 V_{pk-pk}), and the same resonant frequency. The resonant branches were composed of the inductors based on ferrite gapped toroid- and FKP1 (WIMA, Mannheim, Germany)-type capacitors.

Figure 6 presents the waveforms of the resonant branch current and the output voltages of every single HB (which in fact are the voltages of the switches with an odd index). The waveforms in Figure 6a were obtained in MRSCC in the base configuration while the waveforms in Figure 6b were measured in the modified MRSCC.
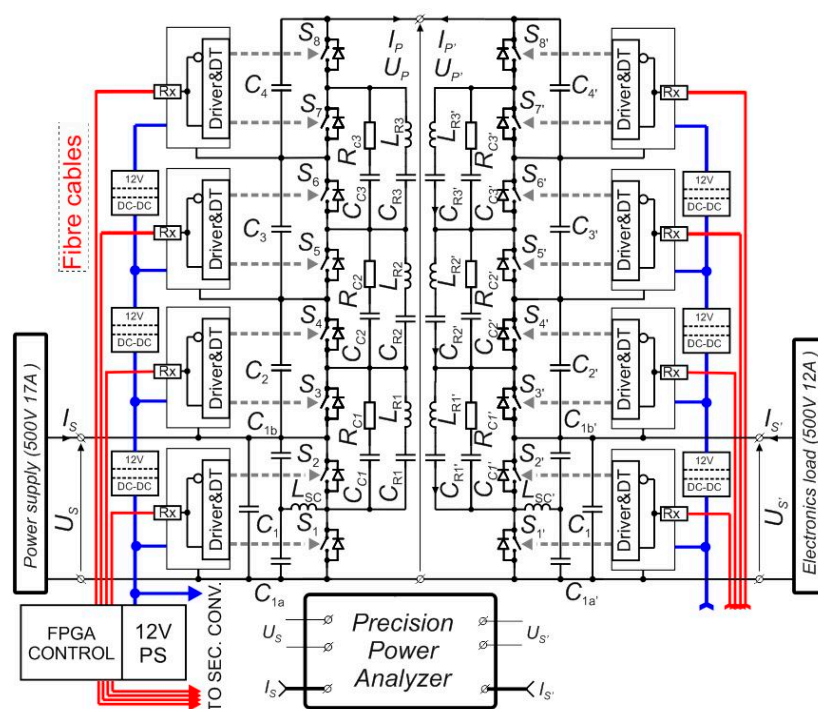

Figure 7. Schematic of the MRSCC laboratory back-to-back setup with modification applied (L_{SC} + $C_{Ck}R_{Ck}$).
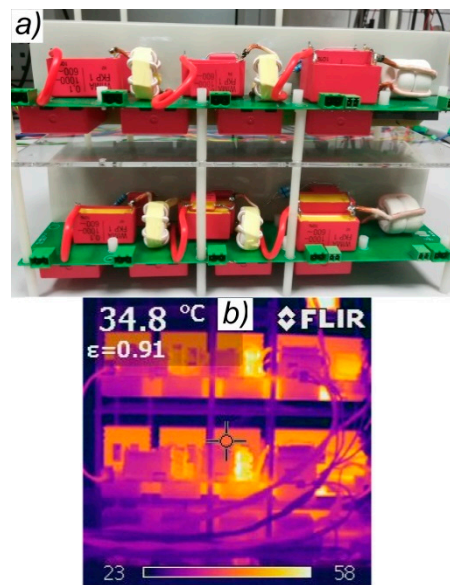
Figure 8. (**a**) Picture of the MRSCC laboratory back-to-back setup (**b**) IR (Infrared) picture under full load (5 kW)—both SiC design.

4.2. Efficiency Measurement Results and Discussion

Figure 9 presents the experimental results related to the efficiency of the MRSCC converter. The measurements presented in Figure 9a,b are related to the single converter but those in Figure 9c are related to the whole cascade. The measurement was performed for different configurations of the converter. The power efficiency of the converter for the base configuration was relatively low (Figure 9c-curves no. 4). The influence of the high idle power losses was significant because a typical peak of the efficiency in the chart efficiency versus power was not observed. Despite this, the efficiency increased with the power load. In the first modification, the $C_{Ck}R_{Ck}$ branches were added but with no inductor L_{SC} (Figure 9c-curves no. 1). The power efficiency was even worse for the low load because the frequency (285 kHz) was higher due to the lack of oscillation breaks in DT intervals. Therefore, the C_{oss} losses were proportionally higher in this case. However, the distortions in dead time intervals were eliminated, which improved of the voltage efficiency. After the application of the commutation supporting inductor L_{SC}, outstanding results were obtained (Figure 9c-curves no. 2). Figure 9a,b presents the detailed results related to the improvement of the efficiency of the converter by a reduction of the C_{oss} losses. As described in Section 3, it was achieved by the application of the supporting inductor (L_{SC}) and operation at the appropriate peak current of L_{SC} during commutations. Figure 9a presents the waveforms of the rising slope of the low side transistor in a half bridge for a different peak value of the L_{SC} current, and Figure 9b presents the respective idle power measurements for the SiC-based design. The results were performed on the experimental setup with SiC switches operating with 285 kHz. The current of L_{SC} should be low but sufficient to effectively perform the transition. A current of L_{SC} that is too high causes hard switching and increases of the losses (Figure 9c). It is remarkable that the idle mode power losses were reduced from approximately 100W in the case when $I_{LSCpk} = 0A$ to nearly 3 W for $I_{LSCpk} = 6A$.
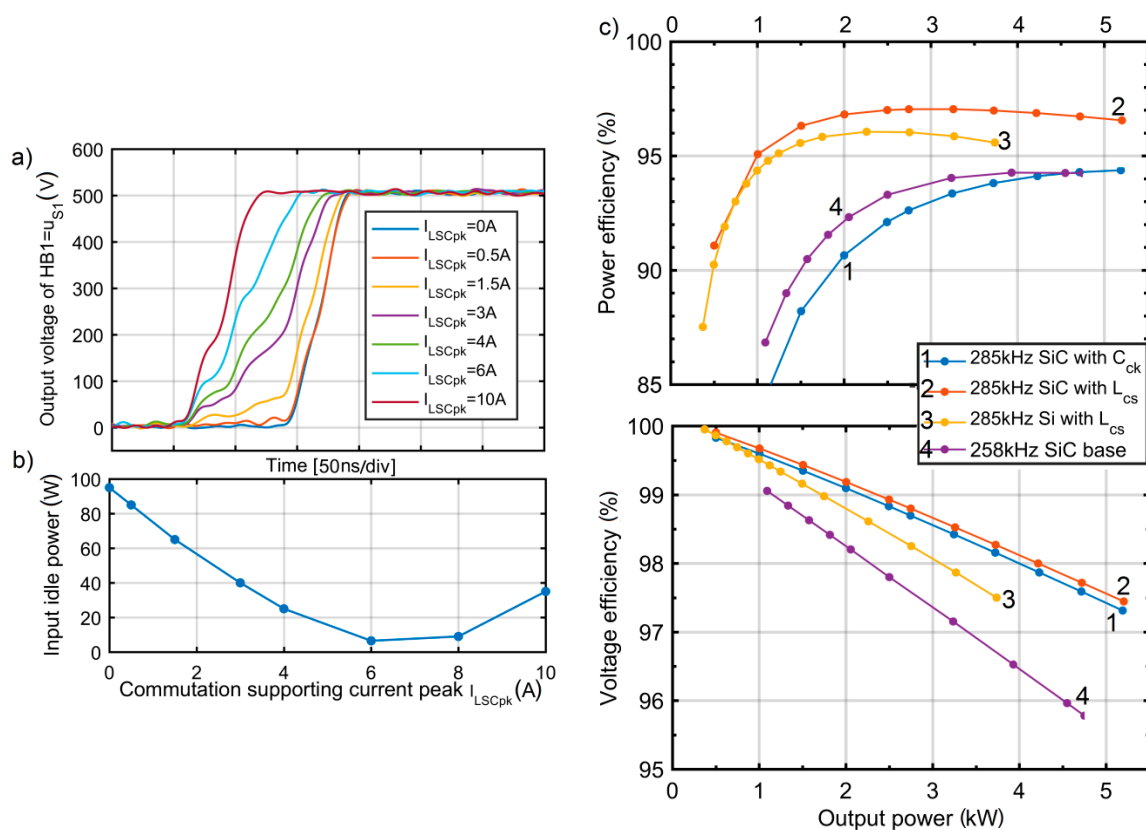
Figure 9. Experimental results: (**a**) waveforms of voltage rising slope HB1. (**b**) idle power losses of the single MRSCC converter-SiC design 285 kHz, (**c**) Power and voltage efficiency characteristics vs. output power for different configurations of the cascaded setup. Yokogawa WT1800 Precision Power Analyzer.

For further references, the power and voltage efficiency curves are presented in Figure 9c-curves no. 3. The parameters of the Si design were insignificantly worse only when compared to outstanding SiC. Higher R_{DSon} losses for Si MOSFETs (Table 1) limited the voltage efficiency and maximum load of the converter. The Si-based design was not able to operate with 285 kHz without the L_{SC} supporting inductor due to huge commutation losses (in theory, 270 W per single converter based on Table 2 and simple calculation). This extreme case shows how effective the proposed modification is. In Table 2, the power consumed by a single non-loaded HB is listed (for different transistors, given frequency, and common DC link voltage). As can be noticed, the power losses are significant, especially for Si devices, even when the types with definitely higher R_{DSon} are compared. The results of the case of the Si-based design L_{SC} inductor and f_s = 285 kHz are presented in Figure 9c-curve no. 3.

A thermography picture presented in Figure 8b shows that the heating of both the converters was nearly the same. It means that the efficiency of a single converter can be properly estimated on the basis of the efficiency results presented in Figure 9c taking into account half of the total losses in the system. Therefore, the peak efficiency of the SiC-based MRSCC with the L_{SC} inductor was approximately equal to 98.5%.

5. Conclusions

In this paper, the research results under the operation of a modified SiC and Si-based MRSCC converters were presented. The MRSCC converter is a relatively novel topology and its improvement was proposed in this paper. The solution assumes the application of a commutation supporting inductor to reduce the switching losses associated with Coss in a converter made up of any number of levels.

The majority of research was performed in the 5 kW laboratory setup, which demonstrates the feasibility of boost and buck operation of the MRSCC. The conversion between the levels of 500 and 2 kV at a switching frequency 285 kHz, with the use of switches with VDS = 900 and VDS = 650 V, was demonstrated. Both the converters were tested simultaneously in the system with a common high voltage DC link. The input and output of the system remained on a low voltage level, which made it possible to perform high-precision efficiency measurements. Furthermore, it is a good example of a low-cost laboratory test setup for high voltage ratio converters.

The major goal of the research focused on a verification of the topology improvement in a four-level bi-directional MRSCC with a 0.5/2 kV voltage conversion ratio with the use of SiC and Si switches. It was accomplished with very promising results and the following conclusions:

- The solution with a commutation supporting inductor in MRSCC is feasible and brings a significant increase of the power efficiency.
- A near-total elimination of the C_{oss} power losses was observed in MRSCC with the commutation supporting inductor and the suitable switching applied.
- An increase of the voltage efficiency was observed as well (lowering of the output-equivalent series resistance). The voltage gain was more stable vs. load and the difference between the theoretical and practical voltage gain was lower than in the case without the proposed improvements.
- The method is very efficient in MRSCC with Si MOSFET as well. Through the application of the commutation supporting inductor, the performance measured in the case of the Si MOSFET MRSCC increased to the level comparable with the converter based on outstanding SiC switches.
- In the SiC-based MRSCC, a high power efficiency of 98.5% was measured.

The efficiency versus power characteristic showed an insignificant decline when the power increased, which is also beneficial. The voltage drop versus power was not significant in the demonstrated design cases of MRSCC. The best solution of 2.5% of the voltage decrease in the 5 kW range was observed. The results of the heat distribution in the converter showed that it can be regular. Overheating of particular cells was not observed.

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Nomenclature

DT	Dead Time
FOM	Figure Of Merit
HB	Half Bridge
MRSCC	Multi-level Resonant Switched Capacitor Converter
SC	Switched Capacitor
SCVM	Switched-Capacitor Voltage Multipliers
ZVS	Zero Voltage Switch
ZCS	Zero Current Switch
$C_{oss_{low}}\left(u_{DS_{low}}\right)$	Output capacitance characteristic of a MOSFET
F_M	FOM for MOSFET
$I_{GR(k)DTmax}$	Peak current of k-th resonant branch

k_{UTE}	Ideal Voltage Gain
ΔP_{Rds_L}, ΔP_{Rds_H}	Conduction losses for lower HB (S_1, S_2) and for all higher ones (S_3–S_8)
ΔP_{Coss_L}, ΔP_{Coss_H}	losses for lower HB (S_1, S_2) and for all higher ones (S_3–S_8)
P_S	Power of lower voltage side
r_{DSon_L}, r_{DSon_H}	On state resistance for lower switches (S_1, S_2) and for all higher ones (S_3–S_8)
U_p, I_p	Voltage, Current Higher Side
U_S, I_S	Voltage, Current Lower Side
U_{HB}	DC link voltage of a Half Bridge

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