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Wide-Supply-Voltage-Range CMOS Bandgap Reference for In Vivo Wireless Power Telemetry

Ruhaifi Bin Abdullah Zawawi [1], Wajahat H. Abbasi [1], Seung-Hwan Kim [2], Hojong Choi [3,*] and Jungsuk Kim [4,*]

1 Department of Health Science and Technology, Gachon Advanced Institute for Health Sciences & Technology, Incheon 21999, Korea; ruhaifi@bme.gachon.ac.kr (R.B.A.Z.); wajahat@bme.gachon.ac.kr (W.H.A.)
2 R&D Center, Metabiomed Corporation, 215 Osongsaenmyeong1-ro, Chenongu 28161, Korea; mbclub@metabiogw.bizmeka.com
3 Department of Medical IT Convergence Engineering, Kumoh National Institute of Technology, 350-27, Gum-daero, Gumi 39253, Korea
4 Department of Biomedical Engineering, Gachon University, 534-2 Hambakmoe-ro, Incheon 21936, Korea
* Correspondence: hojongch@kumoh.ac.kr (H.C.); jungsuk@bme.gachon.ac.kr (J.K.)

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Abstract: The robustness of the reference circuit in a wide range of supply voltages is crucial in implanted devices. Conventional reference circuits have demonstrated a weak performance over wide supply ranges. Channel-length modulation in the transistors causes the circuit to be sensitive to power supply variation. To solve this inherent problem, this paper proposes a new output-voltage-line-regulation controller circuit. When a variation occurs in the power supply, the controller promptly responds to the supply deviation and removes unwanted current in the output path of the reference circuit. The proposed circuit was implemented in a 0.35-µm SK Hynix CMOS standard process. The experimental results demonstrated that the proposed reference circuit could generate a reference voltage of 0.895 V under a power supply voltage of 3.3 V, line regulation of 1.85 mV/V in the supply range of 2.3 to 5 V, maximum power supply rejection ratio (PSRR) of −54 dB, and temperature coefficient of 11.9 ppm/°C in the temperature range of 25 to 100 °C.

Keywords: bandgap voltage reference; inductive link; implantable biomedical; line regulation; wireless power telemetry

1. Introduction

Implantable medical devices (IMDs) are highly demanded in many clinical applications to treat disorders, restore sound, monitor biological parameters of the human body, or restore vision, such as with retinal prosthetics [1,2]. Power to the IMDs must be supplied in vivo from the external world. At the early stage of the IMDs, a wire connection passing through the skin is employed to directly provide power to the implants without a power transfer loss [3,4]. However, the transcutaneous wire connection causes an infection on the skin and soft tissue [5], resulting in the wire no longer being useful. An infrared (IR) technique has been harnessed to wirelessly transfer power to high-density IMDs, i.e., retinal prosthetics [6]. Although the photovoltaic (PV)-powered stimulation chip can partially elicit responses from ganglion cells, the generated power under IR light is too low to drive other functional blocks in the retinal chip, such as a high-density stimulation array, its digital control logic, and back telemetry, which requires high power consumption. Moreover, the IR-based power telemetry has a critical shortcoming in that it is sensitive to the alignment between the light source and implanted chip. The misalignment frequently caused by an eye movement leads to degradation in the power supply. Therefore, the IR-based power telemetry is not suitable for high-density IMDs.

To date, the power telemetry system based on inductively coupled coils is the most popular method to wirelessly transfer high amounts of power to implants in the body [7–10].

Figure 1 shows the typical architecture of a single-band wireless power telemetry system, in which data signals are modulated on a power carrier [11–13]. This near-field inductive link system is composed of a power amplifier (PA), resonance tanks in the transmitting (L_1 and C_1) and receiving (L_2 and C_2) sides, a rectifier (D_1 and C_3), a bandgap voltage reference (BGR) circuit, and a low-voltage drop regulator (LDO). The coil L_1 captures the AC signal from the power amplifier. The amplified radio frequency (RF) signal is transmitted to L_2 at the desired resonance frequency. The received AC voltage is converted to a rough direct current (DC) voltage with a ripple passing through the rectifier, which is then regulated by the LDO to provide sufficient supply voltages for the digital and analog circuits in the IMD.

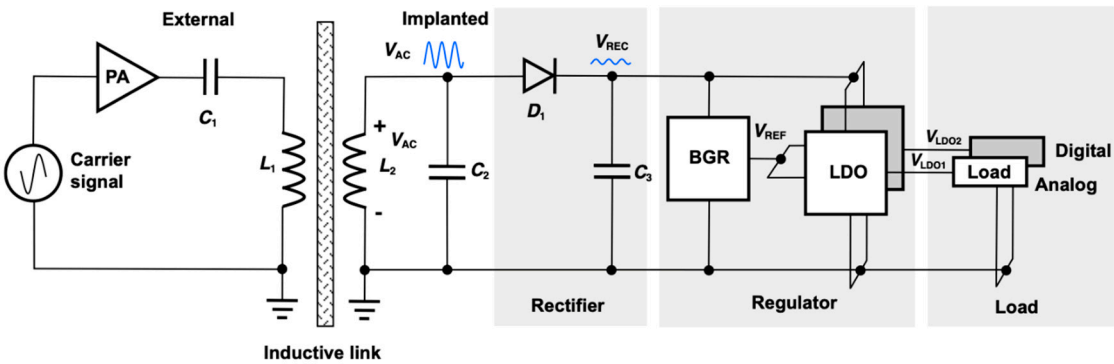


Figure 1. Single-band power telemetry system.

For this power telemetry system using inductively coupled coils, achieving a high power transfer efficiency is essential to minimize the power loss that results in secondary heating effects on the tissue [14]. However, the movement of a patient with the implantable device in his or her body sometimes causes misalignment between coils, thereby degrading the coupling coefficient. This results in variation in the amplitude of the receiving signal, which leads to inefficient rectification. Therefore, the rectified DC signal from the variation in the received power signal should be constantly regulated, and a wide range of input voltages should be provided for other circuits, such as the stimulation array and its digital controllers.

A BGR circuit has a critical function in generating a constant reference voltage (V_{REF} in Figure 1), which is applied to the voltage regulator circuit. The input signal of the BGR depends on the output of the rectifier, and thus the BGR should be immune to any variation in the rectified signal. In addition, the BGR has been known to be stable regardless of any changes in a device process or temperature [15]. The crucial element in the BGR is a current mirror, in which the current generated at the output stage of the BGR should be exactly matched with the proportional-to-absolute-temperature (PTAT) current. Among the various schemes for the current mirror [15], the cascode current mirror has been widely employed in voltage reference circuits to increase the line regulation and power supply rejection ratio (PSRR) [11–13,16]. This is because the cascode structure can suppress the channel-length modulation effect, although minimum-length transistors are adopted in the circuit [15]. The cascode also effectively increases the output resistance of the current mirror circuit. However, the cascode current mirror has two major disadvantages. First, it undergoes a body effect that causes a threshold offset because the source terminals of transistors are different. This disadvantage can be resolved by applying a higher current to the cascode structure circuit. Although this method can significantly decrease the deleterious effect of the threshold offset, it leads to a high power dissipation, which is not suitable for the IMDs operating with low power in the body. Second, the cascode structure requires a high supply voltage to drive all transistors in the saturation region, thus resulting in high power consumption. These two technical challenges become more significant in a nanometer

complementary metal-oxide-semiconductor (CMOS) process that operates with low voltage [15]. Accordingly, a new method for the current mirror in BGR is required to decrease the deleterious effect due to the channel-length modulation.

In this paper, we propose a novel technique to mitigate this deleterious effect. The proposed BGR circuit was equipped with a line regulation control circuit to decrease the channel-length modulation effect in contrast with the proposed works in [17–21]. A basic current mirror [15] was used in the proposed BGR along with the line regulation control circuit adopted at the output stage. The proposed controller dynamically responded to the supply variation and maintained a constant current in the output path, ensuring a stable reference voltage over a wide supply range. In addition, the deviation in the output voltage due to temperature variation was minimized by employing a curvature-corrected control circuit in the proposed BGR. Diode-connected MOS transistors operating in the sub-threshold region were adopted to generate a high-order temperature coefficient that behaved in a manner opposite to that of the bipolar transistor constructed in the conventional BGRs. A high PSRR was achieved by employing a high-gain amplifier that rejected the variation in the power supply. The proposed BGR circuit was designed and fabricated using a 0.35-µm SK Hynix CMOS standard process.

The paper is organized as follows. Section 2 explains the designed architecture of the conventional and proposed BGRs. The working principles of the conventional and proposed BGRs are discussed. Section 3 outlines the simulation and measurement results. Finally, Section 4 concludes this paper.

2. Architecture of the BGR Circuit

2.1. Conventional BGR Scheme

The conventional BGR schematic is shown in Figure 2 [15]. The BGR output voltage, V_{REF}, is the summation of a positive-coefficient voltage V_{PTAT} and a negative-coefficient voltage V_{CTAT}, as shown in the top right corner of Figure 2. The conventional BGR is composed of a startup-circuit, PTAT current generator, and complementary-to-absolute temperature voltage (CTAT) generator that is produced by the bipolar junction transistor Q_3. The high-gain amplifier (*AMP*) forces the voltage at node V_{A} to be equal to that at node V_{B}. From the relationship between the emitter-based voltages V_{EB} of Q_1 and Q_2, I_{PTAT} can be derived as follows:

$$I_{\mathrm{PTAT}} = \frac{V_{\mathrm{T}} \ln(n)}{R_1}, \tag{1}$$

where V_{T} is the thermal voltage, and n is the emitter-area ratio of Q_1 and Q_2. Under the condition that the transistors M_{P3} and M_{P2} are identical in size, I_{PTAT} is copied into transistor M_{P3} from M_{P2}. The output voltage V_{REF} of the conventional BGR can be expressed as:

$$V_{\mathrm{REF}} = \frac{R_2 V_{\mathrm{T}} \ln(n)}{R_1} + V_{\mathrm{EB3}}. \tag{2}$$

By selecting appropriate resistances for R_1 and R_2, we can lower the temperature coefficient of the conventional BGR output voltage. However, the nonlinear voltage of V_{EB3} means the zero-temperature coefficient is difficult to accomplish.

In practice, I_{PTAT} is not mirrored exactly from M_{P2} to M_{P3} because of the channel-length modulation in these transistors. As a result, Equation (2) requires modification.

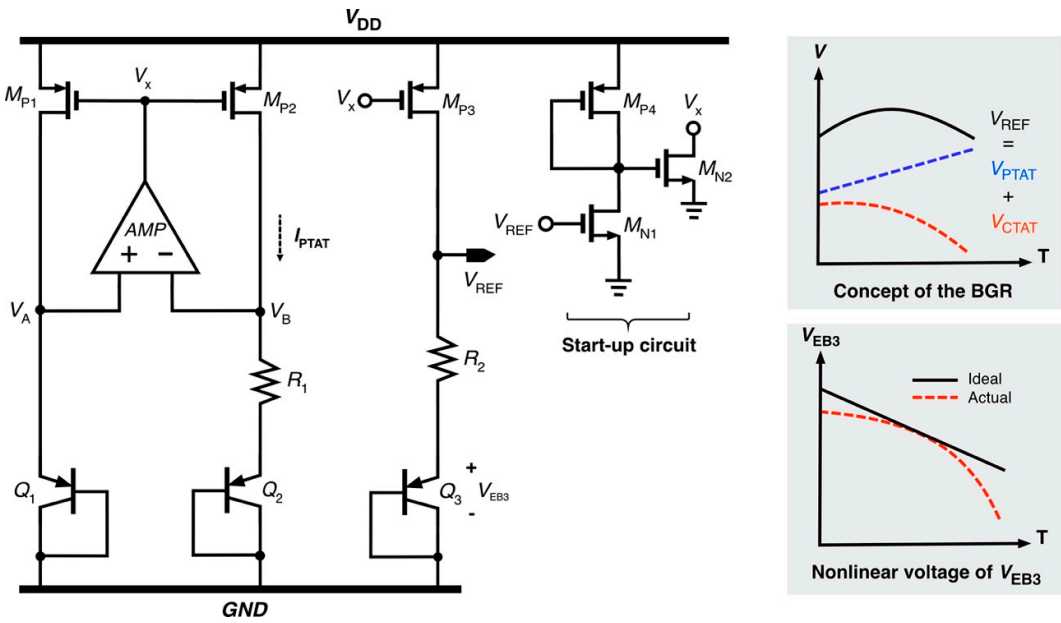


Figure 2. Conventional BGR presented in [15].

Figure 3 depicts the channel-length modulation phenomenon, in which the drain current I_{DS} of an N-metal-oxide semiconductor (NMOS) transistor is illustrated as an example. When the NMOS drain-source voltage V_{DS} increases, the length of the inverted channel region decreases, leaving a gap of non-inverted silicon called a pinch-off region. In the saturation region, I_{DS} is expressed as [15]:

$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}), \tag{3}$$

where μ is the effective mobility of carriers in the channel; C_{ox} is the oxide thickness; W and L are the transistor width and length, respectively; V_{GS}, V_{TH}, and V_{DS} are the gate-source, threshold, and drain-source voltages of the NMOS transistor, respectively; and λ is the channel-length modulation coefficient of the NMOS transistor that has the range of 0.05 to 0.005 V^{-1} [22]. The terms λ and V_{DS} that arise from the channel-length modulation result in the mismatch of I_{PTAT} between M_{P2} and M_{P3}. By considering λ and V_{DS}, Equation (2) can be modified as:

$$V_{REF} = \frac{(1 + \lambda_3|V_{DS3}|)}{(1 + \lambda_2|V_{DS2}|)}\frac{R_2 V_T \ln(n)}{R_1} + V_{EB3}. \tag{4}$$

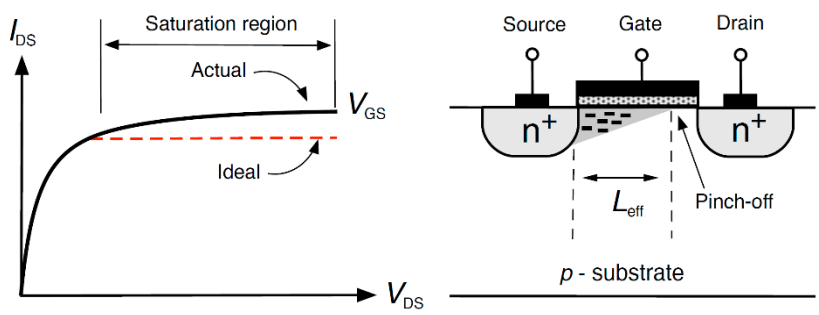


Figure 3. Drain current resulting from channel-length modulation.

Here, λ_2 is assumed to become zero because M_{P2} holds the PTAT current provided in Equation (1). Therefore, Equation (4) can be approximated to:

$$V_{REF} = \frac{(1+\lambda_3|V_{DS3}|)R_2 V_T \ln(n)}{R_1} + V_{EB3} = \frac{(1+\lambda_3|V_{DD}-V_{S3}|)R_2 V_T \ln(n)}{R_1} + V_{EB3}. \quad (5)$$

Here, note that V_{REF} is directly proportional to V_{DD} because of a finite λ. This means that a variation in V_{DD}, which indicates the rectified DC voltage (V_{REC}) with a ripple in Figure 1, can deteriorate the BGR output voltage V_{REF}.

2.2. Proposed BGR

The proposed BGR concept is depicted in Figure 4, where MOS transistors operating in the sub-threshold region are utilized to generate a high-order temperature coefficient instead of bipolar junction transistors (BJTs). To effectively compensate for the deviation in V_{REF} that arises from inconsistent V_{DD} (= V_{REC} in Figure 1) and temperatures related to V_T in Equation (5), we devised a new line regulation controller (LRC) and temperature variation controller (TVC) for the BGR circuit. First, the LRC works to compensate for the variation in V_{REF}, termed ΔV here, which is affected by the change in V_{DD} (= V_{REC} in Figure 1). Specifically, ΔV is subtracted by the LRC output voltage (V_{LR}) that has the same slope as V_{REF} (Figure 4a). As a result, the proposed BGR can output a constant V_{REF} that is insensitive to variation in V_{DD} (Figure 4c). Second, the TVC performs a function in compensating for temperature variation in BGR, thereby producing a constant V_{REF}. The MOS transistors adopted to configure the proposed BGR in this design generate a positive temperature coefficient between T_1 and T_2 (Figure 4b). This is subtracted by the TVC's non-linear output voltage V_{NL}, which has a shape similar to that of V_{REF}. Thus, the proposed BGR can generate a constant voltage over a wide temperature range (Figure 4d). Finally, the high-gain amplifier (*AMP*) adopted in Figure 5 can minimize variation in V_{REF} occurring at high frequencies by continuously tracking the ripples of the unregulated supply voltage.

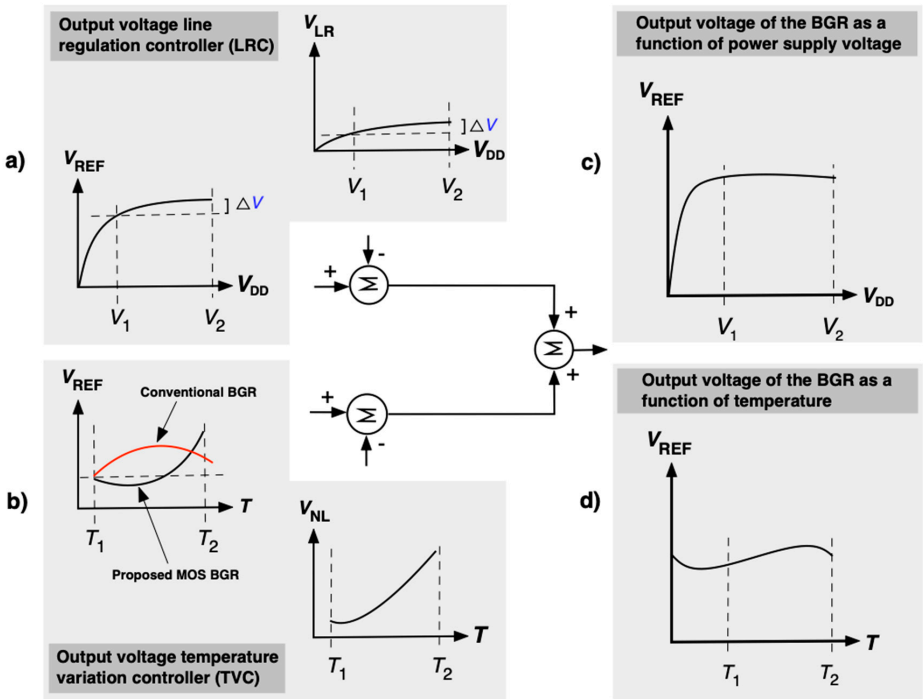


Figure 4. Proposed BGR concept (**a**) line regulation controller output voltage, (**b**) temperature variation controller output voltage, (**c**) BGR output voltage after compensation for V_{DD} variation, and (**d**) BGR output voltage after temperature compensation.

Figure 5 shows the proposed BGR circuit consisting of a start-up circuit, PTAT current generator, LRC, and TVC. The high-gain amplifier (*AMP*) in the PTAT generator is realized using a two-stage amplifier with a p-type MOS (PMOS) input differential pair. In the proposed circuit, the transistors Q_1 and Q_2 in the conventional BGR are replaced with M_{N1} and M_{N2}, both of which operate in the sub-threshold region.

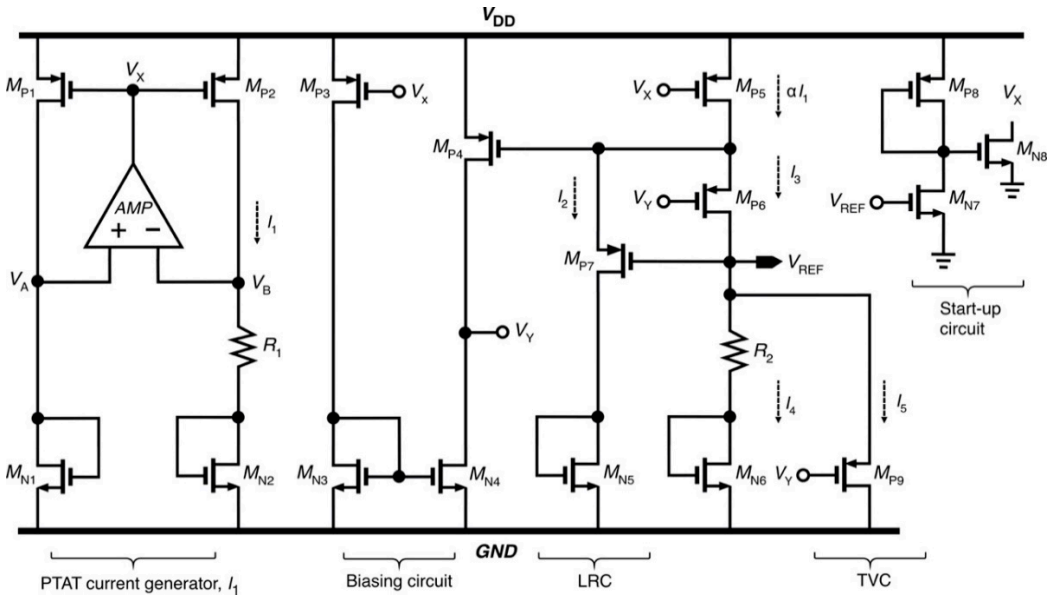


Figure 5. Proposed BGR circuit.

As a result, the drain current of M_{N1} and M_{N2} in the sub-threshold region is given as:

$$I = \mu C_o\left(\frac{1}{m}\right)\left(\frac{W}{L}\right)\left(\frac{n_1 kT}{q}\right)^2 \exp\left[\frac{q}{n_1 kT}\left(V_{GS} - V_{TH} - \frac{n_1 kT}{q}\right)\right] \times \left[1 - \exp\left(\frac{-mqV_{DS}}{n_1 kT}\right)\right], \tag{6}$$

where k is the Boltzmann constant; T is the temperature; q is the electron charge; W and L are the width and length of the transistor, respectively; μ is the effective mobility of carriers in the channel; and C_0 is an oxide capacitance. The parameters m and n_1 are the process-dependent parameters of the transistor. In the PTAT current generator in Figure 5, V_A becomes equal to V_B because of the high-gain amplifier; therefore:

$$V_{GS1} = I_1 R_1 + V_{GS2}. \tag{7}$$

From Equation (7), I_1 can be expressed as:

$$I_1 = \frac{V_{GS1} - V_{GS2}}{R_1} = \frac{\Delta V_{GS}}{R_1}, \tag{8}$$

where ΔV_{GS} expressed as (derivation of ΔV_{GS} shown in Appendix A):

$$\Delta V_{GS} = \frac{n_1 kT}{q} \ln\left[\frac{(W/L)_2}{(W/L)_1}\right]. \tag{9}$$

By substituting Equation (9) into (8), the expression for I_1 is modified as:

$$I_1 = \left(\frac{1}{R_1}\right)\frac{n_1 kT}{q} \ln\left[\frac{(W/L)_2}{(W/L)_1}\right]. \tag{10}$$

V_{REF} can be derived from the circuit in Figure 5 as follows:

$$V_{\mathrm{REF}} = \alpha I_1 R_2 - (I_2 + I_5)R_2 + V_{\mathrm{GS6}}, \tag{11}$$

where α is the ratio of the size of M_{P5} to that of M_{P2}. By substituting Equations (10) into (11) and incorporating the channel-length modulation in M_{P5}, the output voltage reference V_{REF} results in the following form:

$$V_{\mathrm{REF}} = \alpha(1 + \lambda_5|V_{\mathrm{DS5}}|)\frac{n_1 kT}{q} ln\left[\frac{(W/L)_2}{(W/L)_1}\right]\frac{R_2}{R_1} - (I_2 + I_5)R_2 + V_{\mathrm{GS6}}. \tag{12}$$

Equation (12) can be rewritten as:

$$V_{\mathrm{REF}} = V_{\mathrm{REF0}} + \underbrace{\alpha(\lambda_5|V_{\mathrm{DS5}}|)\frac{n_1 kT}{q}\ln\left[\frac{(W/L)_2}{(W/L)_1}\right]\frac{R_2}{R_1}}_{V_{\mathrm{REF1}}} - \underbrace{(I_2 + I_5)R_2}_{V_{\mathrm{LR}}}, \tag{13}$$

where V_{REF0} is the voltage reference with no effect of the channel length-modulation, given as:

$$V_{\mathrm{REF0}} = \alpha\frac{n_1 kT}{q} ln\left[\frac{(W/L)_2}{(W/L)_1}\right]\frac{R_2}{R_1} + V_{\mathrm{GS6}}. \tag{14}$$

Unlike Equation (5), Equation (13), which arises from the proposed BGR circuit, has additional terms, V_{REF1} and V_{LR}, which are used to compensate for the variation in V_{REF}. The variation in V_{REF} with respect to V_{DD} can be eliminated when:

$$\frac{\delta V_{\mathrm{REF1}}}{\delta V_{\mathrm{DD}}} = \frac{\delta V_{\mathrm{LR}}}{\delta V_{\mathrm{DD}}}. \tag{15}$$

Note that the source-drain voltage of the PMOS transistor M_{P9} is constant, and I_5 proportionally changes with V_{DD} because of the gate voltage V_{Y} of M_{P9}. In contrast, the gate terminal of M_{P7}, depending on the V_{REF} node, is always constant and the source voltage changes only when variation occurs in V_{DD}. This means that we can obtain a zero-slope V_{REF} in Equation (13) by adjusting I_2, which is determined by properly selecting the size of M_{P7}. Therefore, the proposed BGR circuit can generate a constant V_{REF} that is immune to variation in V_{DD}.

The temperature dependency of V_{REF} can be analyzed using Equation (12), which can be rewritten as:

$$V_{\mathrm{REF}} = \underbrace{\alpha(1 + \lambda_5|V_{\mathrm{DS5}}|)\frac{n_1 kT}{q}\ln\left[\frac{(W/L)_2}{(W/L)_1}\right]\frac{R_2}{R_1} - I_2 R_2}_{V_{\mathrm{PTAT}}} + \underbrace{V_{\mathrm{GS6}}}_{V_{\mathrm{CTAT}}} - \underbrace{I_5 R_2}_{V_{\mathrm{NL}}}. \tag{16}$$

We can observe the existence of two terms in Equation (16) contributing to the PTAT voltage, while V_{GS6} and $I_5 R_2$ generate the CTAT voltage and second-order curvature correction, respectively, in this scenario. The study in [23] reported that the parameter n_1 in Equation (16) is not constant; consequently, the parabolic shape of ΔV_{GS} was produced due to the variation in n_1. The output voltage variation due to n_1 is compensated by generating V_{NL} as shown in Equation (16). Referring to Figure 5, M_{P9} is biased from the CTAT voltage V_{Y}, thereby allowing additional current I_5 to flow through the transistor as the temperature increases. V_{Y} is generated across M_{N4}, and this can be explained by first considering the PTAT current I_3, which flows through M_{P6}. Accordingly, the source voltages of M_{P6} and M_{P7} and the gate voltage of M_{P4} increase proportionally with the temperature. With the fixed voltage of V_{DD}, the drain voltage of M_{P4} decreases, maintaining M_{N4} in the triode region. In the proposed design, the low voltage of V_{Y} is produced in the millivolt range such that the gate-source

voltage of M_{P9} is larger than its threshold voltage. Table 1 shows all parameters used for the proposed BGR in Figure 5.

Table 1. Parameters for transistors and resistors used for the proposed BGR circuit.

Component	Parameter	Component	Parameter
M_{P1}, M_{P2}	W = 10 µm, L = 5 µm	M_{N1}, M_{N2}, M_{N3}	W = 3.5 µm, L = 1 µm
M_{P3}	W = 20 µm, L = 1 µm	M_{N4}	W = 50 µm, L = 1 µm
M_{P4}	W = 2 µm, L = 5 µm	M_{N5}	W = 2 µm, L = 1 µm
M_{P5}	W = 50 µm, L = 1 µm	M_{N6}	W = 0.9 µm, L = 1 µm
M_{P6}	W = 5 µm, L = 1 µm	M_{N7}	W = 80 µm, L = 1 µm
M_{P7}	W = 1 µm, L = 25 µm	M_{N8}	W = 10 µm, L = 1 µm
M_{P8}	W = 25 µm, L = 1 µm	R_1	40 kΩ
M_{P9}	W = 1 µm, L = 1.5 µm	R_2	20 kΩ

3. Simulation and Experimental Results

The proposed BGR circuit was designed using Cadence IC6.1.5 and Calibre v2014 and then was fabricated in an SK Hynix 0.35-µm CMOS standard process. Figure 6 shows the BGR's microchip photograph and layout that occupied an active area of 112 µm × 60 µm. Common centroid and interdigitated layout techniques were used to decrease the process gradient effects between transistors and resistors.

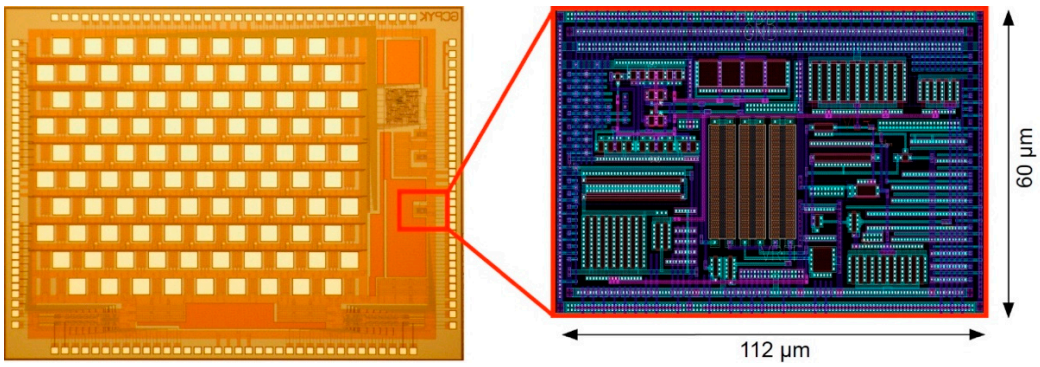
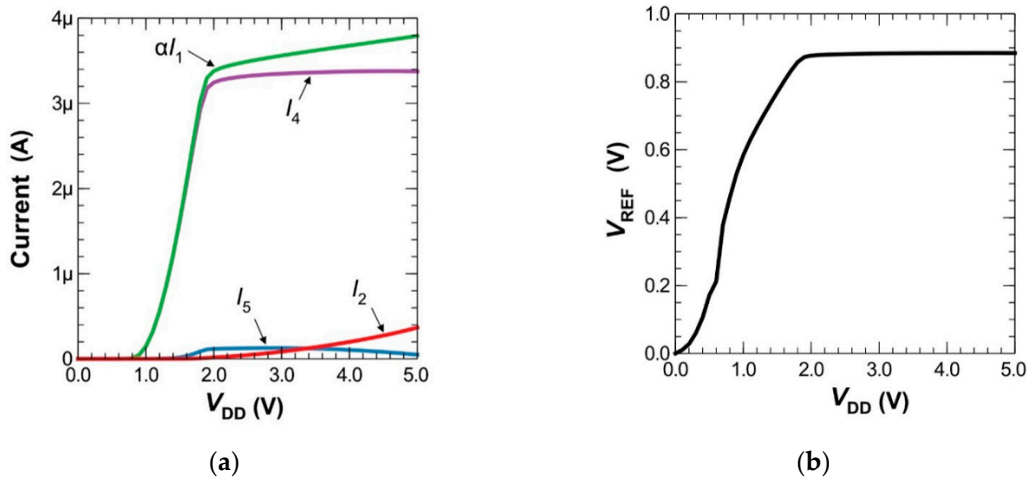


Figure 6. Microchip photograph and layout of the proposed BGR.

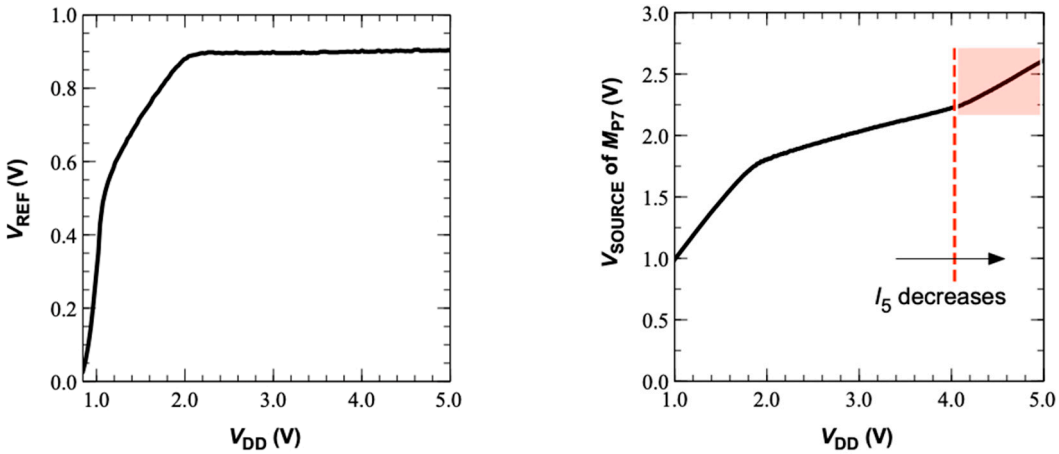
Figure 7 shows the DC response simulation results of the proposed BGR in which the supply voltage varied from 0 to 5 V. The waveforms in Figure 7 corroborate the important currents and voltages in Equations (11) to (15). As expected, αI_1 and I_2 (both are indicated in Figure 7a) increased with increasing V_{DD}, while I_5 behaved conversely to αI_1 and I_2. As Equation (13) indicates, V_{LR} was the voltage drop across R_2 and was the established voltage resulting from the sum of I_2 and I_5 in R_2. By optimizing I_2 in V_{LR}, a nearly zero-slope I_4 ($I_4 = \alpha I_1$-I_2-I_5) was produced as V_{DD} varied from 2 to 5 V (Figure 7a). The stable current of I_4 satisfied the condition stated in Equation (15); as a result, a supply-insensitive V_{REF} was generated (Figure 7b).

Using an Agilent parameter analyzer (Model 4156C), we measured V_{REF} and M_{P7}'s source voltage, which are depicted in Figure 8. As a measured result, V_{REF} had a variation of 4.8 mV over the supply voltage ranges that varied from 2.3 to 5 V. This resulted in a static supply dependency of +1.8 mV/V. The mismatch of 11.1% between the measured result of +1.8 mV/V and the simulated one of +1.6 mV/V emanated from random process mismatches [24]. Overall, the graph of V_{REF} shown in Figure 8a agreed with the simulated V_{REF} shown in Figure 7b.



(**a**) (**b**)

Figure 7. Simulated DC responses of the proposed BGR: (**a**) PTAT current through M_{P5}—αI_1, current through the line regulation control circuit—I_2, current through R_2 and M_{N6}—I_4, and current through the output voltage compensation circuit—I_5. (**b**) Output reference voltage—V_{REF}.



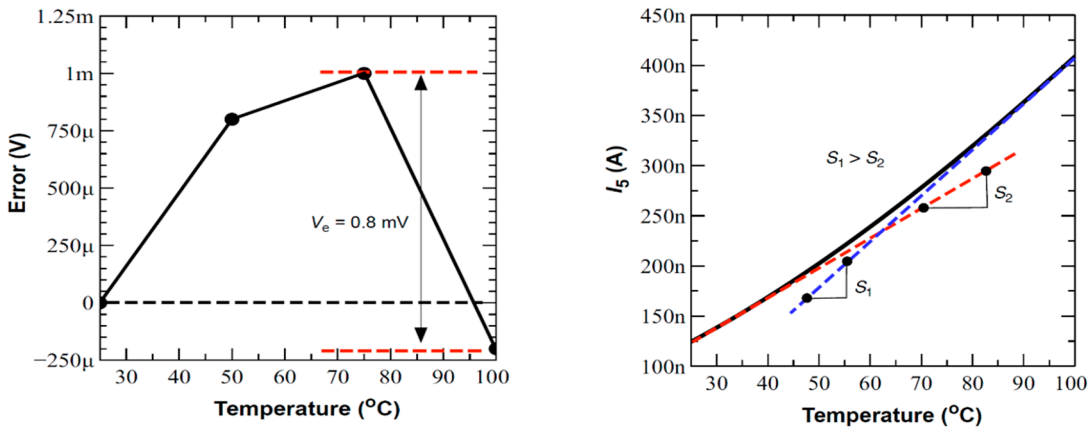
(**a**) (**b**)

Figure 8. Measured voltages of the proposed BGR: (**a**) output reference voltage and (**b**) source voltage of M_{P7}.

Figure 8b shows the non-linear increment of the source voltage of M_{P7} as V_{DD} increased, which contributed to I_2 shown in Figure 5. When V_{DD} increased to 4 V, the slope of the signal became more positive until 5 V. This can be explained by referring to the graph of I_5 in Figure 7a. When V_{DD} was 4 V, I_5 decreased, causing more current to flow through R_2, which produced a higher V_{REF}. Here, M_{P6} operated in the triode region and acted as an active resistor, thereby increasing the voltage at the source terminal of M_{P7} to maintain the same current supplied by M_{P5}. M_{P7} performed the function of sinking as much current as that caused by the increase in the source terminal voltage (Figure 8b), thereby pulling V_{REF} back to its initial voltage level.

Figure 9a,b show the measured temperature variation in the proposed BGR and the simulated temperature compensation current I_5. In this experiment, we set the operating temperature range to change from 25 to 100 °C under a power supply voltage of 3.3 V, where a maximum variation error of 0.8 mV was observed. The quadratic curve in Figure 9a verified the proposed temperature compensation technique. V_{NL}, which is shown in Equation (16), was the product of I_5 and R_2. As Figure 9b shows, the simulated I_5 increased with the temperature. Accordingly, V_{NL}, shown in Figure 4b, increased and significantly pulled the V_{REF} down at high temperatures. This was because

the slope of S_1 was higher than that of S_2 (Figure 9b). Therefore, M_{P9} (Figure 5) operated to significantly decrease the temperature variation in the reference voltage.



(**a**) (**b**)

Figure 9. (**a**) Measured error voltage of V_{REF} and (**b**) the slope S1 and S2 of the simulated I_5 as a function of the temperature.

We also measured the power supply rejection ratio of the proposed BGR, where the frequency of a sinusoidal ripple signal swept from 1 Hz to 100 kHz was directly applied to V_{DD} shown in Figure 5 without any off-chip filtering capacitors (Figure 10). This result indicated that the proposed BGR can achieve a maximum PSRR of 54 dB within a frequency band of 1 kHz. The PSRR would be further improved if we add power capacitors to pass the ripple in the supply rail to the ground.

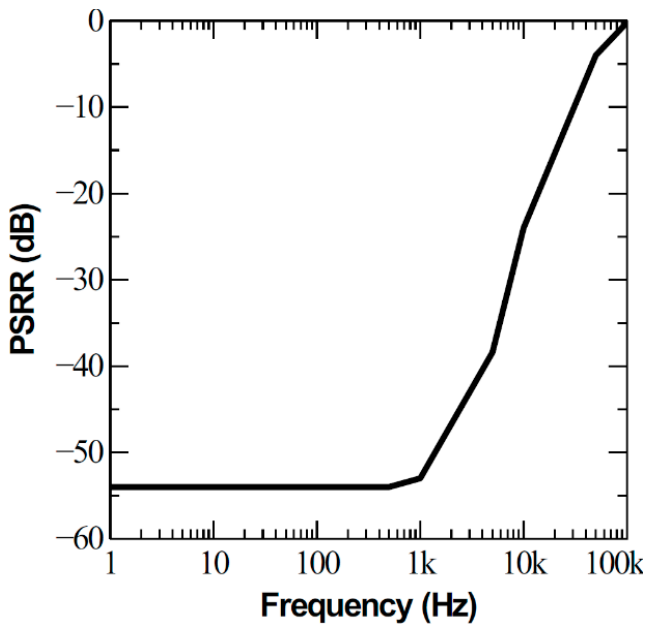


Figure 10. Measured power supply rejection ratio.

The proposed BGR chip performance was demonstrated using a verification platform of the subretinal implant shown in Figure 11a. The transmitter system is composed of a class-E power amplifier and an amplitude-shift-keying (ASK) modulator circuit that is controlled by a microprocessor unit. The power and data signal are wirelessly delivered to the subretinal prosthesis passing through the inductive link. The receiver architecture consists of a rectifier, a regulator (including the proposed

BGR circuit) to generate four different supply voltages of ±1.65 V and ±2.5 V, a demodulator to recover the modulated ASK signal, a digital controller, and a stimulator array. Here, the stimulator works to inject a biphasic current pulse into the bipolar cell inside the eyeball through a microelectrode. The power amplifier transmitted the ASK signal with a data rate of 50 kb/s, peak-to-peak magnitude of 8.6 V, and modulation index of 50%, which was modulated on a power carrier with a clock frequency of 13.56 MHz (zoomed signal in Figure 11b top); the receiver passed through the inductive coils that were placed at the distance of 0.7 cm. The received AC signals (Figure 11b middle) were rectified and fed into the proposed BGR chip. Figure 11b bottom shows a measured V_{REF} of 0.87 V, which was the same as the simulated V_{REF} shown in Figure 7b.

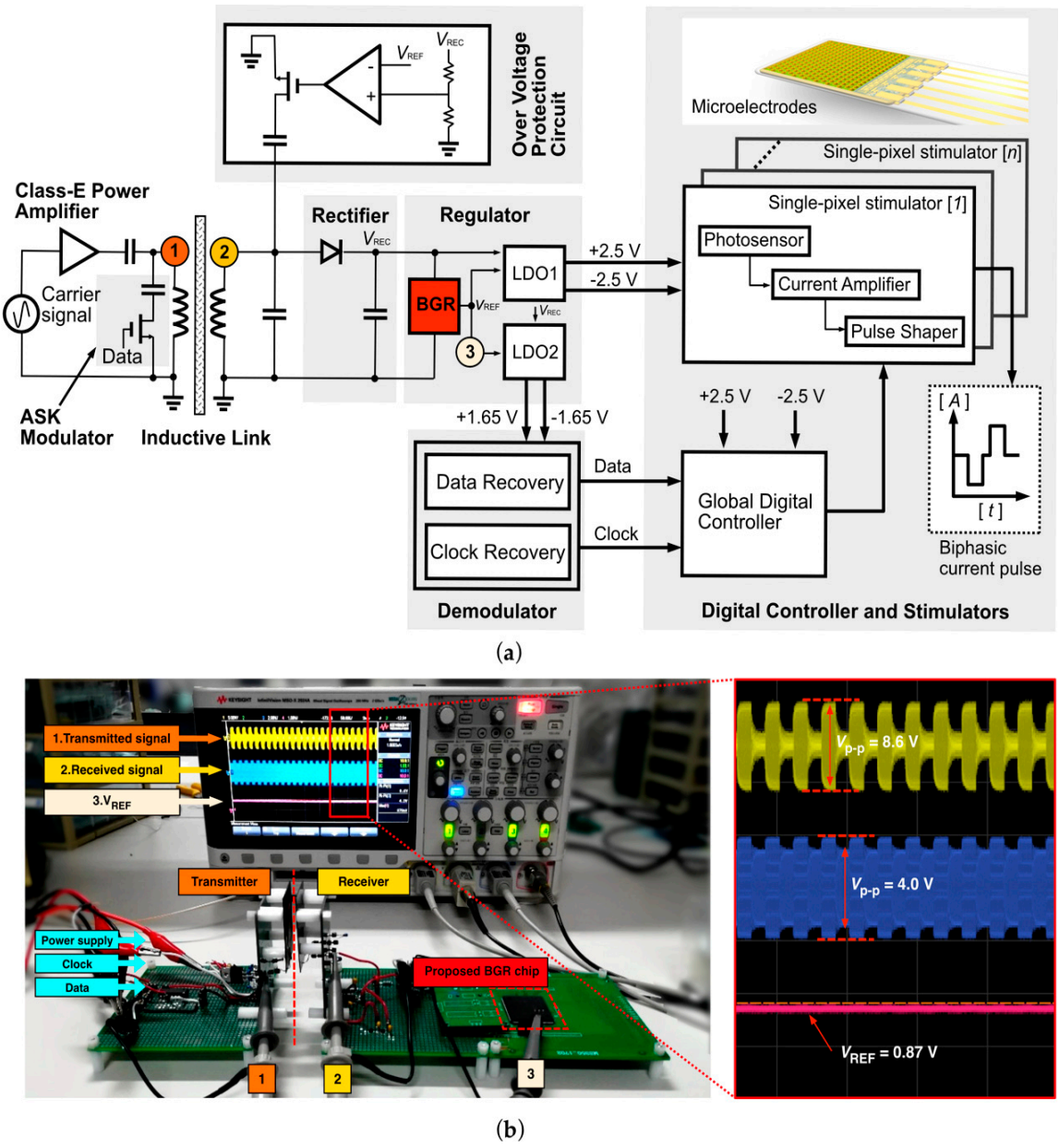


Figure 11. (**a**) Verification platform for subretinal implants using the proposed BGR circuit and (**b**) measured results of the transmitted signal, received signal, and voltage reference.

Table 2 summarizes the overall performance of the proposed BGR at a room temperature of 27 °C along with the bandgap voltage reference circuits in [18,19] for comparison.

Table 2. Electrical parameters.

Parameter	This Work	[18]	[19]
Technology	CMOS 0.35 µm	CMOS 0.18 µm	CMOS 0.18 µm
Supply voltage (V)	3.3	1.2	1.4
Line regulation	1.85 mV/V (2.3–5 V) 0.4 mV/V (2.5–13 V) [1]	0.054%/V (1.2–2)	±0.3 mV (1.1–1.8)
PSRR (dB)	−54	−84	−75
TC (ppm/°C)	11.9	3.4	4
Active area (mm^2)	0.0067	0.036	-

[1] Simulated result for the BGR shown in Appendix B.

4. Conclusions

A novel BGR circuit for wide-supply-voltage-range applications was presented in this paper. The simple implementation of the line regulation and temperature control circuits results in a small active area of the fabricated chip using 0.35-µm SK Hynix CMOS standard process. The overall size of the proposed chip is 0.0067 mm^2. The experimental results prove that the line regulation control circuit stabilizes the output voltage by sinking out some undesirable current due to the supply variation. The temperature compensation circuit clamps the output voltage regardless of the changes in the temperature ranges from 25 to 100 °C. Compared to previous research, the line regulation performance was better in a wide supply voltage range with a smaller area of 0.0067 mm^2. Therefore, we can confirm that the proposed technique in this paper is useful for wide-supply-range applications. For future research, the line regulation performance can be improved by considering the circuit discussed in Appendix B, which is applicable only to high-voltage CMOS processes. In future work, the refined BGR circuit will be fully integrated onto a single chip along with a low-voltage drop circuit, a stimulator array, and its digital controller. Presently, a power management scheme including the proposed BGR circuit is under development in order to supply an average power of 100 mW to a 2000-pixel subretinal prosthetic ASIC, which will be implanted inside the eyeball for blind people.

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Appendix A

The drain currents in M_{N1} and M_{N2} are equal:

$$I_{MN1} = I_{MN2}. \tag{A1}$$

Hence:

$$\frac{I_{MN1}}{I_{MN2}} = \frac{\left(\frac{W}{L}\right)_1 exp\left[\frac{q}{n_1 kT}\left(V_{GS1} - V_{TH1} - \frac{n_1 kT}{q}\right)\right] \times \left[1 - exp\left(\frac{-mqV_{DS1}}{nkT}\right)\right]}{\left(\frac{W}{L}\right)_2 exp\left[\frac{q}{n_1 kT}\left(V_{GS2} - V_{TH2} - \frac{n_1 kT}{q}\right)\right] \times \left[1 - exp\left(\frac{-mqV_{DS2}}{nkT}\right)\right]}. \tag{A2}$$

Taking the natural log of both sides results in the following expression, assuming $V_{GS1} = V_{GS2}$:

$$ln\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} = \frac{q}{n_1kT}\left(V_{GS1} - V_{TH1} - \frac{n_1kT}{q} - V_{GS2} + V_{TH2} + \frac{n_1kT}{q}\right) = \frac{q}{n_1kT}(V_{GS1} - V_{GS2}). \quad \text{(A3)}$$

Rearranging Equation (A3) for ΔV_{GS} ($V_{GS1} - V_{GS2}$) results in:

$$\Delta V_{GS} = \frac{n_1kT}{q} ln\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}. \quad \text{(A4)}$$

Appendix B

The improved BGR scheme shown in Figure A1 can be employed for an extreme environment that requires an unregulated supply above 5 V. The advance in a high-voltage bipolar-CMOS-DMOS (BCD) process allows one to integrate this BGR circuit on a chip. This integrated high-voltage BGR can also be applied for automotive applications operating at a voltage of 40 V in order to provide a reference voltage to data converters and power management blocks. The circuit in Figure A1 disregards its temperature dependency, and the performance of the output voltage regulation can be increased by disconnecting M_{P9} and shorting the gate terminal of M_{P6} to ground. The reason for connecting the gate terminal to the ground is to ensure M_{P6} is always in the triode region. The suggested techniques are for a system implemented using the high-voltage CMOS.

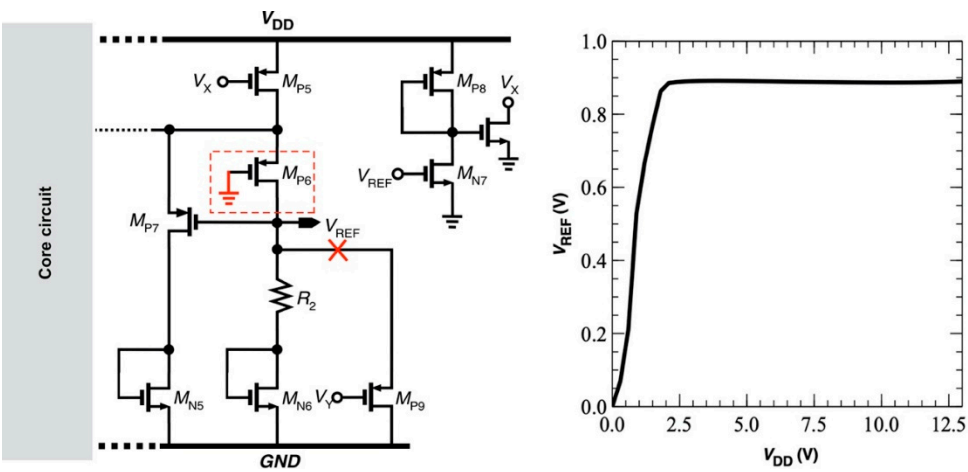

Figure A1. Improvement of the bandgap voltage reference circuit.

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