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A Sliding-Mode-Based Duty Ratio Controller for Multiple Parallelly-Connected DC–DC Converters with Constant Power Loads on MVDC Shipboard Power Systems

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Abstract: The development of powered electronic technology has made many aware of the design and control of ship power systems (SPSs), and has made medium voltage DC (MVDC) architecture the main research direction in the future. The negative impedance characteristic of constant power load (CPL) generated by the coupling of powered electronic converters will seriously affect the stability of the systems if these converters are not properly controlled. The conventional linear control method can only guarantee the small-signal stability of the system near its equilibrium point. When the operating point changes in a large range, linear control methods will be ineffective. More importantly, research for the large-signal stability of the multi-converter system with CPLs is still rarely involved. In this paper, a sliding-mode-based duty ratio controller (SMDC) is proposed for voltage regulation and current sharing of the multiple parallelly-connected DC–DC converters system loaded by CPLs. By controlling the output voltage of each converter with SMDC, large-signal stability of the coupled bus voltage is ensured. Meanwhile, proportional current sharing between the parallel converters is achieved by droop control integrated in the reference value of converter voltage. Simulation studies were conducted in MATLAB/Simulink, where two typical operating conditions, including the variation of load power and bus voltage, were designed to verify the effectiveness of the proposed method. Moreover, a traditional PID controller was used as a comparison to reflect the superiority of the former. Simulation results showed that the proposed method is able to guarantee large-signal stability of the system in the presence of large-scale variations in load power and bus voltage. The output current of the parallel converters can also be distributed in desired proportions according to the droop coefficient.

Keywords: medium voltage direct current; constant power load; voltage stability; current sharing; sliding-mode control; multiple parallelly-connected converters; DC–DC converter

1. Introduction

With the maturity of powered semiconductor technology and the development of high-energy DC equipment [1,2], the medium voltage DC (MVDC) ship power system (SPS) has gradually become the main development trend of integrated power systems for ships [3,4]. Compared with the existing AC system, DC architecture has significant advantages in achieving generator

decoupling, reducing intermediate rectifying links, and improving system operation efficiency [5]. Although control may become simpler because of the decoupling of voltage and phase, DC systems are not exempt from stability issues, which are inherently related to the need for voltage transformation through powered electronic converters [6]. There are many connection forms between the powered electronic converters throughout MVDC SPSs. When a cascading point-of-load converter is tightly regulated, it will behave as a constant power load (CPL) with negative impedance for the source converter [6]. In this case, any slight disturbance will form a positive feedback in the loop, and cause the system to constantly deviate from its original equilibrium point. As most of the loads in SPSs, including propulsion motors, radars, high-energy DC weapons, etc., are controlled by powered electronic converters [7], CPLs play an important role in system stability.

Numerous studies have been proposed for stabilizing DC–DC converters loaded by CPLs; most of the research can be divided into two categories: passive damping methods which based on hardware compensation, and active damping methods which based on control strategies [8]. Passive damping methods mitigate system oscillation by adopting appropriate damping elements, such as adding parallel resistors and LC filters, and increasing storage capacitors [6,9]. Those methods can effectively suppress system oscillation, but usually cause additional power loss, reduce system efficiency, and may lack flexibility.

By designing applicable control strategies, active damping methods can stabilize the system in a more flexible way when dealing with complex operating conditions. According to the characteristics of analysis and control, these methods can be classified into linear or nonlinear. Linear control methods are convenient for achieving bus voltage regulation around a system's equilibrium point. For example, a classical PID controller can achieve steady output voltage regulation by adding virtual resistance embedded in the proportional and derivative controller gains [6,10,11]. However, its limitation is inherent in the use of local linearization; the system can only guarantee small-signal stability.

A SPS needs to meet the requirements of complex working conditions under the premise of ensuring reliability and stability, which puts higher requirements on system's modeling and control. In order to solve the drawbacks above, nonlinear methods are needed to ensure large-signal stability. The feedback linearization method was used in [12] to stabilize a multiconverter system. With state feedback and variable substitution, the nonlinear system was transformed into a linear system; then pole placement was implemented with a PDcontroller to improve system stability. Sliding-mode control is an important approach for nonlinear control and is famous for its robustness. Zhao et al. [13] proposed a sliding-mode duty-ratio controller, which was able to stabilize the bus voltage over the entire operating range. As a systematic controller synthesis method for uncertain systems, backstepping was adopted in [8,14] to deal with the uncertainty of the load power in CPL systems. Passivity-based control provides a system global analysis method from the perspective of energy dissipation. Through energy shaping and damping injection, the stabilization of buck converters with CPLs was achieved using the passivity-based technique [15].

The control methods discussed above are mainly focused on single input to single output, when source converters are multiple and parallelly-connected; the problem to be considered is not only the stability of each individual controller, but also the current sharing between them. As mentioned above, in [12,16], authors studied the stabilization of a MVDC SPS by model reduction and feedback linearization. Although the method was proven to be effective, the requirement for model precision increased the difficulty of its application. Therefore, an offline parameter estimation method was proposed in [17] to improve the linearization and guarantee voltage stability. Synergetic control was used in [18] for an m-parallelly-connected buck converters system; the high-order nonlinear system was reduced by defining macro-variables that incorporate the state variables, and then asymptotic global stability was ensured by the analytical control law. Current sharing methods could be switched between master–slave and democratic by a simple change of control law coefficients. Su et al. [19] and Liu et al. [20] analyzed the stability of DC microgrid with multiple parallelly-connected converters loaded by CPLs without model reduction; line impedance and difference of source input were

considered. Nevertheless, the stabilization methods were mainly focused on a small-signal model. A nonlinear control method considering large-signal stability for a multiple parallelly-connected DC–DC converters system is still urgently needed.

This paper proposes a sliding-mode-based duty ratio controller for the multiple parallelly-connected DC–DC converters system with CPLs. By controlling the output voltage of each converter with a sliding-mode-based duty ratio controller (SMDC), the large-signal stability of the bus voltage is ensured. Current sharing between the parallel converters was conducted by droop control strategy, which was integrated in the SMDC coefficient. Differently from the previous research, the large-signal stability of the multi-converter system with CPLs was considered.

The rest of the paper is organized as follows. In Section 2, modeling of the multi-converter MVDC SPS and the stability issues induced by CPLs are presented. In Section 3, the sliding-mode controller design procedures for DC–DC converters are proposed, including a brief introduction of a conventional sliding-mode controller design; we also describe a SMDC for parallel converters with CPLs, estimation of the control coefficient, and a proportional current sharing strategy for the parallel converters. Finally, implementation of the duty ratio controller is described. Simulation studies are presented in Section 4, for which two types of conditions, including variation of the load power and reference bus voltage, were designed for verification of the proposed controller. Comparisons between the proposed SMDC and a traditional PID controller are presented to reflect the value of the former. Finally, conclusions are presented in Section 5.

2. MVDC SPS Modeling and Instability Induced by CPLs

As the next-generation ship integrated power system for future fleets, the MVDC SPS is expected to have the characteristics of high power density, high reliability, and high stability. It was based on the design considerations in [2] and the recommended practice for MVDC SPS from [7]. A specific model of a zonal MVDC SPS has been presented in [21]. Generators and electrical loads are connected to the longitudinal MVDC bus via powered electronic converters. Bow and stern cross-hull disconnect switches are allocated between the port and starboard MVDC bus to provide the capability of configuring a ring bus, which is able to enhance power system survivability. A SPS with such an architecture is able to maximize a system's operational capability under the constraints of limited size and weight [7].

Taking the voltage stability of the MVDC bus as our research object, the powered electronic converters can be divided into source side and load side. Meanwhile, it is presumed that bow and stern disconnect switches are controlled in XOR state to reduce the difficulty of protection. The schematic diagram of the proposed MVDC SPS is presented in Figure 1.

Consider the rectified generator as a DC voltage source; and the propulsion motors, load centers, and high-energy equipment that regulates the high bandwidth converters can be viewed as an instantaneous CPL. Then the problem can be expressed in a more general form, as a set of multiple parallelly-connected converters loaded by CPLs and resistive loads, as shown in Figure 2. The dynamics of the system can be described by the capacitor voltage and inductor current of the parallel converters in a time-average model [22].

$$\begin{cases} L_i \dfrac{di_{L_i}}{dt} = d_i V_i - v_{C_i} \\ C_i \dfrac{dv_{C_i}}{dt} = i_{L_i} - i_i \end{cases} \tag{1}$$

where

$$i_i = \frac{v_{C_i} - v_B}{r_i} \tag{2}$$

$$v_B \sum_{i=1}^{N} i_i = P_L + \frac{v_B^2}{R} \tag{3}$$

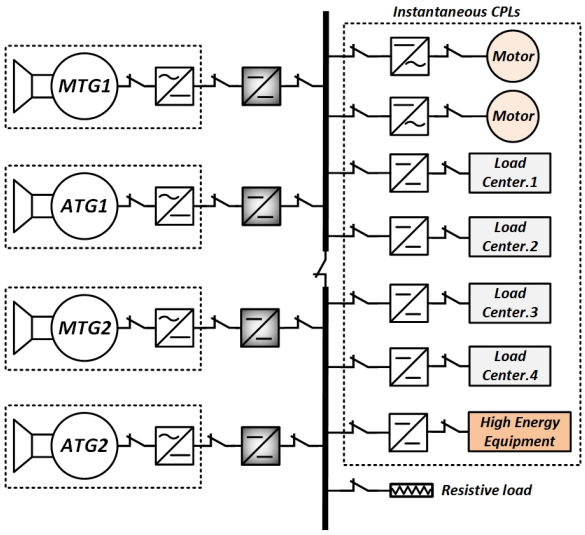


Figure 1. Schematic diagram of the proposed MVDC SPS.

The subscript i in the variables indicates the ith converter, where $i = 1, 2, ..., N$. i_{L_i}, v_{C_i}, and i_i are the inductor current, capacitor voltage, and output current of each converter,; d_i is duty ratio of each converter and the control variable of the system. v_B is the voltage of the MVDC bus, P_L is the power of the integrated CPL, and R is the resistance of the resistive load. L_i, C_i, and r_i are the inductance, capacitance, and line resistance of the ith converter.

The objective of the system is to maintain voltage stability of the MVDC bus and ensure proper current sharing among the source converters in the presence of variation of load power or bus voltage.

For such a complex system, it is difficult to consider the current coupling of the parallel converters directly. Thus, it is assumed that the output current of each converter i_i is proportional to the rated power of its power supply, which is

$$w_i = \frac{P_i}{\sum_i P_i} \tag{4}$$

Since the rated power of each generator is determined, the current sharing coefficient w_i can be viewed as a constant.

In order to illustrate the impact of the negative impedance characteristic of the CPL, we start with small-signal analysis of the system around its equilibrium point. Let $\dot{i}_{L_i} = 0$ and $\dot{v}_{C_i} = 0$; the system equilibrium point can be calculated as $\bar{i}_{L_i} = I_{L_i} = w_i(\frac{P_L}{V_B} + \frac{V_B}{R})$, and $\bar{v}_{C_i} = V_{C_i} = D_i V_i$.

Considering small disturbances in state variables [13]:

$$\begin{cases} d_i = D_i + \tilde{d}_i \\ i_{L_i} = I_{L_i} + \tilde{i}_{L_i} \\ i_i = I_i + \tilde{i}_i \\ v_{C_i} = V_{C_i} + \tilde{v}_{C_i} \\ v_B = V_B + \tilde{v}_B \end{cases} \tag{5}$$

where D_i, I_{L_i}, I_i, V_{C_i}, and V_B are the moving average values; and $\tilde{d}_i$, $\tilde{i}_{L_i}$, $\tilde{i}_i$, $\tilde{v}_{C_i}$, and $\tilde{v}_B$ are the small disturbances.

Moreover, to study the dynamics of the bus voltage v_B, the parallelly-connected source converters are considered as a whole with an integrated equivalent capacitor C_{eq}, where

$$C_{eq}\frac{dv_B}{dt} = \sum_{i=1}^{N} i_{L_i} - \sum_{i=1}^{N} i_i \tag{6}$$

Substituting (5) into (1) and (6), the small-signal model of the system becomes

$$\begin{cases} L_i\dfrac{d\tilde{i}_{L_i}}{dt} = \tilde{d}_i V_i - \tilde{v}_{C_i} \\ C_{eq}\dfrac{d\tilde{v}_B}{dt} = \sum\limits_i \tilde{i}_{L_i} + \left(\dfrac{P_L\tilde{v}_B}{V_B^2} - \dfrac{\tilde{v}_B}{R}\right) \end{cases} \tag{7}$$

Notice that the second addendum in Equation (7) is derived from the following approximation due to the fact that $V_B \gg \tilde{v}_B$:

$$\begin{aligned} \sum_i I_{L_i} - \sum_i i_i &= \left(\frac{P_L}{V_B} + \frac{V_B}{R}\right) - \left(\frac{P_L}{V_B + \tilde{v}_B} + \frac{V_B + \tilde{v}_B}{R}\right) \\ &= \left(\frac{P_L\tilde{v}_B}{V_B(V_B + \tilde{v}_B)} - \frac{\tilde{v}_B}{R}\right) \\ &= \left(\frac{P_L\tilde{v}_B}{V_B^2} - \frac{\tilde{v}_B}{R}\right) \end{aligned} \tag{8}$$

Furthermore, it is presumed that $\tilde{v}_{C_i}$ is related to $\tilde{v}_B$ by $\sum_{i=1}^{N}\tilde{v}_{C_i} = N\tilde{v}_B$; the inductance of each converter is equal to L; and the input source voltages are equal to V. Then the transfer function of the system can be obtained from (7) as

$$H_i(s) = \frac{\tilde{v}_B(s)}{\tilde{d}_i(s)} = \frac{\frac{V}{LC_{eq}}}{s^2 + (\frac{1}{RC_{eq}} - \frac{P_L}{V_B^2 C_{eq}})s + \frac{N}{LC_{eq}}} \tag{9}$$

In order to ensure the stability of the system, the poles of the transfer function need to be kept in the left half plane. That means that the power of the resistive load V_B^2/R needs to be greater than the constant power load P_L, which is impractical in an SPS, since most of the loads are tightly regulated as CPLs.

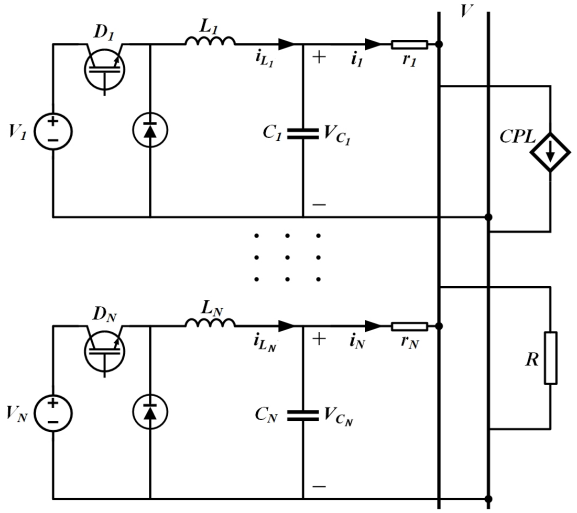


Figure 2. A multiple parallelly-connected buck converter system.

Figure 3 shows the simulation result of the multi-converter system with CPLs and resistive load. The duty cycle of each converter is controlled in open loop, the desired bus voltage is 1000 V, and the power of CPL is 25 kW. When the system simulates without resistive load, bus voltage oscillates with equal amplitude and the system is unstable. When when system simulates with $R = 1\ \Omega$, voltage oscillation quickly reduces and the system is stabilized. As the load impedance increases, the damping effect of the resistive load decreases, and the time required for stabilization increases accordingly until $V_B^2/R < P_L$.

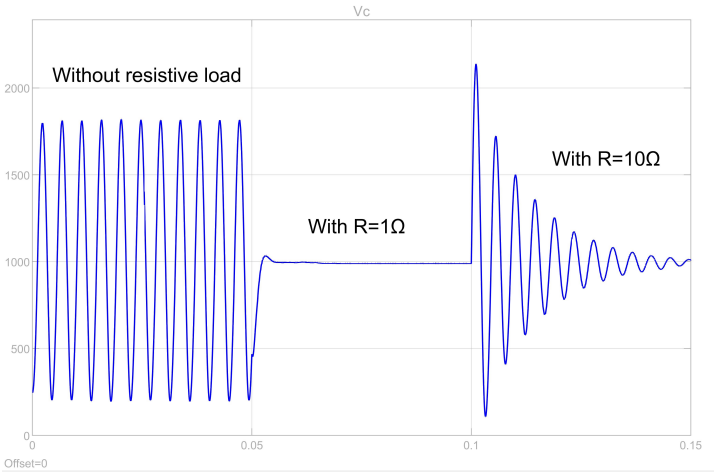


Figure 3. With or without resistive load when controlled in an open loop.

3. The Proposed Sliding-Mode-Based Duty Ratio Controller for DC–DC Converters

In order to achieve large-signal stability of the system without changing its hardware structure, a nonlinear control method is needed. As a classic method in nonlinear control, sliding-mode control is famous for its robustness, and its capability of dealing with uncertainty of parameters in the system designing process. In sliding-mode control, trajectories are forced to reach a sliding manifold in finite time and to stay on the manifold for all time thereafter. By using a lower order model, the sliding manifold is designed to achieve the control objective [23].

3.1. The Conventional Sliding-Mode Controller for the DC–DC Converter

Taking a single input single output buck converter with a constant power load as an example, a brief introduction of a conventional sliding-mode controller design procedure is presented [24,25].

Consider a special case of single converter for (1), where $N = 1$ and $v_C = v_B$. A sliding-mode surface σ for this system is designed as

$$\sigma = c_1 e_v + c_2 \int e_v dt + c_3 \dot{e}_v \tag{10}$$

where $e_v = V_{ref} - v_C$ is the tracking error of converter output voltage; c_1, c_2, c_3 are the control parameters termed sliding coefficients.

To make the system's state converge to the sliding surface through controller action, a switching control law is implemented as follows:

$$u = u_{\text{sw}} = \frac{1}{2}\left[1 + \text{sgn}(\sigma)\right] = \begin{cases} 1, & \sigma > 0 \\ 0, & \sigma < 0 \end{cases} \tag{11}$$

Define a candidate Lyapunov function as $V = \sigma/2$; then, $\dot{V} = \sigma\dot{\sigma} < 0$ must always be satisfied in order to ensure controller stability and convergence to the sliding surface. Additionally, considering (1), (10), and (11), the ranges of sliding coefficients c_1, c_2, c_3 can be determined.

Finally, the switching control law u_{sw} can be directly used as the signal for the switching circuit (e.g., MOSFET, IGBT). However, the switching frequency of the circuit will be variable, which will make the controller very sensitive to disturbances and cause great difficulties in circuit design in practical applications.

3.2. The Proposed SMDC for Parallel Converters with CPLs

In MVDC SPS, the primary objective is the stability of bus voltage. Choose the converter voltage v_{C_i} as the state variable; then let the tracking error be $\tilde{x}_i = V_{C_i}^{ref} - v_{C_i}$, where $V_{C_i}^{ref}$ is the reference value of the converter voltage. In order to have the system track $v_{C_i} \equiv V_{C_i}^{ref}$, a sliding surface $s = 0$ is defined as

$$s_i = \left(\frac{d}{dt} + \lambda_i\right)^2 \left(\int_0^t \tilde{x}_i dt\right) = \dot{\tilde{x}}_i + 2\lambda_i \tilde{x}_i + \lambda_i^2 \int_0^t \tilde{x}_i dt \tag{12}$$

The Lyapunov function of the system is defined as

$$V(s) = \sum_{i=1}^{N} \frac{1}{2} s_i^2 \tag{13}$$

Rewrite s_i as

$$s_i = a_{1_i} \dot{\tilde{x}}_i + a_{2_i} \tilde{x}_i + a_{3_i} \int_0^t \tilde{x}_i dt \tag{14}$$

To ensure the stability of the control system, the time derivative of the Lyapunov function must always be negative when $s \neq 0$; that is,

$$\dot{V}(s) = \sum_{i=1}^{N} s_i \dot{s}_i < 0 \tag{15}$$

The time derivative of s_i is

$$\dot{s}_i = a_{1_i} \ddot{\tilde{x}}_i + a_{2_i} \dot{\tilde{x}}_i + a_{3_i} \tilde{x}_i \tag{16}$$

The first-order and second-order derivative of the tracking error $\tilde{x}_i$ can be calculated as

$$\dot{\tilde{x}}_i = -\dot{v}_{C_i} = \frac{1}{C_i}(i_i - i_{L_i}) = \frac{1}{C_i}\left(\frac{v_{C_i} - v_B}{r_i} - i_{L_i}\right) \tag{17}$$

$$\ddot{\tilde{x}}_i = \frac{i_{C_i}}{r_i C_i^2} - \frac{\dot{v}_B}{r_i C_i} - \frac{1}{L_i C_i}(d_i V_i - v_{C_i}) \tag{18}$$

where

$$\dot{v}_B = \frac{1}{C_{eq}} \sum (i_{L_i} - i_i) = \frac{\sum i_{C_i}}{C_{eq}} \tag{19}$$

Substituting (17)–(19) into the expression of $\dot{s}_i$ yields

$$\dot{s}_i = \frac{a_{1_i}}{C_i}\left(\frac{i_{C_i}}{r_i C_i} - \frac{\sum i_{C_i}}{r_i C_{eq}} - \frac{d_i V_i - v_{C_i}}{L_i}\right) - a_{2_i}\frac{i_{C_i}}{C_i} + a_{3_i}(V_{C_i}^{ref} - v_{C_i}) \tag{20}$$

The equivalent control $\bar{d}_i$ of the duty ratio controller that would achieve $\dot{s}_i = 0$ is thus

$$\bar{d}_i = \frac{1}{V_i}\left[v_{C_i} + \left(\frac{L_i}{r_i C_i} - \frac{a_{2_i}}{a_{1_i}} L_i\right) i_{C_i} - \frac{L_i}{r_i C_{eq}} \sum i_{C_i} + \frac{a_{3_i}}{a_{1_i}} L_i C_i (V_{C_i}^{ref} - v_{C_i})\right] \tag{21}$$

Moreover, in order to satisfy the sliding condition despite the uncertainty in system dynamics, a discontinuous term is added to d_i as

$$d_i = \bar{d}_i + \frac{k_i}{V_i}\text{sgn}(s_i) \tag{22}$$

where sgn$[\cdot]$ is the sign function, and k_i is a positive constant. By choosing an appropriate k_i, the large-signal stability of the system can be ensured, with

$$\dot{V}(s) = \sum_{i=1}^{N} s_i \dot{s}_i = \sum_{i=1}^{N} s\left(0 - \frac{a_{1_i} V_i}{L_i C_i}\frac{k_i}{V_i}\text{sgn}(s_i)\right) = -\sum_{i=1}^{N}\frac{a_{1_i}}{L_i C_i}k_i|s_i| < 0 \tag{23}$$

3.3. Robustness of the Controller to Parameter Inaccuracy

Note that the equivalent capacitor C_{eq} in Equation (19) is an estimated value for the entire parallelly-connected system. In an ideal situation when the line resistance r_i is neglected and the source voltages are identical, C_{eq} can be calculated by $C_{eq} = \sum C_i$ as presented in [12].

In practice, there will be a certain deviation between the actual capacitance value and the theoretical value due to the influence of circuit parameters. Robustness of the controller to inaccurate estimation of the parameters is the key to controller design.

Firstly, it is presumed that $\hat{C}_{eq} = \sum C_i$ is the estimated value for C_{eq}; then, the equivalent control becomes

$$\hat{d}_i = \frac{1}{V_i}\left[v_{C_i} + \left(\frac{L_i}{r_i C_i} - \frac{a_{2_i}}{a_{1_i}}L_i\right) i_{C_i} - \frac{L_i}{r_i \hat{C}_{eq}}\sum i_{C_i} + \frac{a_{3_i}}{a_{1_i}}L_i C_i (V_{C_i}^{ref} - v_{C_i})\right] \tag{24}$$

Substituting (22) and (24) into (20) yields

$$\dot{s}_i = \frac{a_{1_i}}{r_i C_i}\left(\frac{1}{\hat{C}_{eq}} - \frac{1}{C_{eq}}\right)\sum i_{C_i} - \frac{a_{1_i}}{L_i C_i}k_i \text{sgn}(s_i) \tag{25}$$

To ensure large-signal stability of the system, $\dot{V}(s)$ needs to be negative definite. Thus $\dot{V}(s_i) < 0$ should always be satisfied when $s_i \neq 0$,

(1) If $s_i > 0$, $\dot{s}_i$ needs to be smaller than 0, which yields

$$k_i > \frac{L_i \sum i_{C_i}}{r_i}\left(\frac{C_{eq} - \hat{C}_{eq}}{C_{eq}\hat{C}_{eq}}\right) \tag{26}$$

(2) If $s_i < 0$, $\dot{s}_i$ needs to be greater than 0, which yields

$$k_i > \frac{L_i \sum i_{C_i}}{r_i}\left(\frac{\hat{C}_{eq} - C_{eq}}{C_{eq}\hat{C}_{eq}}\right) \tag{27}$$

Since (26) and (27) need to be simultaneously satisfied, k_i needs to meet the condition

$$k_i > \frac{L_i \sum i_{C_i}}{r_i}\left|\frac{C_{eq} - \hat{C}_{eq}}{C_{eq}\hat{C}_{eq}}\right| \tag{28}$$

Notice that $\sum i_{C_i} = C_{eq}\frac{dv_B}{dt}$. Considering discrete time control, the maximum gradient of the bus voltage affordable can be presented in

$$\max\left\{\frac{dv_B}{dt}\right\} = \frac{\Delta V_{max}}{\Delta T} \tag{29}$$

where ΔT is the switching cycle of the duty ratio controller, and ΔV_{max} is the maximum deviation allowed in each cycle. Moreover, it is assumed that the actual value of the equivalent capacitance C_{eq} is related to the estimation value $\hat{C}_{eq}$ by $C_{eq} = \alpha \hat{C}_{eq}$, where $\alpha \in (0, 2)$ considering a 100% estimated deviation. Thus (28) can be transformed into

$$k_i > \frac{L_i}{r_i} \frac{\Delta V_{max}}{\Delta T} |\alpha - 1| \tag{30}$$

Then the range of k_i can be determined.

3.4. Proportional Current Sharing between the Parallelly-Connected Converters

Consider the current sharing issues between the parallelly-connected buck converter system in Figure 2; Equation (2) can be reformulated as

$$\begin{aligned} v_{C_1} - i_1 r_1 - v_B &= 0 \\ v_{C_2} - i_2 r_2 - v_B &= 0 \\ &\vdots \\ v_{C_N} - i_N r_N - v_B &= 0 \end{aligned} \tag{31}$$

It can be observed that the current sharing is determined by the converter output voltage v_{C_i}, cable resistance r_i, and bus voltage v_B.

As mentioned above, the objective of system voltage regulation is to stabilize the bus voltage at a reference value, and line resistance is usually a fixed value. Therefore, the current sharing could be achieved by adjusting the reference value of v_{C_i} on the basis of bus voltage regulation, which is

$$V_{C_i}^{ref} = V_B^{ref} + i_i r_i = V_B^{ref} + w_i r_i I_{load} \tag{32}$$

where $I_{load} \equiv \sum_{i=1}^{N} i_i$, and $i_i = w_i I_{load}$. So far, a simplified load sharing can be realized by the open loop method in Equation (32), but its performance heavily depends on the value of the line resistance. Specifically, the larger the line impedance, the greater the difference between converter output voltage and bus voltage. The ratio of steady-state voltage ripple to this difference is comparatively smaller, and thus the output current is more stable. However, the reality is just the opposite: line impedance is usually small; thus, open-loop current sharing often makes it difficult to achieve the desired effect.

Therefore, a closed-loop proportional current sharing scheme is achieved by

$$V_{C_i}^{ref} = V_B^{ref} + w_i r_i I_{load} - \left(K_p e_i + K_i \int_0^t e_i dt + K_d \frac{de_i}{dt} \right) r_i \tag{33}$$

where $e_i = i_i - w_i I_{load}$. The error between the converter output current and the expected value is fed back to the original output through a PID link, so that the output current is more smooth and stable.

3.5. Parameter Selection and Implementation of the Duty Ratio Controller

The control block diagram of each duty ratio controller is presented in Figure 4. In order to ensure the stability and convergence speed of the system, the parameters of the controller need to be properly designed.

Except for the control parameters a_{1_i}, a_{2_i}, and a_{3_i}, other parameters, such as the current sharing coefficient w_i and the control coefficient k_i of the switching function, have already been determined.

Notice that a_{1_i}, a_{2_i} and a_{3_i} affect the dynamics of the sliding-mode surface and the reaching time of the controller. Meanwhile, (12) and (14) conform to the standard form of second-order linear system equation under critical damping state, $\ddot{x} + 2\omega_n \dot{x} + {\omega_n}^2 x = 0$, with $a_{2_i}/a_{1_i} = 2\omega_n$ and $a_{3_i}/a_{1_i} = {\omega_n}^2$.

Define $\omega_n = 2\pi f_{bw}$, where f_{bw} is the bandwidth and is commonly selected as 1/10 of the sampling frequency [13].

Then, the output of the proposed SMDC can be expressed as

$$d_i = \frac{1}{V_i}\left[v_{C_i} + \left(\frac{L_i}{r_i C_i} - \frac{a_{2_i}}{a_{1_i}}L_i\right) i_{C_i} - \frac{L_i}{r_i \hat{C}_{eq}} \sum i_{C_i} + \frac{a_{3_i}}{a_{1_i}} L_i C_i (V_{C_i}^{ref} - v_{C_i})\right] + \frac{k_i}{V_i}\mathrm{sgn}(s_i) \quad (34)$$

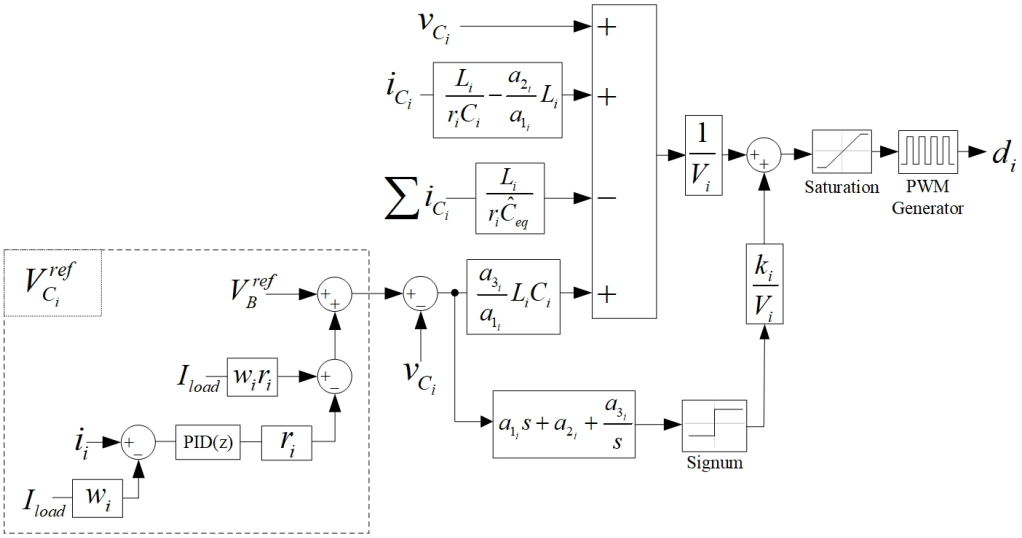


Figure 4. Block diagram of the duty ratio controller.

After the process of saturation and PWM generation, finally we can get the control signal required by the converter gate.

In practice, the difficulty of obtaining state variables should be considered. Measurement of the output voltage v_{C_i} of each converter and the bus voltage v_B is necessary. Measuring capacitor current i_{C_i} and its summation could be complicated. In the application process, we can obtain i_{C_i} by differentiating v_{C_i}.

4. Simulation

Simulation studies were performed to verify the effectiveness of the proposed algorithm. The experimental system was built in MATLAB/Simulink with the Simscape Electrical library.

As shown in Figure 5, the system consisted of four distributed sources and one integrated load; the source converters were parallelly connected via MVDC bus, and the integrated CPL is depicted by a constant current source. As resistive loads have the effect of suppressing voltage oscillation, pure CPL was considered here for higher requirements on controller design. Moreover, circuit parameters of the simulation system are presented in Table 1.

For the MVDC SPS, the control objective was to maintain voltage stability of the MVDC bus and balance load sharing of the source converters by designing an appropriate duty ratio controller which is adaptable for various operating conditions.

Two types of operating conditions, i.e., variation of load power demand and variation of reference bus voltage, were considered to verify the effectiveness of the proposed controller, as shown in Figure 6.

The parameters of the PID controller for current feedback in Equation (33) were designed as $K_p = 5$, $K_i = 10$, and $K_d = 0.01$.

The coefficient k_i of the switching function in Equation (34) can be determined by Equation (30) if we define the affordable voltage deviation in each cycle to be $\Delta V_{max} = 1V$, and then $k_1 = 200$, $k_2 = 190$, $k_3 = 180$, $k_4 = 170$.

Considering that the ratio of the rated power of each generator was 4:3:2:1, the current sharing coefficients of the parallel converters were designed as 0.4, 0.3, 0.2, and 0.1 for converters 1–4.

With $f_{bw} = 1000$ Hz, we can get $a_{2_i}/a_{1_i} = 1.256 \times 10^4$, and $a_{3_i}/a_{1_i} = 3.944 \times 10^7$. Thus the remaining control parameters can be calculated.

Furthermore, a traditional PID controller is introduced as a comparison; the controller is defined as

$$D_{PID} = K_P \varepsilon_i + K_I \int \varepsilon_i + K_D \frac{d\varepsilon_i}{dt} \tag{35}$$

where $\varepsilon_i = \left(V_B^{ref} + w_i r_i I_{load}\right) - v_{C_i}$, and $K_P = 5, K_I = 10, K_D = 0.01$.

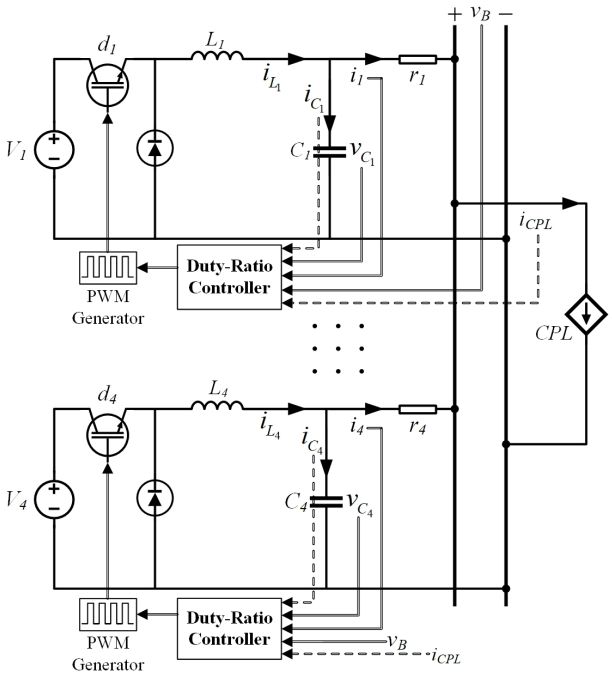
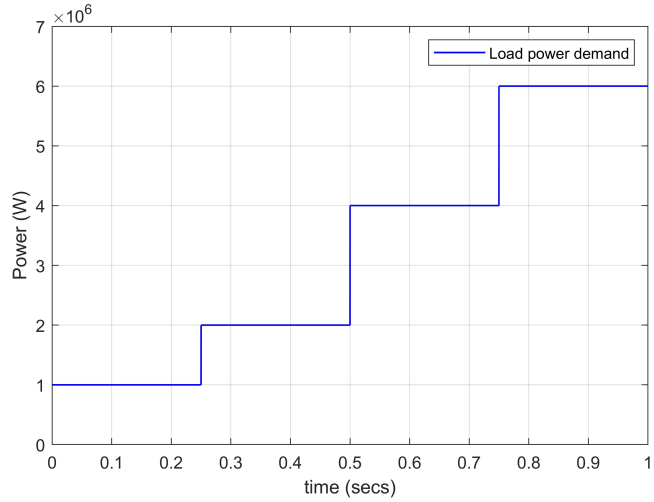


Figure 5. Circuit block diagram of the simulation system.

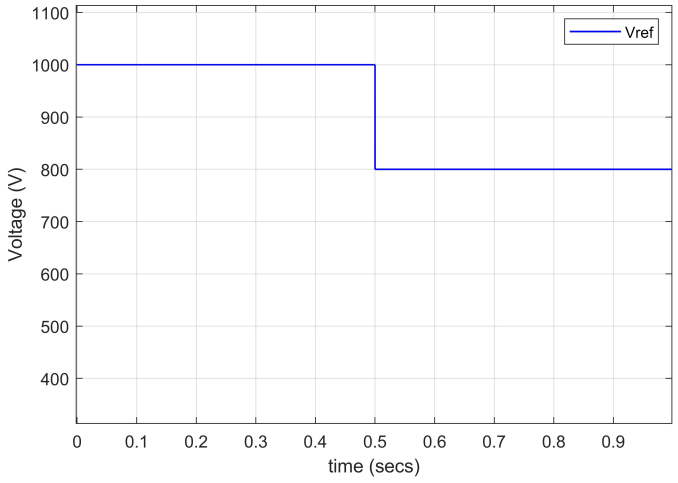
Table 1. Circuit parameters of the simulation system.

Symbol	Physical Meanings	Parameter Settings
f	sampling frequency	10 kHz
L_i	Inductance of the i_{th} converter ($i = 1, 2, 3, 4$)	2/1.9/1.8/1.7 mH
C_i	Capacitance of the i_{th} converter ($i = 1, 2, 3, 4$)	4.8/4.7/4.6/4.5 mF
r_i	Line resistance of the i_{th} converter ($i = 1, 2, 3, 4$)	0.01 Ω
V_i	Input voltage of the i_{th} converter ($i = 1, 2, 3, 4$)	1500 V
V_{ref}	Reference value of v_B	1000 V
P_{Load}	Rated power of the CPL	1 MW
I_{Load}	Rated current of the CPL	1 KA



(**a**)

Figure 6. *Cont.*



(**b**)

Figure 6. Two types of operating conditions. (**a**) Step changes in the load power demand. (**b**) Variation of the reference value of the bus voltage.

4.1. Load Power Variation

In the first case, the load power of CPL made large-scale variations during the simulation time. As shown in Figure 6a, the CPL was initially 1 MW, and then instantaneously changed to 2 MW at 0.25 s, 4 MW at 0.5 s, and finally, 6 MW at 0.75 s.

Figure 7 shows the voltage response and load sharing conditions of the multi-converter system under control of the proposed SMDC controller during step changes in CPL. As shown in Figure 7a, when load power changes significantly, the bus voltage will generate an instantaneous voltage drop and quickly return to the given reference value under the action of the SMDC controller. The transient recovery time is within 0.01 s and the steady state voltage ripple is 2 V (0.2%), which is far less than the specified value 2 s and 5% in the IEEE standard for MVDC SPS [7,26]. Figure 7b shows the output voltage response of each parallelly-connected converter. As the load current increases, the output voltage difference of each converter increases accordingly due to the use of droop control strategy.

Figure 7c,d shows the output current and output power of each converter, It can be seen that the distribution of output current and power of each source converter always maintains a ratio of 4:3:2:1, except for several transient processes.

As a comparison, Figure 8 shows the voltage response and load sharing under the control of the PID controller during step changes in CPL. As we can see in Figure 8a, the bus voltage is well controlled at initial state. Although the control accuracy is not perfect, it also meets the requirements of the IEEE std. While when the load power changes to 2 MW, the bus voltage starts to oscillate at a 2% level. When the load power continues to increase, the voltage oscillation increases accordingly, and finally, the voltage collapses.

Figure 8c shows the current sharing between each converter. Although the distribution roughly maintains the ratio of 4:3:2:1 at initial state, the current sharing process is not stable due to the insufficient accuracy of the voltage control and the absence of current feedback. Similarly, in Figure 8d, when bus voltage becomes unstable, the power sharing cannot be balanced either. Eventually, the whole system becomes unstable.

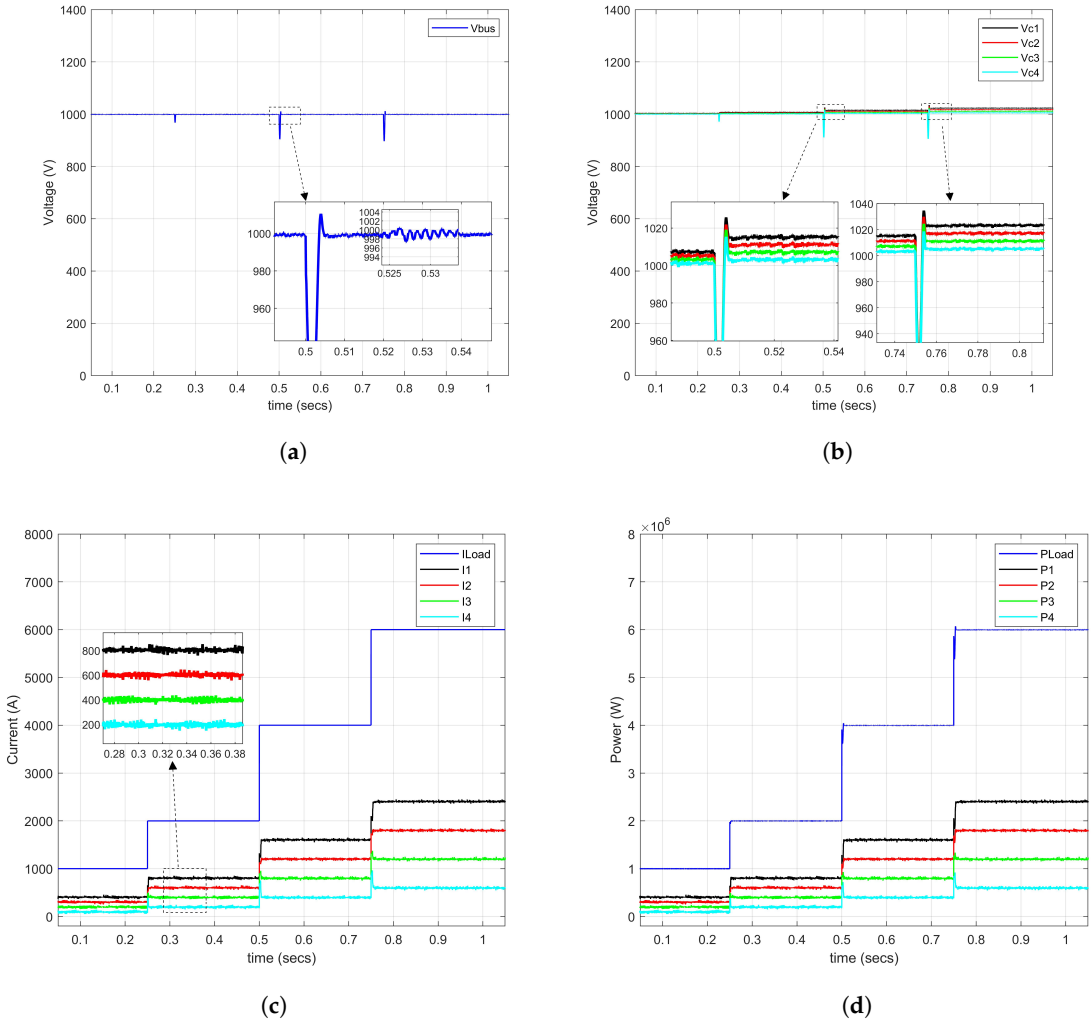
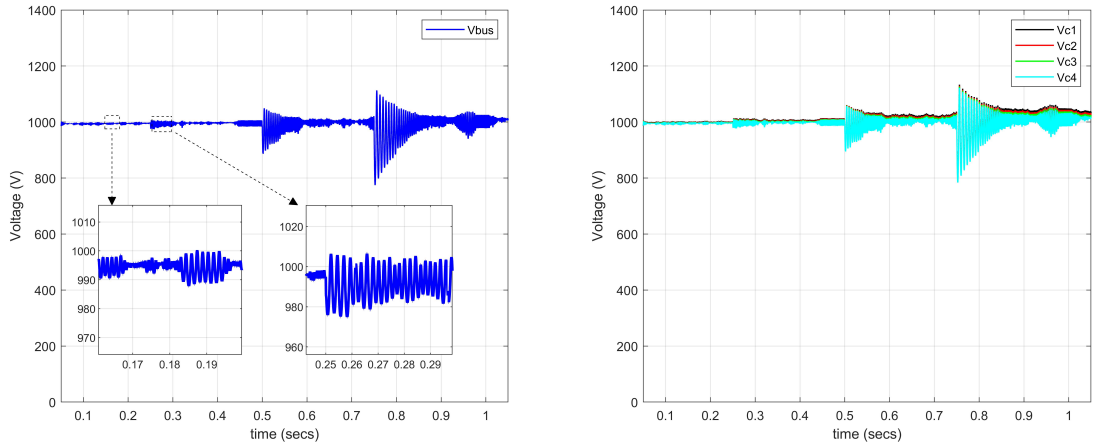
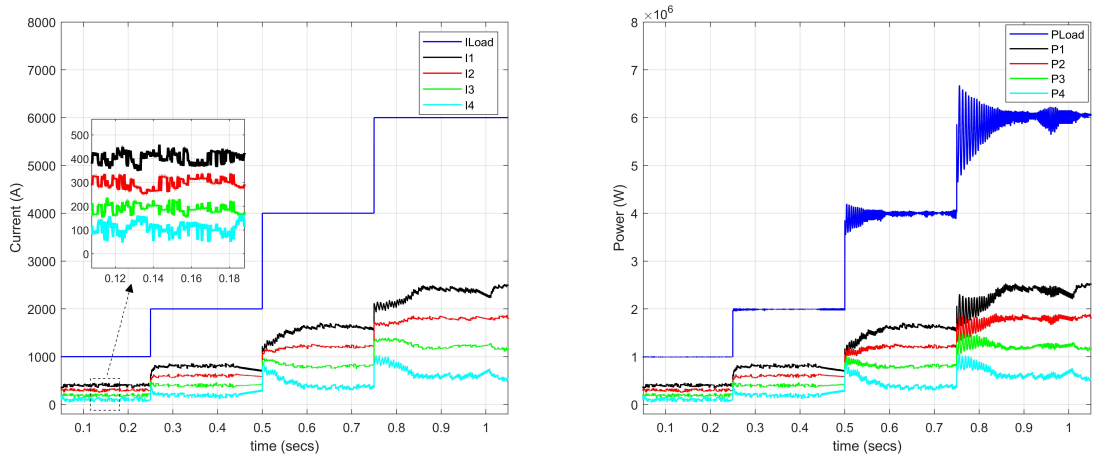


Figure 7. Voltage response and load sharing conditions under SMDC control during step changes in constant load power (CPL). (**a**) Main bus voltage. (**b**) Output voltage of each converter. (**c**) Output current of each converter. (**d**) Output power of each converter.



(**a**) (**b**)

Figure 8. *Cont.*



(**c**) (**d**)

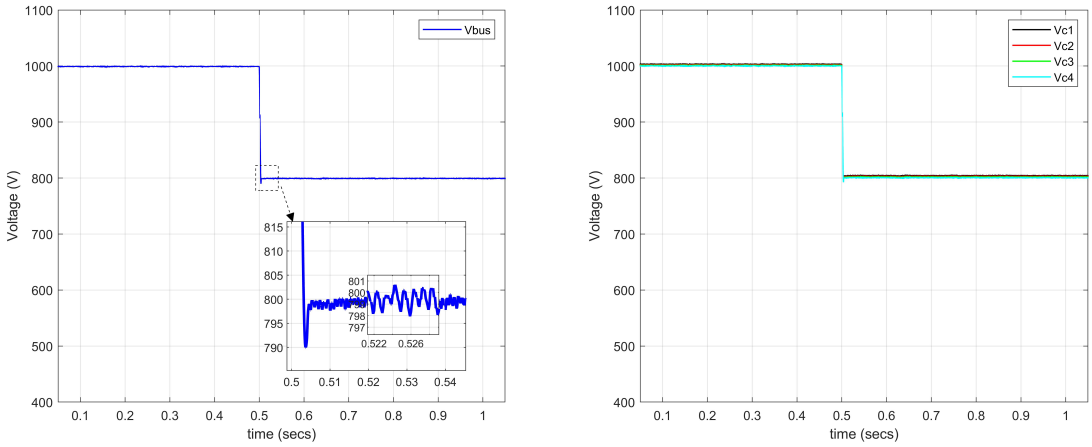
Figure 8. Voltage response and load sharing conditions under PID control during step changes in CPL. (**a**) Main bus voltage. (**b**) Output voltage of each converter. (**c**) Output current of each converter. (**d**) Output power of each converter.

4.2. Reference Voltage Variation

In the second case, the reference value of the MVDC bus changes from 1000 V to 800 V at 0.5 s, as shown in Figure 6b.

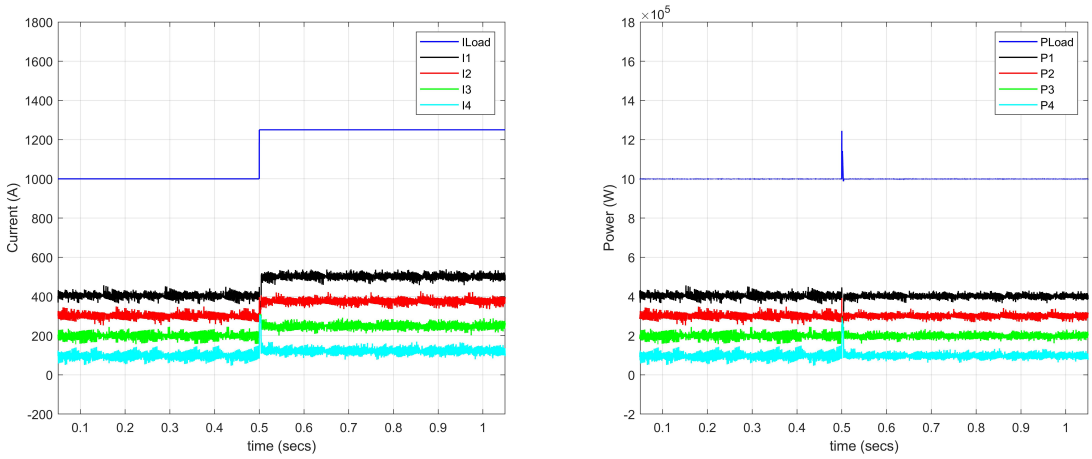
Figure 9 shows the voltage response and load sharing conditions under SMDC control during step changes in reference bus voltage. From the simulation we can see that the voltage is well controlled at all times. A more specific view is presented in Figure 9a: the transient recovery time is within 0.005 s and the steady-state voltage ripple is within ±2 V.

Figure 9c,d shows the current sharing and power sharing conditions of the parallel converters. It can be seen that except for the transient process from 0.500–0.505 s, the output current and output power of each converter is always balanced at a ratio of 4:3:2:1, and the load power of the integrated CPL is maintained at 1 MW.



(**a**) (**b**)

Figure 9. *Cont*.



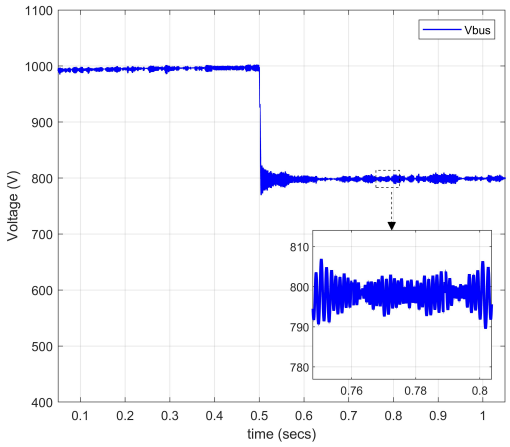
(**c**) (**d**)

Figure 9. Voltage response and load sharing conditions under SMDC control during step changes in reference bus voltage. (**a**) Main bus voltage. (**b**) Output voltage of each converter. (**c**) Output current of each converter. (**d**) Output power of each converter.

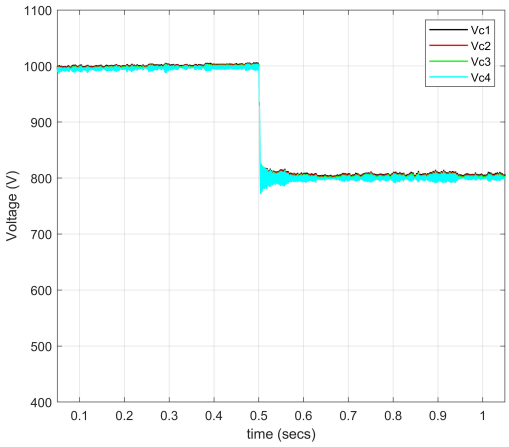
Likewise, the results of the PID controller are shown in Figure 10.

As shown in Figure 10a, the bus voltage can remain stable most of the time, but the transient recovery time is more than 0.1s, which is longer than that of the SMDC, and the steady-state voltage ripple is bigger. Furthermore, by comparing Figures 9c and 10c, we can see that the load balancing effect obtained by the SMDC is better than that of PID.

By comparing SMDC and PID under these two typical operating conditions, we can see the limitation of the linear controller, that is, it can only keep small-signal stability near its equilibrium point. By contrast, the proposed SMDC is able to stabilize the multiple parallelly-connected converter system in the presence of large-scale variations of load power or bus voltage, and realize stable and smooth current sharing in desired proportion.

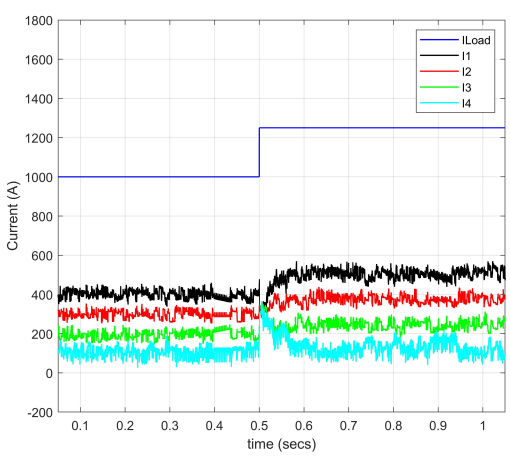


(**a**)

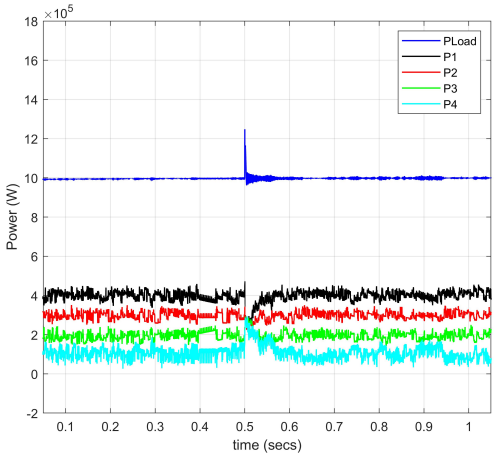


(**b**)

Figure 10. *Cont*.



(**c**)



(**d**)

Figure 10. Voltage response and load sharing conditions under PID control during step changes in reference bus voltage. (**a**) Main bus voltage. (**b**) Output voltage of each converter. (**c**) Output current of each converter. (**d**) Output power of each converter.

5. Conclusions

In this paper, a multiple parallelly-connected DC–DC converters system loaded by CPLs was analyzed; the problems of voltage stabilization and current sharing were considered. Due to the inherent negative impedance characteristics of CPL and its nonlinearity exhibited when cascaded with the source converter, a nonlinear control method is needed to ensure large-signal stability of the system. Therefore, a sliding-mode-based duty ratio controller was proposed to control converter voltage, by which large-signal stability of bus voltage is ensured. The droop control method with load current feedback is integrated in the reference value of converter output voltage for proportional current sharing. Two types of conditions, including load power variation and reference bus voltage variation, were considered in simulation studies to verify the effectiveness of the proposed SMDC. A traditional PID controller was used as a comparison to reflect the advantage of the SMDC. The simulation results show that the SMDC has better performance in face of large-scale load power variation and reference bus voltage variation, while the PID controller can only stabilize the system around the initial

equilibrium point. Meanwhile, we can get a better current sharing effect with the SMDC; the output current of the parallel converters can be well distributed in the desired proportions due to accurate voltage control and droop control with current feedback.

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Abbreviations

The following abbreviations are used in this manuscript:

MVDC	Medium voltage direct current
SPS	Shipboard power system
CPL	Constant power load
SMDC	Sliding-mode-based duty-ratio controller

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