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Impact of Submodule Faults on the Performance of Modular Multilevel Converters

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Abstract: Modular multilevel converter (MMC) is well suited for high-power and medium-voltage applications. However, its performance is adversely affected by asymmetry that might be introduced by the failure of a limited number of submodules (SMs) or even by severe deviations in the values of SM capacitors and arm inductors, particularly when the number of SMs per arm is relatively low. Although a safe-failed operation is easily achieved through the incorporation of redundant SMs, the SMs' faults make MMC arms present unequal impedances, which leads to undesirable internal dynamics because of unequal power distribution between the arms. The severity of these undesirable dynamics varies with the implementation of auxiliary controllers that regulate the MMC internal dynamics. This paper studied the impact of SMs failure on the MMC internal dynamics performance, considering two implementations of internal dynamics control, including a direct control method for suppressing the fundamental component that may arise in the dc-link current. Performances of the presented and widely-appreciated conventional methods for regulating MMC internal dynamics were assessed under normal and SM fault conditions, using detailed time-domain simulations and considering both active and reactive power applications. The effectiveness of control methods is also verified by the experiment. Related trade-offs of the control methods are presented, whereas it is found that the adverse impact of SMs failure on MMC ac and dc side performances could be minimized with appropriate control countermeasures.

Keywords: ac/dc converter for medium and high-voltage applications; modular multilevel converter; submodule fault; fault-tolerant control and operation

1. Introduction

To date, modular multilevel converter (MMC) is a preferred technology for high-power medium/high-voltage distribution and transmission applications due to ease of scalability, modularity, reduced power losses, and high-quality ac and dc side waveforms [1]. However, the use of submodules (SMs) with floating distributed capacitors in MMC results in complex internal dynamics, which necessitates the adoption of a complex multi-layer control system compared to that of conventional voltage source converters.

Typically, the common-mode current of balanced MMC consists of dc and harmonic components, and its dc component acts as a link between the dc power and the power flowing through SMs, which constitute the MMC arms. The harmonic components of the common-mode current circulate between the arms, which are widely referred to as circulating currents representing undesirable parasitic components that add losses and increase SM capacitor voltage ripples [1]. In contrast, the differential-mode currents of an internally balanced MMC are the fundamental output currents

that flow in the ac side and responsible for power transfer between the MMC arm and ac-side output circuit. Normally, the SM capacitor voltages affect the synthesis of ac and dc side voltages of the MMC, i.e., the differential- and common-mode voltages, respectively. To reduce such couplings, several control methods exist in the open literature for suppression of the circulating current and regulation of the capacitor voltages independent of dc-link voltage [2].

SM, arm, and phase-leg voltages/energies represent three important elements or layers that must be controlled to minimize MMC internal dynamic interactions during normal and abnormal conditions. To manage the voltage differences between SMs within each arm, SM voltage balancing algorithms based on either centralized sorting or distributed control are employed [3,4]. Generally, MMCs with de-coupled internal-external dynamics respond faster to active power and dc voltage set-points; exhibit reduced output voltage distortion during major transients and overall impacts of cross-modulation on ac and dc side waveforms [5,6]. Wide-ranging research efforts have been invested into high-level controllers (capacitor voltage/energy sum controllers in arm and phase-leg levels) [7,8], in which predominantly ideal (identical) passive components are usually assumed. Although a large number of SMs may reduce the adverse effects of capacitance tolerances, passive component tolerances remain a prevalence issue, particularly, for MMCs, with a relatively low number of SMs per arm as anticipated in medium-voltage (MV) applications. Therefore, it is imperative to account for uncertainties due to passive component tolerances during MMC design and maintenance stages [9–12]. In this line, the adverse effects of asymmetrical cell capacitances on the ac output voltage of MMC that employs three-level flying capacitor SMs have been identified when the energy-based balancing approach was used in the high-level controllers that regulate the MMC internal dynamics [10]. The work in [11] has revealed the inducement of fundamental frequency ripple in the dc-link current of the MMC with asymmetrical arm inductances and proposed a voltage-based active control method to suppress the induced fundamental frequency ripple from the dc-link current.

On the other hand, a fault that happened in MMC SMs may cause operational issues ranging from distortion of ac and dc side voltages and currents to total disruption of power transfer. Methods for SMs fault detection and identification are proposed in [13–15], while increased MMC resiliency to SM faults through the concept of redundant SMs are discussed in [16] and [17]. With regard to the SM fault tolerance capability of the MMC, several SM-fault control methods have been discussed [18–21]. Two approaches are proposed, and the respective features are presented in [18]. The fundamental common-mode current ripple during SM faulty has been claimed in [19], and a dq-frame-based control method is proposed. However, this method depends on phase lock-loop for the ripple. Further research in [20,21] has proposed proportional resonant (PR) based control methods to suppress the fundamental ripple, but the control effects on the overall operation are not analyzed. Besides, in most previous works, the predominant assumption is that the number of faulty SMs is less than the number of redundant SMs or within a hot redundancy configuration, while the extreme condition, in which the number of faulty SMs is larger than the redundant SMs, is seldom discussed. In these cases, SM capacitor voltages would be increased, within a safe margin, for continuous operation.

Based on the preliminary findings in [22], this paper considered the adverse effects of MMC asymmetry caused by SM fault on both dc and ac sides when mainstream balancing control methods are employed. The differential-mode voltage balancing control method reduces the fundamental component in the common-mode and dc-link currents of the MMC with significant passive component tolerances. However, its effectiveness is limited since it is not direct control but via minor ripple injection, and its control objective is to nullify the differential-mode capacitor voltage sums. Considering the random nature of the passive component tolerance distribution within one phase-leg of an MMC-based power conversion system, the proportional-resonant (PR)-based controller that operates at the fundamental frequency was studied to suppress any fundamental circulating component that may arise in the three-phase common-mode currents. Comparatively, control effects on both ac and dc side performances were investigated in this paper. This paper is organized as follows. Section 2 provides a brief review of MMC operation fundamentals, and Section 3 discusses the issues that

arise due to component tolerance and SM fault. Section 4 introduces the internal control methods against internal imbalance. Section 5 verifies the effectiveness and assesses the performances of control methods. Finally, Section 6 summarizes this paper.

2. MMC Basic Operation

Figure 1 shows a three-phase half-bridge MMC, with V_{dc} and I_{dc} representing dc bus voltage and current, respectively. Each phase-leg consists of upper and lower arms, and each arm comprises a reactor with nominal inductance $\overline{L_{ARM}}$ and N series-connected SMs. Each SM consists of a capacitor with nominal capacitance $\overline{C_{SM}}$ and an IGBT-based half-bridge circuit. The term circulating current represents the ac component of the common-mode current, i_{cm}. The i_{cm} is mainly caused by cross-modulation of the upper and lower arms or, simply, the interaction of the arm voltages, currents, and switching functions. Strategies of the inner-arm SM voltage balancing and the second-order circulating current suppression have been widely discussed [2–5]. Figure 1 also shows a generic MMC connected into the ac grid through an interfacing transformer.

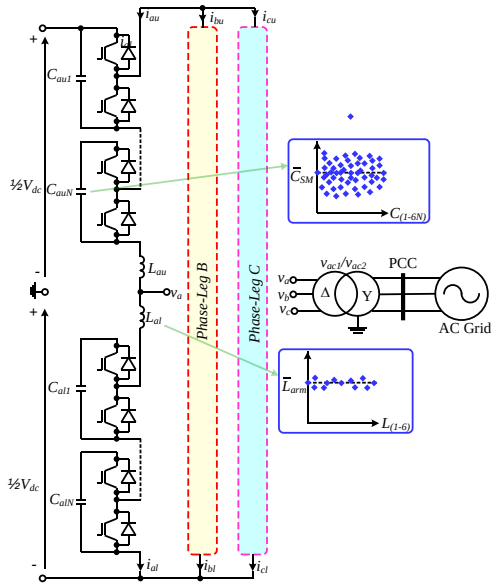

Figure 1. Modular multilevel converter (MMC) topology configuration.

Under the ideal condition, each MMC arm has an equivalent capacitance C_{ARM}, which can be calculated as:

$$C_{ARM} = \frac{\overline{C_{SM}}}{N} \tag{1}$$

As the arm equivalent capacitance is alternatively charging and discharging, the MMC internal power can be dynamically balanced as it transfers power between ac and dc sides.

Figure 2 visualizes the MMC power paths, which can be divided into ac and dc loops. The dc loop depicted in Figure 2 represents the conduction path through dc output to MMC phase-leg, in which the common-mode current of each phase follows, which consists of ac and dc components ($i_{cm} = I_d + i_h$, where I_d and i_h are dc and harmonic components of i_{cm}). In a three-phase MMC, the dc components of the common-mode currents of the phase legs add to the dc-link currents that flow in the positive and negative dc poles at the upper/positive and lower/negative dc nodes. In this way, the MMCs exchange power with the dc side. The ac components of the common-mode currents of the MMC phase legs are predominantly second-order harmonics and add to zero at upper and lower dc-link nodes; they represent parasitic currents, which increase the MMC SM capacitance requirement for a given voltage ripple and semiconductor losses. In contrast, the depicted ac loop represents

the conduction path through which each MMC phase-leg exchanges active power with ac side and fundamental frequency ac current flows. The output phase current represents the differential-mode current; for example, for a phase A, $i_a = i_{au} - i_{al}$, where i_a, i_{au}, and i_{al} are output and upper and lower arm currents. In a balanced three-phase MMC, the fundamental frequency components of the currents add to zero at positive and negative dc nodes; while in an internally unbalanced MMC with asymmetrical ac and dc loops in the phase-legs, the asymmetries introduce zero and negative sequence fundamental frequency components in the common-mode currents of the phase-legs, which may leak into dc side and appear as fundamental frequency ripples in the dc current.

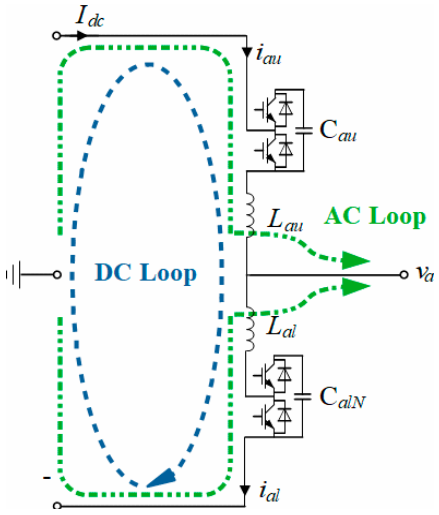

Figure 2. Diagram of MMC internal dynamics (phase A).

3. Internally Unbalanced MMC

The manufacturing process introduces significant inaccuracies and deviations in the values of passive components from the nominal. Therefore, instead of ideal and identical parameters, the practical MMC passive parameters can be assumed as a random distribution shown in Figure 1, with the inherent tolerances included. Commonly, circuit parameter tolerances are neglected to facilitate modeling, analysis, and controller design of complex energy conversion systems, such as the MMC. Nonetheless, it is essential to take countermeasures to neutralize any potential adverse implications of circuit parameter tolerances on MMC performance [10], for the following reasons:

1. Because of a large number of passive components, parameter uncertainties due to manufacturing tolerances are inevitable and vary with several factors, including lifetimes.
2. Although the SM capacitor voltage balancing controller or algorithm distributes the total dc voltage across each arm equally amongst the SM capacitors, the switching devices of each SM only withstand an SM capacitor voltage. However, asymmetry due to parameter tolerances or SM faults may cause unequal power contribution and voltage distribution between the MMC arms. Thus, the current and voltage stresses in the switching devices and heat distribution may differ between arms.
3. Besides, capacitance and inductance differences between arms may actuate unbalanced fundamental frequency common-mode currents, which tend to leak into the dc side and appear as an undesirable current ripple in the dc current [23]. This is mainly because of the inherent power balancing mechanism of the MMC operation: in order to keep ac-dc power balance, different capacitor charge/discharge rate is induced, leading to fundamental frequency current difference between upper and lower arms.

The imbalance between upper and lower arms of one phase-leg, created by SM faults on the MMC internal dynamics, can be explained with the aid of the ac and dc loop described earlier. It is

well-established from the literature that the incorporation of redundant SMs can protect active and passive components of SMs from damage due to excessive over-voltage. However, with the hot redundancy approach, which is extensively studied, the post-fault voltage stresses on the MMC switching device and SM capacitor may differ from the pre-fault condition [18]. When an SM fails, it will be bypassed, and MMC continues to operate as normal, following a brief period of transients. For the simplicity of the analysis, this paper assumed that all the N SMs in the MMC arms are in use, and N_F SMs become faulty. Therefore, the equivalent arm capacitance is:

$$C'_{ARM} = \frac{\overline{C_{SM}}}{N - N_F} \tag{2}$$

Hence, 10% of the total number of SMs in a particular arm have failed and bypassed, leading to an 11% increase in the arm equivalent capacitance; hence, this scenario resembles an extreme case of passive component tolerances. Therefore, the consequences of SM faults are similar to that caused by passive components' tolerances, in which SM fault appears as a vertical asymmetry between the upper and lower arms of the same phase-leg and horizontal asymmetries relative to the healthy phase-legs. The work in [23] has demonstrated that the horizontal asymmetries between the phase-legs have negligible effects on dc-loop dynamics during steady-state, even though the phase-legs equivalent capacitances store different energies. In contrast, the vertical asymmetry has several operational implications, specifically, contamination of common-mode current by circulating current at the fundamental frequency, which increases semiconductor losses and contributes to the inducement of fundamental frequency ripple on the dc side, and reduced exploitable modulation index range, which generates the differential-mode voltage in the ac output. Throughout this paper, the sum and difference of arm capacitor voltage sums are referred to as the common- and differential-mode capacitor voltage sums of each phase-leg, respectively. For example, the common- and differential-mode capacitor voltage sums for phase-leg A are $\sum V_{c,a} = \sum_k^N V_{c,au} + \sum_k^N V_{c,al}$ and $\Delta V_{c,a} = \sum_k^N V_{c,au} - \sum_k^N V_{c,al}$, respectively, where $\sum_k^N V_{c,au}$ and $\sum_k^N V_{c,al}$ are phase-leg A upper and lower arm capacitor voltage sums.

4. MMC Internal Dynamics Controllers

Figure 3 shows a generic depiction of the MMC control structure, which consists of internal dynamic and external system-level controllers, and modulator that generates the gating signals for the SMs. The internal dynamic controllers of the MMC operate at three levels, namely, SM, arm, and phase-leg. These controllers ensure adequate distribution of voltage stresses across the followings: SMs semiconductor switches and capacitors; upper and lower arms, to avoid narrowing of modulation index control range; phase-legs, to enable SM capacitor voltage regulation independent of the dc-link voltage and to prevent the development of ac and dc circuit currents between the phase-legs. In other words, the latter reduces interactions between MMC internal and external dynamics. The ac output (external) controllers include the following: positive and negative sequence separation stage; outer system-level controllers that regulate active power or dc voltage and reactive powers or ac voltage; inner positive and negative currents controllers that generate the principle modulation functions for the arms.

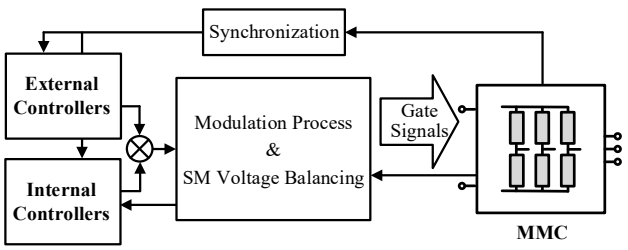

Figure 3. Diagram of MMC control structure.

Although theoretically, each MMC arm exchanges zero average power during one period, tolerances of the passive components lead to different levels of background energy stored in the SM capacitors, and presentation of different impedances by the MMC arms. Thus, the instantaneous power of the passive components deviates from their nominal values at the fundamental frequency. As voltage (or energy) of each arm is usually controlled by corresponding inter-arm balancing controllers, (also known as differential-mode capacitor voltage sum controller or vertical controllers), the power imbalance due to asymmetries of conduction paths will be compensated largely by injection fundamental frequency circulating currents into the common-mode loops. The asymmetries of energy levels and conduction path impendence lead to unequal contributions from the vertical balancing controllers of three phase-legs; hence, unequal fundamental currents in the common-mode loops. Recall that the vertical balancing controllers prioritize nullification of vertical voltage/energy asymmetry between the upper and lower arms over unintended consequences of injection odd-order harmonics into the common-mode currents [23]. Without a dedicated controller, a vertical asymmetry of any kind results in unbalanced fundamental common-mode currents in three phase-legs and thereby the development of fundamental frequency oscillations in the dc-link and increased semiconductor losses.

Two internal controllers to be assessed are:

4.1. Scheme-A

Conventionally, the common- and differential-mode capacitor voltage sums are controlled equally across all three-phase legs using the internal dynamic controllers shown in Figure 4. The regulation of average SM capacitor voltage (common-mode capacitor voltage sum) is achieved through the manipulation of common-mode current in conjunction with the common-mode capacitor voltage/energy sum controller (where $\sum_{j=1}^{N} V_{cj}$ and $\sum_{j=1}^{N} E_{cj}$ represent the common-mode capacitor voltage and energy sums per phase-leg, respectively). To eliminate the steady-state dc mean value error and suppress the 2ω circulating current, a PIR (proportional integral and resonant) controller with a resonant frequency at 2ω is adopted. This controller decouples SM capacitor voltage from the input dc-link voltage, hence the synthesis of the ac voltage from the dc-link voltage. A differential-mode capacitor voltage (or energy) sum control regulates arm active power using fundamental common-mode current injection, with another resonant frequency ω component. Since the performances of energy-based internal dynamic control methods deteriorate as the stored energies in the arms vary rapidly with SM capacitance tolerances [22], the voltage-based balancing method shown in Figure 4 was adopted in this paper. From this point, it is referred to as control scheme A. From the ac side point of view, this method is able to maximize the use of full modulation index control range for the synthesis of the arm and ac output voltages, as determined by the minimum arm capacitor voltage sum. However, the by-product of this method is slightly higher fundamental current ripples in the dc loops and in the dc-link current.

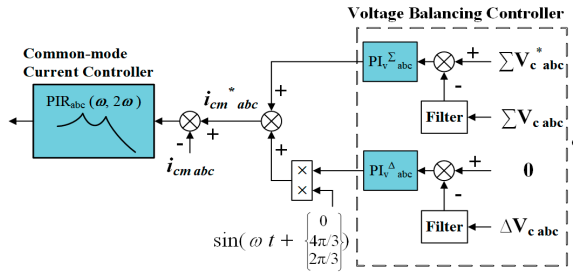

Figure 4. Diagram of the common- and differential-mode capacitor voltage sum controller (Scheme-A) [23].

4.2. Scheme-B

Since SM faults in one or multiple arms of the MMC lead to vertical and horizontal capacitance asymmetries, with the former cases, fundamental frequency ripples to appear in the common-mode currents, and a direct fundamental current ripple suppressing method (referred to as Scheme-B)

displayed in Figure 5 is proposed. Instead of targeting differential-mode capacitor voltage sums, the Scheme-B suppresses the fundamental frequency ripple in the common-mode current directly. This method uses an additional fundamental frequency PR controller to cancel the fundamental components in common-mode currents, thereby suppressing the dc-link current ripple, which is predominantly of fundamental frequency in the internally asymmetric MMC. However, the potential disadvantage of the proposed direct suppression of fundamental circulating current method is that the modulation-index control range might be reduced. In this method, the MMC arm with a smaller capacitor voltage sum would limit the ac voltage synthesis. Therefore, a dedicated design margin is needed to enable full exploitation of the modulation index control range in practical MMC under all operating conditions. Figure 6 illustrates potential impact of unequal or imbalance upper and lower capacitor voltage sums in the same phase-leg on modulation index control range (synthesis of the maximum arm or output ac voltage), assuming the SM capacitor of voltage sum of each arm is regulated at least at V_{dc0}, where V_{dc0} represents the nominal dc-link voltage. Notice that under the ideal case of internally balanced MMC, when the upper and lower arm voltages are limited by the nominal input dc-link voltage V_{dc0}, the maximum peak output phase ac voltage is $\frac{1}{2}V_{dc0}$ for sinusoidal references and can rise to 0.577 V_{dc0} ($V_{dc0}/\sqrt{3}$) with 3rd harmonic injection. Notice that when upper and lower arms of a phase-leg suffer from unequal SM capacitor voltage sums, the arm with the least capacitor voltage sum defines the maximum safe limits for the synthesis of the output ac voltage. Should the arm with the largest capacitor voltage sum successfully synthesizes the requested voltage set by its modulation function, and the arm with the least capacitor voltage sum fails to synthesize the target voltage, the common-mode voltage that the phase-leg presents at the dc side may contain fundamental component besides the dc voltage. These may further exacerbate fundamental frequency ripples in the dc current. Besides, the imbalance in the SMs capacitor voltage sums, particularly, between the upper and lower arms, may appear as an imbalance in the differential-mode voltages of the phase-legs, which resemble three-phase output voltages. In Figure 6, $v_{arm,u0}$ and $v_{arm,l0}$ denote the upper and lower arm voltages in the ideal case, corresponding to balanced upper and lower SMs capacitor voltage sums; $v_{arm,u}$ and $v_{arm,l}$ stand for the upper and lower arm voltages under unequal upper and lower SMs capacitor voltage sums, in which the upper arm has the least SMs capacitor voltage sum and limits the maximum attainable ac voltage.

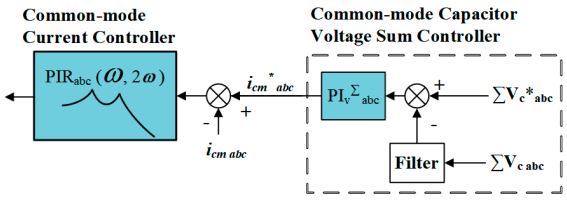

Figure 5. Diagram of internal control structure against inter-arm parametric imbalance (Scheme-B) [23].

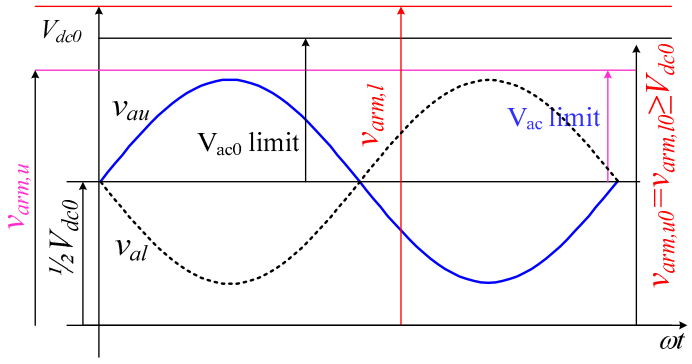

Figure 6. Arbitrary arm voltage of the MMC that suffers from unequal capacitor voltage sums in the upper and lower arms of the same phase-leg.

In summary, since trade-offs exist, it is important to conclusively establish and quantitatively evaluate the performance of the above methods, under SM faults or tolerances conditions. The two trade-off cases are:

1. Prioritization of balanced capacitor voltage sums of the arms over the suppression of fundamental frequency current into the dc loops of three phase-legs;
2. Prioritization of suppressing fundamental frequency currents in the dc loop over active balancing of the capacitor voltage sums of the upper and lower arms.

5. Simulations

This section presents detailed MATLAB-based simulations that assess the MMC performance during SM faults for two different implementations of internal dynamic controllers described earlier, i.e., control schemes A and B, considering two distinct operating points. The simulated MMC models include the following external controllers: active and reactive powers; positive and negative sequence currents. Two control methods for internal dynamics considered in this section are:

1. Scheme-A consists of common- and differential-mode capacitor voltage sum balancing controllers, which include a circulating current suppression controller.
2. Scheme-B consists of common-mode capacitor voltage sum control in conjunction with the proposed direct fundamental circulating current suppression. Circulating current suppression controller is also included.

Sorting-based SM level voltage balancing method is adopted, and modulators based on level-shifted pulse width modulation and phase disposition carriers are used to generate the gating signals for the SMs.

5.1. Impact of SM Faults on MMC Operation for Different Control Schemes

This subsection presents time-domain simulations that illustrate the behaviors of the 20-cell MMC in Figure 7 under SM faults. The parameters of the simulated MMC are listed in Table 1. In this study, two faulted SMs represented 10% of the total SMs per arm, and the SM fault was applied at the upper arm of phase-leg A at 0.4 s, and the two faulty SMs were bypassed.

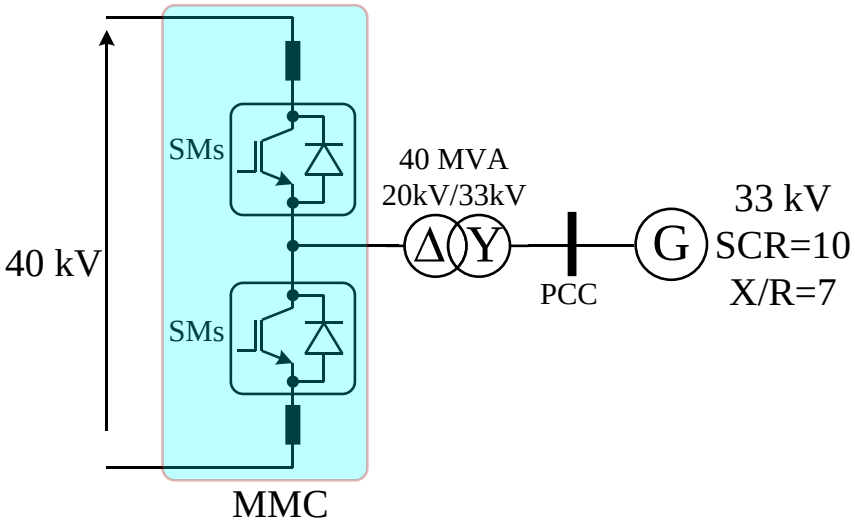

Figure 7. Simplified single line diagram of the 40 kV, 40 MVA, and 20-cell MMC connected to ac grid.

Table 1. Simulation Parameters.

System Parameters		Value
DC voltage	V_{dc}	40 kV
Rated power	S	40 MVA
AC grid line to line voltage	v_{ac2}	33 kV
AC grid frequency	F	50 Hz
Transformer ratio	v_{ac1}/v_{ac2}	20 kV/33 kV
Transformer leakage-inductance	L_T	0.2 pu
Numbers of SMs per arm	N	20
Expected arm inductance value	L	0.18 pu
Expected SM capacitance value	C	6.7 mF
DC cable length	D_{cable}	10 km
DC cable resistance per km	R_{cable}	10 mΩ/km
DC cable inductance per km	L_{cable}	1.4 mH/km
DC cable capacitance per km	C_{cable}	0.1 µF/km

Figures 8 and 9 show simulation waveforms for the control schemes A and B, respectively. These results are obtained when the MMC injects a 1.0 pu (40 MW) active power into the ac grid and regulates reactive power at zero. In contrast, Figures 10 and 11 display simulation waveforms when the MMC injects 0.6 pu (24 MVAr) capacitive reactive power and zero active power into the ac grid, with control schemes A and B, respectively. The 0.6 pu (24 MVAr) represents the maximum capacitive reactive power, which the simulated MMC can inject into the ac grid.

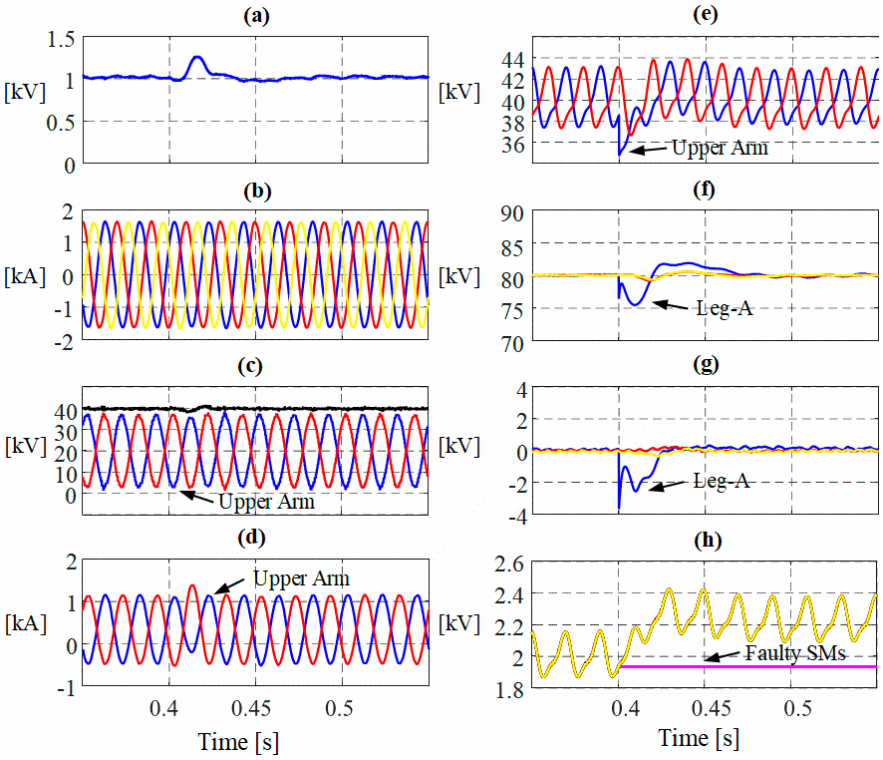

Figure 8. Simulation waveforms of the MMC under submodule (SM) fault and control scheme-A operates in active power mode: (**a**) dc current, (**b**) ac current, (**c**) leg A upper and lower arm voltages superimposed on its common-mode voltage, (**d**) leg A upper and lower arm currents, (**e**) leg A upper and lower capacitor voltage sums, (**f**) common-mode capacitor voltage sums of three phase-legs, (**g**) differential-mode capacitor voltage sums of three phase-legs, and (**h**) leg A upper arm SM voltages.

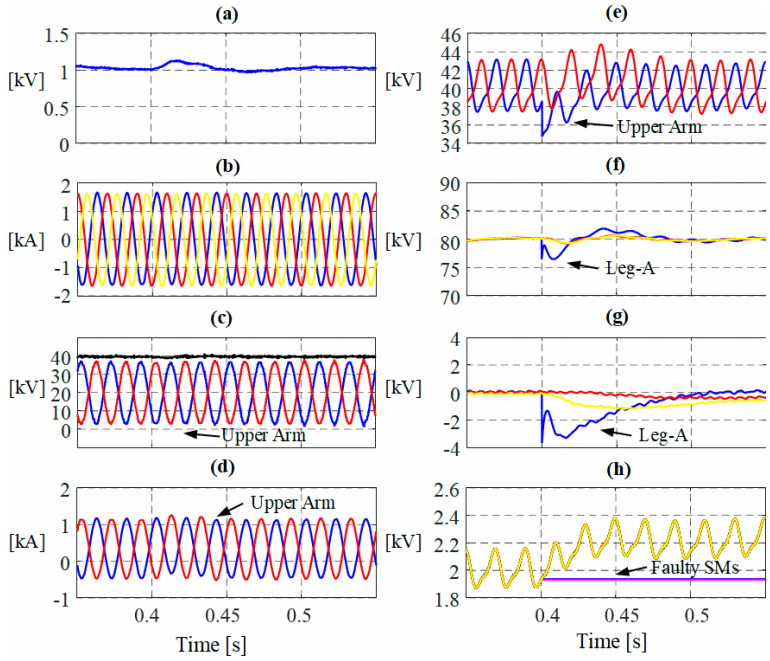

Figure 9. Simulation waveforms of the MMC under SM fault and control scheme-B operates in active power mode: (**a**) dc current, (**b**) ac current, (**c**) leg A upper and lower arm voltages superimposed on its common-mode voltage, (**d**) leg A upper and lower arm currents, (**e**) leg A upper and lower capacitor voltage sums, (**f**) common-mode capacitor voltage sums of three phase-legs, (**g**) differential-mode capacitor voltage sums of three phase-legs, and (**h**) leg A upper arm SM voltages.

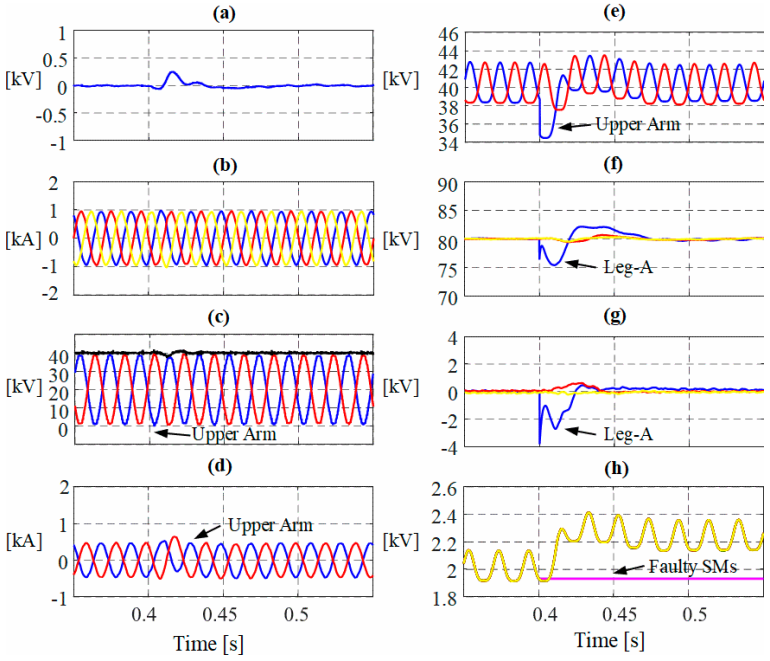

Figure 10. Simulation waveforms of the MMC under SM fault and control scheme-A operates in reactive power mode: (**a**) dc current, (**b**) ac current, (**c**) leg A upper and lower arm voltages superimposed on its common-mode voltage, (**d**) leg A upper and lower arm currents, (**e**) leg A upper and lower capacitor voltage sums, (**f**) common-mode capacitor voltage sums of three phase-legs, (**g**) differential-mode capacitor voltage sums of three phase-legs, and (**h**) leg A upper arm SM voltages.

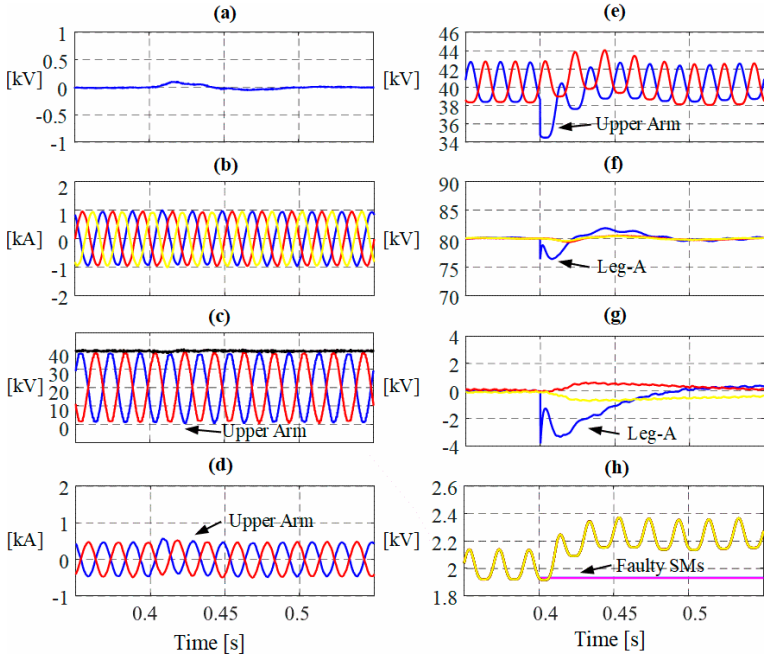

Figure 11. Simulation waveforms of the MMC under SM fault and control scheme-B operates in reactive power mode: (**a**) dc current, (**b**) ac current, (**c**) leg A upper and lower arm voltages superimposed on its common-mode voltage, (**d**) leg A upper and lower arm currents, (**e**) leg A upper and lower capacitor voltage sums, (**f**) common-mode capacitor voltage sums of three phase-legs, (**g**) differential-mode capacitor voltage sums of three phase-legs, and (**h**) leg A upper arm SM voltages.

The observations drawn from results of Scheme-A presented in Figure 8 can be summarized as follows:

1. When the SM fault occurs in the upper arm of leg-A at 0.4 s, the upper arm capacitor voltage sum decreases briefly and quickly recovers by sinking extra dc current, largely, due to the actions of differential-mode capacitor voltage sum or arm voltage balancing controllers of Scheme-A. During the transient period, the upper and lower arm voltages of the faulty phase exhibit brief disturbances, while the three-phase ac output currents remain unaffected, see Figure 8a–e.
2. Following the SM fault, the common-mode capacitor voltage sums of three legs return to their pre-fault set-points, with the deviations emerged in both common- and differential-mode capacitor voltage sums of the three phase-legs (including the faulty phase-leg A) at 0.4 s that are quickly eliminated, see Figure 8f,g. These results demonstrate the importance of inter-arm vertical controllers implemented in Scheme-A.
3. The plots in Figure 8h show that the healthy SM capacitor voltages of the faulty arm (upper arm of phase-leg A) increase due to a reduced number of active SMs that could contribute to the target capacitor voltage sums enforced by collective actions of common- and differential-mode controllers of Scheme-A. After bypass of the faulty SMs, their capacitor voltages do not exhibit any fluctuations associated with fundamental and remnant of 2nd harmonic currents as anticipated.

Simulation waveforms of the 20-cell MMC in Figure 7, with the Scheme-B, are presented in Figure 9. The observations drawn from the results in Figure 9 are as follows:

1. MMC with the use of Scheme-B exhibits slightly different behavior from that with the control scheme A. The dc-link current displayed in Figure 9a exhibits smaller increase, and SM capacitor voltage sum of the faulty leg (an upper arm of phase-leg A) exhibits slightly small under-shoot and over-shoot compared to those with Scheme-A. The smaller increase in the dc current with control scheme B can be attributed to the absence of vertical controllers, which actively inject

additional active powers and fundamental currents into the common-mode loops in order to enforce equalization of the arm capacitor voltage sums.

2. The Scheme-B makes the MMC less sensitive to SM faults and remains capable of synthesizing the output ac voltages that the ac grid imposes at its ac terminals, with three-phase ac output currents remain unaffected, see Figure 9a,e.
3. The common-mode capacitor voltage sums of the three phase-legs remain tightly controlled and less affected throughout as the control scheme B only enforces equal dc voltages across the MMC phase-legs, with the SM level capacitor voltage controller ensuring the imposed dc voltage across the phase-legs being equally distributed across the SM capacitors. These are achieved without paying any attention to the symmetry of upper and lower arm capacitor voltage sums, see Figure 9f,g.
4. The healthy SMs have slightly lower capacitor voltages with Scheme-B than that of Scheme-A due to lower dc voltage across the faulty arm in post-fault condition, as demonstrated by the clear drift the differential-mode voltage displayed in Figure 9g. As in the previous case, the capacitor voltages of the faulty SMs become flat under the post-fault condition.

In addition, the results of fast Fourier transform (FFT) analysis presented in the appendix for the MMC in Appendix A, when it is controlled using the control schemes A and B, respectively, show that the amplitudes of the fundamental frequency component in dc-link current are 11.3 A and 4.1 A, respectively. These results confirm the effectiveness of the Scheme-B in dealing with fundamental frequency ripples in the dc loop (common-mode and dc-link currents) compared to that of the Scheme-A.

The observations, drawn from Figures 10 and 11 when control schemes A and B are used to control the 20-cell MMC in Figure 7, are as follows:

Figures 10a and 11a show that the MMC dc current for the two control schemes is zero, as anticipated during pure reactive power exchange. In line with previous cases, these results show that the dc current of Scheme-A exhibits a brief period of larger temporary over-current due to actions of arm balancing controllers, which force the dc voltages across all arms to be equal.

Figures 10b–d and 11b–d display the three-phase output currents and phase-leg A upper and lower arm voltages superimposed on the common-mode capacitor voltage sum of phase A. Notice that reactive power output reaches the limit as the arm voltage synthesized nearly touches the limits in both cases.

Although the common-mode capacitor voltage sums of the schemes A and B exhibit similar behaviors, the capacitor voltage sums of the upper and lower arms of the faulty phase-leg exhibit slightly different behaviors, see Figure 10e,f and Figure 11e,f. Besides, the differential-mode capacitor voltage sums in Figures 10g and 11g present different convergence patterns, as Scheme-A controls the differential-mode capacitor voltage sum actively.

5.2. Parametric Studies of Asymmetric MMC Operation

To further generalize the findings of the above detailed quantitative studies on asymmetries introduced by the MMC SM faults, additional parametric studies are conducted on a 50-cell MMC using control schemes A and B. The test system parameters are listed in Table 2. To reproduce more representative MMC asymmetries that may arise from SM faults or severe deviations in the values of passive parameters from their nominal values, the SM capacitance (C_u and C_l) and arm inductance (L_u and L_l) of the upper and lower arms are varied within ±10% of their nominal values, C_0 and L_0 (i.e., $0.9C_0 \leq C_{u,l} \leq 1.1C_0$ and $0.9L_0 \leq L_{u,l} \leq 1.1L_0$). In the parametric studies, the 50-cell MMC in Figure 12 injects 100 MW into the ac grid at a unity power factor.

Table 2. Simulation Parameters.

System parameters		Value
DC voltage	V_{dc}	100 kV
Rated power	S	100 MVA
AC grid line to line voltage	v_{ac2}	66 kV
AC grid frequency	F	50 Hz
Transformer ratio	v_{ac1}/v_{ac2}	50 kV/66 kV
Transformer leakage-inductance	L_T	0.2 pu
Numbers of SMs per arm	N	50
Expected arm inductance value	L	0.18 pu
Expected SM capacitance value	C	6.7 mF

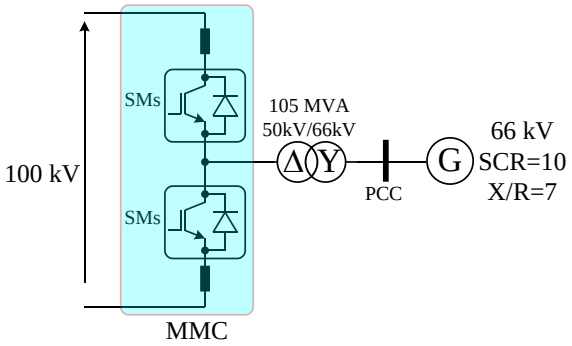

Figure 12. Test system employed in parametric studies with a 50-cell MMC, in which 5 faulty SMs represent 10% of the total number of SMs per arm.

Figures 13 and 14 present side-by-side comparisons of the normalized fundamental frequency ripple in the dc current by its average and maximum achievable modulation range versus average asymmetries in the SM capacitances and inductances between the upper and lower arms of the same phase-leg, for control schemes A and B. The observations drawn from these parametric studies are:

1. Figure 13a,b show that the highest fundamental frequency ripple in the dc current is observed when the upper and lower arms of the same phase-leg simultaneously present a higher mismatch in both SM capacitance and arm inductance, i.e., at extrema of (T_C and T_L) = (−10% and −10%) and (+10% and +10%). In contrast, the lowest fundamental current ripples are observed when T_C and T_L are (0 and 0), (+10% and −10%), and (−10% and +10%), entailing the polarities of SM capacitance, and arm inductance tolerances affect the magnitude of the fundamental current ripple on dc-side current. Notice that these observations are applied to both control schemes.
2. Quantitatively, comparative parametric studies shown in Figure 13a,b confirm that the Scheme-B, which prioritizes suppression of fundamental frequency ripple in the common-mode currents, exhibits a lower residual ripple in the dc current compared to Scheme-A that prioritizes strict management of voltage stress within the converter over dc side waveform quality.
3. Figure 14a,b display the variations of maximum attainable modulation index in faulty leg-A, with control schemes A and B. The active arm balancing control of scheme A helps to preserve the maximum achievable modulation index range during severe SM capacitance and arm inductance asymmetries. In contrast, with Scheme-B, the MMC modulation index range experiences small reduction as the levels of passive parameter mismatch increase. The worst-case reduction observed in the modulation index range is about 1.5%, which corresponds to a small reduction in MMC ac voltage synthesis and reactive power generation capabilities.
4. The Scheme-A ensures a dc offset free in ac output voltage independent of the severity of MMC internal asymmetries at the expense of compromised dc current quality. While Scheme-B increases the risk of dc injection into the ac grid, particularly, when the arms with minimum capacitor

voltage sums are no longer sufficient to synthesize the required ac voltage to exchange the desired active and reactive powers. These observations are in line with the discussions above.

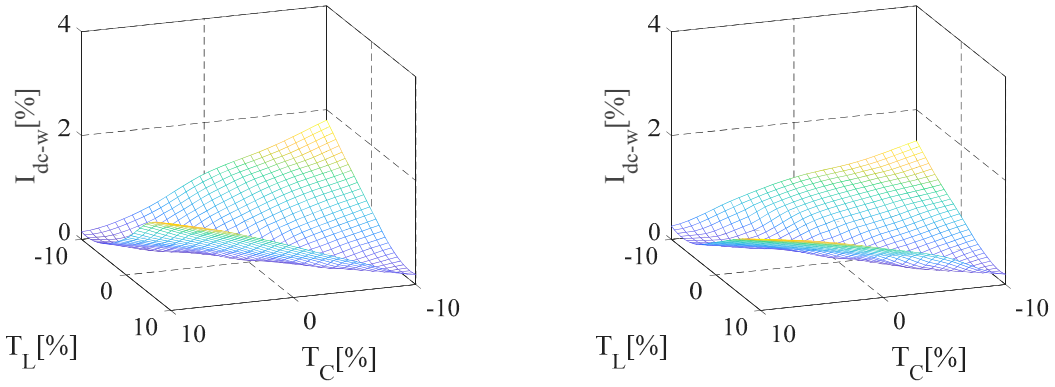

Figure 13. Variation of fundamental frequency dc-link current ripple magnitude (pu) with SM capacitance tolerances T_C and arm inductor tolerances T_L: (**a**) Scheme-A and (**b**) Scheme-B.

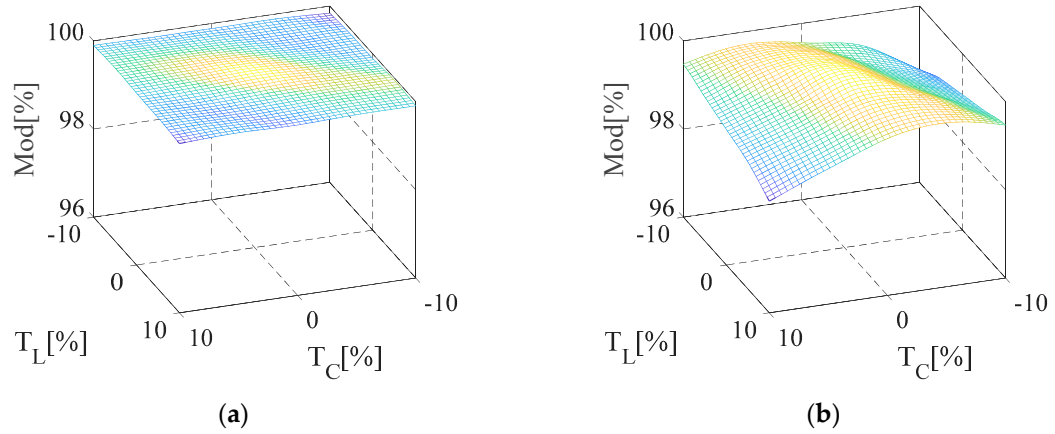

Figure 14. Variation of fundamental frequency dc-link current ripple magnitude (pu) with SM capacitance tolerances T_C and arm inductor tolerances T_L: (**a**) Scheme-A, and (**b**) Scheme-B.

It is worth emphasizing that the 20-cell MMC in previous studies is a good representation of the scenario with low SMs numbers per arm. In such a scenario, the loss of 10% of total SMs per arm in absolute term, namely, two SMs, is of practical significance, particularly from the following point of views: (1) Increased duties on remaining and healthy SMs (frequency of insertion and bypass of SM capacitors). (2) Increased sampling errors in the synthesis of the dc, arm, and output ac voltages. (3) Average switching frequency per device. (4) Increased likelihood of occurrence in a practical system. On the other hand, the 50-cell MMC is a relatively good representation for upper MV applications, in which the likelihood of loss of 10% of the total number of SMs per arm is much lower but remains possible with less impact on the quality of the ac and dc side waveforms and duties on SM capacitors.

6. Experimental Verifications

Since SM faults make the MMCs present unequal equivalent capacitances per arm and per phase-leg bases, this section emulates the steady-state impacts of SM faults through the deliberate use of unequal cell capacitances and arm inductances on experimental test rig of a single-phase grid-connected MMC with three cells per arm, see Figure 15. The MMC test rig is equipped with the following controllers: 1) active and reactive power controller, which sets P = 2kW and Q = 0, 2) inner current controller, circulating current suppression controller, 3) horizontal/common-mode capacitor

voltage sum, 4) level-shifted pulse width modulation with 1 kHz carrier frequency and sorting-based capacitor voltage balancing.

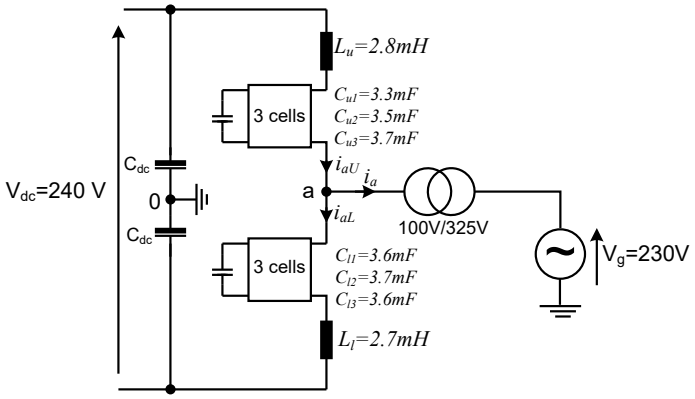

Figure 15. Experimental test of a 3-cell HB-MMC.

Figures 16 and 17 display experimental results when control schemes A and B are employed. Figure 16a,b and Figure 17a,b present upper and lower arm capacitor voltage sums and upper and lower arm currents for the control schemes A and B, respectively. Although both methods appear to work well, it is worth noticing that the Scheme-B exhibits slightly lower ripples in the common-mode current. In line with simulations, the FFT shows that the Scheme-B exhibits slightly lower contamination of the common-mode current by the fundamental frequency component compared to that of the control method A. Despite the few SM numbers of the experimental test rig, the presented experimental results point toward the same conclusions as simulation cases discussed earlier.

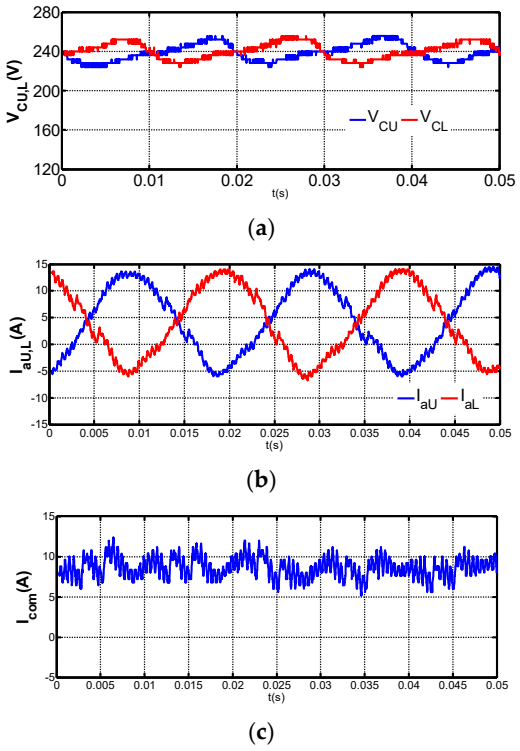

Figure 16. Experimental waveforms of the 3-cell MMC that employs internal Scheme-A: (**a**) upper and lower capacitor voltage sums, (**b**) upper and lower arm currents, and (**c**) common-mode current with the measured fundamental frequency content of 6.6%.

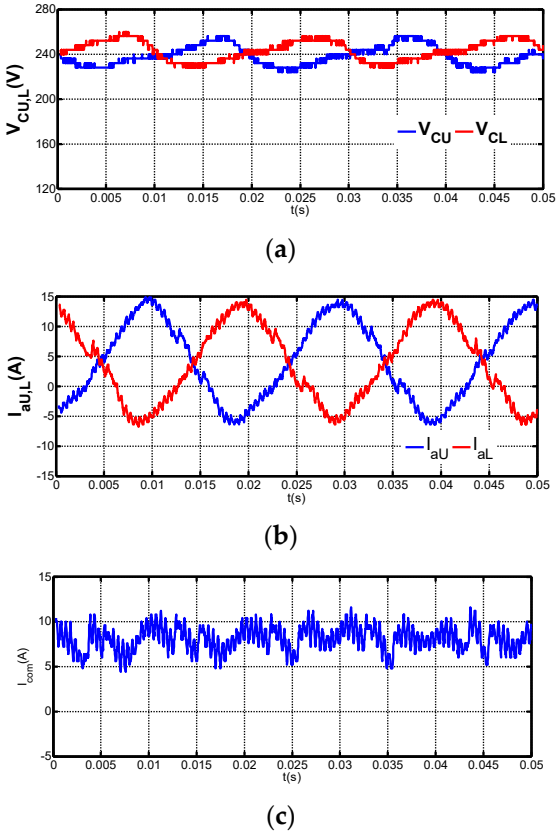

Figure 17. Experimental waveforms of the 3-cell MMC that employs internal Scheme-B: (**a**) upper and lower capacitor voltage sums, (**b**) upper and lower arm currents, and (**c**) common-mode current with the measured fundamental frequency content of 5.4%.

7. Conclusions

This paper has investigated the impacts of MMC internal asymmetries due to SM faults or severe deviations of the SM capacitance or arm inductance values from their nominal values, particularly, on the following aspects: control range, power quality in ac and dc sides, and distribution of voltage stresses across the SM capacitors and semiconductor switches. Moreover, the paper has presented a direct method for fundamental frequency ripple suppression from the dc link, and its performance is compared to a well-performing conventional controller for managing MMC internal dynamics. The investigation has found that the control for actively balancing arm capacitor voltage sums (Scheme-A) is better than the direct fundamental ripple suppression method (Scheme-B) from the ac side viewpoint, but it pollutes dc current with a fundamental frequency ripple. In contrast, the Scheme-B is better than its counterpart A, from the dc side viewpoint; nevertheless, it increases the risk of dc injection into the ac grid and reduction of ac control range.

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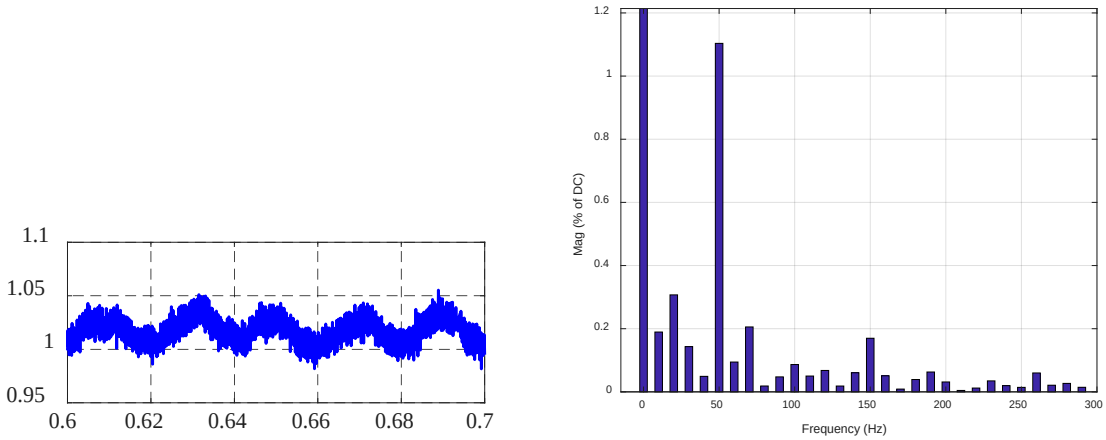
Conflicts of Interest: The authors declare no conflict of interest.

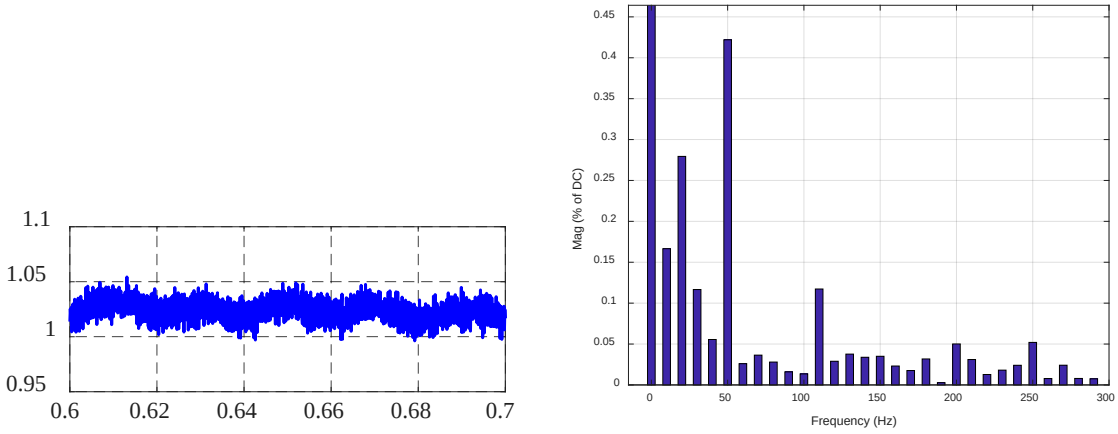
Appendix A

Zoomed waveforms of the dc currents displayed in Figures 8a and 9a and their FFT analyses are shown in Figures A1 and A2, respectively, to further consolidate the previous claims.



(**a**) (**b**)

Figure A1. Additional simulation waveforms. (**a**) Zoomed version of dc-link current displayed in Figure 8a, (**b**) FFT spectrum.



(**a**) (**b**)

Figure A2. Additional simulation waveforms. (**a**) Zoomed version of dc-link current displayed in Figure 9a, (**b**) FFT spectrum.

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