Article

A Novel Multilevel DC-Link Three-Phase T-Type Inverter

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Abstract: This research proposes a four-level T-type inverter that is suitable for low-power applications. The presented topology outranks other types of inverters in terms of a smaller number of semiconductor devices, absence of passive components such as clamping diodes and flying capacitors, low switching and conduction losses, and high efficiency. The proposed topology is free from voltage deviation and unbalanced voltage occurrences that are present in other multilevel converters having clamping diodes or flying capacitors. The proposed inverter can extend to *N* levels using unequal dc-link voltage sources for medium-voltage application. The inverter employs the simple fundamental frequency staircase modulation technique. Moreover, this paper presents a current commutation strategy to prevent the occurrences of short circuit and minimizing the number of required switching devices and switching transitions, resulting in improving the efficiency of the inverter. This paper also analyses the theoretical converter losses showing lower switching and conduction losses when compared to existing four-level inverters. The experimental validation of the proposed inverter shows its operating feasibility and a low output voltage THD.

Keywords: DC–AC power conversion; fundamental frequency staircase modulation; PWM modulation technique; DC–AC inverter; T-Type inverter; unequal dc voltage supplies

1. Introduction

Multilevel inverters have been developed widely in industrial applications in recent decades [1]. The conventional topologies employed for industrial applications are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters [2–4]. However, with higher output voltage levels, the conventional multilevel inverters pose disadvantages such as unbalanced dc-link voltage, practical limits to the number of output voltage level, and high component count [5].

Recently, numerous research has been proposed on asymmetrical and hybrid multilevel inverters, which have different values of dc voltage sources and dc-link circuits that are connected to the midpoint such as the inverter presented in [6]. Various modulation techniques [7–10] and power electronic component technologies [11–14] are needed to achieve the desired output stepped waveforms. Various types of switches have been constructed and validated in [15,16] for different types of inverters

for the purpose of increasing the reliability of the inverters such as to reduce the total count of passive components and to obtain the desired stepped output waveforms [17–19].

Industrial applications constantly require multilevel inverters with high rated power and high-power quality. However, the two requirements cannot be achieved while maintaining low switching frequency [20]. The T-type inverter can be an alternative for low-voltage applications, meeting the requirements of high-power quality at a lower switching frequency [1]. In addition, T-type topology has the advantage of two-level converters, which include low power losses, simple operation, and the positive aspects of the three-level converters, such as higher efficiency and smoother stepped output voltage waveforms [21].

T-type inverters are mainly proposed and constructed for low-power industrial applications since it shows a better performance compared to the conventional inverters [22–27]. Although T-type inverters consist of two switches in series connection in its T-link, the efficiency is higher, and the power losses are lower compared to the conventional inverters. In other words, T-type inverters are also good solutions for low-voltage applications with high power ratings obtained by increasing the phase current [28].

For medium- and high-voltage applications, a bidirectional switch is applied to the midpoint of the T-type inverter and can be an alternative solution to minimize the number of components [29–33]. T-type inverters that are applied for medium-voltage and medium-power applications are known as neutral point piloted (NPP) [34,35] and the transistor-clamped converter (TCC) [36]. Medium-voltage applications are achieved by connecting additional semiconductor switches in series in the main inverter bridge. However, gate-drive control units are required to balance the turn-off voltage of each series-connected switch and smooth transient during the operations [37,38]. Moreover, the series connection increases conduction and switching losses.

This paper proposes a four-level T-type inverter (4LT^{2}C) that generates $0, 1V_{dc}, 2V_{dc}$, and $3V_{dc}$ voltage levels without any capacitors and clamping devices. The presented topology outranks other topologies in terms of efficiency, low output voltage total harmonic distortion, and a low number of switching devices. For the embedded solar system, the 4LT^{2}C can be placed with two isolated batteries for four-level output voltages, which is much less costly than the installation of a bypass filter in a landing application. In addition, the 4LT^{2}C are extendable to N levels by adding auxiliary dc-link circuits that consist of a dc-link source and two semiconductor switches. This work aims to minimize the switching transitions and increase the efficiency of the 4LT^{2}C and extended inverters by decreasing the component count of power components, and conduction and switching losses. In this paper, Section 2 describes the proposed topology, its structure, modulation technique and switching sequences. Section 3 presents the operating principles of the 4LT^{2}C and its extended structure. Section 4 explains the simulation results, presents the efficiency analysis and comparison with other multilevel topologies. The theoretical analysis of the proposed topology shows good performance when compared to other four-level NPC, FC, and CHB in terms of the number of components, simplicity, and high efficiency. Section 5 shows the experimental setup and results of the 4LT^{2}C.

2. The Proposed 4LT^{2}C Converter

2.1. The Proposed Converter Topology and Model

Figure 1 shows the proposed 4LT^{2}C consisting of the conventional two-level *VSC* with active bidirectional switches at the T-link, and multilevel dc-link with unequal voltage sources. In the proposed 4LT^{2}C, the upper switches (Q1, Q3 and Q5) of the three legs are connected to the positive part of the voltage supply, whereas the lower switches (Q2, Q4 and Q6), which operate complementarily with the upper switches, are connected to ground (g). Furthermore, the dc-link with unequal dc voltage sources are connected to the midpoint of the main bridge via two series active bidirectional switches in each leg *a*, *b*, and *c*. The proposed 4LT^{2}C differs from the four-level topology illustrated in [2] because the 4LT^{2}C has reduced dc-link sources and switches for the same output level, resulting in

the reduction of cost and complexity. An increased number of output voltage steps reduces output total harmonic distortion (THD), while a decreased number of semiconductor switches minimizes conduction and switching losses. The 4LT^{2}C three-phase line-to-ground voltages are expressed as [28],

$$
\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{3V_{dc}}{N-1} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}
\tag{1}
$$

where N is the number of voltage levels and $N = 4$ in the proposed inverter, and S_a, S_b, and S_c are the voltage factors at the midpoint of legs a, b, and c, respectively. Moreover, the reference line-to-ground voltages are found as,

$$
\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 3V_{dc}}{2} * \begin{bmatrix} \cos(\omega t) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{3V_{dc}}{2}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}
\tag{2}
$$

where M_a is set to 1 and ωt is the electrical angle. The line-to-neutral voltages are written as,

$$
\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} * \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix}
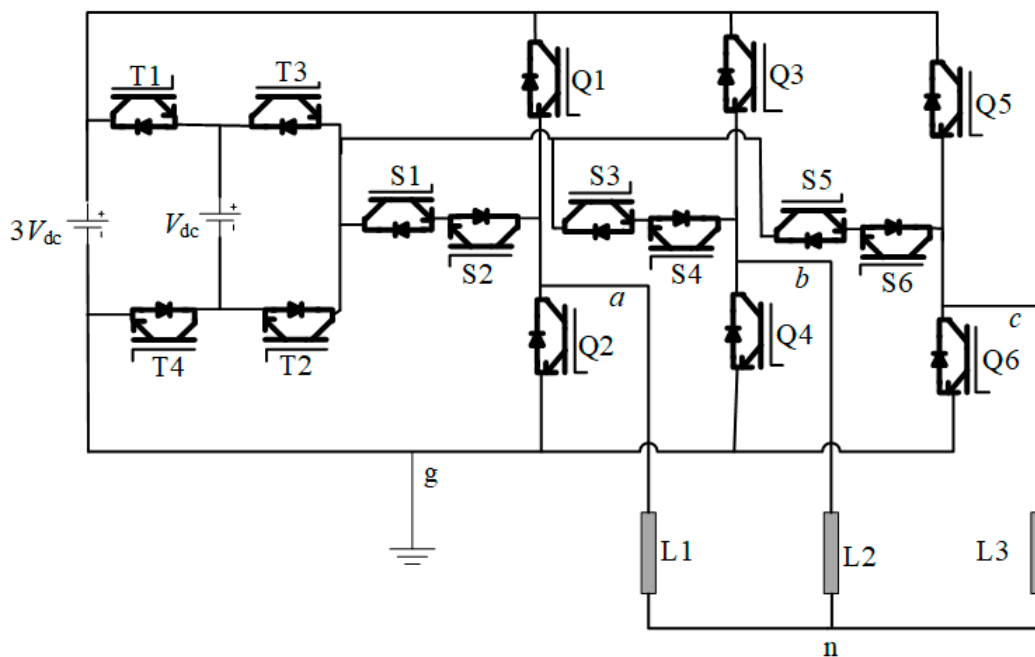\tag{3}
$$

Figure 1. Schematic of the proposed four-level T-type converter (4LT^{2}C) where each single-bridge leg of the T-type *VSC* resembles the shape of the rotated character "T".

2.2. Modulation Technique and Operating Principle

The modulation strategy is a very important feature in designing converters with high efficiency. In the proposed inverter, either the staircase modulation technique [2] or the pulse width modulation technique can be applied successfully.

Table 1 illustrates the four possible switching states of leg a and the corresponding line-to-ground voltage V_{ag} when staircase modulation is employed. Based on the switching sequence shown in Table 1, the line-to-ground voltages in leg a of $3V_{dc}$ is obtained when the upper switch Q1 turns on and

zero is obtained when the lower switch Q_2 turns on. Both Q1 and Q2 cannot turn on at the same time to prevent the shoot-through event. Moreover, with the dc-link combination, each leg can produce $+2V_{dc}$ and $+1V_{dc}$, successively. Note that Table 1 has not considered the method to reduce the number of switching transitions. Table 1 shows that the bidirectional switches in the T-link leg *a* (S1 and S2) have the same switching state in each cycle. During the transition between voltage levels, the current flow is no longer based on the current direction [4].

Table 1. Voltage transition and switching states in leg *a*.

S_a	Q1	S1	S2	Q2	T1	T2	T3	T4	V_{ag}
3	on	off	off	off	on	on	off	off	$+3V_{dc}$
2	off	on	on	off	on	on	off	off	$+2V_{dc}$
1	off	on	on	off	off	off	on	on	$+V_{dc}$
0	off	off	off	on	off	off	on	on	0

Table 2 presents the switching states of Q1–Q6 in the main bridge, T1–T4 in the dc-link and S1–S6 in the T-link. The corresponding voltage sequence in legs *a*, *b*, and *c*, are also shown in the table, where 3, 2, 1, and 0 are related to the dc-link voltage. The highlighted parts in Table 2 shows the switching transitions of the dc-link switches in which T1 and T2 are operated in contrast with T3 and T4. Moreover, Table 2 shows the condition of switches S1 and S2, which are turned on to reduce the switching losses during the transition from $3V_{dc}$ to $2V_{dc}$. When switch Q1 is turned on, leg *a* will generate $3V_{dc}$, and it will not be affected by the state of switches S1 and S2 being turned on. This is due to the current passing through Q1, a low resistance path, as compared to the higher resistance dc-link path via S1 and S2. By controlling S1 and S2 in the on state when Q1 is turned on, the number of turn-on and turn-off transitions are reduced because S1 and S2 are required to be turned on when S_a is 1 or 2. This also effectively increases the efficiency of the inverter. Figure 2 presents the space vector modulation switching states with a modulation index of 1 that can be used as a switching strategy in the proposed 4LT²C. All the parameters of the voltage vector are calculated according to the value of the *d* and *q* components [2]. The *dq* components of the space vector references can be obtained from the following equations [28]

$$V_q = \frac{3V_{dc}}{3(N-1)}(2S_a - S_b - S_c) \tag{4}$$

$$V_d = \frac{3V_{dc}}{\sqrt{3}(N-1)}(S_c - S_b) \tag{5}$$

$$V = V_q - jV_d \tag{6}$$

where S_a, S_b, and S_c are the dc voltage factor at the midpoint of legs *a*, *b*, and *c*. Note that the dc-link switches of the proposed 4LT²C function produce $1V_{dc}$ or $2V_{dc}$ at the output of one of the legs in the main inverter at any one time. Therefore, the voltage sequences of 122, 123, or 221 cannot be achieved with the space vector modulation of the modulation index less than 1. In other words, the synchronization of generating $1V_{dc}$ or $2V_{dc}$ cannot happen since switches T1 and T2 are operating in complementary with switches T3 and T4.

Table 2. Voltage transition and switching states over 1 cycle with reduced switching transitions.

| $S_aS_bS_c$	Q1	S1 S2	Q2	Q3	S3 S4	Q4	Q5	S5 S6	Q6	T1	T2	T3	T4
300	on	on	off	off	off	on	off	off	on	on	on	off	off
310	on	on	off	off	on	off	off	off	on	off	off	on	on
320	on	on	off	off	on	off	off	off	on	on	on	off	off
330	on	on	off	on	on	off	off	off	on	on	on	off	off
230	off	on	off	on	on	off	off	off	on	on	on	off	off
130	off	on	off	on	on	off	off	off	on	off	off	on	on
030	off	off	on	on	on	off	off	off	on	off	off	on	on
031	off	off	on	on	on	off	off	on	off	off	off	on	on
032	off	off	on	on	on	off	off	on	off	on	on	off	off
033	off	off	on	on	on	off	on	on	off	on	on	off	off
023	off	off	on	off	on	off	on	on	off	on	on	off	off
013	off	off	on	off	on	off	on	on	off	off	off	on	on
003	off	off	on	off	off	on	on	on	off	off	off	on	on
103	off	on	off	off	off	on	on	on	off	off	off	on	on
203	off	on	off	off	off	on	on	on	off	on	on	off	off
303	on	on	off	off	off	on	on	on	off	on	on	off	off
302	on	on	off	off	off	on	off	on	off	on	on	off	off
301	on	on	off	off	off	on	off	on	off	off	off	on	on
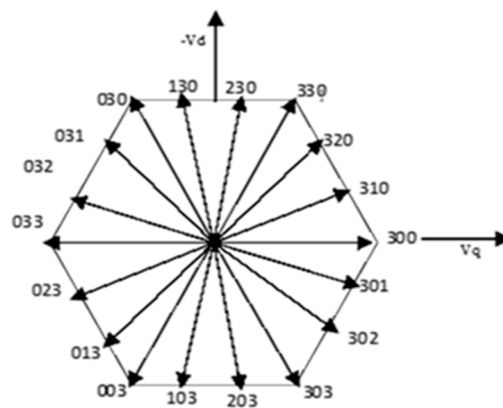
Figure 2. Switching state vectors for 4LT^{2}C [28].

2.3. The Proposed Commutation Strategy and Extended Structure

The inverter is suitable to be operated with staircase modulation, a type of fundamental frequency modulation technique, and PWM and SVM that are high-frequency modulation techniques. However, this paper proposes a commutation strategy in Section 4 that minimizes the number of switching transitions in the 4LT^{2}C when operated in the staircase modulation technique. The efficiency analysis in Section 5 will show that the efficiency of the proposed inverter is increased due to the enhanced staircase modulation.

The switching commutation that requires adequate consideration is elaborated in detail in this section. The current commutation strategy which operates separately from the current direction is taken into account to prevent any short circuit in the dc-link and active bidirectional switches. Furthermore, the switching states of each leg and its line-to-ground voltage are modified to apply a simple turn-on delay and current commutation strategy for all switches.

Table 3 shows the new switching states of leg *a* and the line-to-ground voltage V_{ag} after the switch commutation is considered. As shown in Table 3, applying the current commutation strategy contributes to decreasing the switching times of the dc-link switches, in which case the switching and conduction losses are minimized. Additionally, implementing this strategy enhances the performance of the proposed 4LT^{2}C by increasing its efficiency and reducing power losses [6].

Table 3. Voltage transition and modified switching state in leg *a*.

S_a	Q1	S1	S2	Q2	T1	T2	T3	T4	V_{ag}
3	on	on	off	off	on	on	off	off	$+3V_{dc}$
2	off	on	on	off	on	on	off	off	$+2V_{dc}$
1	off	on	on	off	off	off	on	on	$+V_{dc}$
0	off	off	on	on	off	off	on	on	0

The modified switching state demonstrates that in implementing the current commutation strategy, Q1 and S1 must be closed to achieve $3V_{dc}$. At the same time, Q2 and S2 should be closed to obtain a zero-voltage level. In a multilevel inverter, a short circuit in any leg can occur during a transition between the voltage levels. The duration of the required time between the on state and off state of the switches in a multilevel inverter is the time that the short circuit current occurrence can take place. Therefore, in the proposed topology, the current commutation strategy is applied in order to make the right path for continuous current flow.

Figure 3 presents the current commutation strategy for the transition from $3V_{dc}$ to $2V_{dc}$, which effectively enhances the switching time of $4LT^2C$ to prevent the occurrence of short circuits inside the dc-link circuit. Figure 3a illustrates the positive current commutation during the switching transition of $3V_{dc}$ to the $2V_{dc}$. The midpoint of leg *a* is connected to dc-link source $3V_{dc}$ when Q1 and S1 are turned on. To obtain the voltage of $2V_{dc}$, T1 and T2 are set in an on state. During the commutation from $3V_{dc}$ to $2V_{dc}$, switch Q1 must be turned off first. After the turn-on delay, S2 is also turned on. As shown in Figure 3b, between the turning off Q1 and the turning on S2, the current reverses direction via T1, D_{T2}, S1, and D_{S2} so that the voltage level at the midpoint of leg *a* becomes $2V_{dc}$, while S2 turns on in the zero-voltage condition. However, the negative output current still passes through D_{Q1} when Q_1 is turned off.

Figure 4 shows that the two switches of T3 and T4 in the dc-link are turned on to provide V_{dc} to the bidirectional switches of leg *a* during a negative phase output current. A positive phase output current naturally commutates to D_{Q2} when S1 is turned off. However, a negative phase output current continues to pass through S2, D_{S1}, D_{T3}, and T4 during the turning off of S1. After a delay time, Q2 is turned on and the current commutates to Q2. Figure 5 presents the various extended dc-link for the T-type topology.

Figure 5 shows that the level of dc-link sources in the proposed $4LT^2C$ can be simply extended to increase the number of output voltage levels. The maximum dc voltage is $(2n + 1)V_{dc}$. When $n = 1$, the $4LT^2C$ consisting of T1–T4 and dc sources of $3V_{dc}$ and V_{dc} is achieved. When the dc-link is extended to $n = 2$, the number of additional dc-link switches are T5 and T8 and the dc sources are $5V_{dc}$, $2V_{dc}$, and V_{dc}.
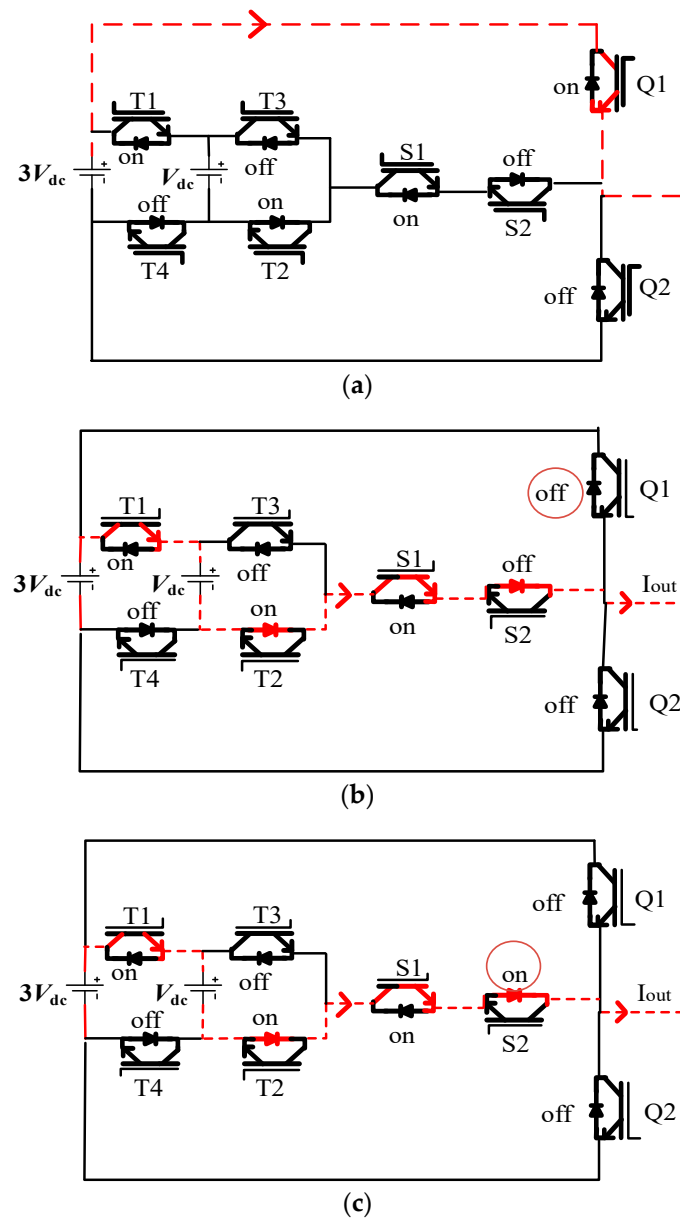
Figure 3. Current commutation during switching transition of positive output current in leg *a*. (**a**) Output voltage level of $3V_{dc}$ (Q1 on and S2 off). (**b**) Output voltage level of $2V_{dc}$ (Q1 off and D_{S2} on). (**c**) Output voltage level of $2V_{dc}$ (Q1 off, D_{S2} on and S2 on with ZVS).

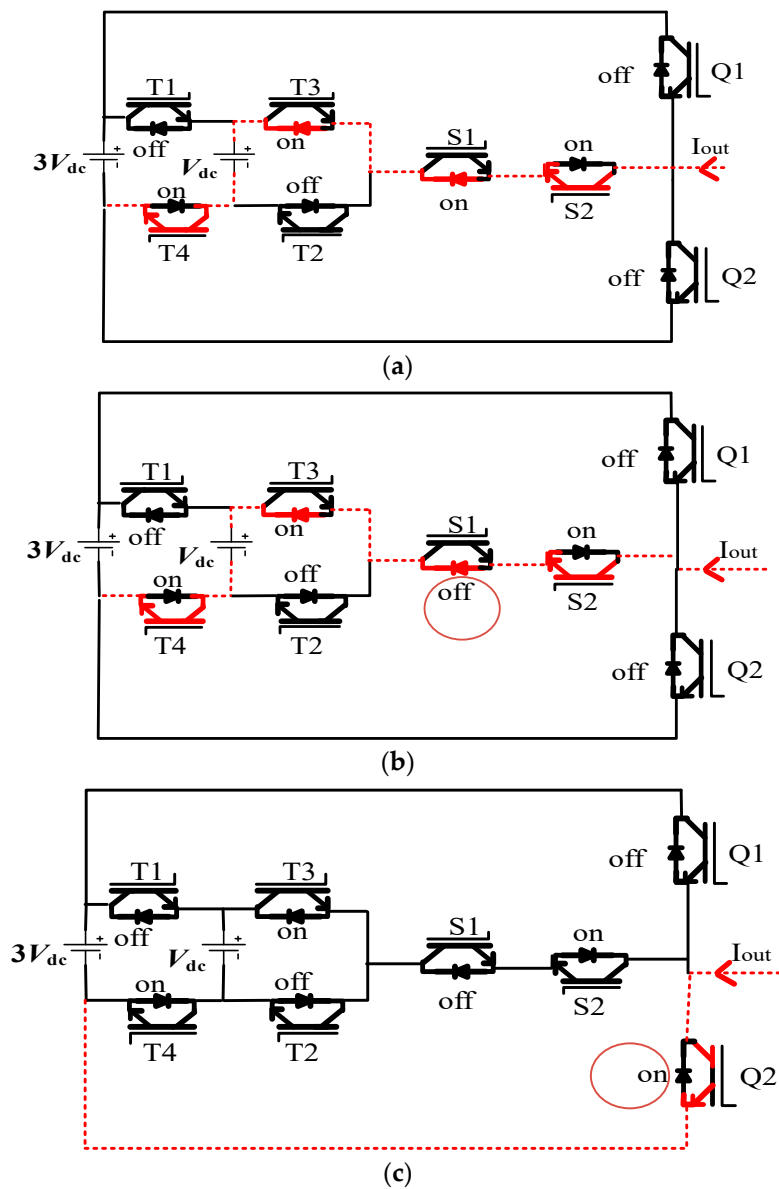**Figure 4.** Current commutation during switching transition of negative output current in leg *a*. (**a**) Output voltage level of V_{dc} (Q2 off and D_{S1} on). (**b**) Output voltage level of V_{dc} (Q2 off and S_1 off on ZVS). (**c**) Output voltage level of 0 (Q2 on and S_1 off).
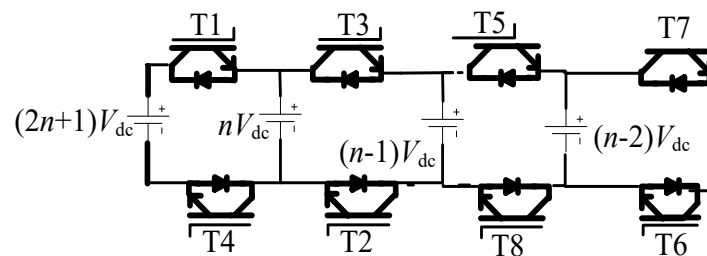

Figure 5. Extended structure of the dc-link of the proposed $4LT^2C$.

3. Simulation Results and Analysis

3.1. Operating Waveforms of the Proposed 4LT²C

Figure 6 depicts the gate switching signals and the idealized line-to-neutral and line-to-line staircase waveforms of the proposed 4LT²C. The levels of line-to-line voltage are $+3V_{dc}$, $+2V_{dc}$, $1V_{dc}$, 0, $-1V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$.
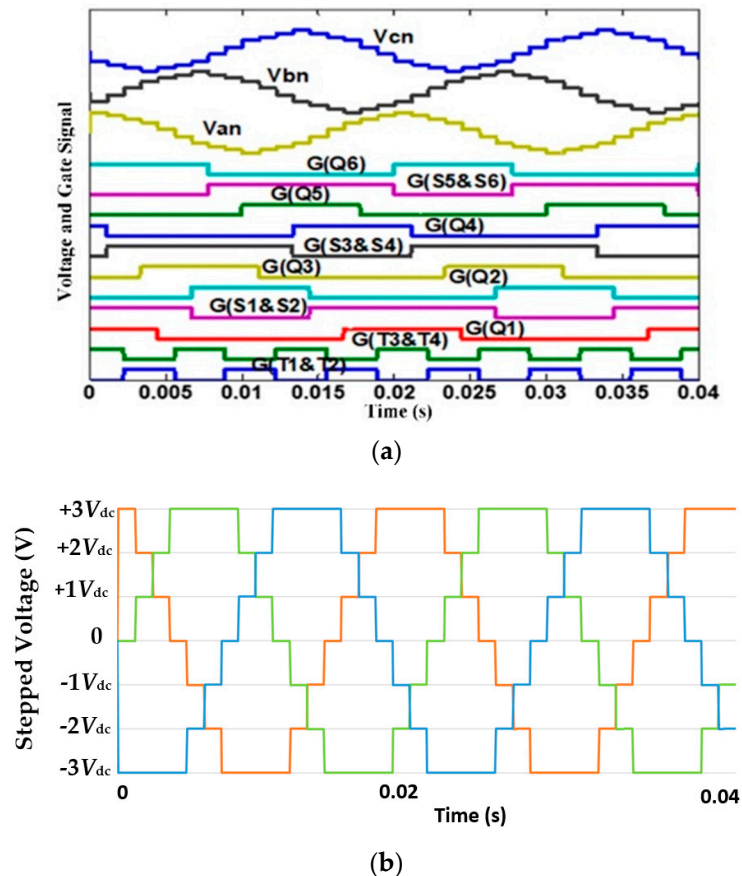
(**a**)

(**b**)

Figure 6. Idealized waveforms. (**a**) Gate signals and the line-to-neutral voltages Vcn, Vbn, and Van. (**b**) Waveforms for the line-to-line voltages Vab, Vbc, and Vca.

Figure 7 depicts the simulation results for the proposed four-level inverter. Note that V_{dc} is equal to 100 V in the simulation. The four-step waveforms of the line-to-line and line-to-ground voltages, and five-step waveforms of the line-to-neutral voltage shown are as per the idealized waveforms of the proposed 4LT²C. Each level of the line-to-line voltage is equal to V_{dc}. The output waveform of the load current is generated in accordance with the output stepped voltages. Therefore, the proposed inverter is validated successfully via simulation.
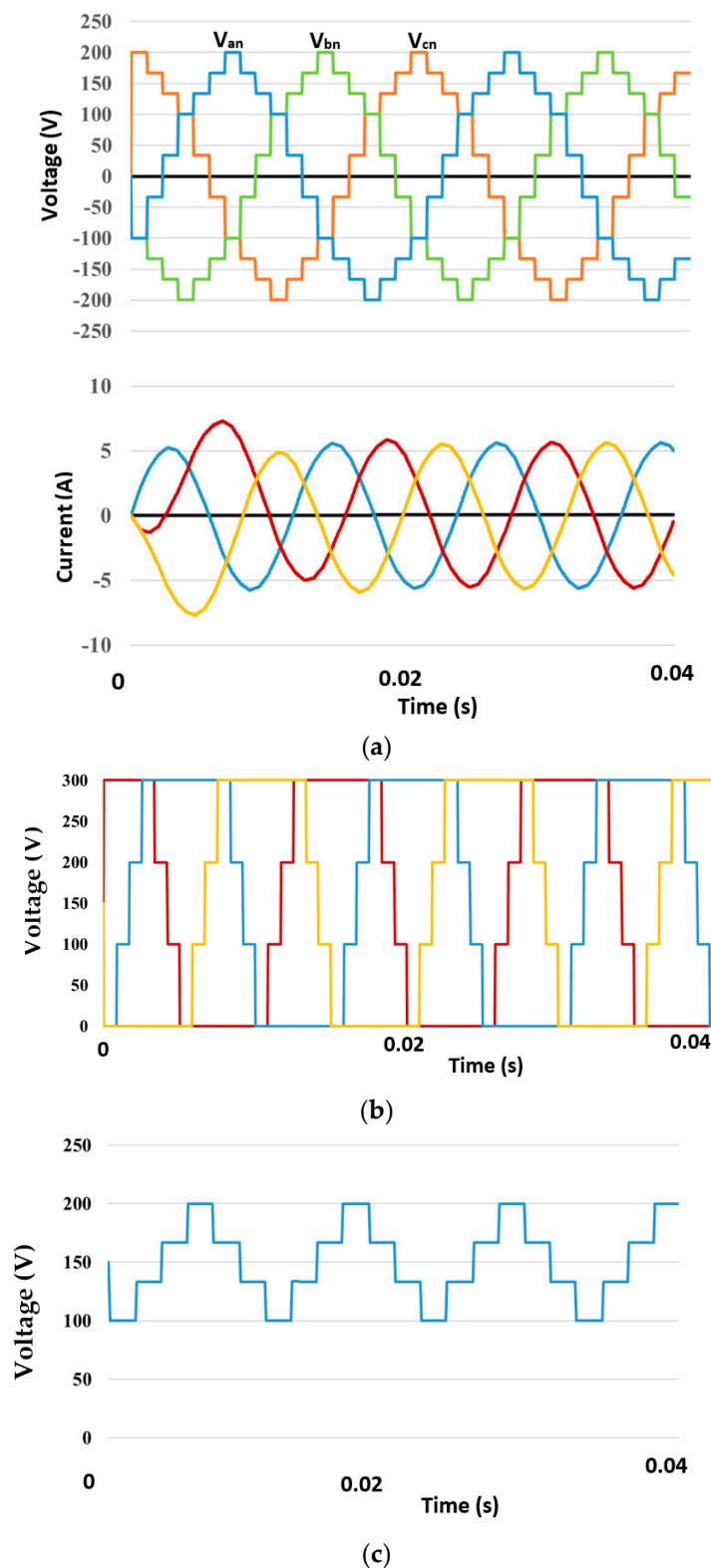
Figure 7. Simulation results for 4LT²C (**a**) line-to-neutral voltages & load current, (**b**) line-to-ground voltages (**c**), and neutral to ground voltage.

3.2. Voltage Transition and Switching Energy Loss of the Proposed 4LT²C and the N-Level Inverter in

Figure 8 shows one leg of the *N*-level inverter in [2] and the proposed 4LT²C that are used in the switching loss analysis. Table 4 and V illustrate the voltage transition and switching energy loss of

components in leg *a* of the proposed 4LT^{2}C and the *N*-level inverter in [2] during positive and negative output currents, respectively. In addition, Table 4 and subcircuits shown in Figures 3 and 4 explain in detail the process of the current commutation and switching transitions of the proposed 4LT^{2}C topology. The analysis of the switching transition in Table 4 indicates that the number of devices in 4LT^{2}C that turn on and off during the voltage transitions is two-thirds of the switching transitions shown in Table 5 for the *N*-level inverter [2]. Thus, the conduction and switching losses significantly decline during the current commutation and voltage transition process. In this case, the total efficiency of the inverter is enhanced accordingly.

Table 4. Switching energy loss of the phase *a* components in the proposed 4LT^{2}C.

Voltage Transition			Switching Energy Loss
$I_{out} \geq 0$			
$+3V_{dc}$	to	$+2V_{dc}$	$E_{Q1,off}$, $E_{Ds2,on}$
$+2V_{dc}$	to	$+3V_{dc}$	$E_{Q1,on}$, $E_{Ds2,off}$
$+2V_{dc}$	to	$+V_{dc}$	$E_{T1,off}$, $E_{DT2,off}$, $E_{T3,on}$, $E_{DT4,on}$
$+V_{dc}$	to	$+2V_{dc}$	$E_{T1,on}$, $E_{DT2,on}$, $E_{T3,off}$, $E_{DT4,off}$
$+V_{dc}$	to	0	$E_{S1,off}$, $E_{DQ2,on}$
0	to	$+V_{dc}$	$E_{S1,on}$, $E_{DQ2,off}$
$I_{out} < 0$			
$+3V_{dc}$	to	$+2V_{dc}$	$E_{DQ1,off}$, $E_{S2,on}$
$+2V_{dc}$	to	$+3V_{dc}$	$E_{DQ1,on}$, $E_{S2,off}$
$+2V_{dc}$	to	$+V_{dc}$	$E_{DT1,off}$, $E_{T2,off}$, $E_{DT3,on}$, $E_{T4,on}$
$+V_{dc}$	to	$+2V_{dc}$	$E_{DT1,on}$, $E_{T2,on}$, $E_{DT3,off}$, $E_{T4,off}$
$+V_{dc}$	to	0	$E_{DS1,off}$, $E_{Q2,on}$
0	to	$+V_{dc}$	$E_{DS1,on}$, $E_{Q2,off}$

Table 5. Switching energy loss of the phase *a* components in the *N*-level inverter proposed in [2].

| Voltage Transition	Switching Energy Loss
$I_{out} \geq 0$	
$+3V_{dc}$ to $+2V_{dc}$	$E_{Q1,off}$, $E_{S1,on}$, $E_{S2,on}$, $E_{Da2,on}$
$+2V_{dc}$ to $+3V_{dc}$	$E_{Q1,on}$, $E_{S1,off}$, $E_{S2,off}$, $E_{Da2,off}$
$+2V_{dc}$ to $+1V_{dc}$	$E_{T1,off}$, $E_{Dz2,off}$, $E_{T3,on}$, $E_{Dz4,on}$
$+1V_{dc}$ to $+2V_{dc}$	$E_{T1,on}$, $E_{Dz2,on}$, $E_{T3,off}$, $E_{Dz4,off}$
$+1V_{dc}$ to 0	$E_{S2,off}$, $E_{S1,off}$, $E_{Q2,on}$, $E_{D2,on}$
0 to $+1V_{dc}$	$E_{S2,on}$, $E_{S1,on}$, $E_{Q2,off}$, $E_{D2,off}$
$I_{out} < 0$	
$+3V_{dc}$ to $+2V_{dc}$	$E_{D1,off}$, $E_{Q1,off}$, $E_{S1,on}$, $E_{S2,on}$
$+2V_{dc}$ to $+3V_{dc}$	$E_{Q1,on}$, $E_{D1,on}$, $E_{S1,off}$, $E_{S2,off}$
$+2V_{dc}$ to $+1V_{dc}$	$E_{DZ1,off}$, $E_{T2,off}$, $E_{Dz3,on}$, $E_{T4,on}$
$+1V_{dc}$ to $+2V_{dc}$	$E_{DZ1,on}$, $E_{T2,on}$, $E_{Dz3,off}$, $E_{T4,off}$
$+1V_{dc}$ to 0	$E_{Da1,off}$, $E_{S1,off}$, $E_{S2,off}$, $E_{Q2,on}$
0 to $+1 V_{dc}$	$E_{Da1,on}$, $E_{S1,on}$, $E_{S2,on}$, $E_{Q2,off}$

(a)

(b)
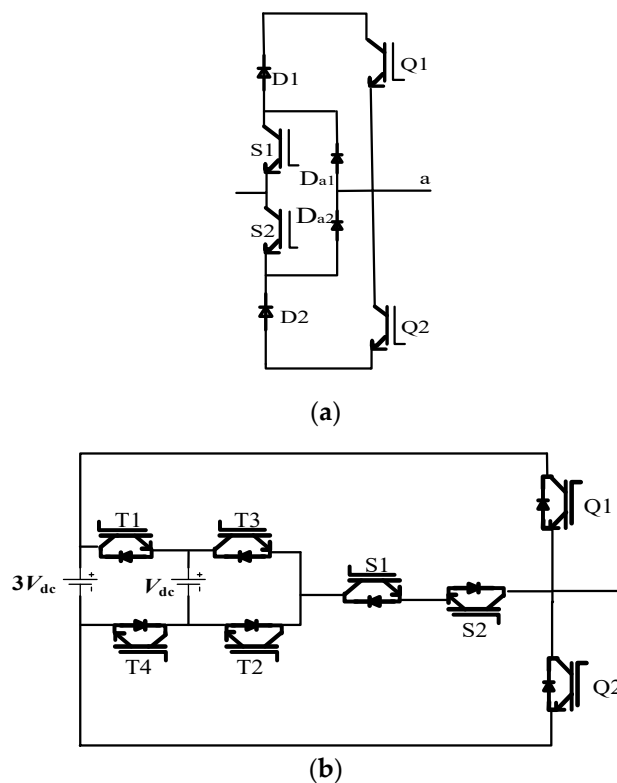
Figure 8. One leg of (**a**) the *N*-level inverter in [2] and (**b**) the 4LT^{2}C.

3.3. Efficiency Analysis of the Proposed 4LT^{2}C and the N-Level Inverter in [2]

The efficiency analysis is carried out by assuming that the proposed converter is connected to a three-phase 20 Ω-7 mH *RL* load. The IGBTs selected are rated at 19 A and 600 V (Model No.-HGTG20N60B3D). Using the information provided in the datasheet and the curve-fitting tool in MATLAB [1], the function of collector–emitter voltage V_{ce} is,

$$V_{ce} = 1.418e^{0.016i(t)} \tag{7}$$

where $i(t)$ is the instantaneous load current. Moreover, the on-state and off-state energy losses E_{on} and E_{off} are

$$E_{on} = 201.6e^{0.04418\ i(t)} - 291.6e^{-0.1265\ i(t)} \times 10^{-6} \tag{8}$$

and

$$E_{off} = 323.9e^{0.05125\ i(t)} \times 10^{-6} \tag{9}$$

In order to estimate the efficiency of the proposed 4LT^{2}C, the conduction and switching losses energy are calculated in different values of output power. This inverter is designed to deliver the rated power of P_{out} = 2.25 kW with dc-link voltages of V_{dc} = 100 V and $3V_{dc}$ = 300 V. The switching loss P_{sw} is calculated as,

$$P_{sw} = \frac{1}{T} \sum (E_{on} + E_{off} + E_{rec}) \tag{10}$$

where E_{rec} is the diode reverse recovery energy dissipation.

The switching losses are calculated by analyzing the voltage transition process from a higher level to a lower level as shown in Tables 4 and 5. The *N*-level inverter in [2] has a higher number of IGBT and diode switching energy losses than the 4LT^{2}C. The total switching loss is the summation of the switching energy loss of IGBT and diodes over one reference period.

The IGBT and diode conduction losses, $P_{\text{cond}_{\text{IGBT}}}$ and $P_{\text{cond}_{\text{diode}}}$ are calculated [28] as,

$$P_{\text{cond}_{\text{IGBT}}} = \frac{1}{T} \int_0^T V_{\text{on}_{\text{IGBT}}} \, i(t) dt \tag{11}$$

and

$$P_{\text{cond}_{\text{diode}}} = \frac{1}{T} \int_0^T V_{\text{on}_{\text{diode}}} \, i(t) dt \tag{12}$$

The conduction losses based on the conducting time, the structure of the inverter and value of the load current. Additionally, Table 6 shows the conducting devices of 4LT²C for phase *a*.

The total losses in the 4LT²C and *N*-level inverter are,

$$P_{\text{T}} = P_{\text{sw}} + P_{\text{cond}_{\text{IGBT}}} + P_{\text{cond}_{\text{diode}}} \tag{13}$$

The efficiency of the converter is calculated as the ratio of the output and input power as,

$$\eta = \frac{P_{\text{out}}}{P_{\text{T}} + P_{\text{out}}} \times 100 \tag{14}$$

Figure 9 compares the switching and conduction losses and the efficiency of the proposed 4LT²C and the *N*-level inverter base on [2] by applying the same operating conditions. Figure 8a,b shows that in the proposed converter, the switching and conduction losses per leg are 35.635 W and 0.6972 W, respectively. The switching and conduction losses per leg in the *N*-level inverter in [2] are 41.757 W and 1.1152 W, respectively. Figure 9c indicates that the 4LT²C reaches the maximum efficiency of 95.38%, while the *N*-level inverter presented in [2] reaches the maximum efficiency of 94.60% at the rated power of 2.25 kW. The proposed converter operates with high efficiency and lower power losses compared to *N*-level inverter in [2] because of the reduced number of IGBTs and minimized number of switching times during a commutation.

Table 6. Conducting devices of the 4LT²C for phase *a*.

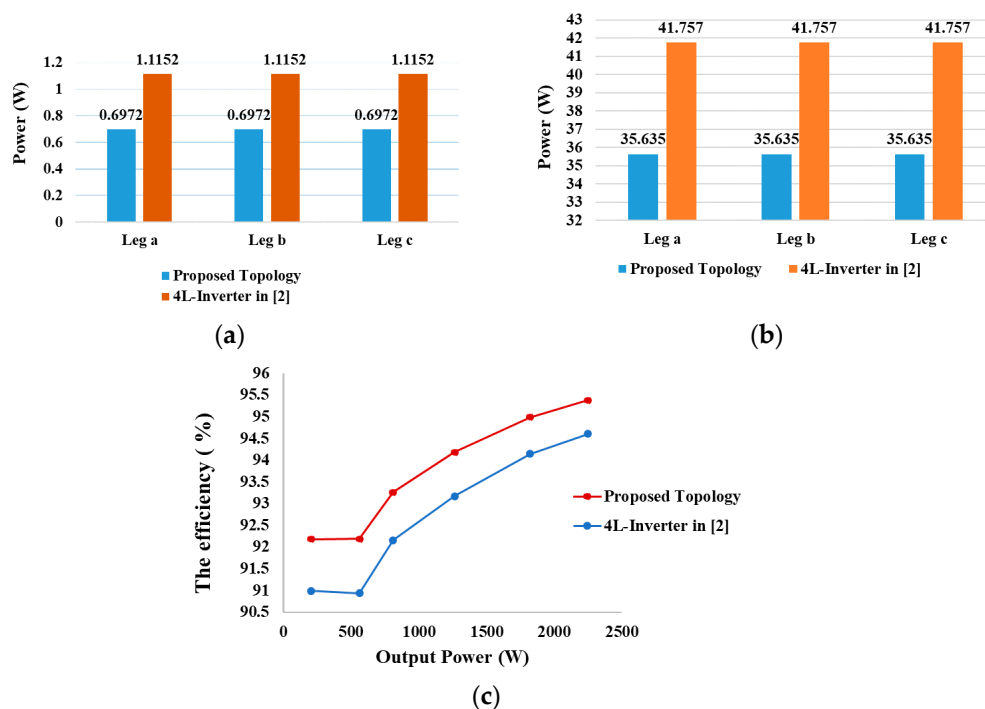| The Current	The Conducting Devices	V_{ag}
Ia > 0	Q1	+3Vdc
	T1, D_{T2}, S1, D_{S2}	+2Vdc
	D_{T4}, T3,S1,D_{S2}	+1Vdc
	D_{Q2}	0
Ia < 0	D_{Q1}	+3Vdc
	D_{T1},T2,D_{S1},S2	+2Vdc
	T4, D_{T3}, D_{S1}, S2	+1Vdc
	Q2	0

(a)

(b)

(c)

Figure 9. Comparison of calculated losses and efficiency between 4LT^{2}C and the four-level inverter in [2]: for M_a = 1 and P$_{out}$ = 2.250 kW. (**a**) Switching losses in each leg. (**b**) Conduction losses in each leg. (**c**) Efficiency as the output power increases to 2.25 kW.

3.4. Comparison of Component and Ratings of the Proposed 4LT^{2}C with Other Multilevel Topologies

Figure 10 presents the topology for the nested multilevel configuration with four-level inverter in [40], four-level inverter proposed in [41] and a typical diode clamped multilevel inverter. Table 7 compares the proposed 4LT^{2}C with the recent four-level inverter from [39,40], the four-level inverter proposed in [2], and the other existing topology shown in Figure 9, in terms of the number of switches, diodes, capacitors and dc sources. It can be clearly seen that the component count in the 4LT^{2}C is lower than the other converters. Therefore, the 4LT^{2}C will perform better than the *N*-level inverter in [2] and the other three multilevel inverters in terms of reduced switching and conduction losses and lower cost. Additionally, the topology presented in [39,40] consists of 18 switches and six flying capacitors. Therefore, the proposed 4LT^{2}C is more advantageous in terms of fewer conduction losses.
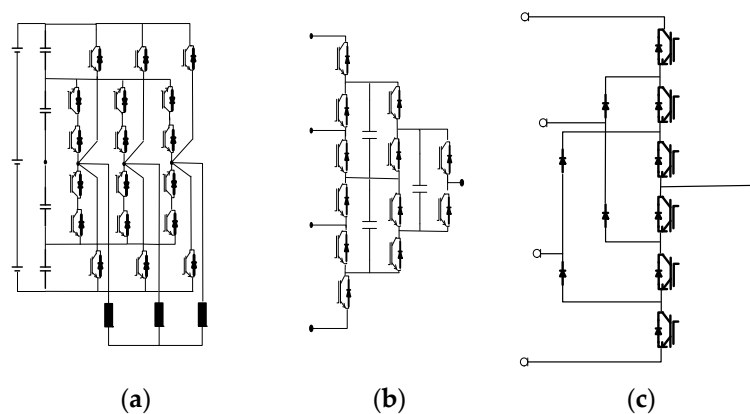

(a)

(b)

(c)

Figure 10. Topologies proposed in the technical literature. (**a**) Nested multilevel configuration with four levels [41]. (**b**) Four-level inverter proposed by [4]. (**c**) Diode clamping multilevel inverter.

Table 7. Comparison between the proposed 4LT²C and other topologies.

Converter Type	4-Level [39,40]	NPC [2]	Figure 7b [2]	Figure 9b [39]	Figure 9a [41,42]	4LT²C
Switches	18	18	16	36	18	16
Extra Diodes	0	18	16	12	6	0
Clamping Diodes	0	12	0	0	0	0
DC Supplies	2	3	2	9	3	2
Capacitors	Yes	No	No	Yes	Yes	No
No. of Levels	4	4	4	4	4	4

Moreover, the absence of flying capacitors in the proposed topology signifies the avoidance of any unbalanced voltage that may occur between the capacitors during the operation of the inverter.

4. The 4LT2C Prototype and Experimental Results

Figure 11 presents the experimental setup to verify the proposed 4LT²C. The setup consists of gate drivers, a dSPACE CP1104, a personal computer to run the switching algorithm developed in MATLAB/Simulink, two isolated dc voltage supplies set at 90 V and 30 V each, 16 IGBT switches (HGT20N60B3D, 19 A, 600 V), heat sinks, and an induction motor (400 V, 0.81 A, 0.3 kW, 50 Hz, 2800 min^{-1}). In addition, device voltage rating in the proposed T-type inverter of N levels is shown in Table 8. The proposed converter is operated using the staircase modulation technique with a fundamental frequency f = 50 Hz.
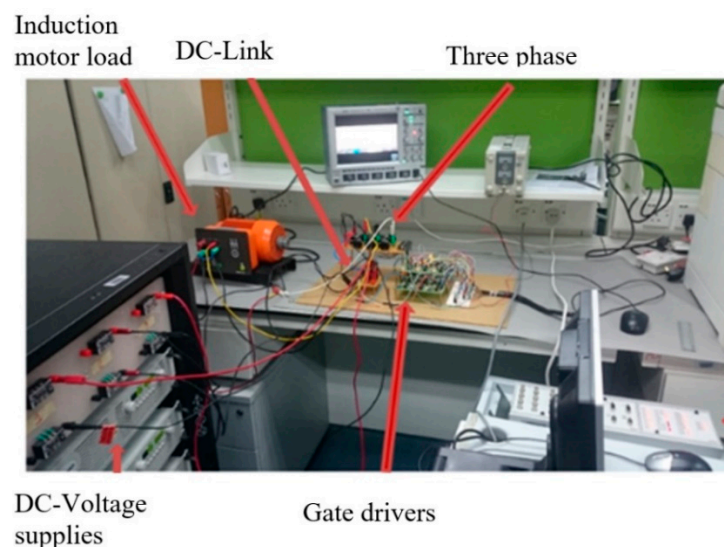

Figure 11. A prototype of the proposed 4LT²C.

Table 8. *N*-level T-Type inverter component rating.

| 4LT²C	Main Bridge Q1–Q6	Main Bridge S1–S6	Dc-Link T1–T4
Rated Voltage	$(N-1)\,V_{dc}$	$(N-2)V_{dc}$	NV_{d}

Figure 12 illustrates the results of the experiment on the proposed 4LT²C. The results above indicate that the outcomes of the experiments are the same as the simulation results shown in Figure 3. Furthermore, Figure 11c shows that the output voltage total harmonic distortion without any filter is 11.836% in the proposed topology. The frequency spectrum presents the occurrence of odd harmonics.
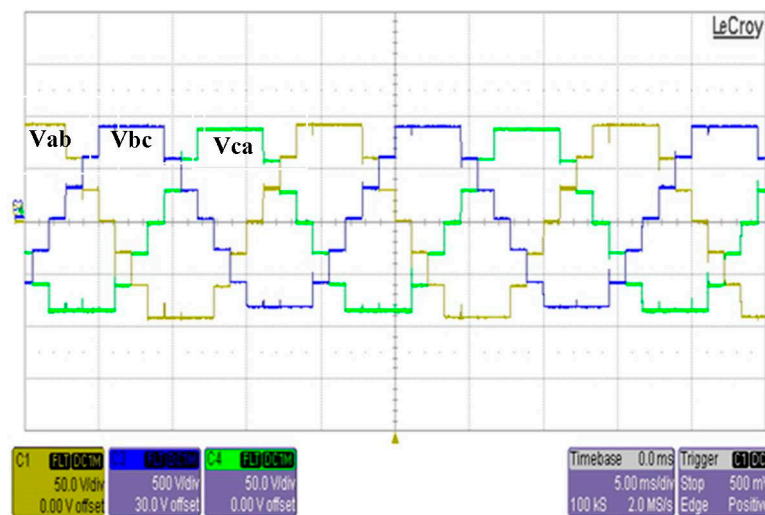
(**a**)
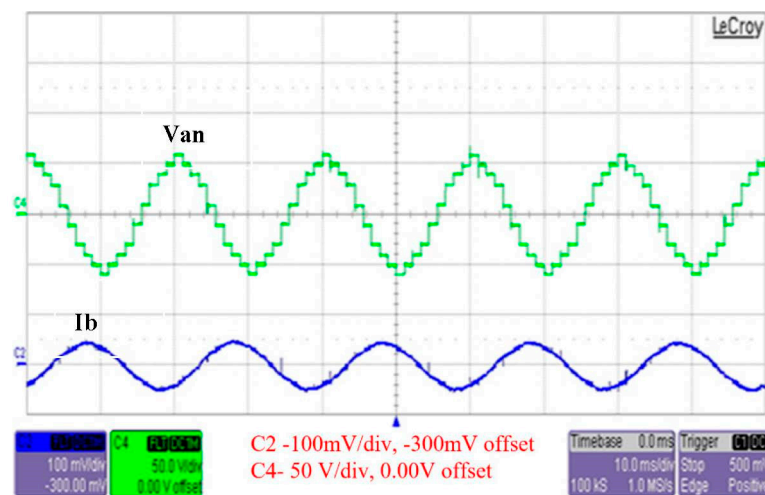
(**b**)
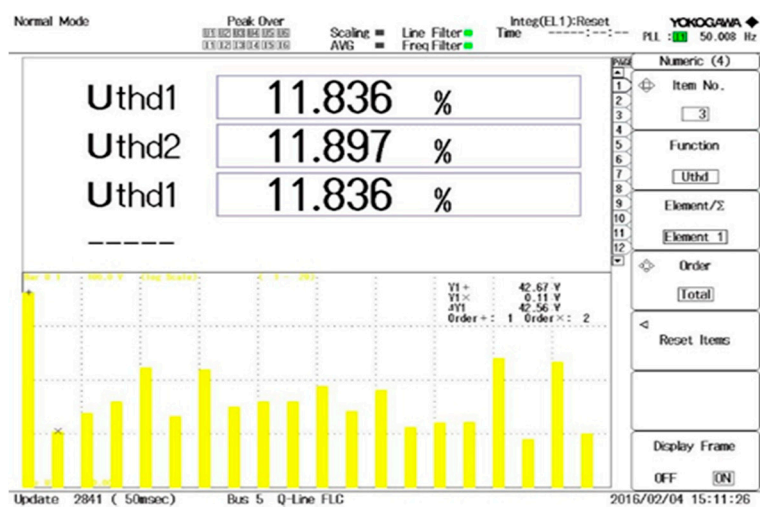
(**c**)

Figure 12. The experimental results for 4LT^{2}C when connected to 0.3 kW induction motor load. (**a**) Line-to-line voltage. (**b**) Line-to-neutral voltage with load current. (**c**) The total harmonic distortion (THD) of the proposed topology.

Components that can be removed by applying an appropriate modulation technique. Thus, the $4LT^2C$ is better than the other common inverters, as indicated in the analysis, discussion, and experimental results.

Table 9 presents the comparison of $4LT^2C$ with the existing four-level multilevel converter topology according to the number of components, rating requirement and blocking voltages. It is understood that the T-type inverter is an improved version of the NPC inverter. However, the comparison as mentioned in the previous sections is also included for the sake of completeness. Furthermore, Table 7 shows that $4LT^2C$ has fewer components than the other types of four-level inverters. In other words, $4LT^2C$ has fewer number of switches compared to the other inverters, thereby decreasing the conduction and switching losses of the inverter.

Table 9. Comparison of neutral point clamped (NPC), cascaded H-bridge (CHB), flying capacitor (FC), and NLT^2C in terms of rating requirement per the *N* level.

Converter Type	Rated Voltage		
	Main Converter Switch	**Clamping Diode**	**Clamping Capacitor**
NPC	V_{dc}	V_{dc}	n/a
FC	V_{dc}	n/a	V_{dc}
CHB	V_{dc}	n/a	n/a
NLT^2C	$(N-1)\,V_d$	n/a	n/a

n/a means not applicable.

The proposed $4LT^2C$ can be used for applications in PV grids and automotive inverter systems [21]. The proposed topology is implemented on induction motor load in the experimental setup. The topology is suitable for low-power applications as it has minimal conduction and switching losses and low component count as compared to the other four-level inverter. The proposed converter can be used for medium-voltage applications. However, a series connection of semiconductor switches in the upper and lower arm of the main inverter may be necessary. Series connection of semiconductor devices comes with problems of unequal switching times and lower reliability. Therefore, the proposed converter is recommended for low-voltage and low-power (<1000 V) applications such as induction motors, photovoltaics, and household appliances.

5. Conclusions

This paper has proposed a three-phase four-level T-type inverter ($4LT^2C$) that can be easily extended to *N* levels by adding the desired number of dc supplies to the variable dc-link. The analysis of the switching operation in the $4LT^2C$ using staircase modulation technique with proposed commutation strategy has shown that the inverter has a low number of switching transitions and hence exhibits lower conduction and switching losses in comparison with other common four-level topologies. The experimental results have verified the operating feasibility of the proposed converter and commutation strategy. A low output voltage THD without any filter is also achieved, resulting in a sinusoidal current with induction motor load. The proposed $4LT^2C$ has advantages in term of a low component count, low conduction and switching losses, and simplicity of the structure for higher-level output voltage as compared to other types of four-level inverter topologies. Moreover, the presented topology consists of no passive components such as clamping diodes and flying capacitors, which results in no issues of voltage deviation and unbalanced output voltages in the $4LT^2C$. Since the proposed converter has a lower switching and conduction loss, and minimized component count, the 4LT2C is recommended for high-efficiency and low-voltage applications at a low cost. In addition, the proposed topology can be implemented in the nanogrid models using different types of PV panels connected to control current DC/DC converter or in hybrid energy storage systems using two isolated batteries. The $4LT^2C$ can also be used for medium-voltage applications. However, the series connection

of semiconductor switches in the upper and lower arms of the main inverter in the topology may be needed.

Abbreviations

$4LT^2C$	Four-level T-type converter
D1~D6, Da1~Dc2, Dz1~Dz4	Inverter diodes
VSC	Voltage source converter
*E*on	Turn-on losses
*E*off	Turn-off losses
*V*ce	The block-voltage or reverse-voltage
P_{cond_IGBT}	Power conduction losses of the IGBT
P_{cond_diode}	Power conduction losses of the diode
Psw	The power switching losses
fsw	The operation switching frequency of switch
g	The inverter ground
Q1~Q6	Switches of the main bridge
T1~T4	Switches of DC-link
G(Q1)~G(Q6)	Switching gate signals
G(T1)~G(T4)	
G(S1)~G(S6)	
Ia, *Ib*, *Ic*, *Iab*	Load currents
Ma	Amplitude of the modulation index
N	Number of output voltage levels
Sa, *Sb*, *Sc*	Inverter switching states
V_{dc}	Voltage step value
Vref	Reference voltage vector
Vd	d-voltage component
Vq	q-voltage component
Vp	Voltage peak amplitude
Vag, *Vbg*, *Vcg*	Line-to-ground output voltages
Van, *Vbn*, *Vcn*	Inverter line-to-neutral voltages
V_{on_IGBT}	Forward voltage drops in IGBT
V_{on_diode}	Forward voltage drops in Diode

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