

Article

Analysis of the DC Fault Current Limiting Characteristics of a DC Superconducting Fault Current Limiter Using a Transformer

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Abstract: Recently, a lot of interesting research has been conducted to solve the fault current problem of the DC system. In long-distance transmission, DC transmission is more economical than AC transmission. The connection of power grids with a DC system can also better control the power flow and provide high stability. However, the control of the fault current in a DC system is more difficult to handle than in an AC system because the DC system does not make a zero point, unlike the AC system. In addition, there is a disadvantage, in that an arc occurs when a circuit breaker operates. In this paper, a new type of DC superconducting fault current limiter (SFCL) is proposed. This new type of SFCL is composed of two superconducting elements, a current limiting resistor/reactor (CLR), and a transformer. With the proposed SFCL, the DC fault current limiting experiments were performed and the DC fault current limiting characteristics of this SFCL due to the component of the CLR were analyzed.

Keywords: DC system; AC system; DC superconducting fault current limiter (SFCL); current limiting resistor/reactor (CLR); transformer; DC fault current limiting characteristics

1. Introduction

With the development of the power transmission method, the power transmission loss is reduced by transmitting power at a high voltage. For long-distance transmission, the DC system is more effective in terms of transmission loss than the AC system. In addition, the connection of power grids to different specifications using the DC system will reduce losses and make it efficient for long-distance transmission, as there is no change in voltage and polarity. Therefore, the DC system is attracting attention because a more stable grid can be kept [1–3]. However, one of the important tasks in the operation of the DC system is the limiting and blocking of the DC current. In the DC system, the DC fault current must quickly be limited to prevent damage to the connected system. As one of the countermeasures, it is necessary to introduce a superconducting fault current limiter (SFCL). The SFCL has the advantage to operate very quickly because it uses the quench phenomenon of the superconducting material itself. In a normal state, the SFCL has no loss of electricity due to having zero resistance. When an overcurrent happens, the quench occurrence in the superconducting element of the SFCL quickly suppresses the increase in the fault current [4–10].

On the other hand, for the application of an SFCL in a real power system, it needs the many superconducting elements comprising the SFCL for a larger capacity of the SFCL. To overcome this, various types of SFCLs have been developed. For example, various structural studies of SFCLs, such as the trigger-type SFCL, double quench-type SFCL and transformer-type SFCL, are underway [11–16]. If an SFCL is applied to a system, it is not necessary to replace the circuit breaker of the transmission and

distribution system when the size of the failure due to the increase in the capacity of the power system increases. Therefore, it can be expected to have a large economic effect in these areas. For example, it may be more economical to apply an SFCL than the cost of replacing the entire circuit breaker with a larger breaking capacity. Research on SFCL has been actively conducted, and in France, research is underway to apply SFCL to the transmission lines, and in Japan, an SFCL for application in the distribution line is being developed. In Korea, a 22.9 kV and 154 kV SFCL is being developed [17–22]. Although the introduction of a large-capacity SFCL may not always be economical in terms of price, the introduction of an SFCL has a great advantage in terms of performance compared to any other current limiter. In addition, the DC system has a difficulty in blocking since a zero point is not created, unlike the AC system. If the high level of fault current is cut off, an arc may occur, and the blocking may also fail. However, if the fault current level is reduced by the SFCL, it will also help to improve breaker operation.

In this paper, the DC fault current limiting characteristics of a DC SFCL using a transformer, as one of the DC SFCLs with two triggering current levels, was analyzed through short-circuit tests. The DC short-circuit experiment was constructed and the DC short-circuit tests for the DC SFCL using a transformer were carried out. Through the DC short-circuit tests, the effective DC current limiting characteristics due to the component of the current limiting resistor/reactor (CLR) comprising the DC SFCL using a transformer were analyzed.

2. Principle of Operation and Experiment of the DC SFCL

2.1. Configuration and Principle of Operation

Figure 1 shows the configuration of a DC SFCL with two triggering current levels, which was reported previously for an AC system [16]. The superconducting element R_{SC2} and CLR are connected in series, and the superconducting element R_{SC1} is configured in parallel with R_{SC2} . This DC SFCL is designed with two superconducting elements to distribute the power burden of the superconducting elements. In addition, a CLR is included to reduce the power burden of the superconducting element. When a small fault current flows, the current is limited by the R_{SC1} element. Conversely, when a large fault current flows, the fault current is sequentially limited by the R_{SC1} and R_{SC2} elements. However, after designing this DC SFCL, it is difficult to adjust the two triggering current levels. To easily change the two current levels and to increase the flexibility for the installation location of the power system, the DC SFCL using a transformer was suggested, as shown in Figure 2. In the DC SFCL using a transformer, the superconducting element R_{SC2} is designed to connect into the secondary side of the transformer and the power burden of the superconducting element is shared by utilizing the turn ratio of the transformer. In this type of DC SFCL, the current value of the quench occurrence in the superconducting element R_{SC2} can be adjusted by utilizing the transformer's turn ratio. Since the power burden by each superconducting element is divided through the CLR element, it can also reduce the power burden of the superconducting element and exhibit the advantage of being more efficient in limiting the fault current.

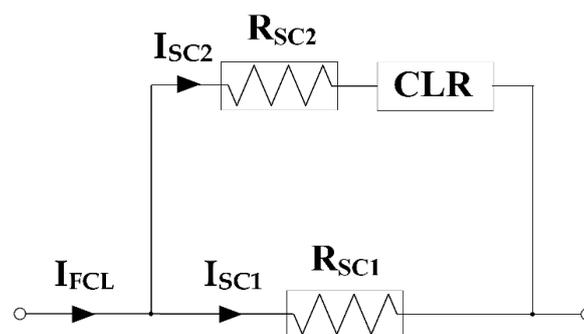


Figure 1. Configuration of the DC superconducting fault current limiter (SFCL).

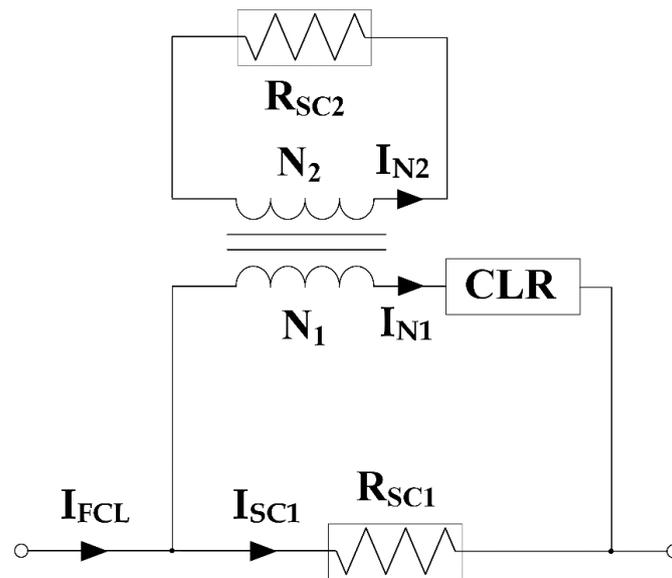


Figure 2. Configuration of DC SFCL using a transformer.

The operation of the DC SFCL using a transformer is the same except that the current in R_{SC2} is proportional to the turn ratio of the transformer (N_1/N_2) for the current in the CLR. Therefore, if the current in R_{SC1} , which only flows into R_{SC1} in a normal time, exceeds its critical current due to the fault current, the quench occurrence in R_{SC1} generates its resistance. The resistance generation in R_{SC1} makes the first DC fault current limiting operation of the DC SFCL using a transformer. Directly after the resistance in R_{SC1} is generated, the current in R_{SC1} is divided into both the R_{SC1} and the CLR. The current in the CLR, i.e., the current in the primary winding of the transformer (N_1), induces the current in R_{SC2} , which is proportional to the turn ratio of the transformer (N_1/N_2). If the current in R_{SC2} exceeds its critical current, the quench in R_{SC2} also occurs. The quench occurrence in R_{SC2} is contributed the second DC fault current limiting operation of this DC SFCL using a transformer. Through sequential quench occurrence in R_{SC1} and R_{SC2} , the DC fault current limiting operation of the DC SFCL with two triggering current levels can be achieved.

2.2. Experimental Structure and Method

To verify the fault current limiting operation of the proposed DC SFCL using a transformer, the DC short-circuit experiment was constructed, and the DC short-circuit tests were performed. Figure 3 is a schematic diagram of the DC experimental circuit with the DC SFCL using a transformer. A three-phase AC voltage (E_S) was converted into a DC voltage (V_{DC}) through a three-phase diode bridge rectifier. Normally, after the main power supplying switch S_S is closed, S_1 and S_2 are respectively closed and opened. The current only flows into R_{Load} connected in series with S_1 . When S_2 is closed, the current flows through R_{Load} and R_{Fire} . Since the equivalent resistance at this time is smaller than R_{Load} , a larger DC current flows into the DC SFCL and a DC short-circuit current can be simulated. In this paper, to simulate the larger current from the short circuit, S_2 connected to R_{Fire} was set to be closed from 0.3 s to 0.4 s after S_1 was connected to R_{Load} and closed at 0.1 s. Finally, the main switch S_S was open to cut off the power supply.

The R_{SC1} superconducting element was connected in parallel with the primary winding of the transformer and the R_{SC2} superconducting element was connected with the secondary side of the transformer. One of two terminals of the CLR was connected in series with the primary winding of the transformer and other terminal of the CLR was connected in parallel with the R_{SC1} superconducting element. The superconducting elements, which was fabricated in $Y_1Ba_2Cu_3O_{7-x}$ (YBCO) thin film form, were set in cryostat at a temperature of 77 K, which was full of liquid nitrogen [11–14]. To protect the superconducting elements used in the experiment, a shunt resistance was connected in parallel

with each superconducting element. With consideration of the superconducting element having the normal resistance between $80\ \Omega$ and $100\ \Omega$, a shunt resistance of $2.3\ \Omega$ as the lower value was selected. On the other hand, the total resistance of the superconducting element, including the lower value of the shunt resistor, is expected to be lower.

The main parameter values of experimental circuit, including the superconducting elements, are shown in Table 1. To investigate the DC fault current limiting characteristics of this SFCL due to the component of the CLR, the resistance and the inductance of the CLR were selected with three values, respectively, as listed in Table 1.

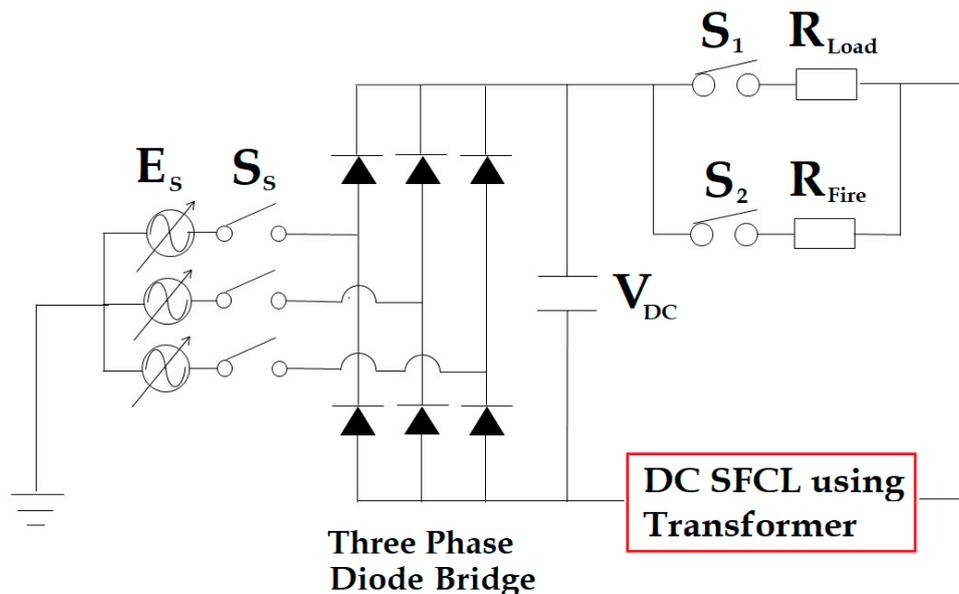


Figure 3. Schematic diagram of the DC experimental circuit with a DC SFCL using a transformer.

Table 1. Main parameter values of the experimental circuit.

DC Test Circuit	Value	Unit
V_{DC}	110	V
R_{Load}	10	Ω
R_{Fire}	2.5	Ω
Transformer and CLR	Value	Unit
Turns Ratio (N_1/N_2)	3	
CLR (R_S)	4.6/2.3/1.15	Ω
CLR (L_S)	6.6/7.5/10	mH
Superconducting elements (R_{sc1} and R_{sc2})	Value	Unit
Fabrication Type	Thin Film	
Material	YBCO	
Critical Current	25	A
Total Meander Line Length	420	mm
Line Width	2	mm
Thin Film Thickness	0.3	μm
Gold Layer Thickness	0.2	μm

3. Result and Discussion

Figures 4 and 5 show the current and the voltage waveforms when the CLR component is a resistance (R_S). The DC fault current was generated by SW_2 closing at 0.3 s. In case of $R_S = 1.15\ \Omega$, as seen in Figure 5a, it could be observed that the voltages in the two superconducting elements (V_{SC1} , V_{SC2}) as well as the primary winding (V_{N1}) were generated directly after the DC fault occurred.

It could be confirmed from Figure 4a that the currents flowing into two superconducting elements (I_{SC1} , I_{SC2}) simultaneously exceeded the critical current (I_C), which caused the voltages in the two superconducting elements.

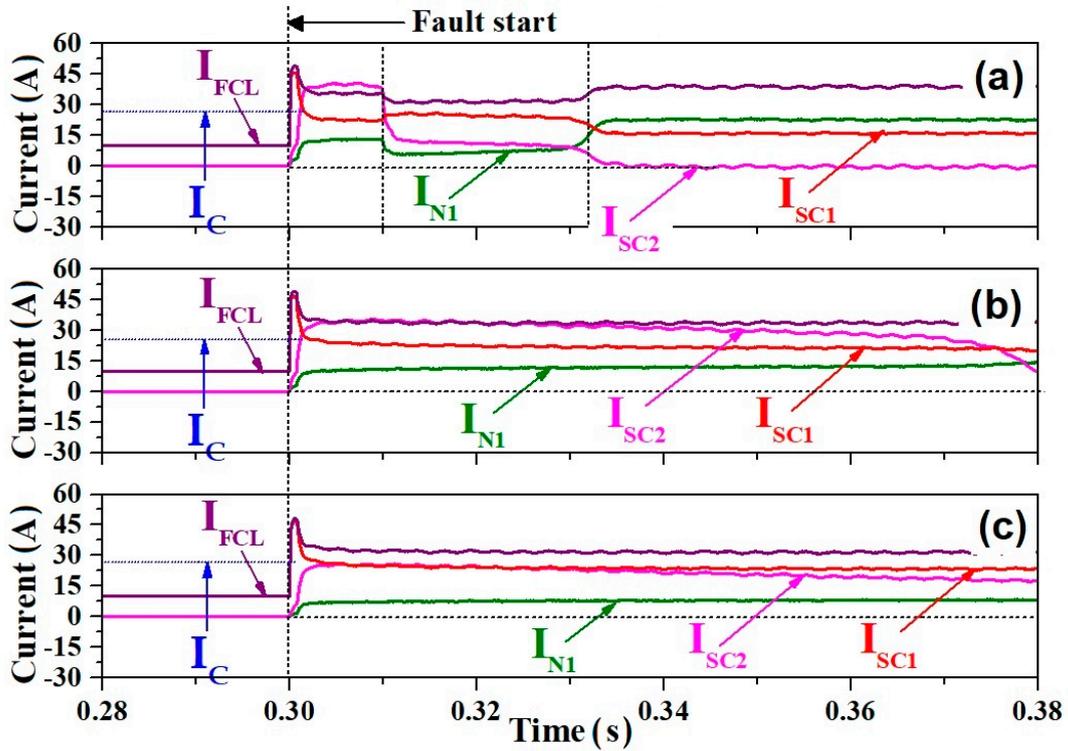


Figure 4. Current waveforms due to the CLR's resistance: (a) $R_S = 1.15 \Omega$; (b) $R_S = 2.3 \Omega$; (c) $R_S = 4.6 \Omega$.

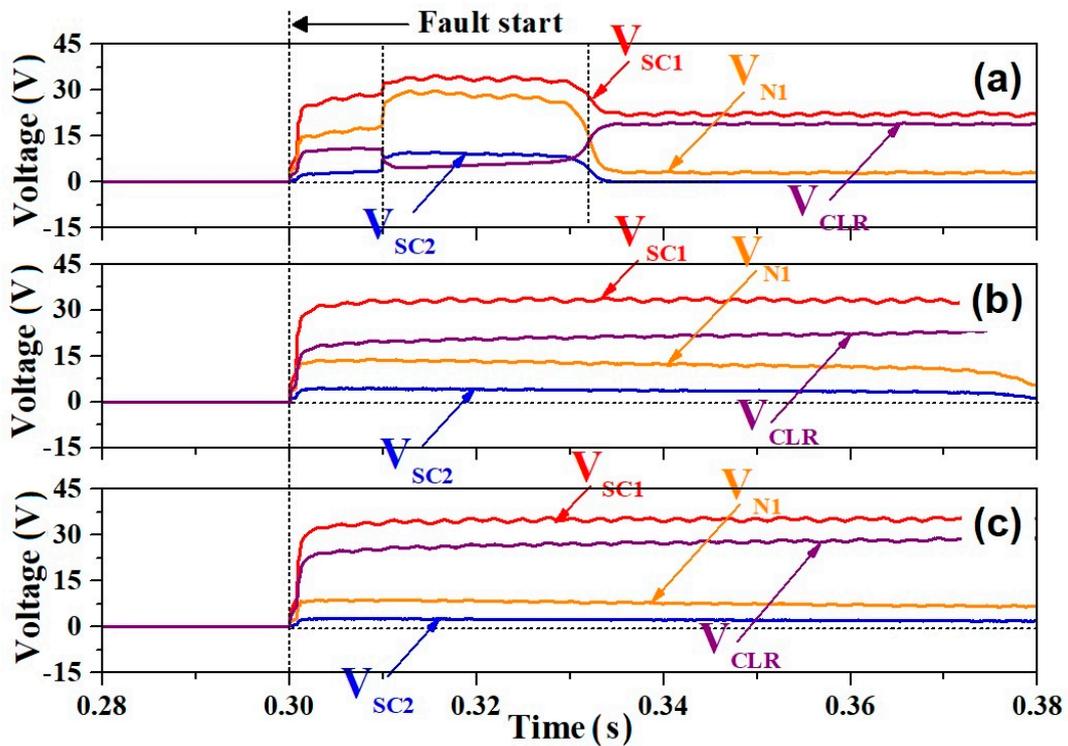


Figure 5. Voltage waveforms due to the CLR's resistance: (a) $R_S = 1.15 \Omega$; (b) $R_S = 2.3 \Omega$; (c) $R_S = 4.6 \Omega$.

Before about 0.31 s after the DC fault occurred, as indicated with the vertical dotted line in Figure 4a, the current in R_{SC1} (I_{SC1}) sharply decreased and the currents in the primary winding and R_{SC2} (I_{N1} , I_{SC2}) increased. On the other hand, at the time of 0.31 s since the fault current occurred, the current in R_{SC2} (I_{SC2}) together with the current of the primary winding (I_{N1}) sharply started to decrease and the current in R_{SC1} (I_{SC1}) smoothly started to increase. After about 0.33 s, as indicated with another vertical dotted line in Figure 4a, the superconducting element R_{SC2} was seen to be recovered into the superconducting state because the voltage (V_{SC2}) dropped to the zero value, as seen in Figure 5a, which made the current in R_{SC2} (I_{SC2}) to have a zero value. Despite the zero current in R_{SC2} , the non-zero current in the primary winding (I_{N1}) is thought to be a result of the magnetizing inductance of the iron core comprising the transformer.

From the viewpoint of the electrical circuit, the DC SFCL with a parallel structure, which consisted of both the R_{SC1} and the transformer, including R_{SC2} , has been analyzed to be applied to increase the limited current in the load (I_{FCL}) because the load current can be divided into the superconducting element R_{SC1} (I_{SC1}) and the primary winding of the transformer (I_{N1}) after the current in R_{SC1} by its quench occurrence is limited. The current in R_{SC2} (I_{SC2}) was almost three times that of the current in the primary of the transformer (I_{N1}) by the turn ratio of the transformer.

In case of $R_S = 2.3 \Omega$, as shown in Figure 4b, although the currents flowing into the two superconducting elements (I_{SC1} , I_{SC2}) seemed to simultaneously exceed the critical current, the current in the primary winding of the transformer (I_{N1}), i.e., the current of the CLR, did not largely increase in the initial fault time because of the larger resistance of the CLR than the CLR with 1.15Ω . It makes the voltage across the primary winding of the transformer (V_{N1}) steadily decreasing, as seen in Figure 5b. In case of $R_S = 4.6 \Omega$, the current and the voltage waveforms were observed to be almost similar to the case of $R_S = 2.3 \Omega$, as shown in Figures 4c and 5c, except that the amplitude of the induced voltage in the primary winding of the transformer (V_{N1}) was more smaller than in the case of $R_S = 2.3 \Omega$. Instead, the voltage across the CLR (V_{CLR}) was shown to have an opposite trend to the one in the primary winding of the transformer (V_{N1}).

Figure 6 shows the instantaneous power waveforms of R_{SC1} , R_{SC2} , and CLR due to the CLR's resistance. In the case of $R_S = 1.15 \Omega$, the initial larger power burden in the R_{SC1} superconducting element (P_{SC1}) directly after the fault occurrence could be observed to be shared with the CLR after the voltage of the R_{SC2} superconducting element (V_{SC2}) recovered into the zero value, as previously shown in Figure 5a. On the other hand, in the case of the CLR's resistance with a larger value ($R_S = 2.3 \Omega$, $R_S = 4.6 \Omega$) than $R_S = 1.15 \Omega$, the power burden in R_{SC1} with a CLR of $R_S = 4.6 \Omega$ was observed to be more larger than the one in R_{SC1} with a CLR of $R_S = 2.3 \Omega$, as seen in Figure 6a. On the other hand, in the case of R_{SC1} with a CLR of $R_S = 4.6 \Omega$, the power burden in R_{SC2} was more decreased than the one in R_{SC2} with a CLR of $R_S = 2.3 \Omega$, as compared in Figure 6b. In addition, a CLR with an $R_S = 2.3 \Omega$ had a little more of a power burden than the one with an $R_S = 4.6 \Omega$, as seen in Figure 6c.

From the above analysis, it was confirmed that a CLR with a larger resistance could derive the higher power burden in R_{SC1} and the lower power burden in the CLR as well.

Figure 7 shows the current waveform in the case that the component of the CLR is an inductance. Similar to the case that the component of the CLR is a resistance, as shown in Figure 5, the limited current in the DC SFCL (I_{FCL}) was observed to be divided into the current in R_{SC1} and the primary of the transformer (I_{SC1} , I_{N1}). On the other hand, unlike the CLR with the resistance, the current in the R_{SC2} superconducting element slowly increases after the DC fault occurrence, and then approaches the peak value ("3" point) only after it exceeds the critical current ("2" point). With a larger inductance of the CLR, the peak value of the current in R_{SC2} is observed to be decreased, as seen in Figure 7. On the other hand, after the current of R_{SC2} approaches the peak value, the approaching time into the zero value ("4" point) takes more time with a larger inductance of the CLR. However, despite the larger inductance of the CLR, the DC fault current limiting effect, after the current in R_{SC2} approaches the peak value, could be not seen, as compared to that in Figure 7c.

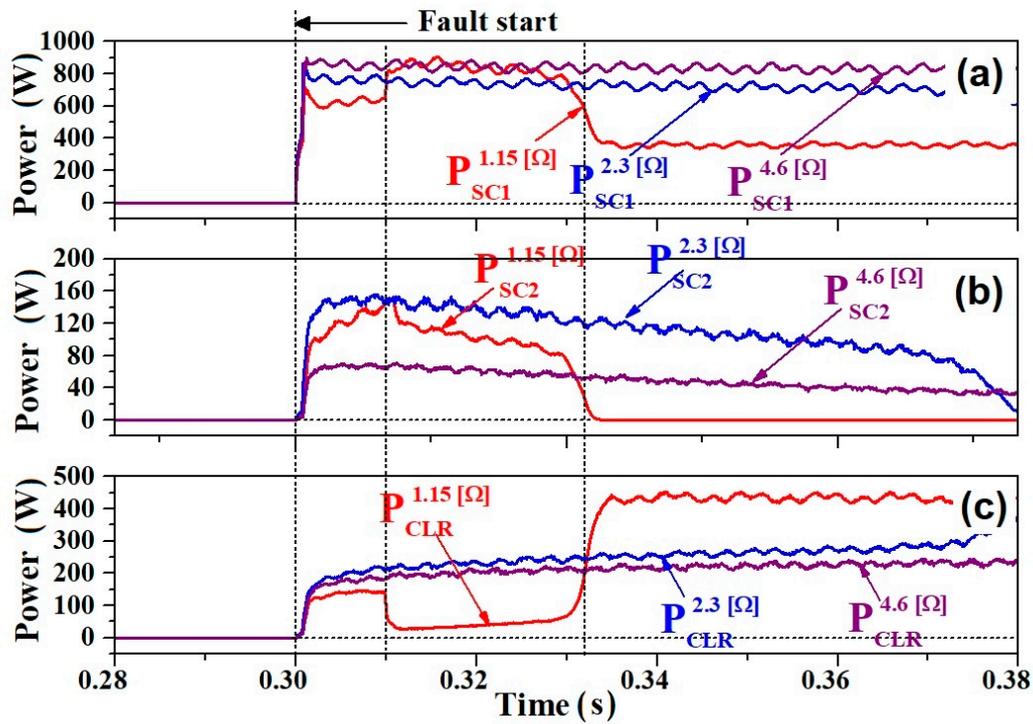


Figure 6. Instantaneous power waveforms due to the CLR’s resistance: (a) power burden arising from R_{SC1} element depending on the CLR’s resistance; (b) power burden arising from the R_{SC2} element depending on the CLR’s resistance; (c) power burden arising from the CLR depending on the CLR’s resistance.

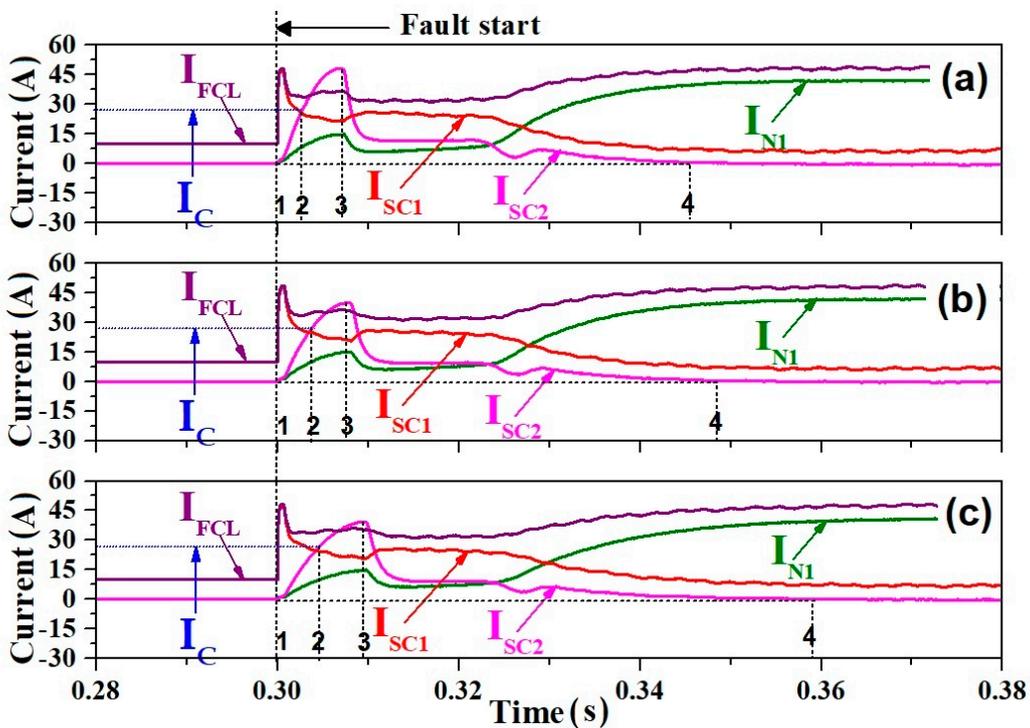


Figure 7. Current waveforms due to the CLR’s inductance: (a) $L_S = 6.6$ mH; (b) $L_S = 7.5$ mH; (c) $L_S = 10$ mH.

Figure 8 shows the voltage waveform in case that a component of the CLR was selected as the inductance. After the DC fault occurs, the voltage across the CLR (V_{CLR}), which sharply increased into

the plus peak value, jumped down into the minus peak value through the zero value and then, again, decreased into the zero value. It is thought to be related to the variation in the current in the primary winding of the transformer (I_{N1}), i.e., the current in the CLR due to the resistance generation of the superconducting element (R_{SC2}). Although the resistances in R_{SC1} and R_{SC2} gradually decrease after the current in R_{SC2} (I_{SC2}) approaches a zero value (“4” point), as shown in Figure 7, the fault current (I_{FCL}) can be seen to be mostly divided into the primary winding of the transformer (I_{N1}) and the R_{SC1} superconducting element (I_{SC1}).

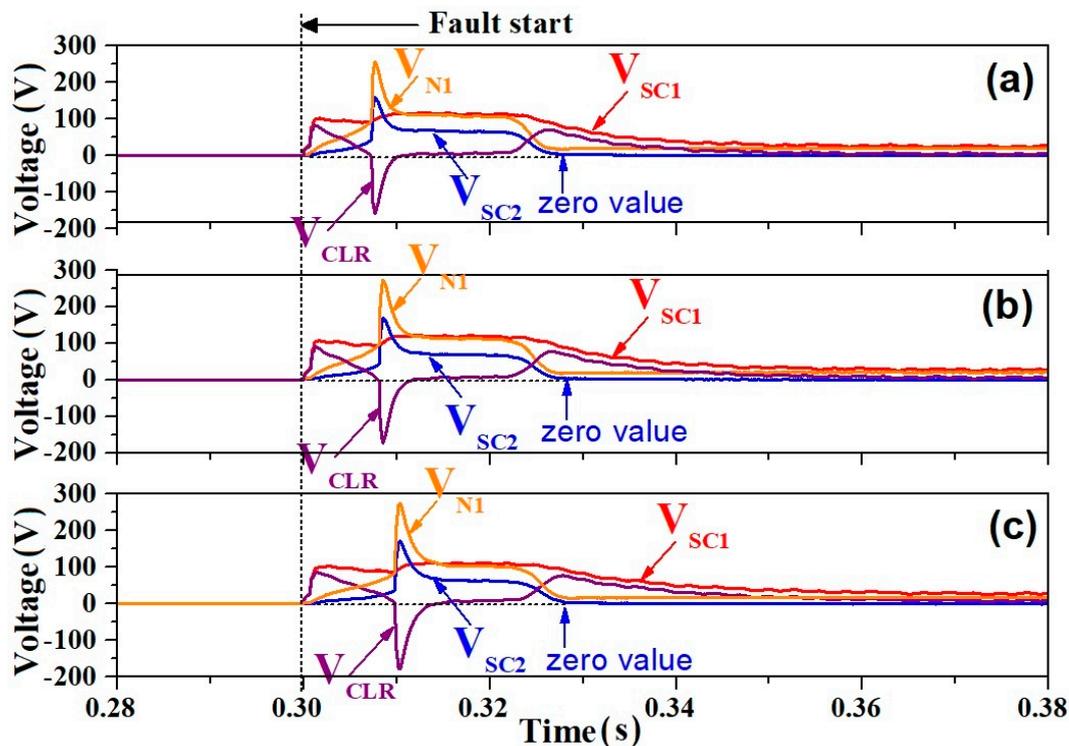


Figure 8. Voltage waveforms due to the CLR’s inductance: (a) $L_S = 6.6$ mH; (b) $L_S = 7.5$ mH; (c) $L_S = 10$ mH.

Figure 9 shows the instantaneous power waveforms of R_{SC1} , R_{SC2} , and the CLR due to the CLR’s inductance. As the inductance of the CLR comprising the DC SFCL increases from 6.6 mH to 10 mH, the time in which the instantaneous power in the R_{SC2} superconducting element (P_{SC2}) arrives to its first peak value is seen to be delayed. Unlike the CLR with the resistance, as shown in Figure 6, the power burdens in R_{SC1} and R_{SC2} (P_{SC1} , P_{SC2}) were shown to be increased (higher). On the other hand, after the voltage in R_{SC2} (V_{SC2}) decreases and drops down to a zero value (as seen in Figure 8), the power burden in the R_{SC2} superconducting element (P_{SC2}) also disappears—almost at the same time—regardless of the inductance value of the CLR, as displayed in Figure 9b.

Figure 10 shows the DC fault current waveforms of the DC SFCL using the transformer according to a component of the CLR. As described in the above figure, the CLR with the inductance has little effect on the DC fault current limiting operation of the DC SFCL using a transformer, except for the initial fault occurrence period in which the DC fault current rises up. The resistance generations of the two superconducting elements (R_{SC1} , R_{SC2}) are thought to be just contributed to the DC current limiting operation flowing into each superconducting element. On the other hand, the CLR with the resistance, if its resistance is higher, was confirmed to have an effective DC fault current limiting operation through the resistance generation of the two superconducting elements.

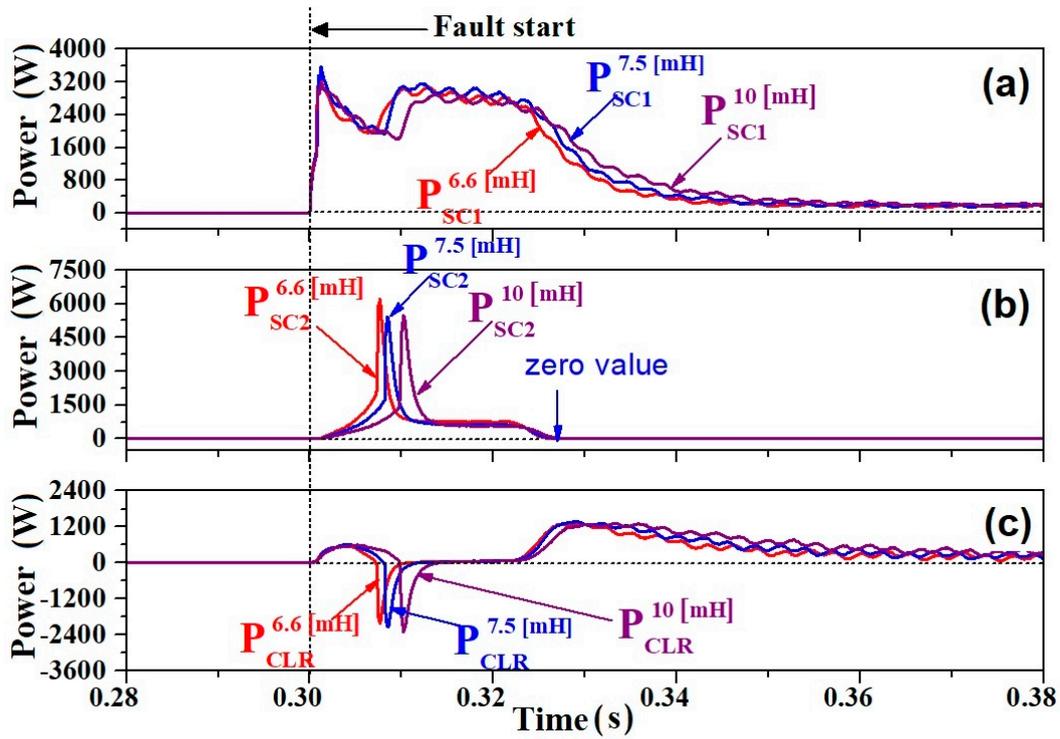


Figure 9. Instantaneous power waveforms due to the CLR’s inductance: (a) power burden arising from the R_{SC1} element depending on the CLR’s inductance; (b) power burden arising from the R_{SC2} element depending on the CLR’s inductance; (c) power burden arising from the CLR depending on the CLR’s inductance.

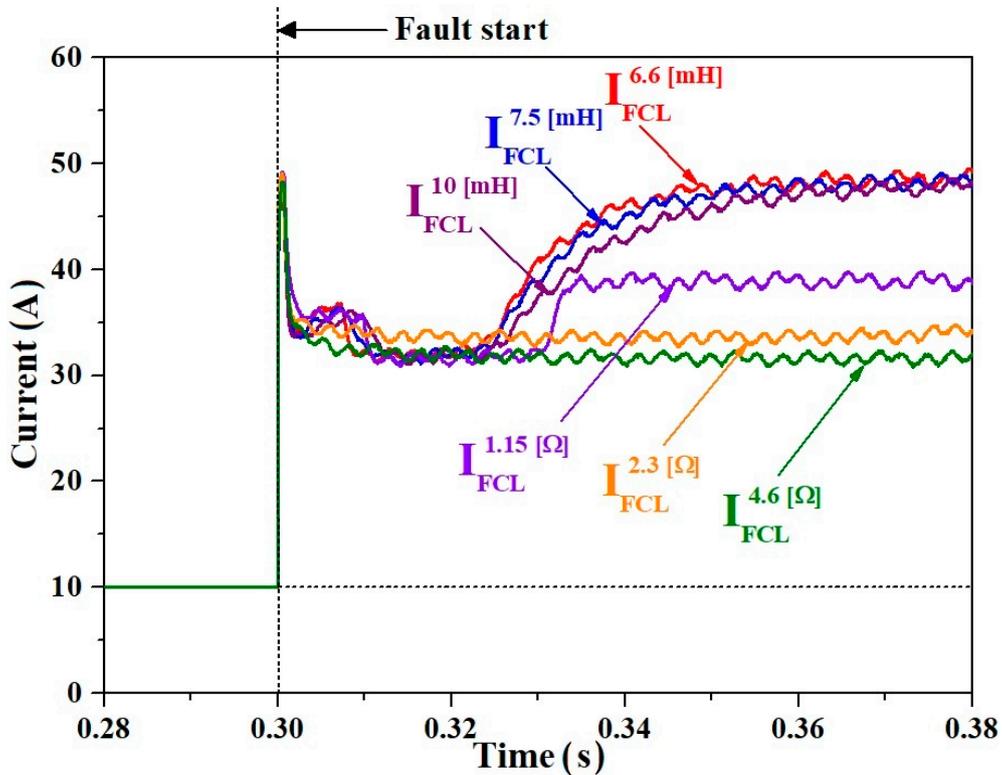


Figure 10. Comparative DC fault current waveforms of the DC SFCL using a transformer dependent on the CLR’s component.

The instantaneous power waveforms of the DC SFCL using the transformer according to the CLR component are also shown in Figure 11. The larger power burden in the DC SFCL with the CLR of the inductance, for the transient initial fault period, was analyzed to be much more focused on two superconducting elements, which agreed with the analysis from Figure 9. It was found that the DC SFCL with the CLR of the resistance had shown the more effective DC fault current limiting operation through the resistance generation of the two superconducting elements together with the lower power burden of the DC SFCL.

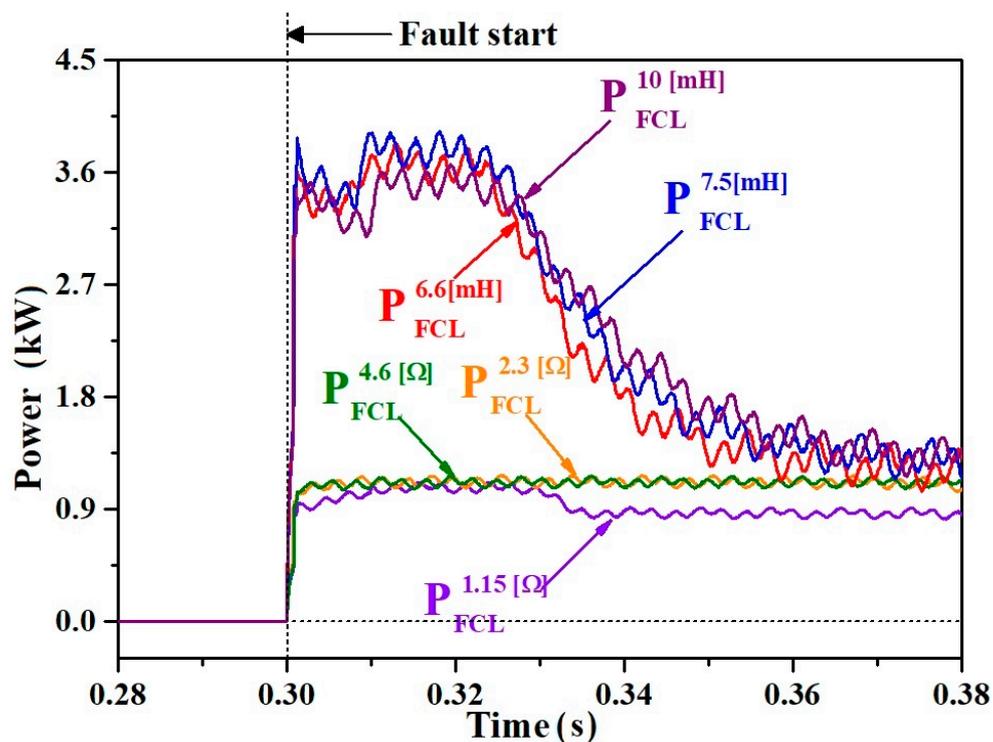


Figure 11. Comparative instantaneous power waveforms of the DC SFCL using a transformer dependent on the CLR's component.

4. Conclusions

In this paper, as one of the DC SFCLs with two triggering current levels, the DC SFCL using a transformer was suggested, and its DC fault current limiting characteristics due to the component of the CLR comprising the DC SFCL using a transformer were analyzed.

In case of the DC SFCL with the CLR as the resistance, the quench in the two superconducting elements almost simultaneously occurred, and the DC fault current could be limited through the slowly increased resistance generation after the sharp increase in the two superconducting elements. Furthermore, the DC SFCL with the CLR, designed with a larger resistance, could derive the higher power burden in R_{SC1} and the lower power burden in CLR.

On the other hand, the DC SFCL with the CLR as the inductance had little effect on the DC fault current limiting operation, although the initial rising of the DC fault current could be suppressed. In addition, the power burdens of R_{SC1} and R_{SC2} in the DC SFCL with the CLR as the inductance were shown to be increased higher than the one with the CLR as the resistance, regardless of the inductance value of the CLR.

In the future, the DC fault current limiting characteristics of the DC SFCL, which has an advantage from the point of view of the DC fault current limiting operation and the DC power burden, will be reported.

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Conflicts of Interest: The authors declare no conflict of interest.

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