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4H-SiC Double-Trench MOSFET with Side Wall Heterojunction Diode for Enhanced Reverse Recovery Performance

Junghun Kim and Kwangsoo Kim *

Department of Electronic Engineering, Sogang University, Seoul 04107, Korea; a0724a@naver.com
* Correspondence: kimks@sogang.ac.kr; Tel.: +82-2-705-8913

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Abstract: In this study, a novel 4H-SiC double-trench metal-oxide semiconductor field-effect transistor (MOSFET) with a side wall heterojunction diode is proposed and investigated by conducting numerical technology computer-aided design simulations. The junction between P+ polysilicon and the N-drift layer forming a heterojunction diode on the side wall of the source trench region suppresses the operation of the PiN body diode during the reverse conduction state. Therefore, the injected minority carriers are completely suppressed, reducing the reverse recovery current by 73%, compared to the PiN body diodes. The switching characteristics of the proposed MOSFET using the heterojunction diode as a freewheeling diode was compared to the power module with a conventional MOSFET and an external diode as a freewheeling diode. It is shown that the switching performance of the proposed structure exhibits equivalent characteristics compared to the power module, enabling the elimination of an external freewheeling diode in the power system.

Keywords: 4H-SiC; double trench; MOSFET; body diode; free-wheeling diode; reverse recovery; heterojunction diode; switching loss

1. Introduction

Silicon carbide (SiC), a wide-bandgap semiconductor, is considered a promising material for the next-generation power system [1–4]. It has a critical electric field of 3 MV/cm, which is ten times higher than that of silicon [5]. Therefore, the resistance of an extremely low drift region can be achieved for high voltage applications. In addition, the thermal conductivity of SiC is three times greater than that of silicon, which suppresses catastrophic failure during the high temperature operation of a device.

Among various SiC-based devices, as shown in Figure 1a, a 4H-SiC UMOSFET was preferred to provide a better tradeoff between breakdown voltage and on-resistance (R_{on}) than a planar VDMOSFET [6–9]. However, a UMOSFET has the disadvantage of a strong electric field in the bottom region of the gate, causing premature breakdown and oxide reliability problems. Recently, a double-trench UMOSFET (DT-UMOSFET) structure, shown in Figure 1b, has been developed to distribute the electric field concentrated on gate oxide to the deep p-type doping of the source region [10–12]. Thus, the DT-UMOSFET has better static performance than a conventional UMOSFET (C-UMOSFET). Consequently, the manufacturers are gradually adopting DT-UMOSFETs when using a power system.

In the power inverter and converter system, an external anti-parallel Schottky barrier diode (SBD) is widely used as a freewheeling diode [13–15]. To reduce the chip size of the module and parasitic components such as stray inductance, many efforts have been made to use the parasitic PiN body diode of a MOSFET as a freewheeling diode. However, there are some problems when using the PiN body diode of a SiC MOSFET. Because the parasitic PiN body diode is a bipolar device, unlike an

SBD, it has a much larger reverse recovery current and a higher turn-on voltage drop. Consequently, it causes the device to increase the overall switching loss of the system [16]. In addition, when the PiN body diode is conducted, a bipolar degradation effect may occur in which the parasitic NPN transistor is switched on [17,18]. Many approaches have been proposed to eliminate the issues mentioned above. The method of carrier lifetime control was adopted to reduce the concentration of minority carriers. However, this method can increase resistance in the drift region and cause metallization contamination [19]. Moreover, Schottky diodes can be integrated directly into the MOSFET; however, this increases the leakage current due to the image charge of the metal–semiconductor junction, and requires an additional cell pitch that reduces the specific on-resistance [20,21]. Contamination by metal for Schottky contact can also occur.

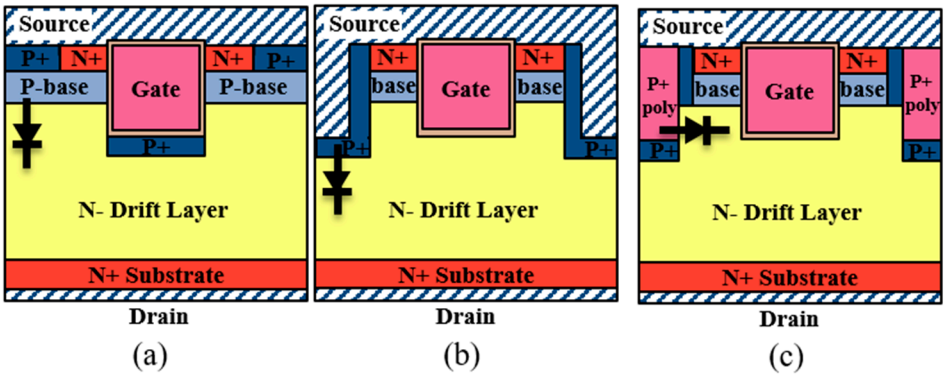

Figure 1. Schematic cross-sectional views of (**a**) C-UMOSFET, (**b**) DT-UMOSFET, and (**c**) DT-HJDUMOSFET.

In this paper, a novel DT-UMOSFET with a self-aligned sidewall heterojunction diode (DT-HJDUMOSFET) is proposed to solve the above-mentioned problem efficiently. The heterojunction diode (HJD) made of polysilicon and 4H-SiC behaves like an SBD due to unipolar action in reverse conduction [22]. Thus, the proposed device features some excellent body diode characteristics, such as reverse recovery and turn-on voltage, and eliminates the bipolar degradation effect. The HJD is integrated into the proposed device, eliminating the need for an additional anti-parallel SBD in the power inverter and converter systems. Hence, the proposed structure minimizes additional fabrication process steps; in particular, no photo-lithography mask is added.

2. Device Structure and Features

Figure 1c shows the schematic cross-sectional view of the proposed DT-HJDUMOSFET structure. Like a DT-UMOSFET, the source trench P+ shielding region of the DT-HJDUMOSFET disperses the electric field concentrated on the gate oxide to mitigate electric field crowding. Accordingly, the breakdown voltage of the DT-HJDUMOSFET can be increased compared to the C-UMOSFET. The main difference is the structure of the body diode. Compared to the DT-UMOSFET, the source trench region of the DT-HJDUMOSFET is deposited by P+ polysilicon. The HJD between the P+ polysilicon and N-drift region acts like an SBD, and the PiN diode is suppressed due to the low turn-on voltage of the HJD.

All structures have the same thickness and doping concentration of 16 μm and 3×10^{15} cm^{-3}, respectively, for a rated breakdown voltage of 1700 V. The length and doping concentration of the channel are 0.7 μm and 1×10^{17} cm^{-3}, respectively. The width and depth of the gate trench are 2.0 μm and 1.8 μm, respectively. The thickness of the gate oxide layer is 50 nm based on process limitation. The DT-UMOSFET and DT-HJDUMOSFET structures have the same width and depth of the source trench; these are 1.0 μm and 1.8 μm, respectively, to proceed simultaneously with the gate trench process.

Figure 2 shows the feasible self-aligned fabrication process steps of the DT-HJDUMOSFET by using TCAD process simulation. The doping concentration in Figure 2 is calculated only with activated

impurities. After the formation of source, base and P+ shielding regions using ion implantation, the source trench process is carried out to make the HJD region. The gate is formed by carrying out thermal oxidation and polysilicon deposition. In addition, P+ polysilicon is deposited to create a heterojunction between P+ polysilicon and the N-drift layer. This means that the self-aligned process that does not require an additional mask is introduced to compose HJD. Lastly, the metallization process is carried out to connect the source electrode. The photoresist has been omitted in Figure 2.

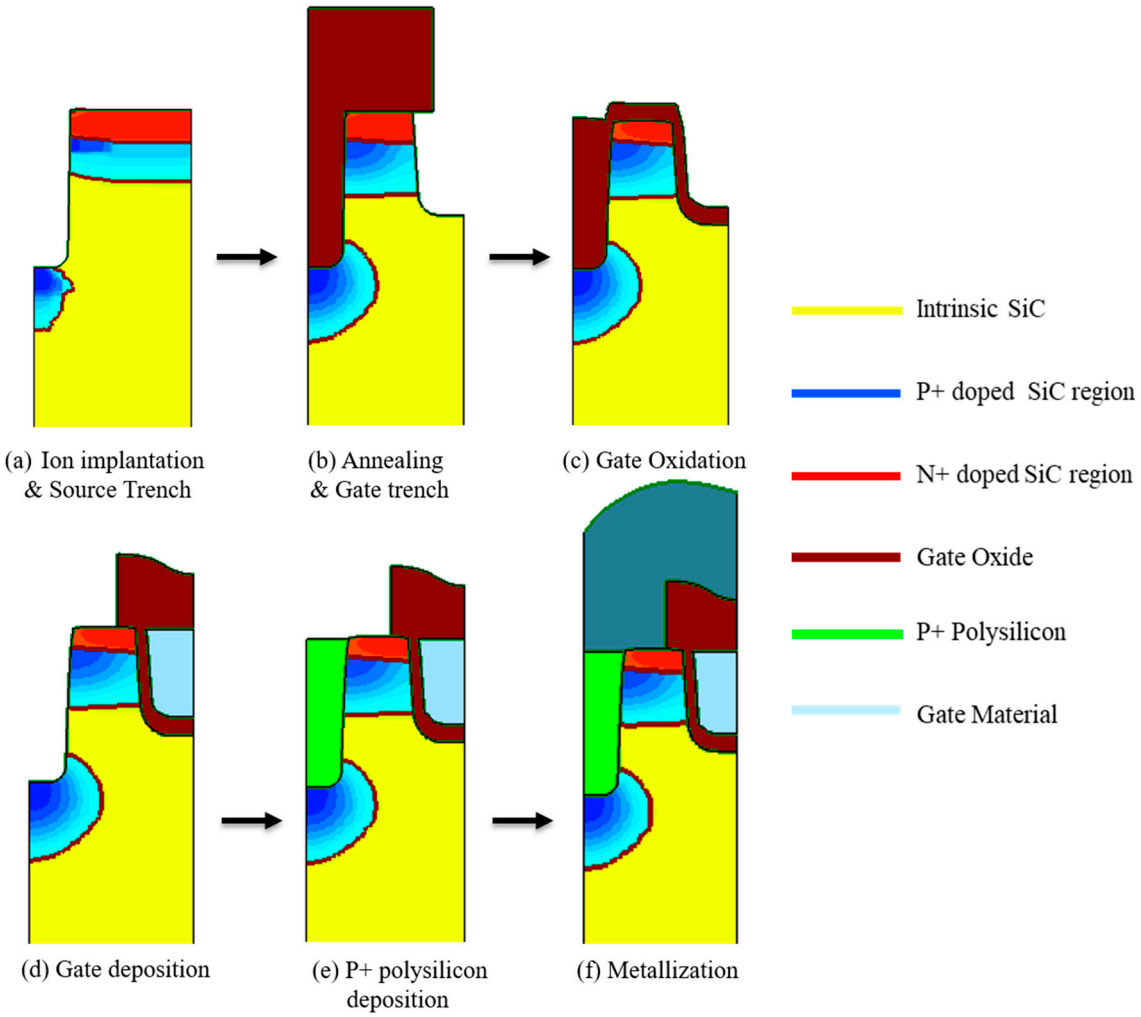

Figure 2. Proposed fabrication procedure of DT-HJDUMOSFET. (**a**) Forming source, base and P+ shielding region through ion implantation and source trench region, (b) annealing and trench gate region, (**c**) gate oxidation, (**d**) gate polysilicon deposition, (**e**) P+ polysilicon deposition to create heterojunction diode (HJD), (**f**) Metallization.

The energy band diagram of the body diode region of the DT-HJDUMOSFET is shown in Figure 3 to explain its body diode operation. Figure 3a shows the schematic view of diode portion in the DT-HJDUMOSFET. The gate and oxide regions are omitted in Figure 3a. There are two diode structures, PiN diode and HJD, along the lines of A-A′ and B-B′, respectively. As shown in Figure 3b,d, when the source-drain voltage is 0 V, there is a potential barrier height of electrons (ϕ_{Bn}) at 2.1 eV and 1.6 eV, respectively. Thus, the transport of the electrons and holes are prohibited due to the formation of a high potential barrier. When the source-drain voltage is 2 V, the energy band of the PiN diode part is shown in Figure 3c. There is still ϕ_{Bn} at 0.8 eV along the PN junction. Thus, no electron movement is generated to produce current.

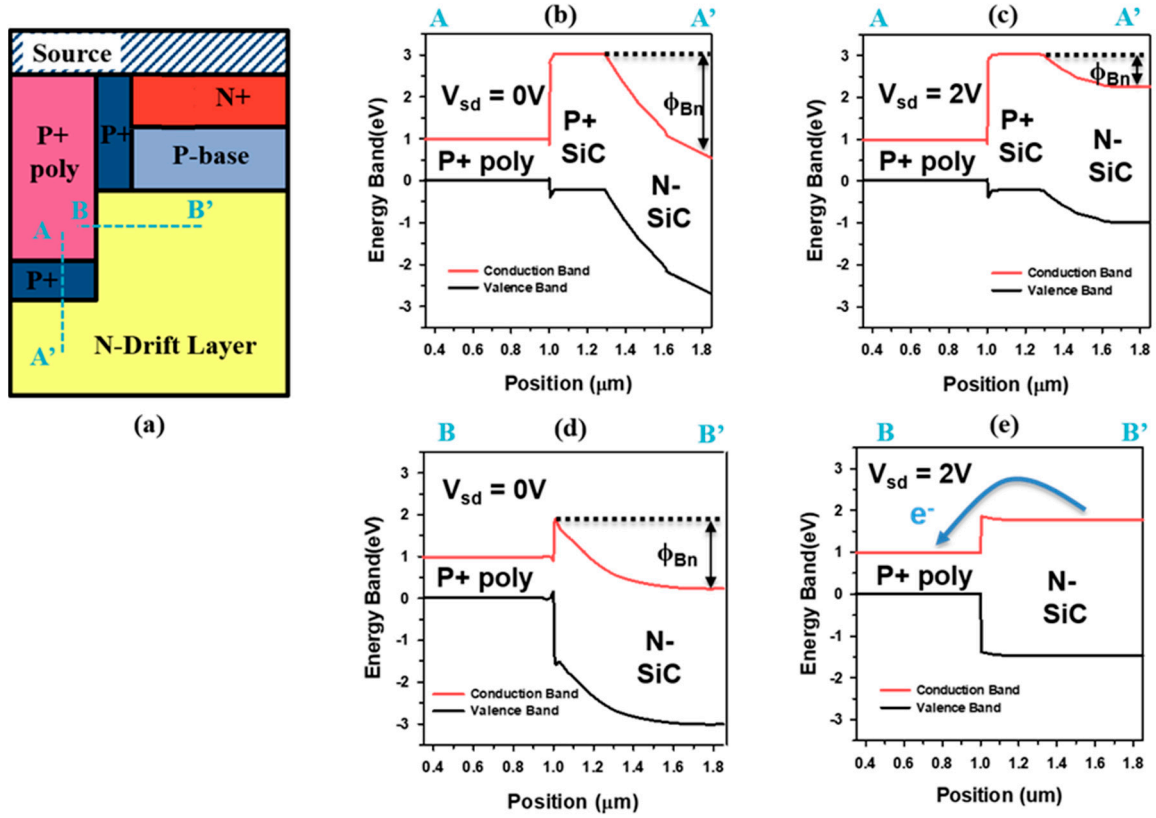

Figure 3. (**a**) Schematic cross-sectional view of DT-HJDUMOSFET's body diode region. Band diagram along A-A′ line with (**b**) V_{sd} = 0 V and (**c**) V_{sd} = 2 V, and along B-B′ line with (**d**) V_{sd} = 0 V and (**e**) V_{sd} = 2 V, respectively.

The differences in HJD compared to PiN diodes under the same conditions are shown in Figure 3e. The transfer of electrons is allowed from N-SiC to P+ polysilicon on the conduction band due to lowered ϕ_{Bn}. However, holes still face a high barrier height when moving to the N-SiC region. Therefore, only the electronic current consists of the body diode current and it acts as a unipolar device. This feature influences the characteristics of the device's body diode.

3. Results and Discussion

In this section, the results of the numerical simulations of three devices, shown in Figure 1, are presented to evaluate electrical characteristics. The characteristics of the devices were analyzed using the two-dimensional and mixed-mode technology computer-aided design (TCAD) simulation tool. The simulation includes the temperature-dependent Shockley–Read–Hall and Auger recombination. The mobility model includes doping-dependent, high-field saturation, and mobility degradation. In addition, anisotropic and incomplete impact ionization effects were considered in this model. TCAD simulation was performed through 2D finite element analysis (FEA) methodology.

3.1. Static Characteristics

Figure 4 shows the static characteristics such as breakdown voltage, on-resistance, and leakage current of the three devices. The forward conduction characteristics are obtained at V_{gs} = 15 V. The on-resistance is compared when the breakdown voltage of each structure is designed to be 1700 V by optimizing the thickness and doping concentration of the epi-layer of each structure. Because there is no JFET resistance between the trench bottom P+ shielding and base region, the DT-UMOSFET and DT-HJDUMOSFET have lower R_{on} (5.67 mΩcm^2) than the C-UMOSFET (16.55 mΩcm^2). In addition, the leakage current levels of the DT-UMOSFET and DT-UMOSFET are slightly higher than that of the

C-UMOSFET owing to the increased PN junction area. However, this difference is very small and can be neglected.

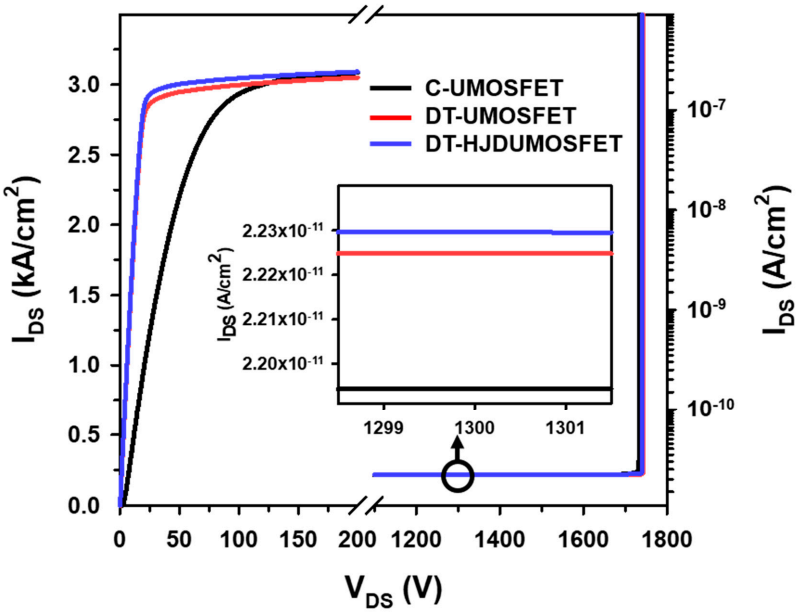

Figure 4. Static characteristics as forward conduction characteristics, breakdown voltages, and leakage current levels of C-UMOSFET, DT-UMOSFET, and DT-HJDUMOSFET.

Figure 5 shows the electric field distribution of the DT-HJDUMOSFET at V_{ds} = 1200 V. Because the critical electric field of silicon is ten times smaller than that of SiC, a large electric field should not be applied to the polysilicon region. As shown in Figure 5, the electric field crowding is clearly visible around the corner of the P+ shielding region. Thus, the P+ shielding region efficiently blocks the electric field applied to the polysilicon sides. Furthermore, the electric field in oxide should not exceed the safety limit (4 MV/cm [23]) at V_{ds} = 1200 V. The excess of safety limit affects the long-time reliability of the device, causing problems such as premature breakdown or hot carrier injection [24]. As shown in Figure 5, the density of the electric field at the gate oxide is less than 4 MV/cm owing to the dispersed field by P+ shielding at the source trench region. In particular, the DT-HJDUMOSFET is the device structure that has superior reliability with respect to high electric field distribution.

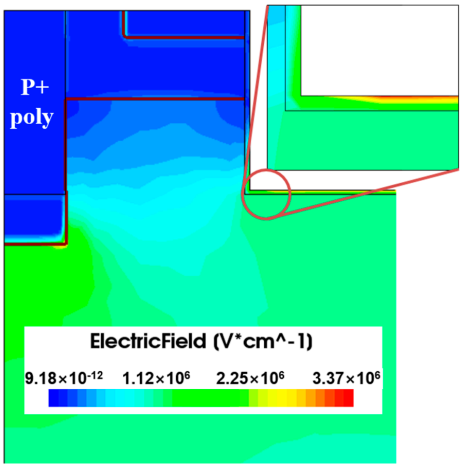

Figure 5. Electric field distribution of DT-HJDUMOSFET at V_{ds} = 1200 V. The magnified area is the bottom gate oxide.

3.2. Body Diode Characteristics

As the DT-HJDUMOSFET is used as a freewheeling diode, its body diode characteristics that can affect its properties of dynamic operation should be considered. The minority carrier lifetime of each device is 1.2 μs by default, and various models related to carrier lifetime are applied. In Figure 6, the density distributions of the minority carriers (holes) of the DT-UMOSFET and DT-HJDUMOSFET are shown. Unlike the DT-UMOSFET, the body diode of the DT-HJDUMOSFET acts like a unipolar device, as shown in the band diagram of Figure 2e. Therefore, the HJD is effective in suppressing minority carrier injection into the drift region. This feature improves characteristics such as thermal stability or reverse recovery of its body diode.

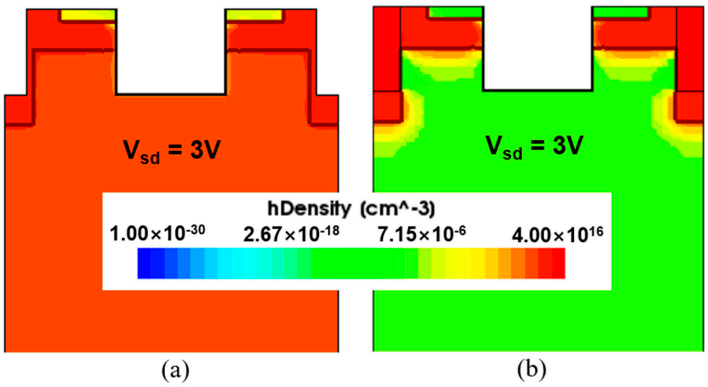

Figure 6. Density distributions of minority carriers (holes) at V_{sd} = 3 V of (**a**) DT-UMOSFET and (**b**) DT-HJDUMOSFET.

Figure 7 shows the reverse recovery current waveforms of the DT-UMOSFET and DT-HJDUMOSFET when load current is 100 A/cm^2. In the DT-UMOSFET, the total reverse recovery charge (Q_{rr}, 2419 nC/cm^2) is made up of injection current as the time derivative of the charge of injected carriers and junction current due to the discharge of junction capacitance. Therefore, the reverse recovery current (I_{rr}) is expressed as follows [25]:

$$I_{rr} = \frac{dQ_{inj}}{dt} + \frac{dQ_j}{dt} \quad (1)$$

where Q_{inj} is the charge of injected minority carriers, and Q_j is the charge of ionized dopant atoms stored in the voltage-dependent junction capacitance.

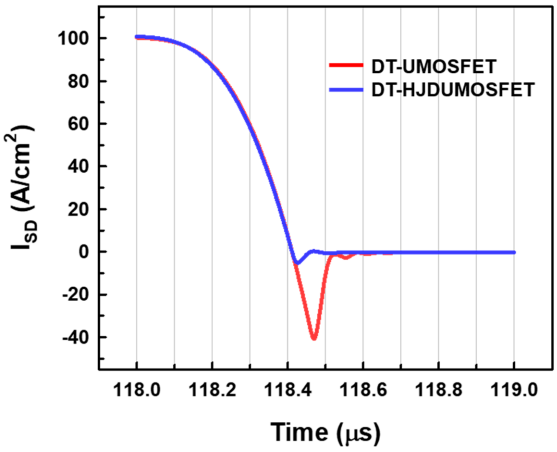

Figure 7. Reverse recovery current waveform of the body diode for DT-UMOSFET and DT-HJDUMOSFET.

In the case of DT-HJDUMOSFET, the total reverse recovery charge (649 nC/cm^2) is significantly reduced by 73% due to the suppressed injection of minority carriers, as shown in Figure 6b. The total current consists of only the junction current from the discharging junction capacitance. The improved reverse recovery characteristics contribute to better dynamic switching loss in the power system.

In Figure 8, the forward conduction characteristics of the body diode are shown according to variations in the temperature of both structures. As shown in Figure 8, the DT-HJDUMOSFET has a lower turn-on voltage than the DT-UMOSFET. In HJD, the on-state voltage drop (V_F), including the resistive voltage drop, is expressed as follows:

$$V_F = \frac{kT}{q}\ln\left(\frac{J_F}{J_S}\right) + R_S J_F \quad (2)$$

where J_F is the forward current density, J_S is the reverse saturation current density, R_S is the total series-specific resistance, k is the Boltzmann constant, and T is the thermodynamic temperature. J_S is derived as follows [26]:

$$J_S = AT^2 \exp\left(-\frac{q\varnothing_b}{kT}\right) \quad (3)$$

where A is the Richardson's constant, and ϕ_b is the barrier height of the junction between SiC and polysilicon.

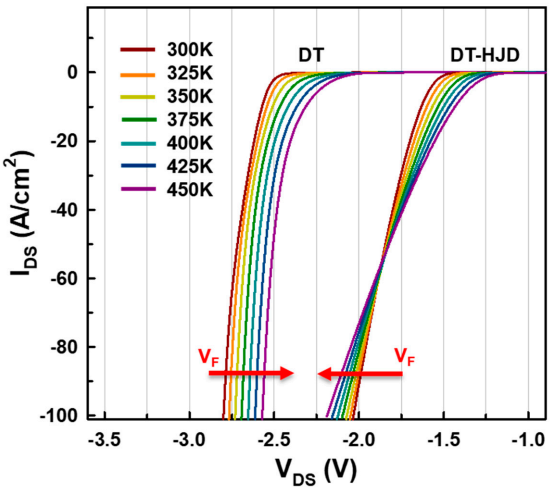

Figure 8. Forward conduction characteristics of the body diode of DT-UMOSFET and DT-HJDUMOSFET in temperature range of 300 K to 450 K.

At a low current level, the voltage drop is associated with the barrier being reduced by the rise in temperature. On the contrary, at a high current level, the resistance of the drift region increases with the rise in temperature, owing to the degradation of electron mobility, and consequently, the on-state voltage drop increases. For the nominal operating current density of 100 A/cm^2, the on-state voltage drop has a positive temperature coefficient, indicating a stable operation of the freewheeling diode.

Furthermore, when the body diode is switched on, the bipolar degradation effect may occur due to a voltage drop across the N+ source and p-base region. However, in the case of DT-HJDUMOSFET, the bipolar degradation effect is suppressed because there is no current flow into the p-base region. Therefore, it is free from the bipolar degradation that is commonly encountered when the body diode is actively used. Thus, we can eliminate an external freewheeling diode, such as an SBD. The comprehensive characteristics of the body diodes of the DT-UMOSFET and DT-HJDUMOSFET are shown in Table 1.

Table 1. Comparison of body diode characteristics.

	DT-UMOSFET	DT-HJDUMOSFET	Unit
Q_{rr}	2419	649	nC/cm^2
t_{rr}	110	47	ns
V_F	2.78	2.02	V
TC [a]	Negative	Positive	-
BD [b]	Yes	No	-

[a] TC: Temperature coefficient of voltage drop; [b] BD: Bipolar degradation effect; Q_{rr}, t_{rr}, and V_F are measured at room temperature.

3.3. Switching Characteristics

In this section, the switching characteristics of the devices are discussed in detail. Figure 9 shows the simulation test circuits for evaluating the switching performance of the devices. The double pulse test circuit is used to test switching characteristics [27]. We analyzed the waveform of the lower-side MOSFET. Instead of using a freewheeling diode such as an SBD, we use the MOSFET as the same type of bottom device. We simulate a single unit, as shown in Figure 9a,c, and a power module combining the DT-UMOSFET and SBD, as shown in Figure 9b. The load inductor is used to replicate circuit conditions in the converter design. The cell area of all devices under test is set to 1.0 cm^2. The gate resistance R_g is set to 1Ω, and the gate turn on-off voltages are 15 V and −5 V, respectively. The load inductance L_d is set to 400 μH, and V_{DD} is 800 V.

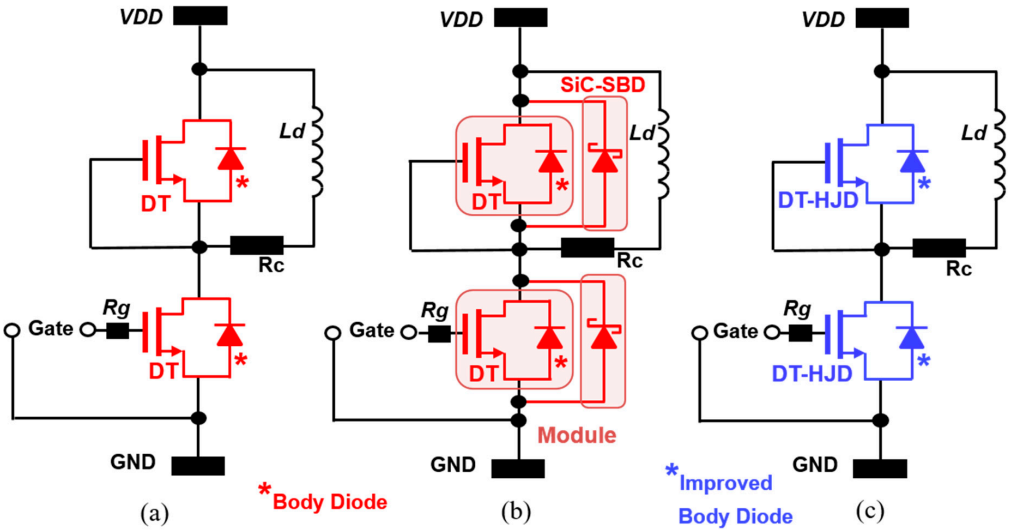

Figure 9. Equivalent test circuit configuration for switching characteristics of (**a**) DT-UMOSFET, (**b**) power module composed of DT-UMOSFET and SBD, and (**c**) DT-HJDUMOSFET.

The switching curves of three cases are shown in Figures 10 and 11. The comprehensive switching characteristics are shown in Table 2. The energy losses during the switching transition is expressed as follows [16]:

$$E_{on}, E_{off} = \int_0^t V_{DS} I_{DS} dt \quad (4)$$

where t is the switching time delay, E_{on} and E_{off} are the energy losses at turn-on and turn-off transient, respectively. The time delay is required to charge and discharge the capacitance of the devices until the gate voltage reaches the Miller plateau value. In the DT-HJDUMOSFET, the integrated HJD does not affect the charge or capacitance of the gate of the device compared to the DT-UMOSFET, and the switching time does not differ in the three cases. Therefore, the energy losses of the devices in the three cases are mainly affected by I_{DS}.

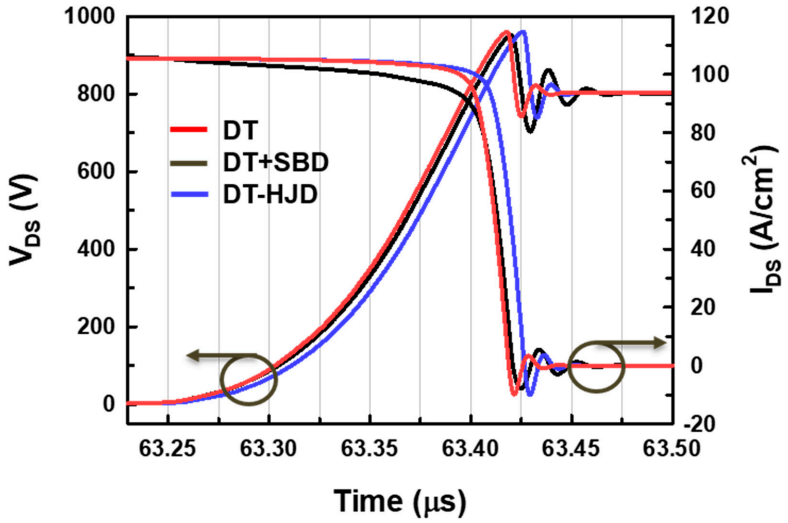

Figure 10. Turn-off curves of DT-UMOSFET, power module composed of DT-UMOSFET and SBD, and DT-HJDUMOSFET.

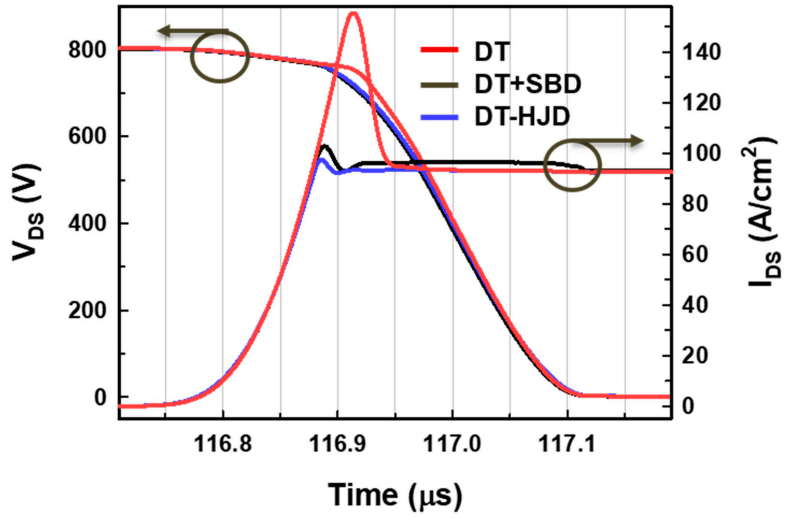

Figure 11. Turn-off curves of DT-UMOSFET, power module composed of DT-UMOSFET and SBD, and DT-HJDUMOSFET.

Table 2. Comparison of switching characteristics.

	DT	DT+SBD	DT-HJD	Unit
E_{off}	0.389	0.384	0.391	mJ/cm^2
E_{on}	0.467	0.376	0.365	mJ/cm^2
I_{peak}	148.9	102.4	96.8	A/cm^2
ND [a]	2	4	2	-

[a] ND: Number of devices in the test circuit.

In the turn-off waveform, the upper-side device, acting as a freewheeling diode, is switched to the forward conduction state. Therefore, there is no current overshoot owing to the reverse recovery charge of the freewheeling diode from the upper-side device, as shown in Figure 10. Therefore, the differences in E_{off} of the three cases are negligible.

By contrast, in the turn-on waveform, the reverse recovery current from the upper-side device affects the switching characteristics of the lower MOSFET, as shown in Figure 11. This increases the current overshoot of the DT-UMOSFET to a great extent. Therefore, the DT-UMOSFET shows a

significant increase in energy loss owing to current overshoot. In our test circuits, the peak current level in turn-on transient (I_{peak}) of 148.9 A/cm^2 and E_{on} of 0.467 mJ/cm^2 are obtained. As shown in Figure 9b, this problem can be addressed by arranging the freewheeling diode, such as the SBD, in parallel, as before. In the power module, current overshoot is suppressed due to the lower reverse recovery current of SBD. As a result, I_{peak} (102.4 A/cm^2) and E_{on} (0.376 mJ/cm^2) are significantly improved.

Meanwhile, the DT-HJDUMOSFET that is not combined with an anti-parallel freewheeling diode does not have high current overshoot because its body diode has a low reverse recovery charge like SBD. In addition, the slightly improved levels of I_{peak} (96.8 A/cm^2) and E_{on} (0.361 mJ/cm^2) are obtained against the power module despite the reduced number of devices in the test circuit, as shown in Figure 9. Compared to the power module, the usage of DT-HJDUMOSFET has an advantage in the removal of parasitic components, such as stray inductance, while achieving an improved performance. Therefore, the DT-HJDUMOSFET structure can play a critical role in the development of advanced power device technology.

4. Conclusions

A novel 4H-SiC double-trench MOSFET with side wall heterojunction diode (DT-HJDUMOSFET) is proposed, and its advantages are analyzed and verified by conducting numerical TCAD simulations. Compared to the DT-UMOSFET, the proposed DT-HJDUMOSFET exhibits a similar specific R_{on} of 5.67 mΩcm^2, breakdown voltage of 1700 V, and does not have a reliability problem with respect to high electric field distribution. Due to the unipolar action of HJD like an SBD, the DT-HJDUMOSFET exhibits a reverse recovery charge that was significantly reduced by 73%, including a positive temperature coefficient of forward voltage drop, compared to the DT-UMOSFET. As a result, the DT-HJDUMOSFET shows enhanced switching characteristics, such that E_{on} and I_{peak} are decreased by factors of ~1.29 and ~1.54, respectively. In addition, compared to the power module configured in parallel with the DT-UMOSFET and SBD, the proposed structure does not degrade the switching performance of the device. Therefore, when we design a power converter circuit, the proposed device structure can reduce the chip size by eliminating the freewheeling diode and remove the parasitic component without performance degradation.

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Conflicts of Interest: The authors declare no conflict of interest.

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