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A Topology Synthetization Method for Single-Phase, Full-Bridge, Transformerless Inverter with Leakage Current Suppression Part I

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Abstract: Single-phase full-bridge transformerless topologies, such as the H5, H6, or the highly efficient and reliable inverter concept (HERIC) topologies, are commonly used for leakage current suppression for photovoltaic (PV) applications. The main derivation methodology of full-bridge topologies has been used based on both a DC-based decoupling model and an AC-based decoupling model. However, this methodology is not suited to the search for all possible topologies, and cannot verify whether they are inclusive. Part I of this paper will propose a new topology derivation methodology based on unipolar sinusoidal pulse width modulation (USPWM) to search all possible full-bridge topologies for leakage current suppression. First of all, a unified circuit model is proposed, instead of the DC- and AC-based models. Secondly, a mathematic method called the MN principle is then proposed to search for all possible topologies, and a derivation procedure is provided. It was verified that all existing topologies could be found using the proposed method; furthermore, seven new topologies were derived. The proposed topology derivation methodology is extended to search topologies under Double-Frequency USPWM (DFUSPWM). Twenty topologies under USPWM and four topologies under DFUSPWM have been derived.

Keywords: transformerless inverter; full bridge inverter; leakage current; NPC topology

1. Introduction

Photovoltaic (PV) sources are among the most promising renewable energy sources, providing clean and emission free energy [1,2]. The single-phase transformerless inverter system has popularly been used, as it has high efficiency and low cost compared with the transformer inverter system. However, the leakage current is a key issue [3–5]. The leakage current generated by PV parasitic capacitors must be limited to satisfy the VDC-AR_N 4015 [6], UL1741 [7], and VDE 0126-1-1 [8] standards. In single-phase, grid-tied inverter systems, half-bridge and full-bridge inverters are typical topologies, as shown in Figure 1.

The Common Mode (CM) current path for grid-tied, transformerless, PV inverter systems is illustrated in Figure 2 [9]. The leakage current path is equivalent to an LC resonant circuit, as shown in Figure 3 [10,11]. V_{AN} and V_{BN} are the voltage difference between points A and N and points B and N, respectively, and L1 and L2 are the output filter inductors. The equivalent CM voltage V_{ecm} is defined as:

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \frac{L2 - L1}{L2 + L1} \tag{1}$$

For the half-bridge inverter in Figure 1a, only the output filter inductor L1 is employed, so L2 = 0. Thus, (1) can be simplified as follows:

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} = V_{BN} \tag{2}$$
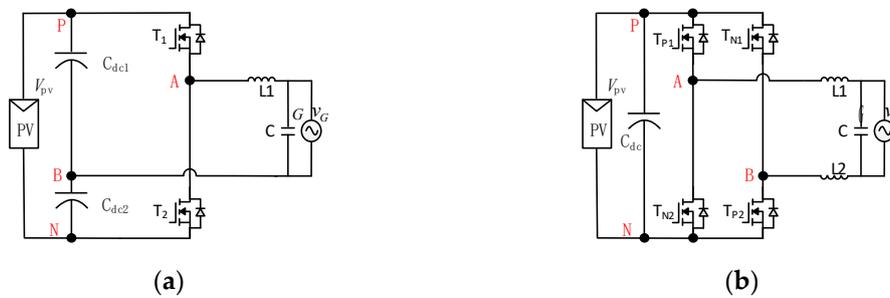
Figure 1. Topologies of (**a**) half-bridge inverter; and (**b**) full-bridge inverter (named H4).
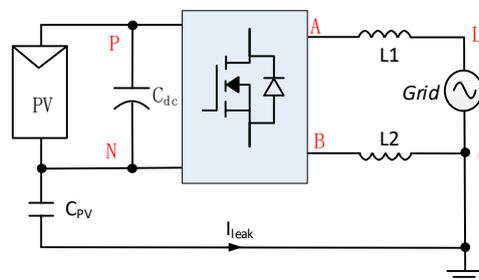
Figure 2. CM current path for transformerless PV inverter.
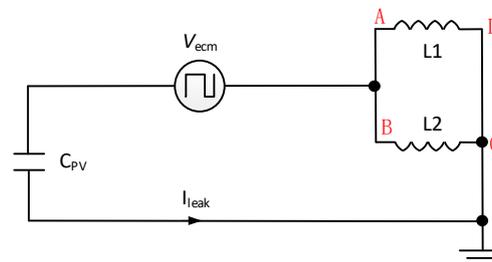
Figure 3. Equivalent circuit for the CM current path.

In Figure 1a, two capacitors, C_{dc1} and C_{dc2}, with equal capacitance values are in series. Capacitor C_{dc2} is charged or discharged by the grid current, and voltage V_{BN} equals half of the input voltage plus the voltage fluctuation of the line frequency. But the high-frequency fluctuation is so small that it can be ignored. So, V_{BN} is approximately constant. However, the DC voltage utilization of half-bridge inverters is only half that of full-bridge topologies, which means that a high-gain boost converter is needed as the first stage. As such, system efficiency and cost will be adversely affected. When two filter inductors are employed (L1 = L2), equation (1) can be simplified as:

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} - 0 = \frac{V_{AN} - V_{BN}}{2} \tag{3}$$

For the full-bridge topology, the leakage current can be eliminated if the common voltage is kept constant. Some state-of-the-art topologies such as H5 [12], HERIC [13,14], and H6 [10,15–43] have been developed. However, there is still a small leakage current because of the parasitic parameters. Thus, the Neutral Point Clamped (NPC) technique is introduced to achieve zero leakage current [44–48]. The full-bridge topologies are divided into DC decoupling model and AC decoupling model [49].

A few rules have been indirectly reported in the literature, as well as some topology synthetization methods such as those based on the DC- and AC-decoupling model, as well as topology derivation methods from H4, H5, and H6. None of the topology synthetization methods currently being used could answer the question of how many topologies could be derived, as there is no unified model. Part I of this paper focus on the topology derivation methodology to achieve small leakage current [50]. It proposes a unified model to replace the DC- and AC-decoupling models based on four rules, including two which have already been reported in the literature [51,52]. More importantly, a mathematic method called the "MN principle" is proposed to derive all the possible topologies. This only focuses on the number of switches in PC and NC modes. The MN principle also verifies that we only need to focus on M ≤ 4, N ≤ 4, because the remaining topologies can always be simplified into one of them. Thus, the method verifies that all possible topologies can be found. The derivation procedures are introduced to determine all the existing topologies and new topologies under unipolar sinusoidal pulse width modulation (USPWM) and Double-Frequency USPWM (DFUSPWM).

Part I of the paper is organized as follows. Section 2 describes the principles of the unified topology model. Section 3 introduces topology derivation under USPWM. The topology derivation under DFUSPWM is introduced in Section 4. Part I of the paper is concluded in Section 5.

2. Principle of Unified Topology Model and Symmetric Methodology

Figure 4 shows the full-bridge topology and a simplified schematic diagram.

| (a) | (b) |
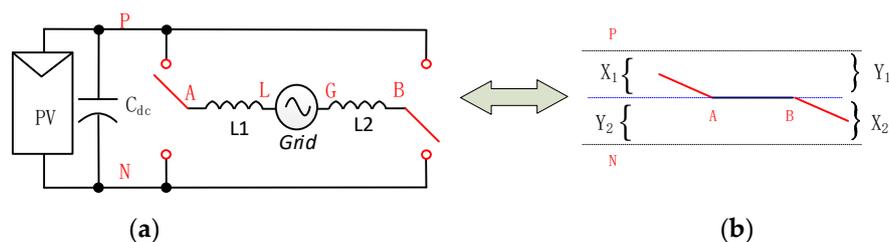
Figure 4. (**a**) Full-bridge topology; (**b**) Simplified schematic diagram of full-bridge topology.

In Figure 4a, point P and point N indicate the positive and negative DC bus terminals, respectively, and point A and point B indicate the first and second arm terminals, respectively. The semiconductor switches are always used to connect or disconnect points P and N to points A and B. Figure 4b shows a simplified schematic diagram of the full-bridge topology. Switches T_{PA}, T_{NA}, T_{PB}, and T_{NB} are the equivalent switches between points P and A, between N and A, between P and B, and between N and B, respectively. It should be noted that each equivalent switch can be a single active switch or several active switches connected in series. V_{PN} is the input voltage. The number of switches between points P and A is X_1, between points B and N is X_2, between points P and B is Y_1, and between points N and A is Y_2.

2.1. Principle of USPWM

Figure 5 shows the principle of USPWM. The differential-mode voltage V_{AB} has three levels: $+V_{PN}$, 0, and $-V_{PN}$. There are four modes in a total line-frequency period. The inverter is working in positive conduction (PC) mode and negative conduction (NC) mode when V_{AB} equals to $+V_{PN}$ and $-V_{PN}$. There are two modes if $V_{AB} = 0$: one is the positive freewheeling (PF) mode when the grid current is positive, and the other is the negative freewheeling (NF) mode when the grid current is negative.
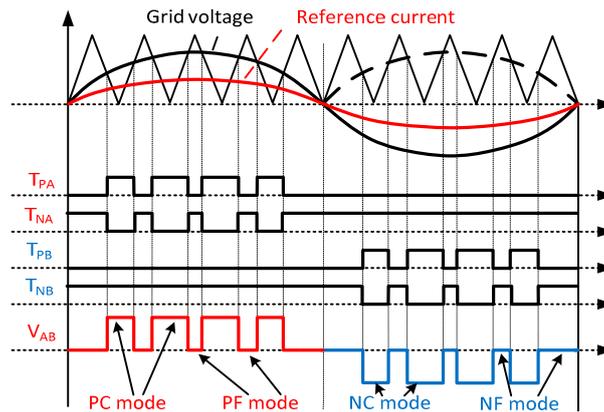
Figure 5. The principle of USPWM.

2.2. Unified Topology Model

Figure 6 shows four modes under USPWM based on the conventional H4 full-bridge topology. As shown in (4), the CM voltage, V_{cm}, is half the input voltage in PC and NC modes, equaling either input voltage V_{PN} or zero in PF mode and NF mode.
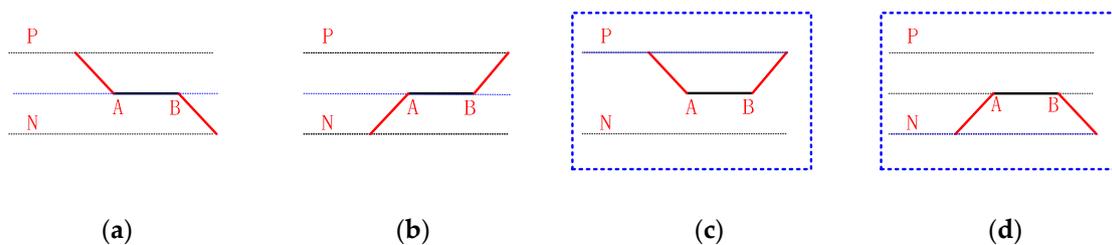
Figure 6. Four modes of H4 topology under USPWM. (**a**) PC mode; (**b**) NC mode; (**c**) PF mode; (**d**) NF mode.

The CM voltage is not constant at switching frequency, which results in high-frequency leakage current.

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} = \begin{cases} = \frac{V_{PN}}{2} & \text{PC mode or NC mode} \\ = V_{PN} \text{ or } 0 & \text{PC mode or NC mode} \end{cases} \tag{4}$$

To minimize the leakage current, the CM voltage must be kept constant. In PC and NC modes, the CM voltage is equal to half of the DC voltage. Thus, the main objective is to keep the CM voltage also being clamped to half of the input voltage in both freewheeling modes (PF and NF).

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} = \begin{cases} = \frac{V_{PN}}{2} & \text{PC mode or NC mode} \\ \cong \frac{V_{PN}}{2} & \text{PC mode or NC mode} \end{cases} \tag{5}$$

A unified topology model in PF and NF modes, as shown in Figure 7, is proposed [50]. All switches that connect points P and N are off. A controllable branch BĈA is added to flow positive current in PF mode, as shown in Figure 7c, and another controllable branch AD̂B flowing negative current is added in NF mode in Figure 7d. The voltage $V_{AB} = 0$ in PF and NF modes. To regulate the leakage current, a unified topology model should be constructed according to the following four rules in PF and NF modes:

Rule #1. Turn off all the connections to points P and N.

All switches connected to the positive DC bus (point P) and the negative DC bus (point N) must be off in the PF and NF intervals.

Rule #2. Short-circuit terminals A and B to get $V_{AB} = 0$.

A, B is short-circuited through one controllable branch in PF and NF modes. One switch and one diode connected in series are used for bidirectional voltage stress and output current flow, respectively. For example, switch T_{PF} and diode D_{PF} are connected in series for positive current flowing from point B to point A. Switch T_{NF} and diode D_{NF} are connected in series for negative current flowing from point A to point B.

Rule #3. Low cost implementation to satisfy Rule #2.

For low cost, the switches which are not connected to points P and N are on to provide output current flow path in PF and NF modes.

Rule #4. Combine PF and NF modes, and cut off the redundant components.

One PF mode and one NF mode implementation are combined to form a topology. The components which are connected in parallel are merged into one as best as they can be. For example, if an extra diode is connected in parallel with the body-diode of a switch, the former is saved to reduce cost, i.e., two switches in parallel are replaced by one switch.

Based on these rules, a systematic methodology called the "MN principle" is proposed, and will be discussed in the following subsection.
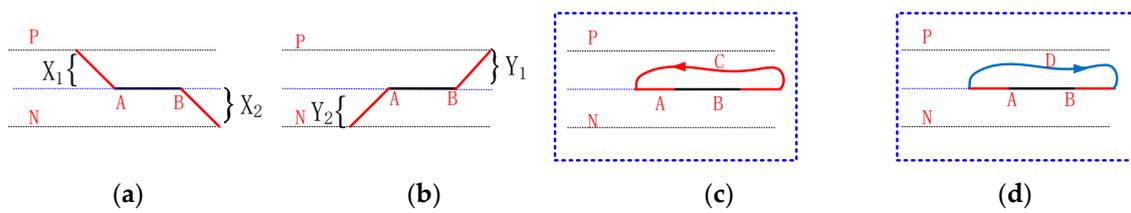
Figure 7. Four modes based on the unified topology under USPWM. (**a**) PC mode; (**b**) NC mode; (**c**) PF mode; (**d**) NF mode.

2.3. MN Principle

A systematic methodology, the MN principle, is proposed to derive all possible full-bridge topologies with small leakage currents. The MN principle can be described as follows. Let M denote the total number of switches that are turned on in PC mode. Since X_1 is the number of switches that connect point P to point A in PC mode, and X_2 is the number of switches that connect point B to point N in PC mode, then

$$M = X_1 + X_2 \tag{6}$$

Similarly, let N denote the total number of switches that are turned on in NC mode. Since Y_1 is the number of switches that connect point P to point B and Y_2 is the number that connect point A to point N in NC mode, then

$$N = Y_1 + Y_2 \tag{7}$$

According to rule #1, points A and B must be disconnected to points P and N, which means that at least one switch is needed for T_{PA}, T_{NB}, T_{PB}, and T_{NA}. Thus, the minimum values of X_1, X_2, Y_1, and Y_2 should be one, as shown in (8).

$$Min(X_1, X_2, Y_1, Y_2) \geq 1 \tag{8}$$

In order to disconnect A, B to P, N in PF and NF modes, according to rule #2, one switch and an extra diode connected in series can be used. Thus, there is one possible way that two switches are in series to implement the equivalent switches T_{PA}, T_{NB}, T_{PB}, and T_{NA}, respectively. For example, two switches, T_{P1} and T_{P2}, are connected in series between points P and A to implement the equivalent switch, i.e., T_{PA}. Switch T_{P1} remains off to disconnect points P and A, and switch T_{P2} remains on to construct the freewheeling branch in PF mode. If three switches, T_{P1}, T_{P2}, and T_{P3}, are in series to

implement the equivalent switch T_{PA}, switch T_{P1} remains off to disconnect points P and A, and two switches T_{P2} and T_{P3} are in series to construct the freewheeling branch in PF mode. However, the two switches, T_{P2} and T_{P3}, can be merged into a single switch. Thus, the maximum value for X_1, X_2, Y_1, and Y_2 are less than or equal to 2. Therefore,

$$Max(X_1, X_2, Y_1, Y_2) \leq 2 \tag{9}$$

From the above analysis, it may be observed that the MN principle can cover all possible topologies. Some of them can be simplified. Thus, only simplified topologies are introduced in the next section.

3. Topology Derivation under USPWM

In this section, several examples are provided to show how to derive topologies from the MN principle, such as M = 2 and N = 2, M = 2 and N = 3, or M = 3 and N = 2.

3.1. Case 1: M = 2 and N = 2

When M = 2 and N = 2, there is only one possibility to choose the combined values of X_1, X_2, Y_1, and Y_2, i.e., $X_1 = 1$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 1$.

Figure 8 shows four modes derived from $X_1 = 1$, $X_2 = 1$, $Y_1 = 1$ and $Y_2 = 1$. The PC and NC modes are shown in Figure 8a. One switch, T_{P1}, is adopted to connect points P and A due to $X_1 = 1$; meanwhile, another switch, T_{P2}, is viewed as a connection between points B and N on $X_2 = 1$ at PC mode. Similarly, two other switches, T_{N1} and T_{N2}, are added in NC mode with $Y_1 = 1$ and $Y_2 = 1$. Figure 8b shows PF mode. According to rule #1, four switches, i.e., T_{P1}, T_{P2}, T_{N1}, and T_{N2}, are off in PF mode. There is no available switch for output current flow. Thus, an extra switch, T_{P3}, and an extra diode, D_{p3}, are added in series. This is the only choice available for PF mode. Similarly, for NF mode, an extra switch, T_{N3}, and an extra diode, D_{N3}, are added in series for output current flow, as shown in Figure 8c.

(a)　　　　　　　　　　　　　　　　(b)　　　　　　　　　　　　　　　　(c)
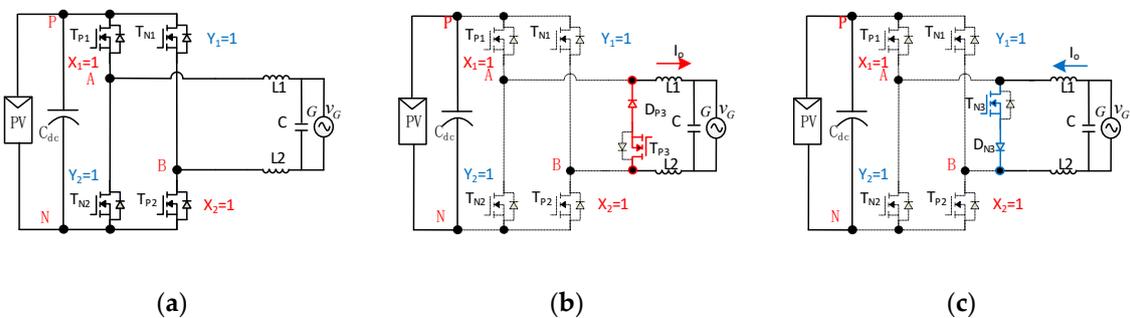
Figure 8. Four modes under $X_1 = 1$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 1$. (**a**) PC and NC modes; (**b**) PF mode; (**c**) NF mode.

Three topologies derived from $X_1 = 1$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 1$ are shown in Figure 9. Figure 9a can be achieved from Figure 8b,c in PF and NF modes. In Figure 9b, the body-diodes of switches T_{P3} and T_{N3} are used to replace the extra diodes in Figure 9a. Figure 9c is another topology in which four diodes plus one switch are used to replace the two switches, T_{P3} and T_{N3}. These are well-known HERIC topologies [13,30].

The topologies from the MN principle may be divided into two families. Those in the first family have extra diode for output current flow in PF and NF modes. In contrast, the topologies in the second family don't use the extra diode, and the body-diode of the switch is used to allow current to flow, as in the case in Figure 9b in PF and NF modes. Thus, two corresponding topological families under M = 2 and N = 2 are shown in Table 1.
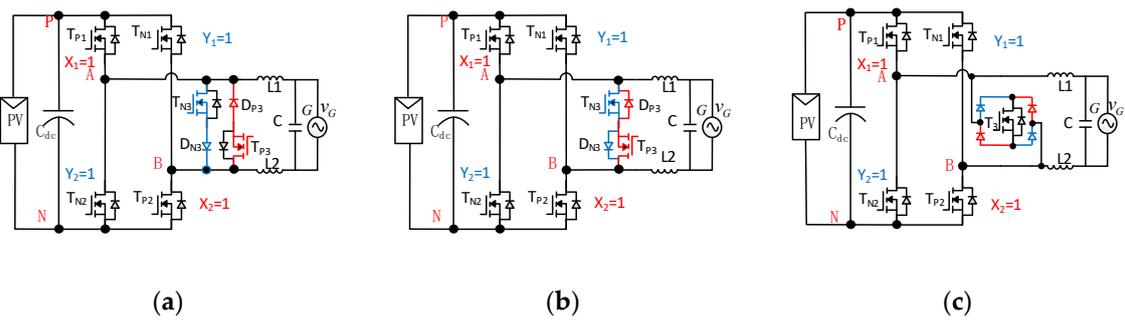
Figure 9. Three topologies under $X_1 = 1$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 1$. (**a**) R1 [13]; (**b**) R2 [13]; (**c**) R3 [30].

Table 1. Topological families under M = 2 and N = 2.

(M, N)	$M = X_1 + X_2$	$N = Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(M = 2, N = 2)	1 + 1	1 + 1	R_1, R_3	R_2

3.2. Case 2: M = 3 and N = 2 or M = 2 and N = 3

For M = 3, N = 2 or M = 2, N = 3, there are same topologies between M = 3, N = 2 and M = 2, N = 3, as they are equivalent by exchanging the two bridges. Thus, M = 3 and N = 2 is made as an example to explain the derivation method. M = 3 and N = 2 means there are two possibilities to choose the combined values of X_1, X_2, Y_1, and Y_2, i.e., $X_1 = 1$, $X_2 = 2$, $Y_1 = 1$, and $Y_2 = 1$, and $X_1 = 2$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 1$. Considering the symmetrical characteristics with respect to terminals P and N, the two cases are the same. For the sake of brevity, only the former case is analyzed below.

Figure 10 shows four modes under $X_1 = 1$, $X_2 = 2$, $Y_1 = 1$, and $Y_2 = 1$. The PC and NC modes are shown in Figure 10a. One switch, T_{P1}, is used to connect points P and A due to $X_1 = 1$; meanwhile, switches T_{P2} and T_{P3} are viewed as a connection between point B and point N as $X_2 = 2$ in PC mode. Similarly, two switches, T_{N1} and T_{N2}, are added in NC mode with $Y_1 = 1$ and $Y_2 = 1$. According to rule #1, switches T_{P1}, T_{P3}, T_{N1}, and T_{N2} are off in PF and NF modes. Switch T_{p2} is on according to rule #3, and one diode D_{p2} is added based on rule #2 in PF mode, as shown in Figure 10b. In NF mode, an extra switch, T_{N3}, plus the diode D_{N3} are added in series to flow negative output current. The diode is added or served by the body diode of switch T_{P2}. Thus, there are two circuits to realize NF mode, as shown in Figure 10c,d.
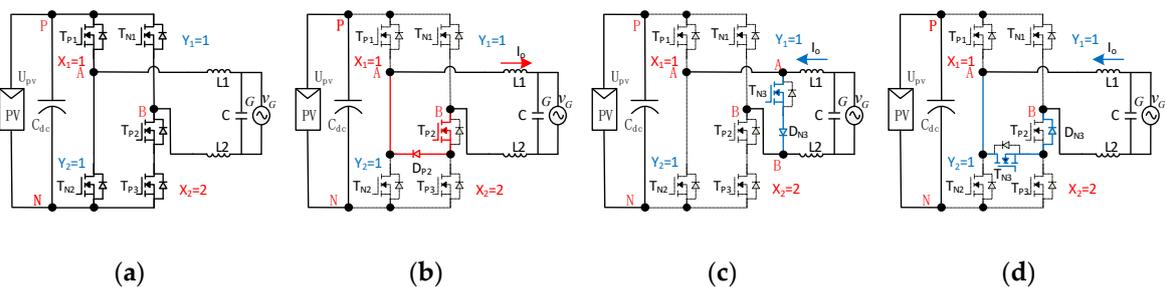
Figure 10. Four modes under $X_1 = 1$, $X_2 = 2$, $Y_1 = 1$, and $Y_2 = 1$. (**a**) PC and NC modes; (**b**) PF mode; (**c**) NF mode #1; (**d**) NF mode #2.

According to Figure 10, there are one circuit in PF mode and two circuits in NF mode. There are only two possibilities to combine PF and NF modes. Correspondingly, the two topologies derived from $X_1 = 1$, $X_2 = 2$, $Y_1 = 1$, and $Y_2 = 1$ are shown in Figure 11. Figure 11a shows the topology which combines the PF mode in Figure 10b and the NF mode in Figure 10c, while Figure 11b shows the topology which combines the PF mode in Figure 10b and the NF mode in Figure 10d. Two topological families under M = 3, N = 2 or M = 2, N = 3 are shown in Table 2.

(a)

(b)
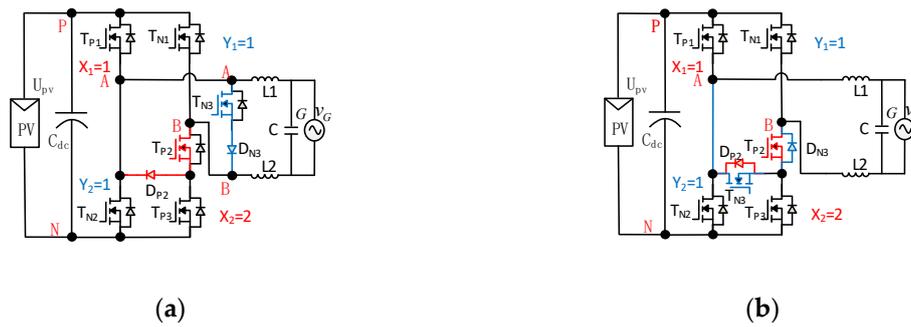
Figure 11. Two topologies derived from $X_1 = 1$, $X_2 = 2$, $Y_1 = 1$, and $Y_2 = 1$. (**a**) R4 [31]; (**b**) R5 [27].

Table 2. Topological families under M = 3 and N = 2 or M = 2 and N = 3.

(M, N)	$M = X_1 + X_2$	$N = Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(M = 2, N = 3) Or (M = 3, N = 2)	1 + 2	1 + 1	R4	R5
	1 + 1	1 + 2		
	2 + 1	1 + 1		
	1 + 1	2 + 1		

3.3. Case 3: M = 3 and N = 3

M = 3, which means there are two possibilities to choose the combined values of X_1 and X_2: $X_1 = 1$, $X_2 = 2$, and $X_1 = 2$, $X_2 = 1$. Similarly, N = 3 yields two possibilities to combine Y_1 and Y_2. One is $Y_1 = 1$ and $Y_2 = 2$ and the other is $Y_1 = 2$ and $X_2 = 1$. It should be noted that the same topologies exist between $X_1 = 2$, $X_2 = 1$, $Y_1 = 1$, $Y_2 = 2$, and $X_1 = 1$, $X_2 = 2$, $Y_1 = 2$, $Y_2 = 1$ when two bridges are exchanged. Thus, there are three possibilities: (1) $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 1$; (2) $X_1 = 2$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 2$; and (3) $X_1 = 1$, $X_2 = 2$, $Y_1 = 1$, and $Y_2 = 2$. Considering the symmetry between terminals P and N, case (1) is the same as case (3). For the sake of brevity, only cases (1) and (2) are analyzed below.

Figure 12 shows four modes under $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 1$. The PC and NC modes are shown in Figure 12a. As shown in Figure 12a, six switches (T_{P1}, T_{P2}, T_{P3}, T_{N1}, T_{N2}, and T_{N3}) are used for $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 1$. According to rule #1, switches T_{P1}, T_{P3}, T_{N1}, and T_{N3} are off in PF and NF modes. One rest switch, T_{P2}, is on according to rule #3, and one diode, D_{P2}, is added based on rule #2 in PF mode, as shown in Figure 12b. Diode D_{P2} can also be served by the body-diode of switch T_{N2}. The reflected PF mode is shown in Figure 12c. For NF mode, switch T_{N2} is on for negative output current flow. An extra diode, D_{N2}, is added, as shown in Figure 12d. The body-diode of switch T_{P2} is served as the diode D_{N2}, as shown in Figure 12e.

According to Figure 12, there are two circuits in PF mode and two in NF mode. There are four possibilities to combine PF and NF modes. Correspondingly, four topologies derived from $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 1$ are shown in Figure 13. Figure 13a shows the topology combining the PF mode in Figure 12b and the NF mode in Figure 12d. Figure 13b shows the topology combining the PF mode in Figure 12b and the NF mode in Figure 12e. Figure 13c shows the topology combining the PF mode in Figure 12c and the NF mode in Figure 12d, and Figure 13d shows the topology combining the PF mode in Figure 12c and the NF mode in Figure 12e.

According to rule #4, the extra diode D_{P2} can be absent due to the presence of the body-diode of switch T_{N2} in Figure 13b. Similarly, the extra diode D_{N2} can be absent owing to the presence of the body-diode of switch T_{P2} in Figure 13c. In Figure 13b–d, the two switches, T_{P1} and T_{N1}, are combined into one switch T_1. Thus, the topologies in Figure 13b–d are the same.
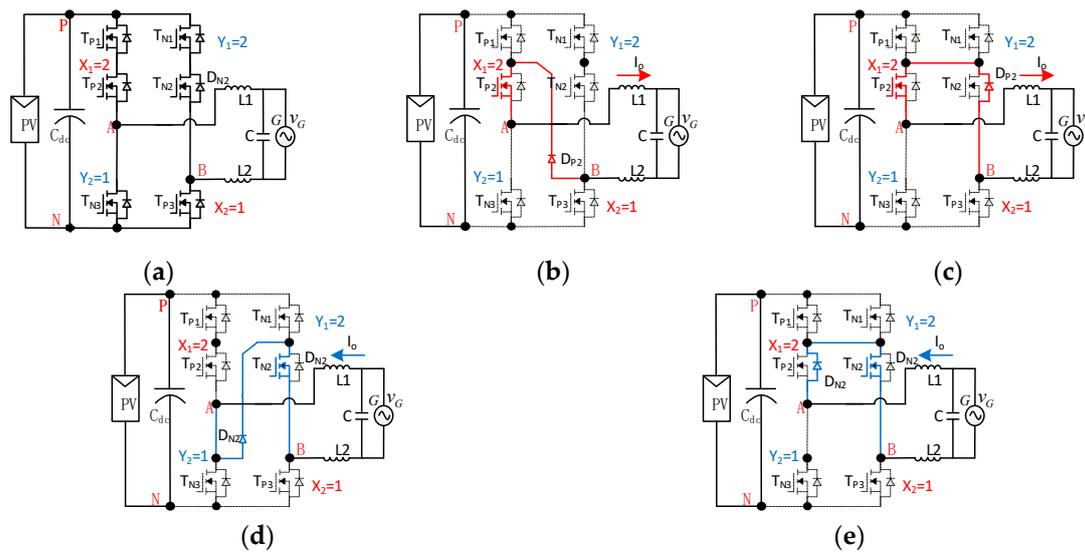
Figure 12. Four modes under $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 1$. (**a**) PC and NC modes; (**b**) PF mode #1; (**c**) PF mode #2; (**d**) NF mode #1; (**e**) NF mode #2.
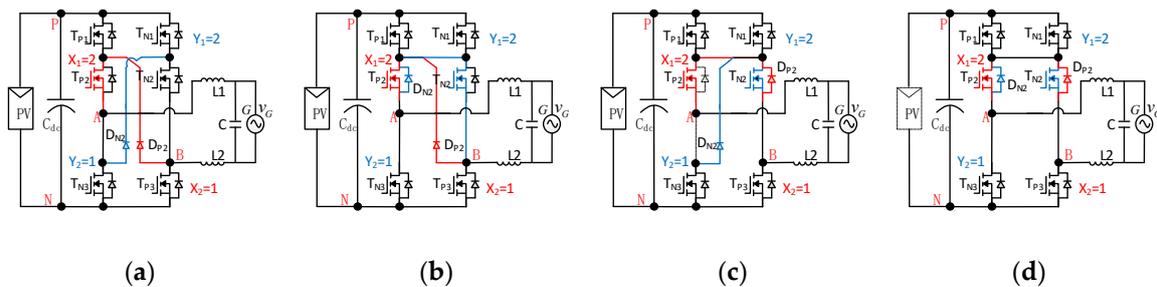
Figure 13. Four topologies derived from $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 1$. (**a**) R6 [16,31]; (**b**) R7 (circuit one); (**c**) R7 (circuit two); (**d**) R7 (circuit three) [12].

Similarly, one topology derived from $X_1 = 2$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 2$ is shown in Figure 14.
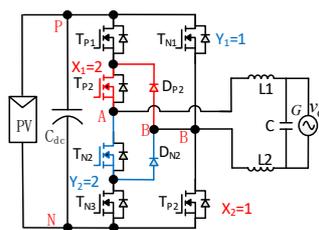
Figure 14. The topology R8 derived from $X_1 = 2$, $X_2 = 1$, $Y_1 = 1$, and $Y_2 = 2$; [38].

Correspondingly, two topological families under M = 3 and N = 3 are shown in Table 3.

Table 3. Topological families under M = 3 and N = 3.

(M, N)	M = $X_1 + X_2$	N = $Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(M = 3, N = 3)	2 + 1	2 + 1	R6	R7
	1 + 2	1 + 2		
	2 + 1	1 + 2	R8	None available
	1 + 2	2 + 1		

3.4. Case 4: M = 3 and N = 4 or M = 4 and N = 3

The same topologies exist between M = 3, N = 4 and M = 4, N = 3, as they are equivalent by exchanging the two bridges. For M = 3 and N = 4, M = 3 means that there are two possibilities to choose the combined values of X_1 and X_2: one is $X_1 = 2$ and $X_2 = 1$, and the other is $X_1 = 1$ and $X_2 = 2$. Similarly, N = 4 means three possibilities to combine Y_1 and Y_2. However, only one combination is available according to Equation (9), i.e., $Y_1 = 2$ and $Y_2 = 2$.

Thus, there are two possibilities to choose the combined values of X_1, X_2, Y_1, and Y_2: one is $X_1 = 1$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$, and the other is $X_1 = 2$, $X_2 = 1$, $Y_1 = 2$, and $Y_2 = 2$. Considering the symmetry between terminals P and N, the two cases are the same. Figure 15 shows four modes under $X_1 = 1$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$.
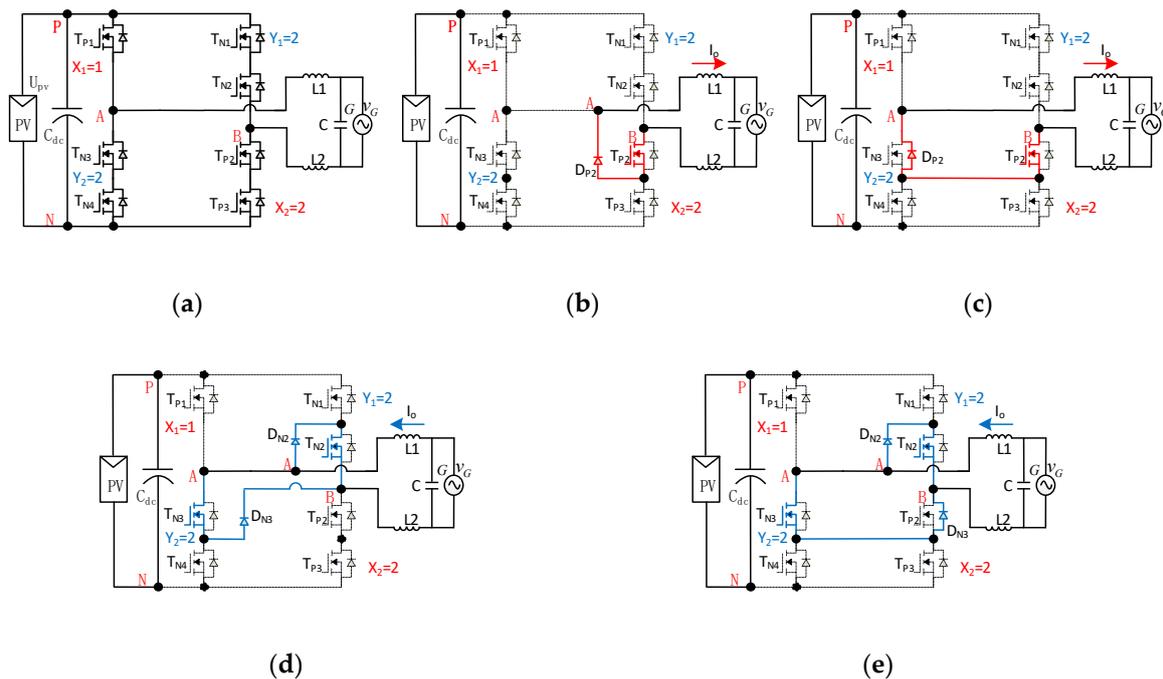
Figure 15. Four modes under $X_1 = 1$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$. (**a**) PC and NC modes; (**b**) PF mode #1; (**c**) PF mode #2; (**d**) NF mode #1; (**e**) NF mode #2.

The PC and NC modes are shown in Figure 15a. Seven switches (T_{P1}, T_{P2}, T_{P3}, T_{N1}, T_{N2}, T_{N3}, and T_{N4}) are used for $X_1 = 1$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$, as shown in Figure 15a. From rule #1, the switches T_{P1}, T_{P3}, T_{N1}, and T_{N4} are off in PF and NF modes. Switch T_{P2} is on according to rule #3, and one diode D_{P2} is added based on rule #2 in PF mode, as shown in Figure 15b. Diode D_{P2} is served by the body-diode of switch T_{N3}; the reflected PF mode is shown in Figure 15c. For NF mode, two switches, i.e., T_{N2} and T_{N3}, are on for negative output current flow according to rule #3, and two extra diodes, D_{N2} and D_{N3}, are added from rule #2, as shown in Figure 15d. The body-diode of switch T_{P2} serves as the diode D_{N3}, as shown in Figure 15e.

According to the above analysis, there are two circuits in PF mode and two in NF mode. Thus, four possible topologies are shown in Figure 16. Figure 16a shows the topology combining the PF mode in Figure 15b and the NF mode in Figure 15d. The other three topologies are shown in Figure 16b–d, respectively; however, they are the same, as diode D_{P2} in Figure 16b and diode D_{N3} in Figure 16c can be absent from rule #4. Furthermore, two switches, i.e., T_{P3} and T_{N4}, are merged into one switch, i.e., T_4.
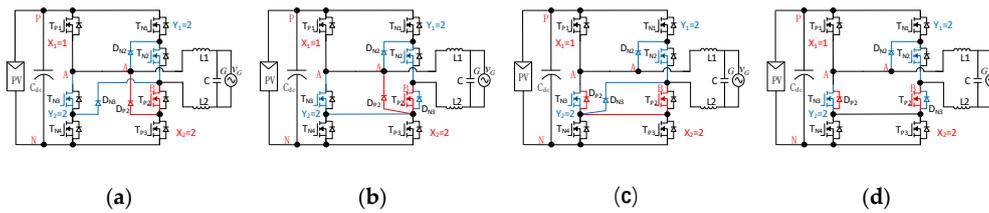
Figure 16. Two topologies derived from $X_1 = 1$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$. (**a**) R9 (new); (**b**) R10 (circuit one); (**c**) R10 (circuit two); (**d**) R10 (circuit three) (new).

Correspondingly, two topological families under M = 3 and N = 4 or M = 4 and N = 3 are shown in Table 4.

Table 4. Topological families under M = 3 and N = 4 or M = 4 and N = 3.

(M, N)	$M = X_1 + X_2$	$N = Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(M = 3, N = 4) or (M = 4, N = 3)	1 + 2	2 + 2	R9	R10
	2 + 2	1 + 2		
	2 + 1	2 + 2		
	2 + 2	2 + 1		

3.5. Case 5: M = 4 and N = 4

In this case, M = 4 and N = 4. According to Equation (9), M = 4 and N = 4 means only one available possibility to choose the combined values of X_1, X_2, Y_1, and Y_2, i.e., $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$.

Figure 17 shows four modes under $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$. As shown in Figure 17a, eight switches ($T_{P1} \sim T_{P4}$ and $T_{N1} \sim T_{N4}$) are used for $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$ in PC and NC modes. With the reference of the above analysis of Cases 1~4, it is easy to make a similar analysis. For the sake of brevity, this is included here.
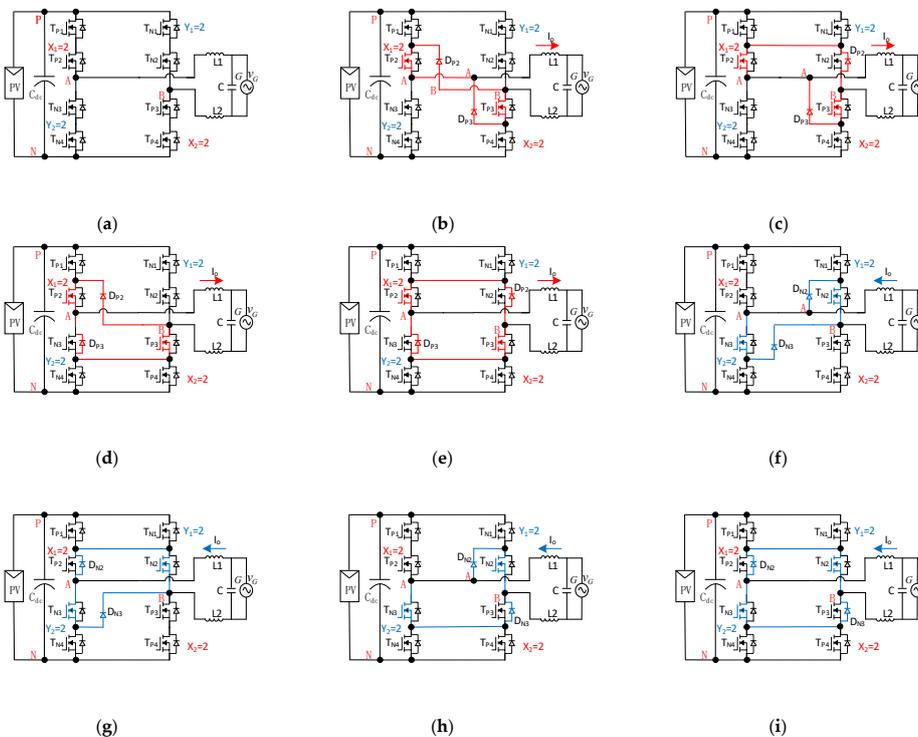
Figure 17. Four modes under $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$. (**a**) PC and NC modes; (**b**) PF mode #1; (**c**) PF mode #2; (**d**) PF mode #3; (**e**) PF mode #4; (**f**) NF mode #1; (**g**) NF mode #2; (**h**) NF mode #3; (**i**) NF mode #4.

It may be observed from Figure 17 that there are four circuits in PF mode and four in NF mode. Thus, sixteen possible topologies may be derived from the MN principle. However, these topologies can be simplified based on rule #4, and the four topologies derived from $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$ are shown in Figure 18.

| (a) | (b) | (c) |
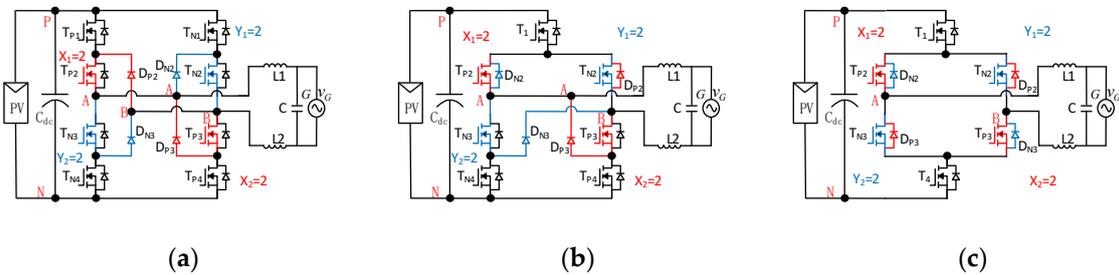
Figure 18. Four topologies derived from $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$. (**a**) R11 (new); (**b**) R12 (new); (**c**) R13 [17].

Two corresponding topological families under M = 4 and N = 4 are shown in Table 5.

Table 5. Topological families under M = 4 and N = 4.

(M, N)	$M = X_1 + X_2$	$N = Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(4, 4)	2 + 2	2 + 2	R11, R12	R12

3.6. All Simplfied Topologies from MN Principle

From the above analysis, two corresponding topological families are summarized in Table 6.

Table 6. Two simplified topological families from MN principle.

(M, N)	$X_1 + X_2$	$Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(M = 2, N = 2)	1 + 1	1 + 1	R1, R3	R2
(M = 2, N = 3) or (M = 3, N = 2)	1 + 2	1 + 1	R4	R5
	1 + 1	1 + 2		
	2 + 1	1 + 1		
	1 + 1	2 + 1		
(M = 3, N = 3)	2 + 1	2 + 1	R6	R7
	1 + 2	1 + 2		
	2 + 1	1 + 2	R8	None available
	1 + 2	2 + 1		
(M = 3, N = 4) or (M = 4, N = 3)	1 + 2	2 + 2	R9	R10
	2 + 2	1 + 2		
	2 + 1	2 + 2		
	2 + 2	2 + 1		
(M = 4, N = 4)	2 + 2	2 + 2	R11, R12	R13

It may be observed from the above analysis that the MN principle can be used to derive all the possible topologies for a single-phase, full bridge, transformerless inverter. Furthermore, thirteen simplified topologies from the MN principle are provided in this paper. All existing topologies (R1–R8, R13) have been covered, and five new topologies marked from R9 to R12 have been found.

For the two topological families with the same M and N, the topologies without an extra diode are of lower cost than those with the extra diode, as the body-diode of switch in the former is used to replace the extra diode; however, the efficiency of the former will likely be a little lower, as that diode has better performance than the body-diode.

(M + N) is the number of conduction switches in PC and NC modes; the bigger (M + N), the higher the conduction loss. Thus, M = N = 2 is the best choice in terms of low conduction loss.

Although M = 4 and N = 4 means large conduction loss under USPWM, the topologies from M = 4 and N = 4 can also work in DFSPWM, where the equivalent switching frequency is double, and the size of the low pass filter is reduced. A detailed description about DFUSWPM will be given in the next section.

4. Topology Derivation under DFUSPWM

In this section, topology derivation methodology is introduced under DFUSPWM. The unified topology model and MN principle are extended to the topologies under DFUSPWM.

4.1. Principle of DFUSPWM

The principle of DFUSPWM is shown in Figure 19. Differential-mode voltage V_{AB} is a three-level waveform.

The levels are $+V_{PN}$, 0, and $-V_{PN}$. There are six modes in total line-frequency period. The inverter is working in positive conduction (PC) mode and negative conduction (NC) mode when V_{AB} equals $+V_{PN}$ and $-V_{PN}$, respectively. There are four modes if V_{AB} equals 0.
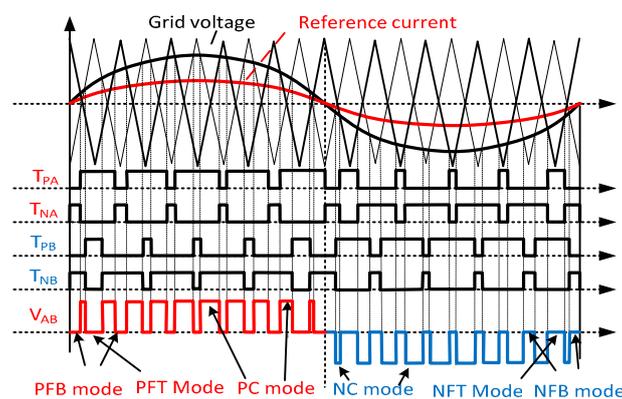
Figure 19. Principle of DFUSPWM.

To achieve double frequency of voltage V_{AB}, there are two interleaved freewheeling modes when the grid voltage is positive: one is used to refer to the freewheeling current flowing through top switch, which is defined as PFT mode. The other one, called "PFB mode" is used to flow freewheeling current through bottom switch. Similarly, two interleaved freewheeling modes, called "NFT mode" and "NFB mode", are used in NF mode. The freewheeling current flows through the top switch in NFT and through the bottom switch in NFB mode.

The modes rotate in the sequence of PFT, PC, PFB, and PC in the positive half cycle of the grid voltage. Similarly, the modes rotate in the sequence of NFT, NC, NFB, and NC in the negative half cycle. Thus, the frequency of output voltage V_{AB} is double the switch frequency.

The six modes based on H4 topology in DFUSPWM are shown in Figure 20. The PC and NC modes are shown in Figures 20a and 20b, respectively. In the positive half cycle of grid voltage, two PF modes, i.e., PFT and PFB, are shown in Figure 20c,d. Similarly, two NF modes, i.e., NFT and NFB, are shown in Figure 20e,f in the negative half cycle of the grid voltage.
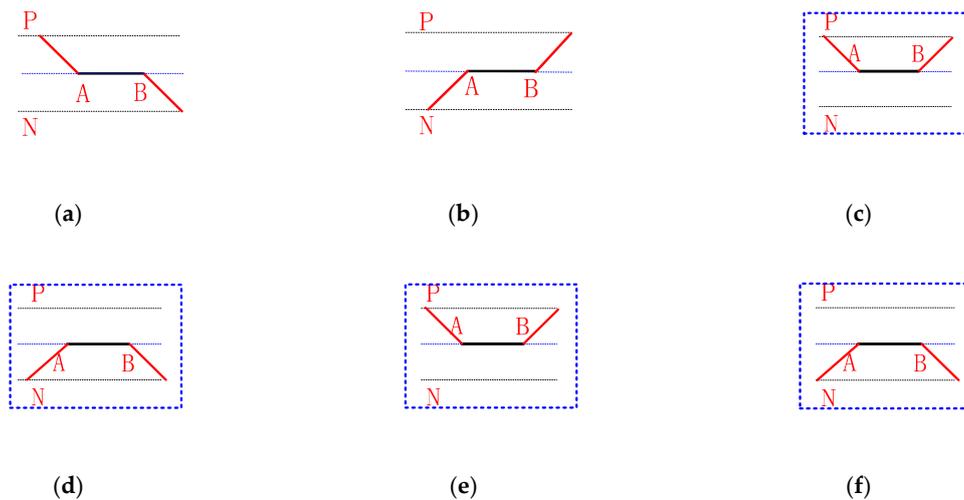
Figure 20. Six modes based on H4 topology under DFUSPWM. (**a**) PC mode; (**b**) NC mode; (**c**) PFT mode; (**d**) PFB mode; (**e**) NFT mode; (**f**) NFB mode.

4.2. Unified Topology Model of DFUSPWM

Figure 21 shows six modes from the unified topology model under DFUSPWM.
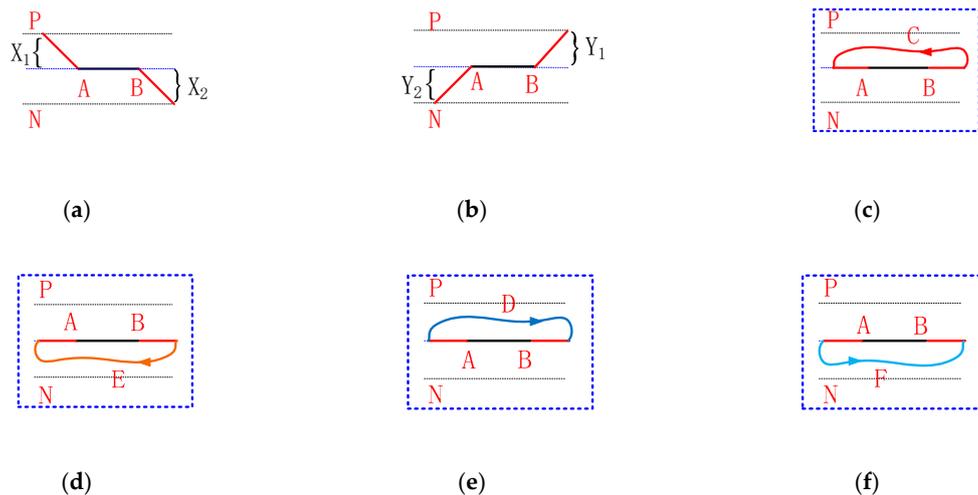
Figure 21. Six modes based on unified topology under DFUSPWM. (**a**) PC mode; (**b**) NC mode; (**c**) PFT mode; (**d**) PFB mode; (**e**) NFT mode; (**f**) NFB mode.

All rules under USPWM mentioned in Section 2 are also suitable for DFUSPWM. According to rule #1, points A and B must be disconnected from points P and N in the four freewheeling modes, i.e., the two PF modes and the two NF modes. From rule #2, the branch between points A and B is short-circuited for output current flow. Two new controlled branches, B$\hat{C}$A and B$\hat{E}$A, are added to flow the positive current in Figure 21c,d. Two controlled branches, A$\hat{D}$B and A$\hat{F}$B, are added to flow the negative current in Figure 21e,f.

For DFUSPWM, there are two PC modes in a switching period. Thus, according to rule #1, there are at least two couple switches to alternately turn on/off to achieve double frequency. For example, there are two switches, i.e., T_{P1} connected to point P and T_{P2} connected to point A, between point P and point A, and two, i.e., T_{P3} connected to point B and T_{P4} connected to point N, between point B and point N. Switches T_{P1} and T_{P2} are connected in series, as are T_{P3} and T_{P4}. Switches T_{P1} and T_{P3} turn on/off at the same time, and T_{P2} and T_{P4} are kept on or off at the same time. Thus, there are two possibilities to disconnect points P and A, and points B and N: one is that switches T_{P1} and T_{P3} turn off. The other is that switches T_{P2} and T_{P4} turn off. Once switches T_{P1} and T_{P3} turn off in PFT mode,

switch T_{P2} is kept on and can be used to construct a freewheeling branch because it connects to point A. Similarly, switch T_{P3} is kept on and serves to construct a freewheeling branch in the PFB mode when switches T_{P2} and T_{P4} turn off. Thus, two PF modes can be achieved when $X_1 = 2$ and $X_2 = 2$. The same is true with $Y_1 = 2$, $Y_2 = 2$.

Figure 22 shows six modes under $X_1 = 2$, $X_2 = 2$, $Y_1 = 2$, and $Y_2 = 2$. The PC and NC modes are shown in Figure 22a. Eight switches ($T_{P1} \sim T_{P4}$ and $T_{N1} \sim T_{N4}$) are used. The same driving signals are provided for couples of switches T_{P1} and T_{P3}, T_{P2} and T_{P4}, T_{N1} and T_{N3}, and T_{N2} and T_{N4}.
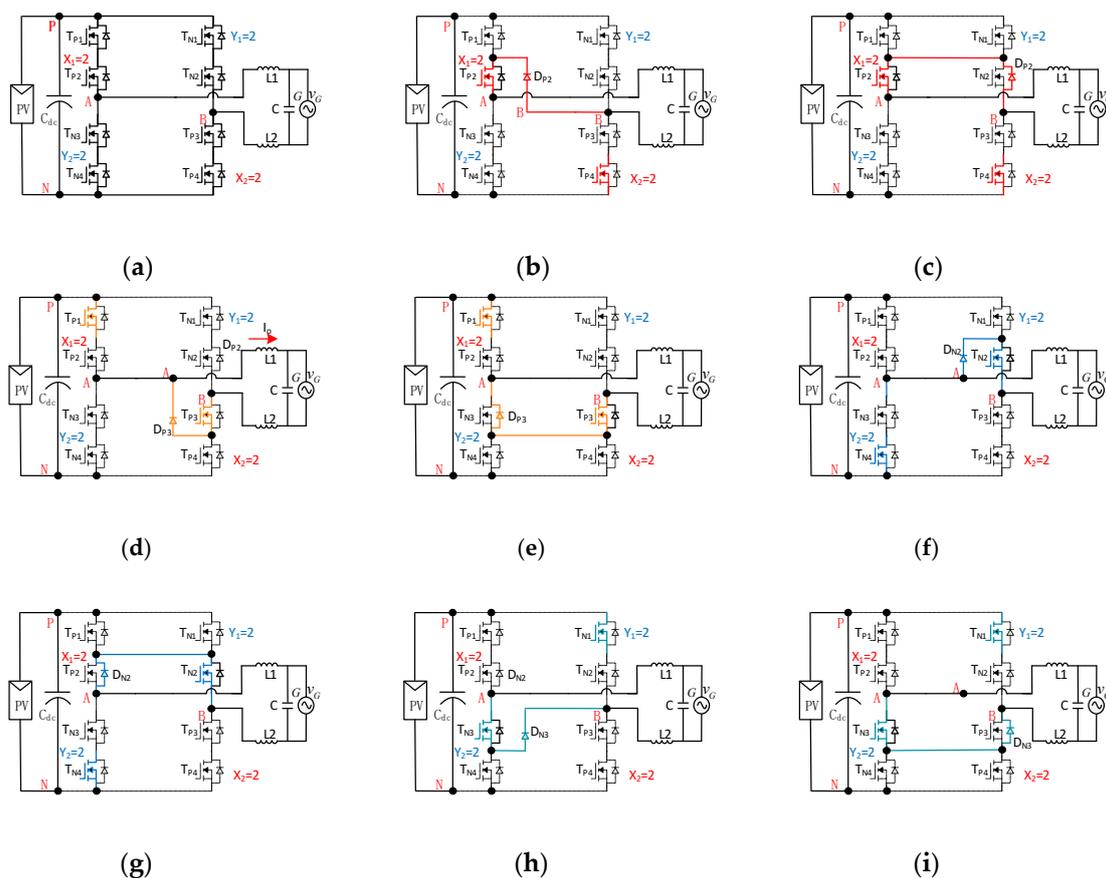
Figure 22. Six modes of M10 topology. (**a**) PC and NC modes; (**b**) PFT mode #1; (**c**) PFT mode #2; (**d**) PFB mode #1; (**e**) PFB mode #2; (**f**) NFT mode #1; (**g**) NFT mode #2; (**h**) NFB mode #1; (**i**) NFB mode #2.

In PFT mode, switches T_{P1}, T_{P3}, T_{N1}, T_{N2}, T_{N3}, and T_{N4} are off, and switches T_{P2} and T_{P4} are on. One diode, D_{P2}, is added for the positive output current flow, as shown in Figure 22b. Diode D_{P2} is served by the body-diode of switch T_{N2}. The reflected PFT mode is shown in Figure 22c.

In PFB mode, switches T_{P2}, T_{P4}, T_{N1}, T_{N2}, T_{N3}, and T_{N4} are off, and switches T_{P1} and T_{P3} are on. One diode, D_{P3}, is added for positive output current flow, as shown in Figure 22d. Diode D_{P3} is served by the body-diode of switch T_{N3}, as shown in Figure 22e. It is easy to make a similar analysis for NFT and NFB modes. Figure 22f,g show the two NFT modes, while the two NFB modes are shown in Figure 22h,i.

It should be noted from the above analysis that there are two PFT modes, two PFB modes, two NFT modes, and two NFB modes. There are eight possible topologies through choosing one PFT mode, one PFB mode, one NFT mode, and one NFB mode. According to rule #4, the four typical topologies in Figure 23 are derived from the MN principle.

(a)   (b)   (c)
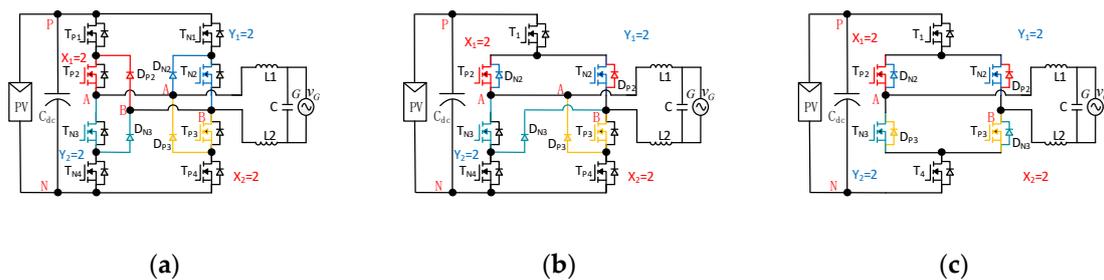
Figure 23. Four topologies derived from MN principle under DFUSPWM. (**a**) R11 (new); (**b**) R12 (new); (**c**) R14 [17].

Two corresponding topological families under DFUSPWM are shown in Table 7.

Table 7. Two topological families from MN principle under DFUSPWM.

(M, N)	$X_1 + X_2$	$Y_1 + Y_2$	Family with Extra Diode	Family without Extra Diode
(M = 4, N = 4)	2 + 2	2 + 2	R11, R12, R13	R14

5. Conclusions

In this paper, a topology derivation methodology under USPWM is proposed to determine all possible full-bridge topologies for small leakage current. A unified circuit model based on USPWM is provided. Secondly, a mathematic method called the "MN principle" is then proposed to determine all possible topologies. Four rules and a derivation procedure are also provided. Thirteen simplified topologies are derived using this method. All existing topologies have been covered, and four new topologies have been found. These topologies can be classified into two topology families: the first includes topologies in which extra diodes are used for current flowing, while the body-diode functions as the extra diode to flow freewheeling current in the second family topologies. Finally, the proposed method is extended to the topologies under DFUSPWM, and three corresponding topologies have been derived, and two new topologies found.

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