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Optimal Energy Efficiency Tracking in the Energy-Stored Quasi-Z-Source Inverter

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Abstract: In this paper, the interaction between the energy storage (ES) power distribution and system efficiency enhancement is researched based on the energy stored quasi-Z-source inverter. The corresponding current counteraction, stress reduction, power loss profile, and efficiency enhancement around the embedded energy storage units are studied in details. Firstly, the current counteraction effect on the device current is presented with the embedded ES source. The corresponding reduction in the device current stress is revealed. Then, the detailed device power loss expressions with current redistribution in the impedance network are explored mathematically. A quasi-inverted-trapezoidal power loss profile is found with the embedded source power distribution. To further increase the overall system efficiency, an optimal energy efficiency tracking strategy is proposed for the ES-qZSI (energy-stored quasi-Z-source inverter) based on the power distribution control. Both the simulation and the experiment verified that the power loss is reduced by over 40% through the proposed efficiency enhancement method. The device current and loss analysis for the embedding of energy storage can also be extended to the operating range optimization in other ES systems.

Keywords: ES-qZSI; energy storage unit; power loss analysis; optimal operation

1. Introduction

The energy storage system (ESS) has been attractive in various ancillary services for renewable energy generation and other applications [1,2]. To supply energy for longer durations and improve the benefits provided by multi-energy storage systems, the optimal overall efficiency should be achieved considering each subordinate energy storage. Different from the power generation applications with maximum power point tracking (MPPT) requirement, like PV and wind turbines, an ideal energy storage system usually aims to achieve maximum energy efficiency tracking (MEET) [3,4]. A MEET scheme for the micro-grid was studied [5] through the optimal power distribution. The optimization criterion is based the system achieving high efficiency with a battery at a low state of charge (SOC). Improving efficiency through power distribution regulation was proposed [6]. These power distribution methods were also applied for applications such as electric vehicles and elevators [7–9]. MEET has proved to be effective for power conversion system (PCS) applications in AC or DC micro-grids. However, owing to the fluctuation in output power and SOC, the MEET for ESSs does not currently have the capability to handle a wide operation range.

The energy-stored quasi-Z-source inverter (ES-qZSI) is characterized by single-stage power conversion and high efficiency. Its operation principle with multiple energy storages, including both battery and ultra-capacitor, has been demonstrated [10,11]. The topology was researched widely for applications such as photovoltaic power generation and electric vehicles [12–14]. Methods like soft-switching and modulation strategy, aiming at device current stress reduction, were applied for efficiency improvement [15–17]. An optimal power distribution to improve efficiency has been given in [18,19], but the principle and operation range are still obscure due to the lack of interaction studies on the impedance network, the switching device stress, and the energy storage units.

In this paper, the principle for the current counteraction and stress reduction around the energy-storage units embedding in the ES-qZSI is studied in detail. The device power loss with the current redistribution in the impedance network is explored mathematically. A quasi-inverted-trapezoidal power loss profile is found with power distribution between the input source and the embedded source. Finally, a wide range optimal energy efficiency tracking technology in the ES-qZSI is proposed. The effectiveness of the theatrical analysis and proposed method are validated by both a simulation and experiment. The power loss of the ES-qZSI can be reduced by more than 40% compared with the conventional qZSI.

2. Principle of Current Counteraction in ES-qZSI

The circuit of the ES-qZSI is demonstrated in Figure 1. The input of the ES-qZSI, denoted as source 1, is connected with a DC source, such as PV, which is similar to the conventional qZSI topology. Compared with the conventional qZSI topology, an energy storage unit, such as a battery, is embedded parallel with the capacitor C_2 in the ES-qZSI and is denoted as source 2.

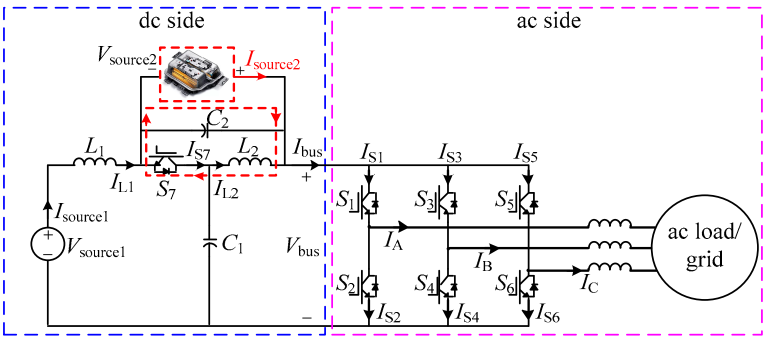


Figure 1. Current counteraction in the ES-qZSI.

The system can be separated into two parts by the DC-bus based on the system operation, as shown as the AC and DC sides in Figure 1. In the shoot-through (ST) state, the switch S_7 in the DC side turns off and at least one phase leg in the AC side is short-circuited. In the non-shoot-through (NST) states, S_7 turns on and S_1–S_6 operate like the conventional voltage source inverter (VSI) [18].

Due to the embedded energy storage unit, V_{bus} is clamped by the voltages of sources 1 and 2. Then S_7 and the ST state are adopted to distribute the power between the two sources. Based on the power conservation, the source current distribution in the ES-qZSI is derived as Equation (1) [18], where D represents the ST duty ratio, $I_{source1}$ represents the current from source 1, and $I_{source2}$ represents the current from source 2. The current allocation of the two sources is achieved through the regulation of the ST duty ratio.

$$I_{bus} = (1 - 2D)I_{source1} + DI_{source2} \tag{1}$$

Compared with the conventional qZSI, the current from source 2 has an impact on the internal current distribution of the impedance network on the DC side. For the traditional qZSI, the inductor current I_{L2} is clamped by the inductor current I_{L1} due to the zero average currents through C_1 and C_2, as shown in Equation (2), where V_{bus} is the DC-link voltage, P_o is the output power, and B is the ratio between V_{bus} and the voltage of source 1.

$$I_{L2} = I_{L1} = \frac{BP_o}{V_{bus}},\ B = \frac{V_{bus}}{V_{source1}} \tag{2}$$

For the ES-qZSI, the injected current from the embedded source 2 flows through the inductor L_2 and counteracts I_{L1}, as shown in Figure 1. Therefore, I_{L2} is reduced. The current counteraction effect is demonstrated in Equations (3)–(5) based on the power conservation and the ampere-second balance, where $P_{source2}$ is the power of source 2 and K is the distribution ratio between $P_{source2}$ and P_o.

$$I_{L1} = \frac{(1-K)BP_o}{V_{bus}} \tag{3}$$

$$I_{L2} = I_{L1} - I_{source2} = \left(B - \frac{KB(B+1)}{B-1}\right)\frac{P_o}{V_{bus}} \tag{4}$$

$$K = \frac{P_{source2}}{P_o} \tag{5}$$

According to Equations (3)–(5), the inductor currents in ES-qZSI can be redistributed with K, which is the ratio of the power from source 2 to the output power. The inductor currents of qZSI in Equation (2) is a special case where $I_{source2} = 0$ or $K = 0$. The embedded energy storage unit can help reduce both I_{L1} and I_{L2} by sharing part of the output power.

3. Stress Reduction and Power Loss Profile in ES-qZSI

3.1. Device Stress Analysis for ES-qZSI

The inductor current redistribution due to current counteraction can ease the switching device current stress in ES-qZSI. The current stress reduction is demonstrated with the current commutation in different states in Figure 2.

During the ST state, as demonstrated in Equation (6) and Figure 2(a2), the ST current I_{ST} equals the sum of I_{L1} and I_{L2}, where the output power P_o can be expressed as Equation (7). M represents the modulation index, I_{ph} represents the amplitude of the phase current, and φ represents the power factor angle.

$$I_{ST} = I_{L1} + I_{L2} = 2\left(B - \frac{B^2K}{B-1}\right)\frac{P_o}{V_{bus}} \tag{6}$$

$$P_o = \frac{\sqrt{3}}{2} M V_{bus} I_{ph} \cos\varphi \tag{7}$$

For the AC-side switch devices, as the three-phase ST method [15] is adopted, the ST current is shared equally by the three bridges, and the device stress in any bridge is derived as:

$$I_{Sn\text{-}ST} = \frac{1}{3} I_{ST} + \frac{1}{2} I_{ph} \tag{8}$$

During the NST states, S_1–S_6 conduct the phase currents, so the device current stress is the same as the conventional VSI [20]:

$$I_{Sn\text{-}NST} = I_{ph} \tag{9}$$

According to Figure 2(a1), the current expression of S_7 in the DC side during the NST state is:

$$I_{S7} = I_{L1} + I_{L2} - I_{dc\_link} = I_{ST} - I_{dc\_link} \tag{10}$$

I_{dc_link} is the DC-link current and its expression is 0, $\pm I_A$, $\pm I_B$, and $\pm I_C$ based on the states of S_1–S_6 [21]. Combining Equations (6), (8), and (10), the ST current and the current stress in S_1–S_7 can be alleviated through the power provided by the energy storage unit. This indicates that the device loss can be reduced and the energy transfer efficiency can be improved through power distribution in the ES-qZSI.

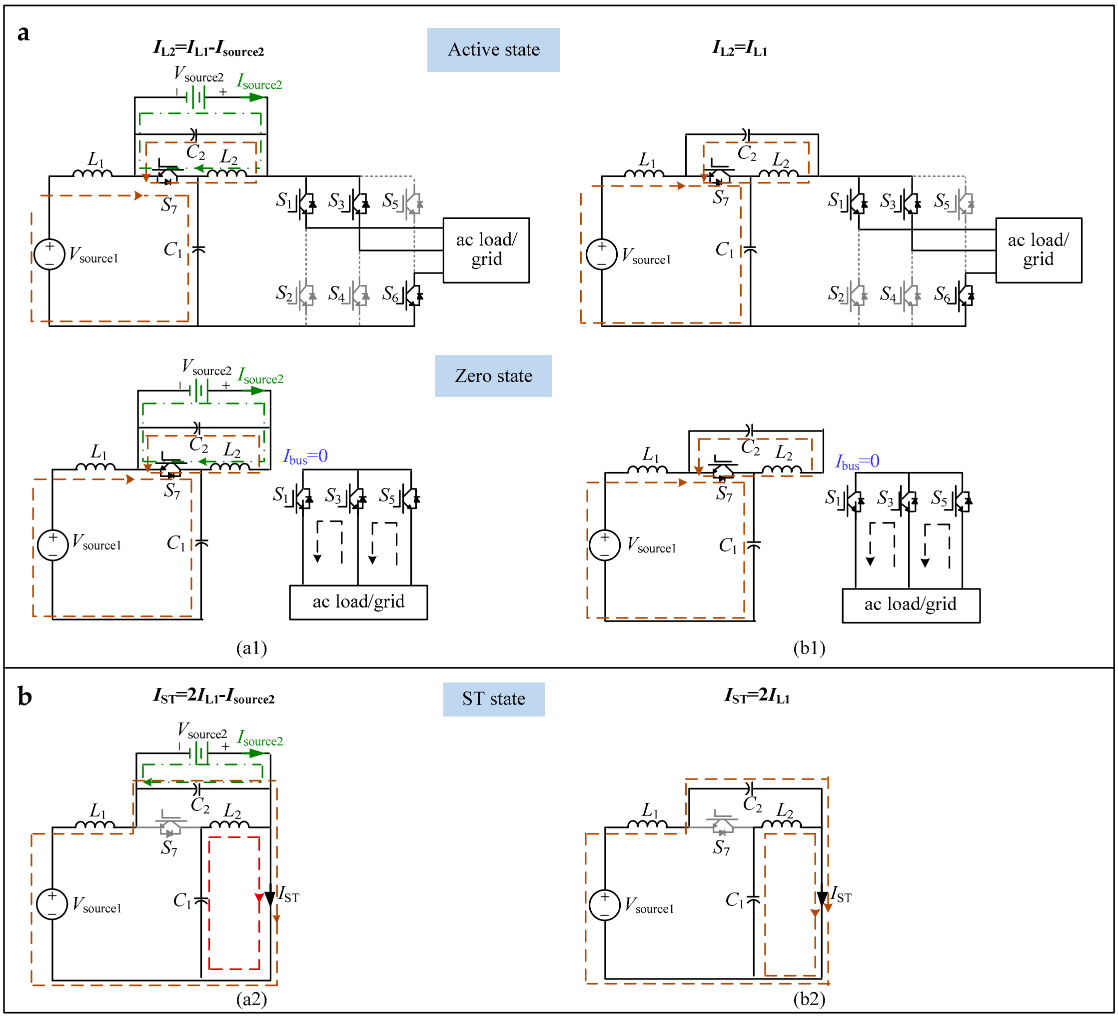


Figure 2. Current commutation of the ES-qZSI and qZSI in different states: (**a**) ES-qZSI; (**b**) qZSI.

3.2. Power Loss Profile Derivation for ES-qZSI

In this section, the switching and conduction loss of the AC and DC sides are presented with the power distribution in ES-qZSI. The device current expressions in Section 3.1 are adopted for the power loss modeling. The inductors losses are also included. Due to the low internal resistance, the power loss of the energy storage unit is far less than in the power electronic devices. Therefore, the power loss of the energy storage unit can be neglected. The derivation is demonstrated in Appendix A and the result is shown in Table 1. Due to the combination of the ST current and the phase current in the devices S_1–S_7, as in Equations (8) and (10), the zero-crossing point of device current and the commutation duration of the diode change. Its effect on the device power losses is represented by the coefficients α_1–α_6 in Table 1.

According to Table 1, the variation in the system power losses with respect to I_{ST} is demonstrated in Figure 3. It can be seen that the system power losses can be divided into three types based on their variation profiles.

(1) As shown in Equations (8) and (9), the coefficient of I_{ST} is smaller compared with that of I_{ph}. Therefore, the AC side device switching loss $P_{sw\text{-}ac}$ and conduction loss $P_{con\text{-}ac}$ are mainly dominated by I_{ph} and are relatively insensitive to I_{ST}, as shown in Figure 3.

(2) The coefficient of I_{S7} in Equation (10) increases. Therefore, the DC-side device switching loss $P_{sw\text{-}S7}$ and conduction loss $P_{con\text{-}S7}$ are more sensitive to I_{ST}. It can be seen from Table 1 that $P_{sw\text{-}S7}$ varies as a V-type curve. Its minimum value appears at the operation point O_1 where I_{ST} reaches zero. For $P_{con\text{-}S7}$, the variation curve also presents as a V-type curve, as shown in Figure 3. According to

Equation (10), I_{ST} is fully counteracted by I_{ph} at the operation point O_2 where I_{ST} equals I_{ph}, and thus the minimum value of $P_{\text{con-S7}}$ appears.

(3) As shown in Table 1, P_{L} is a quadratic function of I_{ST}. Thus, the profile P_{L} varies like a parabolic curve. Its minimal point is located between O_1 and O_2, so the variation in P_{L} within this operation range is flat.

The total system loss P_{loss} can be obtained by combining $P_{\text{con-S7}}$, $P_{\text{sw-S7}}$, P_{L}, $P_{\text{con-ac}}$, and $P_{\text{sw-ac}}$. As the profiles of $P_{\text{con-S7}}$ and $P_{\text{sw-S7}}$ are V-type curves with different minimal points, their combination forms a quasi-inverted-trapezoidal profile with a flat valley. The parabolic profile of P_{L} also contributes to shaping a quasi-inverted-trapezoidal profile, whereas $P_{\text{con-ac}}$ and $P_{\text{sw-ac}}$ have a minimal effect on the total power loss profile. Thus, P_{loss} appears as a quasi-inverted-trapezoidal profile with respect to I_{ST}, as shown in Figure 3. The flat valley of P_{loss}, which represents the optimal efficiency operation range, is located between the minimal points of $P_{\text{con-S7}}$ and $P_{\text{sw-S7}}$ (O_1–O_2).

Table 1. Power loss of the ES-qZSI.

Item		Expression	Coefficient
Switching loss	DC side	$P_{\text{sw-S7}} = 2\alpha_1 f_s V_{\mathrm{bus}} \lvert I_{\mathrm{ST}} \rvert$	$\alpha_1 = \begin{cases} E_{\mathrm{IGBT}} & I_{\mathrm{ST}} < 0 \\ E_{\mathrm{Diode}} & I_{\mathrm{ST}} \geq 0 \end{cases}$
	AC side	$\begin{aligned} P_{\text{sw-ac}} &= 2\alpha_2 f_s V_{\mathrm{bus}} \lvert I_{\mathrm{ST}} \rvert + \frac{6}{\pi}(E_{\mathrm{IGBT}} + E_{\mathrm{Diode}}) f_s V_{\mathrm{bus}} I_{\mathrm{ph}} \\ &+ \frac{1}{\pi}\alpha_3 f_s V_{\mathrm{bus}} \left[\sqrt{9I_{\mathrm{ph}}^2 - 4I_{\mathrm{ST}}^2} - 2\lvert I_{\mathrm{ST}} \rvert \arccos\frac{2\lvert I_{\mathrm{ST}} \rvert}{3I_{\mathrm{ph}}} \right] \end{aligned}$	$\alpha_2 = \begin{cases} E_{\mathrm{Diode}} & I_{\mathrm{ST}} < 0 \\ E_{\mathrm{IGBT}} & I_{\mathrm{ST}} \geq 0 \end{cases}$
Conduction loss	DC side	$\begin{aligned} P_{\text{con-S7}} &= (1-D) r_{\mathrm{on}} I_{\mathrm{ST}}^2 + (1-D) V_{\mathrm{CE0}} I_{\mathrm{ST}} - \sqrt{3}\alpha_5 M I_{\mathrm{ST}} \cos\varphi \\ &+ \frac{M}{2\pi} r_{\mathrm{on}} I_{\mathrm{ph}}^2 (3 + 2\cos 2\varphi) + \alpha_6 \end{aligned}$	$\alpha_3 = \begin{cases} E_{\mathrm{IGBT}} + E_{\mathrm{Diode}} & \lvert I_{\mathrm{ST}} \rvert / I_{\mathrm{ph}} \leq 1.5 \\ 0 & \lvert I_{\mathrm{ST}} \rvert / I_{\mathrm{ph}} > 1.5 \end{cases}$
	AC side	$\begin{aligned} P_{\text{con-ac}} &= \frac{6(1-D)}{\pi} V_{\mathrm{CE0}} I_{\mathrm{ph}} + \frac{6-3D}{4} r_{\mathrm{on}} I_{\mathrm{ph}}^2 \\ &+ 2D V_{\mathrm{CE0}} \lvert I_{\mathrm{ST}} \rvert + \frac{2}{3} D r_{\mathrm{on}} I_{\mathrm{ST}}^2 \\ &+ \frac{2}{\pi}\alpha_4 D \left(\sqrt{9I_{\mathrm{ph}}^2 - 4I_{\mathrm{ST}}^2} - 2\lvert I_{\mathrm{ST}} \rvert \arccos\frac{2\lvert I_{\mathrm{ST}} \rvert}{3I_{\mathrm{ph}}} \right) \end{aligned}$	$\alpha_4 = \begin{cases} 2V_{\mathrm{CE0}} & \lvert I_{\mathrm{ST}} \rvert / I_{\mathrm{ph}} \leq 1.5 \\ 0 & \lvert I_{\mathrm{ST}} \rvert / I_{\mathrm{ph}} > 1.5 \end{cases}$ $\alpha_5 = \begin{cases} r_{\mathrm{on}} I_{\mathrm{ph}} & I_{\mathrm{ST}} \geq I_{\mathrm{ph}} \ or \ I_{\mathrm{ST}} \leq 0 \\ r_{\mathrm{on}} I_{\mathrm{ph}} + V_{\mathrm{CE0}} & 0 < I_{\mathrm{ST}} < I_{\mathrm{ph}} \end{cases}$
Inductor loss		$P_{\mathrm{L}} = r_{\mathrm{L}} \left(\frac{P_o + V_{\mathrm{source2}} I_{\mathrm{ST}}}{V_{\mathrm{bus}}} \right)^2 + r_{\mathrm{L}} \left(\frac{-P_o + V_{\mathrm{source2}} I_{\mathrm{ST}} + V_{\mathrm{source1}} I_{\mathrm{ST}}}{V_{\mathrm{bus}}} \right)^2$	$\alpha_6 = \begin{cases} -\frac{\sqrt{3}}{2} M V_{\mathrm{CE0}} I_{\mathrm{ph}} \cos\varphi & I_{\mathrm{ST}} \geq I_{\mathrm{ph}} \\ \frac{\sqrt{3}}{2} M V_{\mathrm{CE0}} I_{\mathrm{ph}} \cos\varphi & I_{\mathrm{ST}} < I_{\mathrm{ph}} \end{cases}$

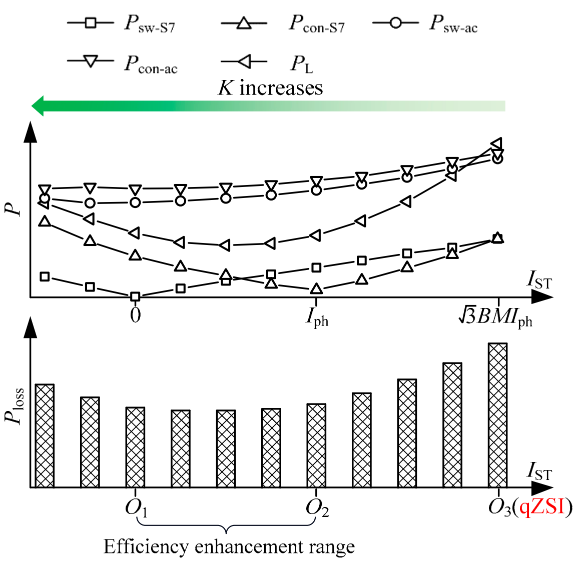


Figure 3. Power loss variation profile with respect to the shoot-through current I_{ST}.

According to Equations (6) and (7), the conventional qZSI operates at O_3 where K is zero and I_{ST} equals $\sqrt{3}BMI_{\mathrm{ph}}$ (B means the ratio of V_{bus} to V_{source1}, M means the modulation index and I_{ph} means the amplitude of the phase current). For high boost ratio applications, like $BM \geq 1$, O_3 is located outside the optimal efficiency operation range (O_1–O_2), as shown in Figure 3. Thus the efficiency gets enhanced in the ES-qZSI compared with the conventional qZSI.

4. Optimal Energy Efficiency Tracking and Practical Implementation

An optimal energy efficiency tracking method is presented in this section to guide the ES-qZSI working at the optimal operation range O_1–O_2. From Equations (6) and (7), the expression of K is derived as:

$$K = -\frac{B-1}{\sqrt{3}B^2} \cdot \frac{I_{ST}}{MI_{ph}\cos\varphi} + \frac{B-1}{B} \tag{11}$$

Then, the corresponding power distribution ratios at O_1 ($I_{ST} = I_{ph}$) and O_2 ($I_{ST} = 0$) can be obtained as:

$$K_{O1} = \frac{B-1}{B},\ K_{O2} = \frac{B-1}{B} - \frac{B-1}{\sqrt{3}B^2 M\cos\varphi} \tag{12}$$

According to Equation (12), the optimal efficiency tracking can be implemented based on the regulation of K. The control scheme is embedded in the vector control for the ES-qZSI, as shown in Figure 4a. The practical implementation for optimal efficiency tracking is divided into three steps and demonstrated by the flowchart in Figure 4b.

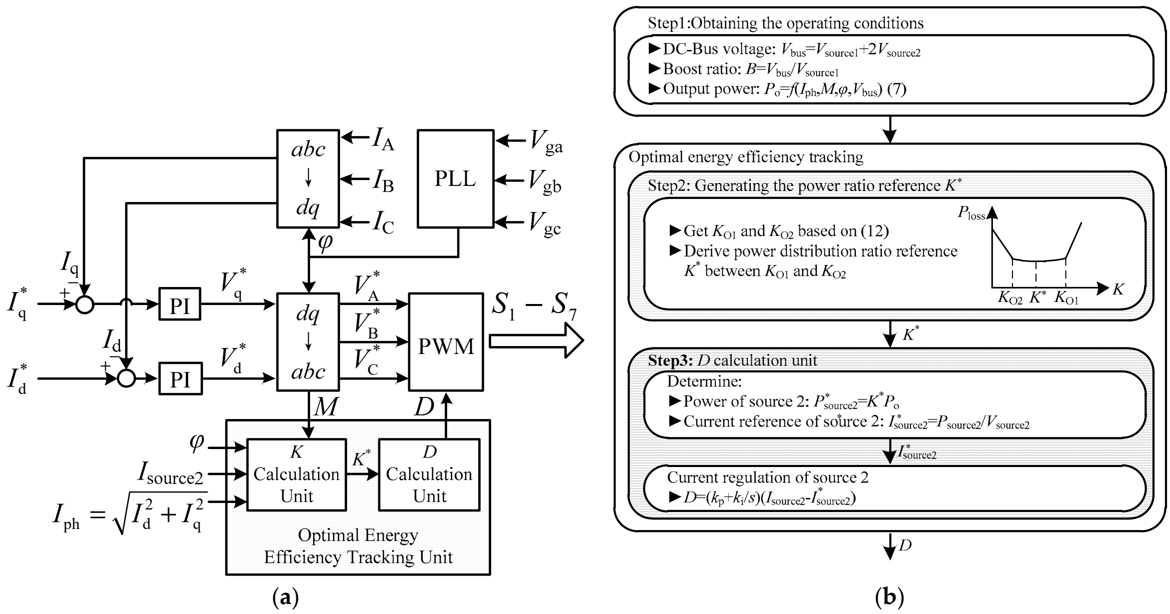


Figure 4. Implementation of the proposed optimal energy efficiency tracking: (**a**) System control scheme; (**b**) flowchart for optimal energy efficiency tracking unit.

Step 1: Obtain the system operation parameters like $V_{source1}$, $V_{source2}$, I_{ph}, M, and φ. Then, calculate P_o according to Equation (7).

Step 2: Based on Equation (12), find the boundaries of the efficiency enhancement range K_{O1} and K_{O2}. Select the K reference between K_{O1} and K_{O2}.

Step 3: Calculate the reference value of I_{source} based on Equation (5). Then, the ST duty ratio D is adopted to regulate I_{source} based on Equation (1).

Figure 5 shows the theoretical loss with different output powers. It is obtained from the parameters in Table 2. We found that the power losses related to S_7 and inductors are significantly reduced in the energy efficiency enhancement range. The system efficiency of ES-qZSI working within K_{O1}–K_{O2} improved compared with the conventional qZSI ($K = 0$). The efficiency enhancement was found to be effective for different output powers.

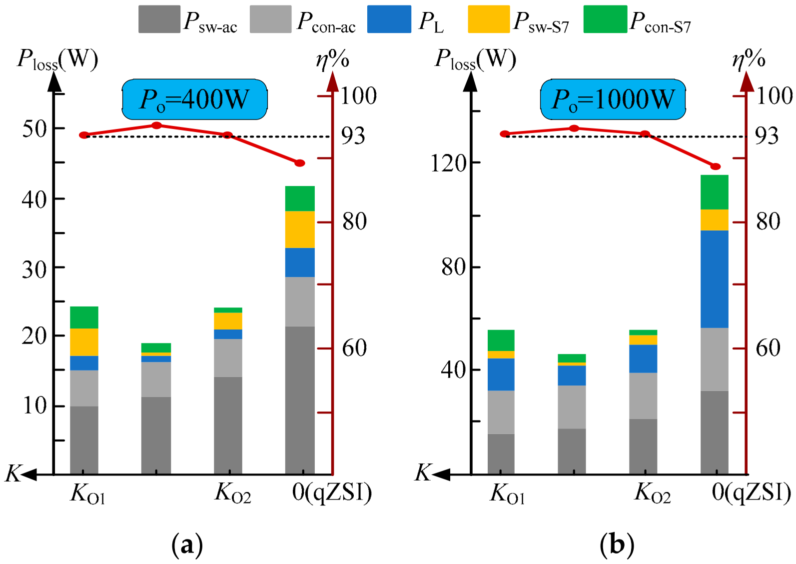


Figure 5. Theoretical power loss by the optimal energy efficiency tracking: (**a**) P_o = 400 W; (**b**) P_o = 1000 W.

Table 2. System parameters of the test platform.

Item	Value
Frequency of the grid f_g	50 Hz
Switching frequency f_s	10 kHz
Voltage of source 2 $V_{source2}$	50 V
Voltage of source 1 $V_{source1}$	100 V
Inductors L_1, L_2	4 mH
Capacitors C_1, C_2	820 µF
Inductor parasitic resistance r_L	80 mΩ
Switching Device S_1–S_7	IKW40N120T2

5. Simulation and Experimental Verification

The effectiveness of the proposed analysis and optimal energy efficiency tracking was verified by a simulation and an experiment. The simulation was performed with the software platform PLECS based on the parameters from the datasheet of the switching device. The experimental platform is demonstrated in Figure 6 and the system parameters are listed in Table 2.

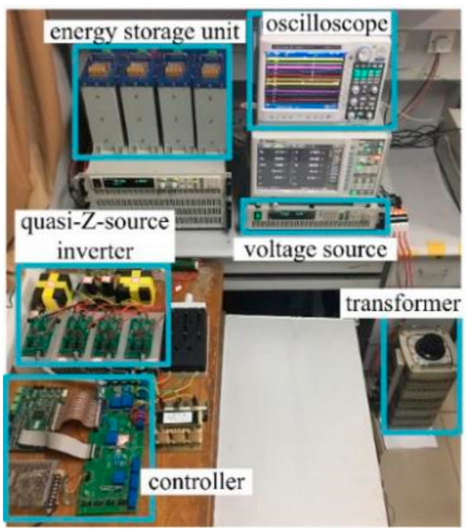
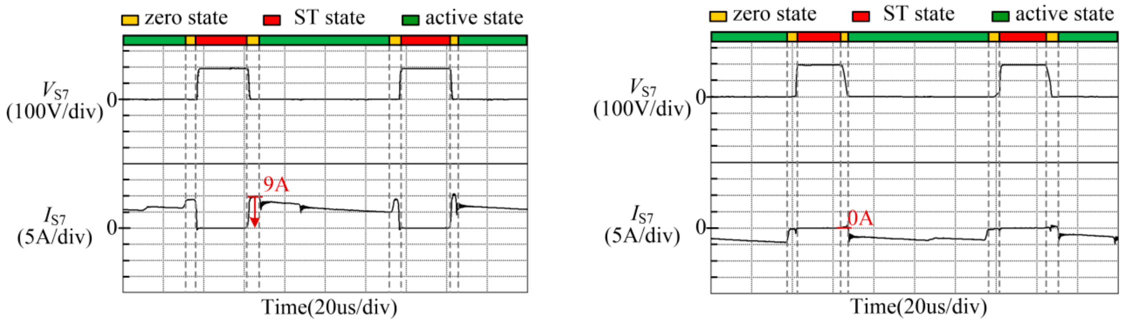


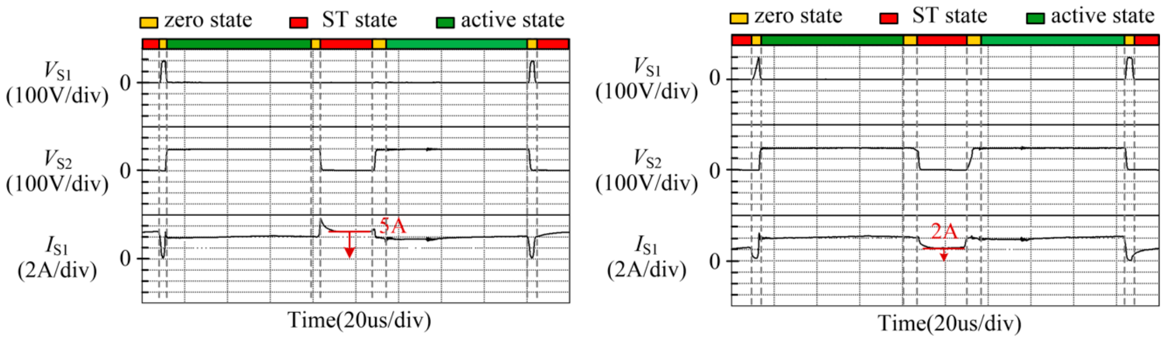
Figure 6. Platform for experimental test.

Figures 7 and 8 show the device current waveforms in one switching period for the DC and AC sides. The output power was 400 W. Figure 7 shows the current waveform of S_7 on the DC side. In the conventional qZSI (K = 0), the current stress for S_7 in the active states is 9 A, which is much larger than the phase current (3.8 A). This results in S_7 suffering from large current stress. In Figure 7b, the operation point O_1 is reached when K is 0.5. Thus, I_{ST} decreases to zero and the current stress for S_7 in the active states is close to the phase current value (3.8 A). Thereby, the current stress alleviation based on Equation (10) was verified.



(**a**) (**b**)

Figure 7. Experimental waveform of I_{S7} under same output load power: (**a**) power distribution ratio K = 0; (**b**) power distribution ratio K = 0.5.



(**a**) (**b**)

Figure 8. Experimental waveform of I_{S1} in ST state under same output load power: (**a**) Power distribution ratio K = 0; (**b**) Power distribution ratio K = 0.5.

Figure 8 shows the current waveform of S_1 on the AC side during one switching period. The current during the ST state reduced from 5 to 2 A as K increased from 0 to 0.5. The results match the calculation based on Equation (8) and I_{ST} and I_{ph} in Figure 7.

The experimental power loss profile between O_1 and O_3 is demonstrated in Figure 9. A low valley appears within the operation range of O_1–O_2, verifying the analysis for profile of P_{loss}. From the experiment, the total power loss was reduced by up to 40% with the power distribution regulation in ES-qZSI compared with the conventional qZSI. More than 70% of reduction was provided by S_7 and the passive components.

Figure 10 shows the simulation verification for the optimal energy efficiency tracking method. Initially, the system works as the conventional qZSI with K = 0. A large current value in I_{ST} can be observed. After that, the optimal energy efficiency tracking is activated and the system enters the optimal operation range. $I_{source2}$ from the energy storage units helps to reduce I_{ST}. Then, the system efficiency is improved by more than 4% through the regulation of the power distribution.

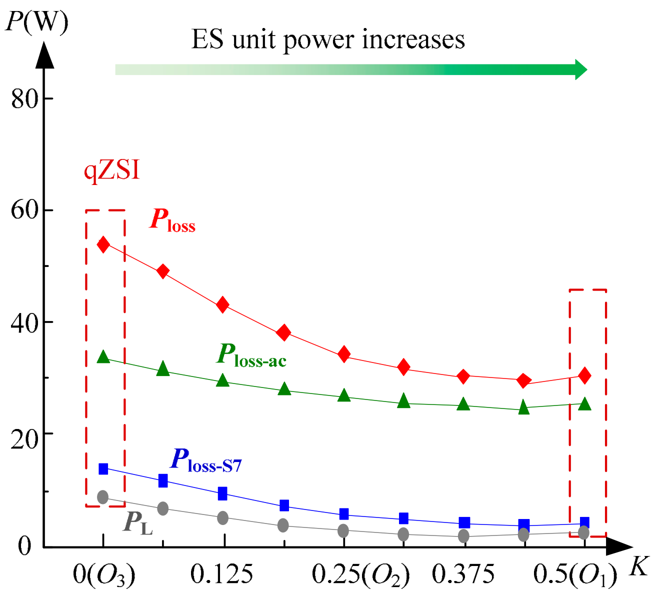


Figure 9. Experimental power loss profile with respect to the power distribution ratio.

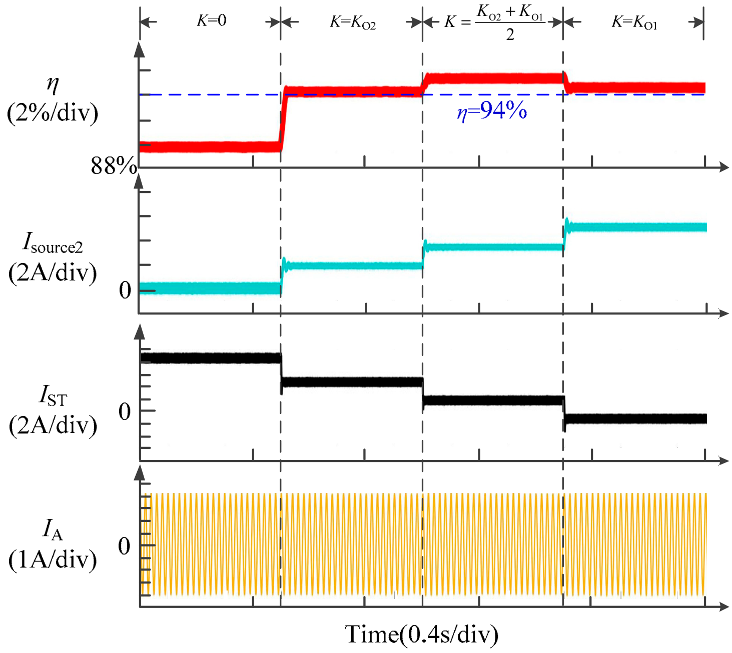


Figure 10. Simulation verification for the proposed efficiency enhancement method.

The related experimental results are shown in Figure 11. With increasing $I_{source2}$, the system efficiency increased to over 93%. Meanwhile, the shoot-through current increased up to 8 A when $K = 0$, which caused large current stress on S_7. Through the power distribution, the ST current was reduced to nearly zero, which relieved the current stress on S_7.

Figure 12 demonstrates the experiment waveforms to validate the optimal energy efficiency tracking method with a load power variation. In Figure 12a, the optimal energy efficiency tracking is not used and $I_{source2}$ is kept unchanged. Thus, I_{ST} increased when the load power increased, and the efficiency decreased to below 92%. In Figure 12b, $I_{source2}$ is regulated according to the optimal energy efficiency tracking method. The system operated around O_1 when I_{ST} was kept at a low value during the output power variation. Then, the efficiency was maintained above 92% and the optimal energy efficiency tracking was verified.

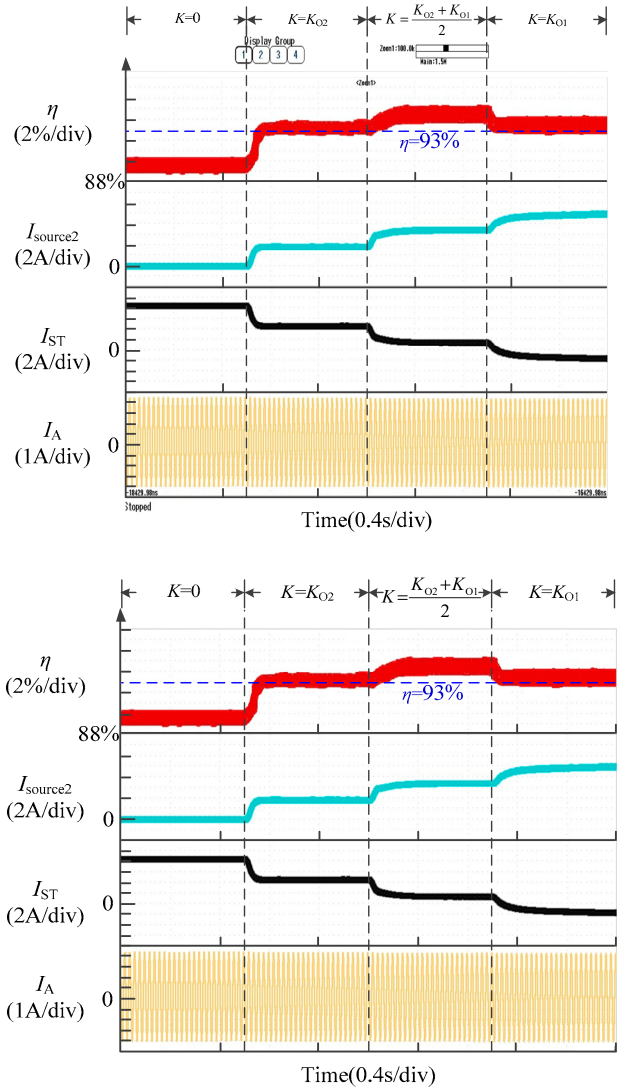


Figure 11. Experimental waveforms for the validation of the proposed efficiency enhancement method.

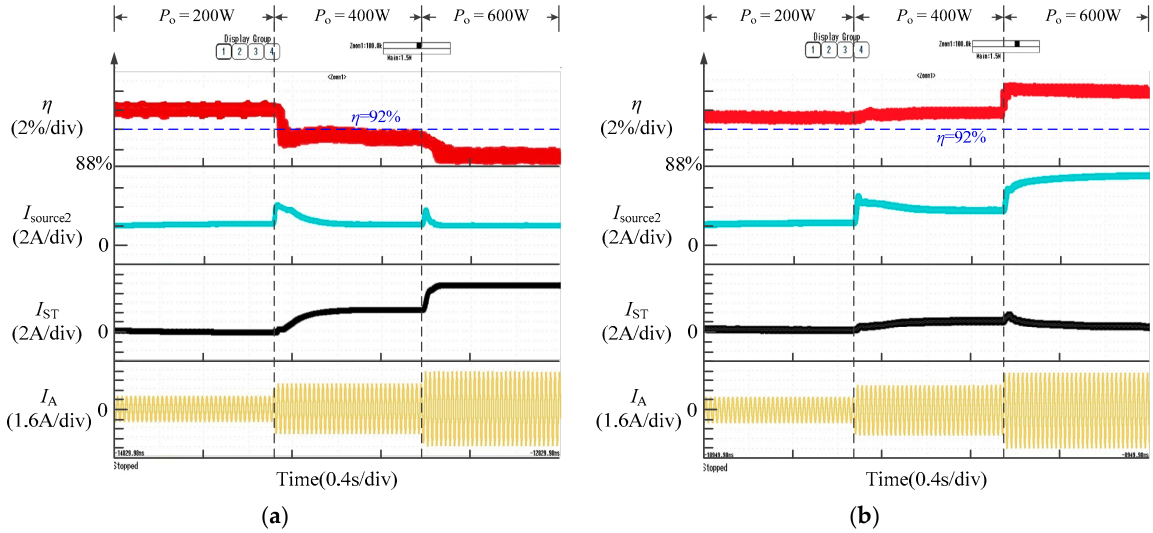


Figure 12. Experimental verification with load variation: (**a**) without and (**b**) with optimal energy efficiency tracking.

6. Conclusions

This paper presented a detailed system power loss analysis for the ES-qZSI from the power distribution view. The current counteraction effect was studied to alleviate the device current stress. An efficiency enhancement scheme was then presented based on the quasi-inverted-trapezoidal loss profile and power distribution around the embedded energy storage units. The effectiveness of the proposed efficiency enhanced method was verified by a simulation and an experiment, resulting in a power loss decrease of over 40%. The analysis and proposed scheme may also be extended to other impedance-source-network-based energy storage systems.

Author Contributions: S.H., Z.L., and J.Z. developed the ideas of this research; Z.L. and S.H. performed the simulations and the experiments; X.Y. and S.H. revised the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

V_{bus}	Voltage of the DC link
V_{source1}	Voltage of source 1
V_{source2}	Voltage of source 2
$I_{\text{dc\_link}}$	DC-link current
I_{bus}	Average value of DC-link current
I_{source1}	Current of source 1
I_{source2}	Current of source 2
D	Shoot-through duty ratio
I_{ST}	Shoot-through current
P_{o}	Output power
P_{source1}	Power of source 1
P_{source2}	Power of source 2
η	Efficiency of the system
K	Power distribution ratio for source 2
I_{L1}, I_{L2}	Current of inductors L_1 and L_2
B	Boost ratio, $V_{\text{bus}}/V_{\text{source1}}$
M	Modulation index
I_{ph}	Peak value of the phase current
I_{Sn}	Current of switching device S_n
I_{A}, I_{B}, I_{C}	Phase currents
E_{Diode}, E_{IGBT}	Switching energy loss of diode and IGBT (insulated gate bipolar transistor) per unit voltage and per unit current
f_{s}	Switching frequency
E^*_{on}, E^*_{off}	Energy loss during turn-on and turn-off processes from the datasheet
V_{ref}, I_{ref}	Turn-off voltage and turn-on current in the test condition from the datasheet
I^*_{rrm}	Peak value of the reverse recovery current of the diode
t^*_{rr}	Reverse recovery time of the diode
$P_{\text{sw-S7}}$, $P_{\text{con-S7}}$	Switching and conduction loss of DC side
$P_{\text{sw-ac}}$, $P_{\text{con-ac}}$	Switching and conduction loss of AC side
f_{g}	Frequency of the grid
T_{s}	Switching period
T_1, T_2	Operation time for the active vectors
V_{CE0}	Forward voltage drop of IGBT or diode
r_{on}	On resistance of IGBT or diode
r_{L}	Parasitic resistance of inductors L_1 and L_2

Appendix A

Appendix A.1. Switching Loss Derivation

The following derivation is based on the assumption that the current switching ripples are slight and can be neglected. For the DC side, two switching actions of S_7 occur in one switching period with the seven-segment SVPWM (space vector pulse width modulation) algorithm. According to Equation (10) and Figure 2, I_{S7} switches between I_{ST} and zero when the system switches between the zero state and the ST state. Thus, the switching loss of S_7 can be written as:

$$P_{\text{sw-S7}} = \begin{cases} 2f_s E_{\text{Diode}} V_{\text{bus}} I_{\text{ST}} & I_{\text{ST}} > 0 \\ -2f_s E_{\text{IGBT}} V_{\text{bus}} I_{\text{ST}} & I_{\text{ST}} < 0 \end{cases} \tag{A1}$$

where E_{diode} and E_{IGBT} are expressed as:

$$E_{\text{IGBT}} = \frac{E_{\text{on}}^* + E_{\text{off}}^*}{V_{\text{ref}} I_{\text{ref}}},\ E_{\text{Diode}} = \frac{V_{\text{ref}} I_{\text{rrm}}^* t_{\text{rr}}^*}{2V_{\text{ref}} I_{\text{ref}}} = \frac{I_{\text{rrm}}^* t_{\text{rr}}^*}{2I_{\text{ref}}} \tag{A2}$$

For the AC side, the switching loss of all devices are the same for a balanced three-phase system. Taking S_1 as an example, the switching loss can be written as:

$$\begin{aligned} P_{\text{sw-S1}} &= f_g \sum_{i=1}^{N} E_{\text{IGBT}} V_{\text{bus}} I_{\text{A}} + f_g \sum_{i=1}^{N} E_{\text{Diode}} V_{\text{bus}} I_{\text{A}} + 2f_g \sum_{i=0}^{N_1} E_{\text{Diode}} V_{\text{bus}} \left(\tfrac{1}{2} I_{\text{A}} - \tfrac{1}{3} I_{\text{ST}}\right) \\ &+ 2f_g \sum_{i=N_1+1}^{N} E_{\text{IGBT}} V_{\text{bus}} \left(\tfrac{1}{3} I_{\text{ST}} - \tfrac{1}{2} I_{\text{A}}\right) \end{aligned} \tag{A3}$$

The phase current in phase A can be expressed as Equation (A4). N_1 represents the device current zero crossing point in ST state and is expressed as Equation (A5). Then, the switching loss on the AC side can be obtained as Equation (A6).

$$I_{\text{A}} = I_{\text{ph}} \cos\left(\frac{\pi}{N} i + \varphi\right),\ N = \frac{f_s}{2f_g} \tag{A4}$$

$$N_1 = \frac{N}{\pi} \arccos \frac{2|I_{\text{ST}}|}{3I_{\text{ph}}} \tag{A5}$$

$$P_{\text{sw-ac}} = 6P_{\text{sw-S1}} \tag{A6}$$

Appendix A.2. Conduction Loss Derivation

The voltage drop on the switching device can be expressed as:

$$V_{\text{on}} = V_{\text{CE0}} + r_{\text{on}} I_{\text{on}} \tag{A7}$$

According to Equation (10), I_{S7} is related to the output voltage vector. Based on the symmetry, the loss in one grid period is six times of that in one sector of the SVPWM. Here, the conduction loss in sector I (with output voltage vector 100 and 110) is shown as $P'_{\text{con-S7}}$ in Equation (A8).

$$\begin{aligned} P_{\text{con-S7}} &= 6P'_{\text{con-S7}} \\ P'_{\text{con-S7}} &= \underbrace{f_g \sum_{i=1}^{N/3} \left(V_{\text{CE0}} |I_{\text{ST}}| + r_{\text{on}} I_{\text{ST}}^2\right)(T_s - T_1 - T_2 - DT_s)}_{\text{Zero state}} + \underbrace{f_g \sum_{i=1}^{N/3} \left[V_{\text{CE0}} |I_{\text{ST}} - I_{\text{A}}| + r_{\text{on}} (I_{\text{ST}} - I_{\text{A}})^2\right] T_1}_{\text{Vector 100}} \\ &\underbrace{+ f_g \sum_{i=1}^{N/3} \left[V_{\text{CE0}} |I_{\text{ST}} + I_{\text{C}}| + r_{\text{on}} (I_{\text{ST}} + I_{\text{C}})^2\right] T_2}_{\text{Vector 110}} \\ T_1 &= MT_s \sin\left(\tfrac{\pi}{3} - \tfrac{\pi}{N} i\right),\ T_2 = MT_s \sin\left(\tfrac{\pi}{N} i\right) \end{aligned} \tag{A8}$$

The phase current in phase C is expressed as:

$$I_{\text{C}} = I_{\text{ph}} \cos\left(\frac{\pi}{N} i + \varphi + \frac{2\pi}{3}\right) \tag{A9}$$

The conduction loss of the AC side are six times that of S_1 with the balanced three phase-system. The conduction loss of S_1 can be written as:

$$\begin{aligned} P_{\text{con-ac}} &= 6P_{\text{con-S1}} \\ P_{\text{con-S1}} &= 2f_g \sum_{i=1}^{N} V_{\text{CE0}}\left|\tfrac{1}{2}I_A - \tfrac{1}{3}I_{\text{ST}}\right|DT_s + 2f_g \sum_{i=1}^{N} r_{\text{on}}\left(\tfrac{1}{2}I_A - \tfrac{1}{3}I_{\text{ST}}\right)^2 DT_s \\ &\quad + f_g(1-D)T_s \sum_{i=1}^{N}\left(V_{\text{CE0}}|I_A| + r_{\text{on}}I_A^2\right) \end{aligned} \tag{A10}$$

The accumulation items in Equations (A3), (A8), and (A10) are approximated by the definite integrals, and then the approximate expression of $P_{\text{sw-ac}}$, $P_{\text{con-S7}}$, and $P_{\text{con-ac}}$ can be obtained as shown in Table 1.

Appendix A.3. Inductor Conduction Loss Derivation

For the inductors L_1 and L_2, as the ripple of inductor current is slight and neglected, the inductor loss is mainly determined by the copper DC loss, which is expressed as:

$$P_L = r_L\left(I_{L1}^2 + I_{L2}^2\right) \tag{A11}$$

Combining Equations (3)–(5) and (A11), P_L is obtained as demonstrated in Table 1.

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