Analysis and Implementation of Multilevel Inverter for Full Electric Aircraft Drives

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Abstract: In modern aircrafts, hydraulic or pneumatic actuators have been already replaced with electric counterparts, but the advancement of the inverter and motor technology has made possible that the propulsion system can be powered by electrical sources. These high power requirements can not be efficiently fulfilled by using a typical two level converter; the multi-level converter represents a suitable solution for this application. This paper presents a cascaded H-bridge, a 9-level permanent magnet synchronous motor drive for full electric aircrafts. Harmonic analysis is presented considering different levels of a multi-level inverter. Simulation results and experimental validation with a test-rig confirms the accuracy of the proposed system.

Keywords: full electric aircraft (FEA); cascaded H-bridge (CHB); multi-level inverter; permanent magnet synchronous motor (PMSM); total harmonic distortion (THD)

1. Introduction

Due to increasing power efficiency demand, reduced high operating cost and most importantly reduced air pollution, mobility is changing drastically and great attention is focused on the electrification in transportation. To accomplish this, power electronics (PE) and electric machines are needed and required to be much more reliable, efficient, compact, quieter and with high power density. The electrically propelled vehicle is dependent majorly on the PE to meet challenges like specific power, energy storage capabilities, thermal management of the system and most importantly safety [1]. In the conventional aircraft, actuation, de-icing, air conditioning, cabin pressurization, fuel pumping and other systems, are powered by hydraulic, pneumatic and mechanical actuators and propulsion system is powered by kerosene. In a full electric aircraft (FEA), all power systems, including propulsion are powered by electrical sources. This leads to increased dominance of power electronics, which opens the research window for the cleaner sky [2].

Currently, there are more than two hundred electric aircraft demonstrators approaching different methodologies which grew the number of electrically driven aircraft development approximately by 30% in last year [3]. Some of them include CityAirbus 4-seater all-electric eVTOL, which is comprised of eight 100 kW electric motors with a DC bus of 800 V [4]. Airbus is also exploring its wings on large aircrafts like series hybrid e-fan *X* that features 2 MW power converter having a DC bus of 3 kV [5]. In this race, a hybrid electric propulsion system by Bell also developed a system with six 100 kW motors to produce a power of 600 kW [6]. The required on-board electric power of a Boeing 787 is provided by four 250 kVA generators and two 225 kVA auxiliary power units (APU) [2,7]. In the existing Boeing 737, the electrical system capacity is 100 kW, which in the recent model is increased over 1 MW. Generally speaking, if an electric powertrain is adopted, very high power and medium voltage drives become mandatory and cascaded H-bridge (CHB) multi-level inverters (MLIs) represent

an attractive solution for the numerous advantages in terms of high efficiency, power quality and because of the use of low rated power devices, including the novel wide band gap (WBG) devices like gallium nitride (GaN) and silicon carbide (SiC). While conventional two level inverters suffer from high dv/dt, high blocking voltage across power device, common mode voltage, etc., which may lead to issues such as overheating and failures of motor winding, MLIs offer sinusoidal like output voltage profile, reduced dv/dt and consequently lower stress on power devices and on the motor, redundancy and reduced total harmonic distortion (THD). It can also handle high power with low switching frequency and thus lower switching losses, low common mode voltage, low stress in the motor bearings and in turn increasing the life of the motor [8–10].

The modern wide band gap (WBG) devices will play a crucial role in the race of electrification of high efficient PE converters for full electric aircrafts, bearing higher temperature. There are various works in the literature which demonstrate the merits of WBG for FEA. The paper [11], for instance, demonstrates a 2-level inverter of 50 kW using SiC devices to achieve high power density of the aircraft, resulting in saving of energy. On the other hand, the modern WBG operate at frequency higher than typical Si devices and this could increase electromagnetic interference (EMI) giving rise to higher di/dt and dv/dt ratios [1]. Hence, an alternative approach both at system and component levels has to be adopted. Nonetheless, SiC and GaN devices are still a quite immature technology with high cost. Their use requires re-design of the whole power converter system including gate drivers and so on.

A megawatt scale medium voltage three level active neutral point clamped power converter is proposed for high efficiency and high density aircraft hybrid propulsion systems in [12]. The paper [13] gives the detailed analysis for different modulation techniques and the LCL filter requirements using a five-level CHB inverter. The space agencies like NASA are exploiting the possibility of MLI for FEA application. For the electrically propelled aircraft research program, General Electric is considering a 1 MW, 3-level inverter with 2.4 kV DC-link voltage [14]. In the powertrain applications, electric machines represent the heart. In 2017, Airbus replaced one of the four jet engines by a 2 MW electric motor [5]. Numerous kinds of machines are being used for the power generation of the engine, such as switch reluctance [15], permanent magnet (PM) [16] and special designed induction machines [17]. Very often, machines are multi-phase with 5, 6 or even more phases. The literature shows that PM machine has attractive features when compared to others to fit the requirement of FEA, because it offers high power density [15], efficiency, reliability and ruggedness. The performance comparison in [18], among many others, proves their superiority.

This paper proposes a multi-level CHB inverter to feed three phase permanent magnet synchronous motor (PMSM) for FEA powertrain applications. The study of multi-phase and fault tolerant solutions, more suitable in terms of reliability, is in progress and will be the subject of future papers. Section 2 presents the mathematical formulation of the whole system. In Section 3, advantages of MLI for FEA drives are discussed. The study is presented for *l*-level CHB MLI topologies, that justifies that the 9-level one gives the best trade-off between performance and cost [19]. Therefore, the 9-level inverter is considered for the explanation of MLI drive, but analysis is presented for 2, 5, 7 and 9-level inverter configurations. Simulated results and experimental implementation are presented in Section 4. Section 5 gives some conclusions.

2. CHB 9-Level Inverter Powertrain

2.1. Operation of 9-Level Inverter

CHB 9-level topology consists of four H-bridge modules per phase supplied with equal dc voltage sources, i.e., $V_{dc}/4$. Considering the phase A, the semiconductor devices are denoted as S_{1a}, S_{2a}, ... up to S_{16a}, as shown in Figure 1. In each H-bridge, switches of the same leg such as S_{1a}, S_{4a} and S_{5a}, S_{8a} and so on, are operated in complimentary fashion. In a similar manner, phase B and C are configured, $120°$ and $240°$ delayed from phase A, respectively. To obtain the staircase output waveform, the switching states are applied as shown in Table 1. To reduce losses, the switching states are selected in

a manner that only one switch has to be turned on, when the level is changed. The adopted modulation technique is the level-shifted carrier (LSC)-based PWM technique, with triangular wave C_j, j = 1, 2, ..., 8 as carrier with frequency equal to 10 kHz, as in Figure 2. This modulation technique eliminates the sector identification and complex timing calculations, which are necessary for the implementation of space vector PWM (SVM) technique. To obtain the same reference voltage waveforms of SVM, a third harmonic component has been introduced in order to increase the linear modulation range [20].

ω_{ref} = Speed Reference
ω_r = Speed Feedback

i_{dref}, i_{qref} = Current Reference
i_d, i_q = Current Feedback
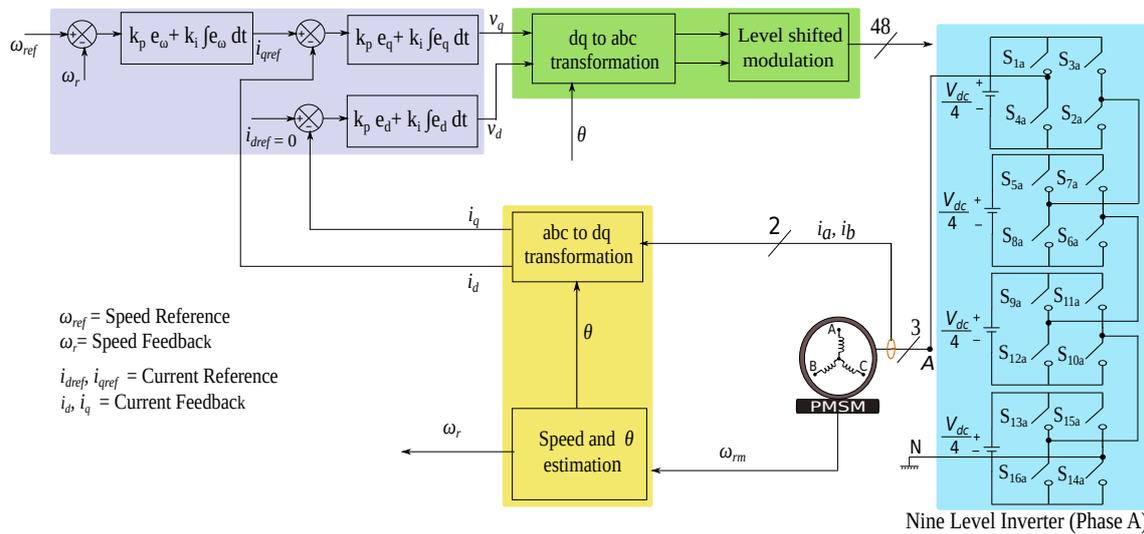
Figure 1. Block diagram of the 9-level inverter drive.
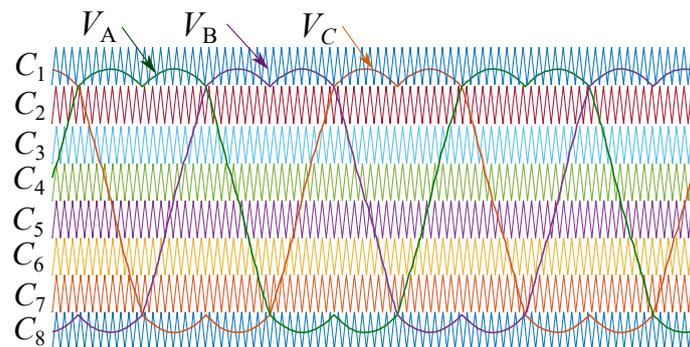
Figure 2. Carrier and modulating waveforms for LSCPWM.

Table 1. Nine voltage levels and their switching states.

V_{xN} *	Level	Switching States							
		S_{1a}	S_{3a}	S_{5a}	S_{7a}	S_{9a}	S_{11a}	S_{13a}	S_{15a}
V_{dc}	8	1	0	1	0	1	0	1	0
$3V_{dc}/4$	7	1	0	1	0	1	0	0	0
$2V_{dc}/4$	6	1	0	1	0	0	0	0	0
$V_{dc}/4$	5	1	0	0	0	0	0	0	0
0	4	0	0	0	0	0	0	0	0
$-V_{dc}/4$	3	0	1	0	0	0	0	0	0
$-2V_{dc}/4$	2	0	1	0	1	0	0	0	0
$-3V_{dc}/4$	1	0	1	0	1	0	1	0	0
$-V_{dc}$	0	0	1	0	1	0	1	0	1

* x = A, B, C.

2.2. Operational Principle of PMSM

In this study, aiming to investigate the behavior of multi-level PMSM drive, the conventional field oriented control (FOC) technique is implemented. Mathematical model of PMSM is formulated in *d-q* co-ordinates as

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} R_s + L_d\rho & -\omega_r L_q \\ \omega_r L_d & R_s + L_q\rho \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_r\phi \end{bmatrix}. \tag{1}$$

where v_d, v_q and i_d, i_q are stator voltages and currents in *d-q* axis, respectively, ρ is the differential operator, R_s is stator resistance, ω_r and ϕ are electrical angular speed and flux linkage of PMSM, respectively. L_d and L_q are stator inductances which have the same value L, a surface mounted type of PMSM is used. This type of motor has a small rotor diameter with low inertia and hence, finer dynamic performance. The electromagnetic torque T_e is given by

$$T_e = \frac{3}{2}\text{P}\,\phi i_q. \tag{2}$$

where P is number of pole pairs of the motor. The mechanical speed ω_{rm} is

$$\omega_{rm} = \frac{1}{J}\int(T_e - T_l - B\omega_{rm})dt. \tag{3}$$

where T_l, B, J are load torque, viscous friction coefficient and moment of inertia of the motor, respectively. The electrical speed of the machine can be obtained by using $\omega_r = \text{P}\,\omega_{rm}$. The electrical angle of the rotor θ is estimated from incremental encoder. Figure 1 shows the two cascaded control loops, outer is speed loop and the inner one is the current loop. For the speed control of drive, the speed error is generated by comparing the speed reference ω_{ref} with the obtained speed ω_r. This error is processed by speed PI controller, returning the current reference i_{qref}. The i_q is subtracted from i_{qref}, generating an error that is handled by the *q* PI controller, giving v_q stator voltage. The FOC method decouples the *d* and *q* axis, referring *d* to flux control and *q* to torque control. The stator voltage v_d is estimated from the error generated by comparing flux controller reference, i.e., zero and i_d. The v_d and v_q are converted to reference voltages V_A, V_B and V_C, for the comparison with carrier waves as explained in Section 2.1. The transformations from *dq* to *abc* and vice versa are performed using Clarke's and Park's transformations.

3. Analysis of CHB Multi-Level for FEA

In this section, the advantages obtained by using a CHB multi-level inverter in terms of THD% and torque ripple are discussed in detail. The harmonic mitigation is a great concern for power quality of converters as well as of overall FEA system. THD% is calculated using the following formula

$$\text{THD} = \frac{\sqrt{\sum_{n=2,3,\dots}^{49} H_n^2}}{H_1} \tag{4}$$

where H_n is the amplitude of the *n*th harmonic. For harmonic spectrum, in the y-axis, the amplitude of the *n*-harmonic H_n with respect to the fundamental H_1, in percentage value, is indicated. The considered fundamental frequency is 300 Hz and modulation index (MI) is 0.8. Figures 3a,b and 4a,b show the harmonic spectrum of output voltage of 2, 5, 7 and 9-level inverters, respectively.

It can be observed that the 2-level inverter has higher amplitude of dominant harmonics 31st and the 35th than that of the 9-level inverter. The harmonic spectrum of line-line voltage for 2, 5, 7 and 9-level inverter configurations without using a filter, are presented as shown in Figures 5a,b and 6a,b, respectively. It can be seen that in the 9-level inverter, all harmonics do not have significant amplitude at the considered frequency range. The current harmonic spectrum for all configurations are also presented as shown in Figures 7a,b and 8a,b, respectively. This signifies that 9-level configuration

requires a very light filter with respect to the 2-level inverter configuration. To obtain the same performances of 9-level configuration, a 2-level inverter must be used with higher switching frequency. In this case, the first not mitigated harmonic displaces to high order, but also switching, iron and copper losses increase.

(**a**)　　　　　(**b**)
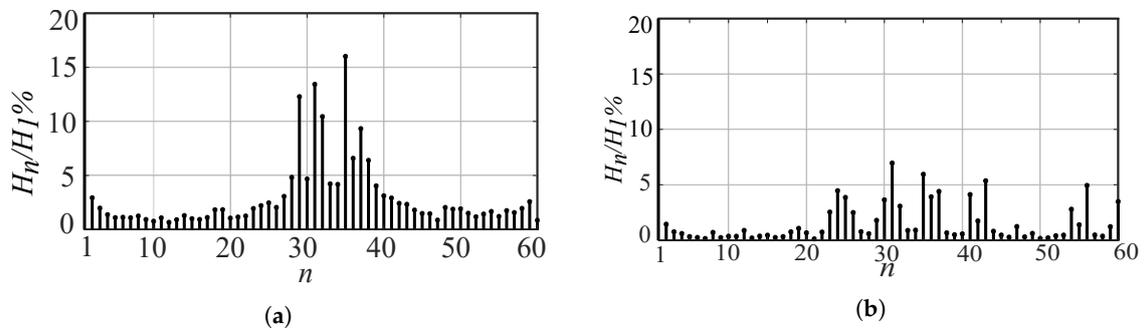
Figure 3. FFT of the output phase voltage: (**a**) TLI. (**b**) 5-level inverter.

(**a**)　　　　　(**b**)
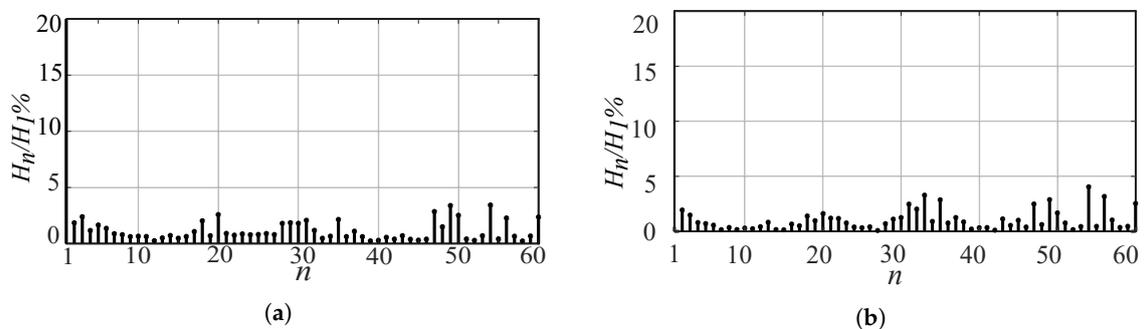
Figure 4. FFT of the output phase voltage: (**a**) 7-level inverter. (**b**) 9-level inverter.

(**a**)　　　　　(**b**)
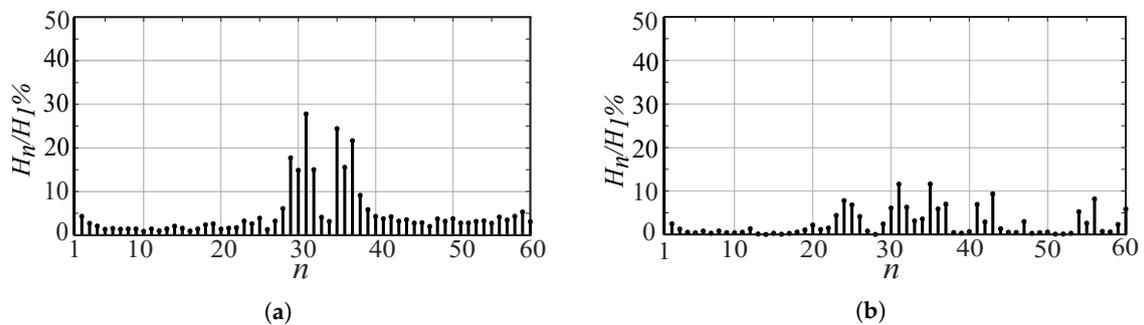
Figure 5. FFT of the output line-line voltage: (**a**) TLI. (**b**) 5-level inverter.

(**a**)　　　　　(**b**)
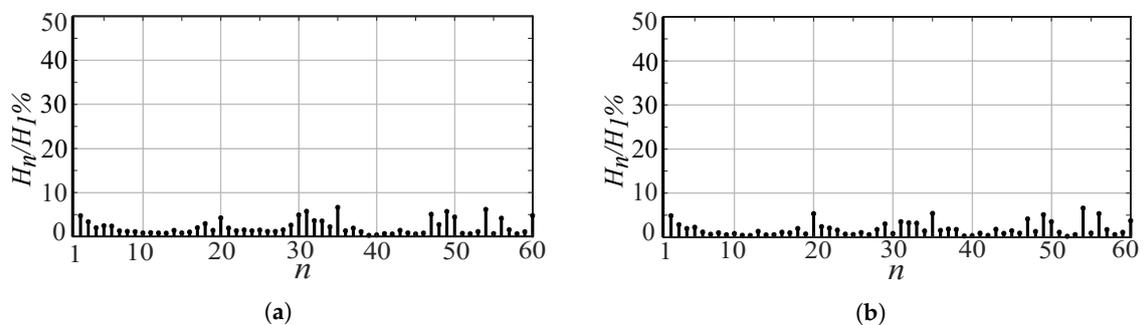
Figure 6. FFT of the output line-line voltage: (**a**) 7-level inverter. (**b**) 9-level inverter.

(**a**) (**b**)
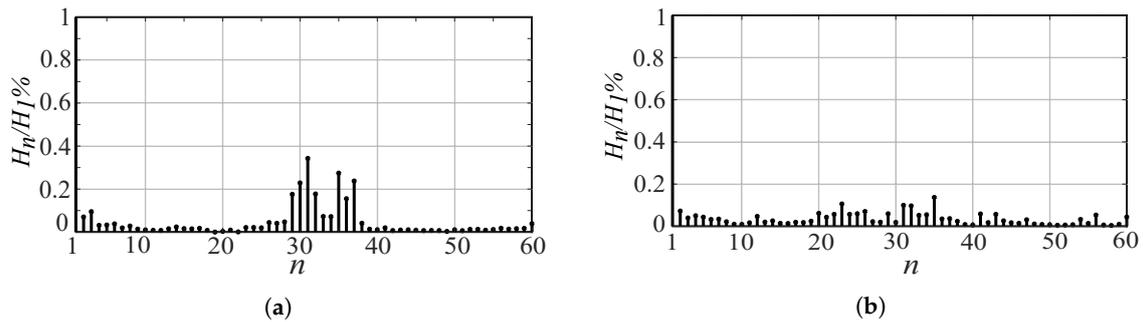
Figure 7. FFT of the phase current: (**a**) TLI. (**b**) 5-level inverter.

(**a**) (**b**)
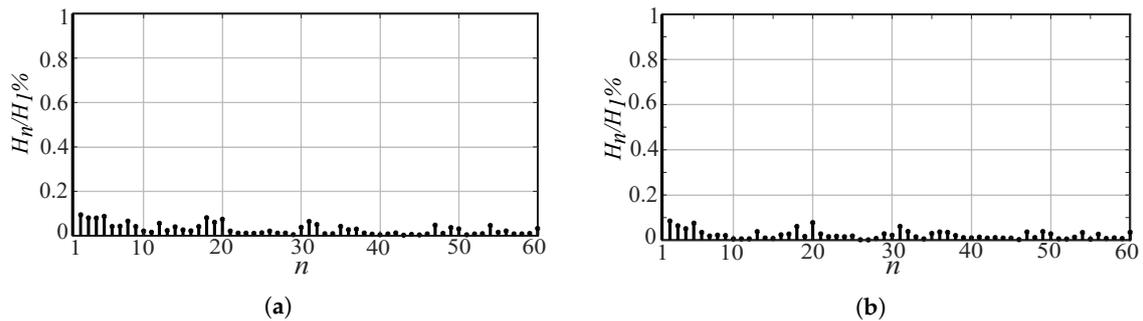
Figure 8. FFT of the phase current: (**a**) 7-level inverter. (**b**) 9-level inverter.

An investigation about the use of the *l*-level inverter powertrain for FEA is performed for l = 2, 5, 7, 9, for different MIs of the drive. Figure 9a shows THD% as a function of MI. For MI = 1, THD% = 56% for the 2-level inverter and THD% = 8.29% for the 9-level inverter. For the 5 and 7-level inverters, THD% is 16.62% and 9.95%, respectively. For the 9-level inverter, at MI = 0.8 and 0.4, THD% = 8.05% and 19.05%, respectively. Considering the 9-level inverter, if MI decreases from 0.8 to 0.4, THD% increases from 8.05% to 19.05%.

The analysis of torque ripple as a function of MI, for 2, 5, 7 and 9-level inverters is shown in Figure 9b. The y-axis quantities represent the percentage torque values with respect to its nominal value. At MI = 0.8, torque ripple for 2, 5, 7 and 9-level inverters is 0.138, 0.109, 0.0871 and 0.06617, respectively and for MI = 0.2, it is 0.268, 0.1547, 0.099 and 0.073, respectively. These results show that the 9-level inverter gives better performance compared to other configurations in terms of THD and torque ripple. A conventional 2-level inverter contains 6 high rated switches, while 9-level configuration contains 48 switches, but since the DC-link voltage is shared among them, they can be low rated devices.

(**a**) (**b**)
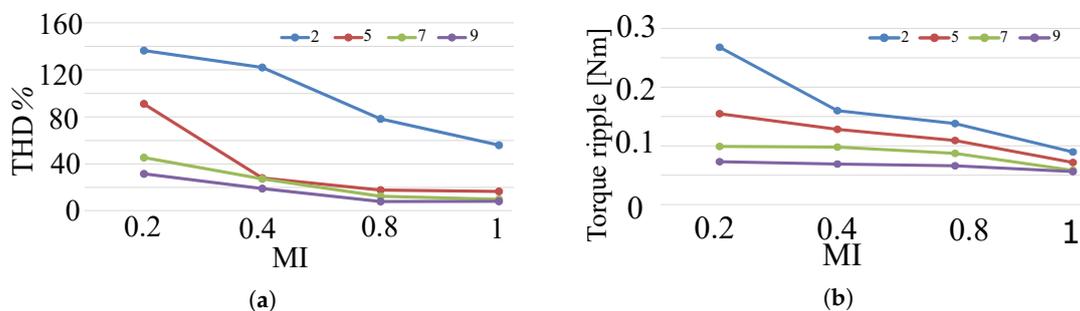
Figure 9. Comparison between 2, 5, 7 and 9-level inverter configurations: (**a**) total harmonic distortion (THD)%. (**b**) Torque ripple.

The efficiency of the drive is affected by high THD, torque ripple, switching and conduction losses, stress across the devices and this indirectly affects the life of the motor. The high torque ripple of the drive leads to vibrations, noise and wear of the machine. This not only damages the machine, but also the shaft and gearbox. The additional considered advantage of CHB MLI is that the total DC-link V_{dc} is

used to create levels, so each power switch has to share 1/4 (for 9-level inverter) of the total DC voltage. The switches have to bear less voltage stress across them, reducing dv/dt. High dv/dt indirectly affects the longevity of motor by dielectric heating of the insulation material [21]. Therefore, the promising use of multi-level inverters for FEA could significantly increase the life of the motor [22]. This sharing of voltages also makes it easier to find the lower voltage devices with lower price, which may reduce overall production and maintenance cost. These results show that the 9-level inverter gives better performance compared to the other configurations in terms of THD and torque ripple. Conventional TLI contains 6 high rated switches, while the 9-level configuration contains 48 switches. Since the DC-link voltage is shared among them, they can be low rated devices.

4. Results

This section presents simulation and experimental results considering the 9-level inverter that feeds PMSM for FEA application. Considering the transition from 2-level to 5-level to 7-level to 9-level, the 8 carrier waveforms, the phase voltage and the speed are shown in Figure 10. Figure 11 shows simulated results of the phase voltage, the line-line voltage and the phase current at a steady state speed of 1200 RPM. In addition, the zoomed view of these waveforms are shown. Figure 12 shows simulated speed feedback that follows the reference when speed changes from 500 RPM to 3000 RPM. There is a small change in torque and phase currents before it reaches the steady state, as shown in Figure 12. In Figure 13, a variation of torque from 0.1 Nm to 1 Nm is considered; little variation of speed and currents is observed.

Figure 14 shows the block diagram of the hardware implementation of 9-level inverter powertrain. The CHB 9-level inverter powertrain includes 12 H-bridge modules communicating with the control board through dedicated SPI channels. Each H-bridge uses STW120NF10 MOSFETs (100 V, 120 A), and is rated for 3.5 kW; moreover, it includes a local Texas Instruments TMS320F28379D DSP, which is in charge of I/O and A/D conversion, but it is expected to assume the role of computational engine for fault detection, diagnosis and reconfiguration algorithms. It is shown in Figure 14. The same H-bridge is available with 1200 V, 35 A insulated gate bipolar transistors (IGBTs), thus allowing to obtain more than 200 kW and 2.4 kV output voltage, which is a suitable power level for light aircrafts. It is expected to replace the three phase motor with a six phase motor under development. The new configuration requires 24 H-bridges, hence the control board is capable to offer a 9-level redundant converter. The control board mainly consists of 5CEBA9F31 CYCLONE V FPGA, 10M16DAF484 MAX10 CPLD and TMS320F28379D DSP. The internal architecture of the control board is as shown in Figure 15. The whole system, i.e., H-bridges, control board and auxiliary circuits, has been developed by DigiPower srl, an innovative SME based in L'Aquila, Italy.
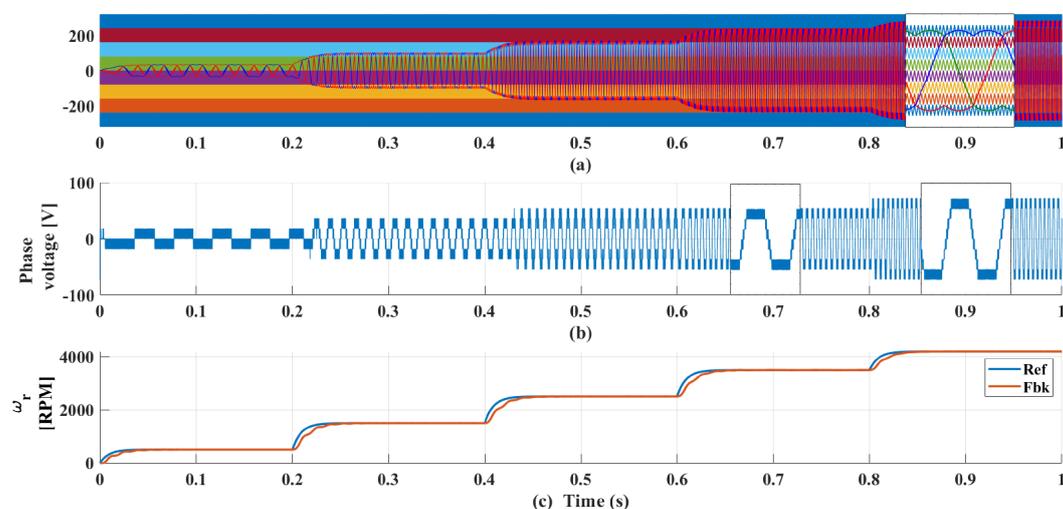
Figure 10. Simulation result obtained by using the 9-level inverter: (**a**) Eight carrier waveforms and modulating waveforms. (**b**) Phase voltage. (**c**) Speed reference (Ref) and speed feedback (Fbk).
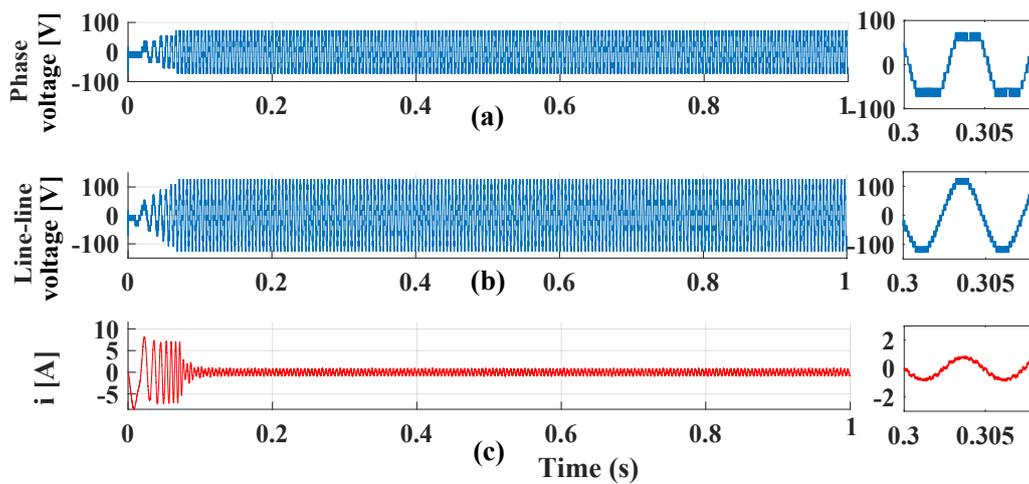
Figure 11. Simulation result of the 9-level inverter: (**a**) Phase voltage. (**b**) Line-line voltage. (**c**) Phase current.
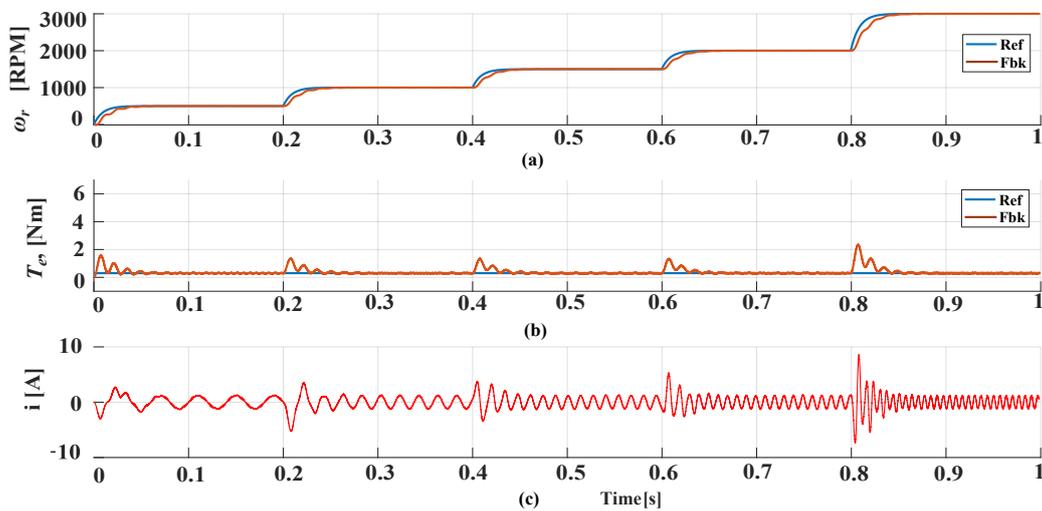
Figure 12. Simulation result of the 9-level inverter when the speed is varied: (**a**) Speed reference and its feedback. (**b**) Torque reference and feedback. (**c**) Phase current.
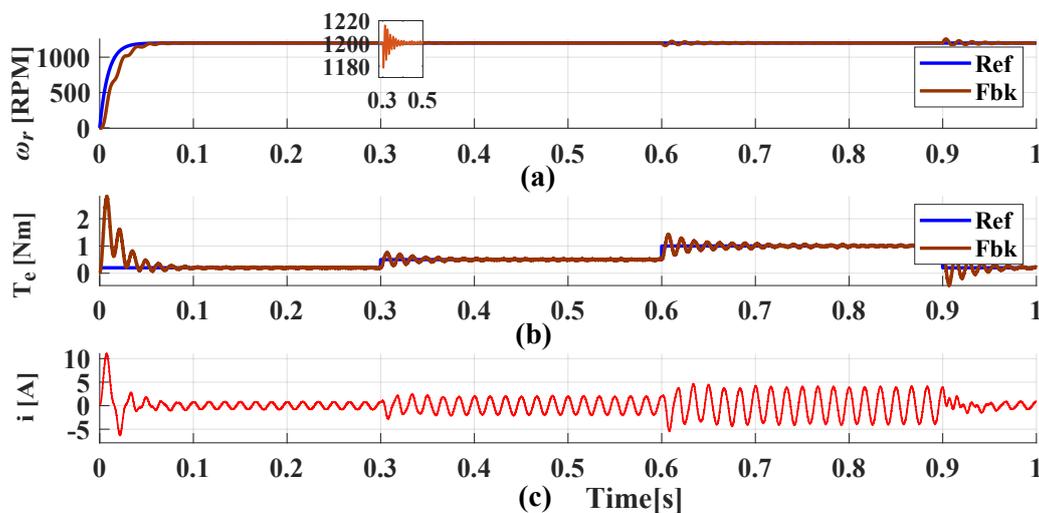
Figure 13. Simulation result of the 9-level inverter: (**a**) Speed reference and its feedback. (**b**) Torque reference and its feedback. (**c**) Phase current.
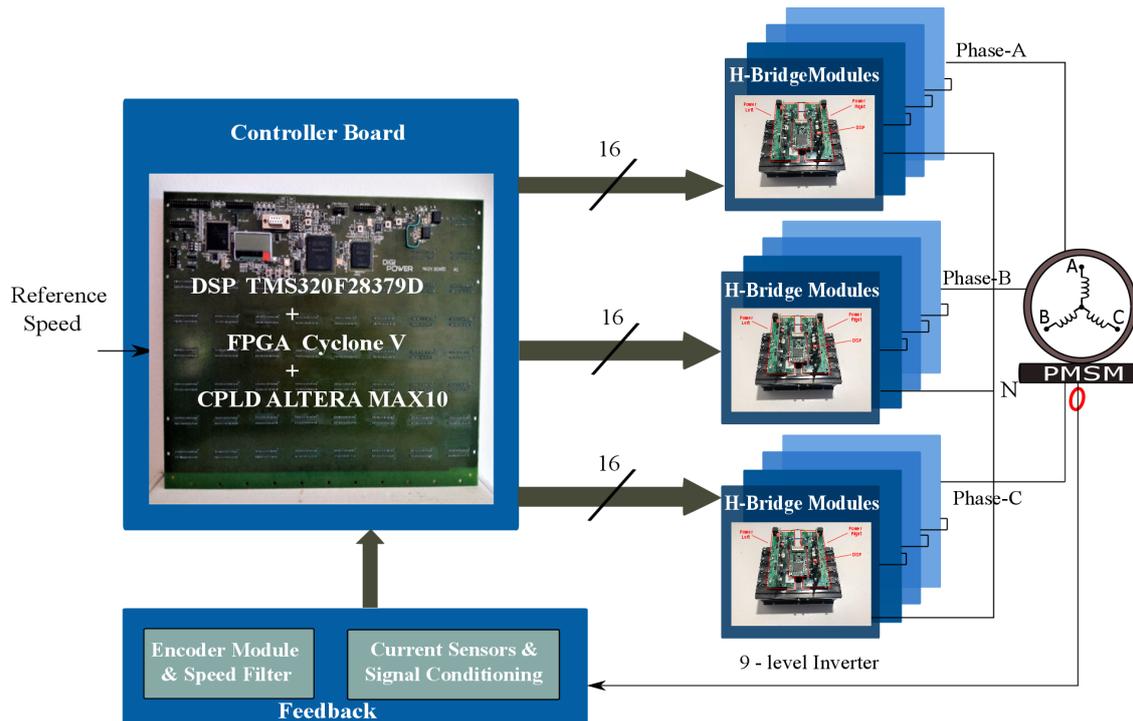
Figure 14. Block diagram of hardware implementation of the 9-level inverter drive.

Figure 15. Control board architecture.

Control board is capable to control up to 48 H-bridges and offers large computational capability and a full set of I/O channels including Ethernet [23]. The complete test rig is shown in Figure 16. Each H-bridge has its own DSP and both voltage and current sensors; communications between the control board and H-bridges are bidirectional, therefore the whole system has intrinsic fault tolerance capability. Each H-bridge will provide local fault details, then if a fault occurs in power switches, the local DSP will communicate with the control board which can isolate that H-bridge and reconfigure

the system, if the fault tolerant algorithm is implemented. The control logic block of FOC of the drive is implemented in DSP. The reference speed is the input of DSP, PI controllers are implemented in DSP, which generates the reference voltages V_A, V_B and V_C. These reference voltages are scaled down from 0 to 8 levels and PWM pulses are generated and sent to FPGA, where the switching states for each level are generated with dead time equal to 4 μs. The speed of the motor is sensed using incremental encoder, and it is calibrated in DSP. The currents of phases *A* and *B* are sensed using two LEM sensors, which are calibrated in DSP. The motor specifications are as shown in Table 2.

Table 2. Specifications of permanent magnet synchronous motor (PMSM).

Parameter	Symbols	Values
Rated power	P	6 [kW]
Rated current	I	5.3 [A]
Rated torque	T_e	3 [Nm]
Stator winding resistance	R_s	0.15 [Ω]
Stator winding inductance	L	0.85 [mH]
Rotor inertia	J	2.9 [Kg.m^2]
Pole pair	p	3
Rated speed	ω	6000 [RPM]
Permanent magnet flux	ϕ	0.0557 [Wb]
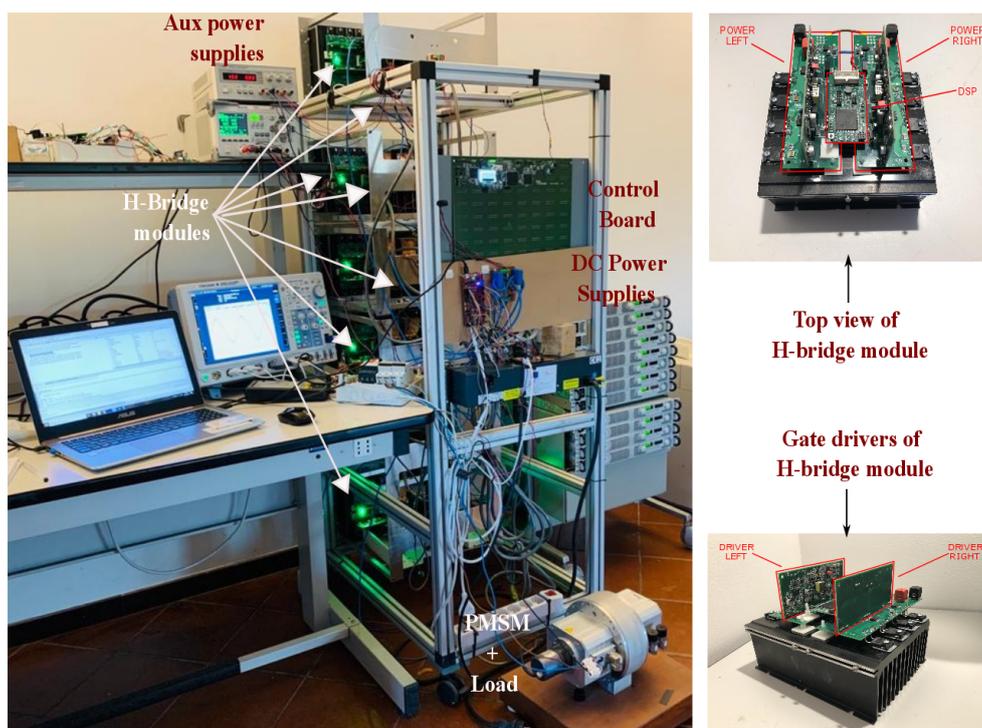
Figure 16. Test rig of cascaded H-bridge (CHB) 9-level inverter drive.

Figure 17a shows the experimental phase voltage and phase current waveform. Figure 17b shows the speed feedback when the motor is accelerated and decelerated. In particular, following the speed profile: from 3000 RPM to −3000 RPM to 3000 RPM to 600 RPM to −600 RPM to −3000 RPM, the speed feedback follows the speed reference, as shown in Figure 17b. It is also visible that when there is an increase in the speed reference, the phase current increases correspondingly. Figure 18a shows i_d and i_q when the motor is accelerated from 1000 RPM to 3600 RPM. This change affects mainly i_q, while i_d remains fairly constant. Similarly, when the speed is reduced from 3600 RPM to 1000 RPM Hz, the same behavior is observed as shown in Figure 18b. When the speed changes from −3000 RPM to 600 RPM, a little variation of torque is observed as shown in Figure 19a. A magnification of the last

Figure is given in Figure 19b. The harmonic spectrum of the 9-level inverter is shown in the Figure 20. The span of the figure is 40 kHz, and the center is at 20 kHz. It is visible that the dominant harmonic present is at 33rd harmonic order, which is 10 kHz. This dominant harmonic is magnified and shown in the figure with its sidebands, validating the simulated harmonic spectrum.

(**a**)   (**b**)
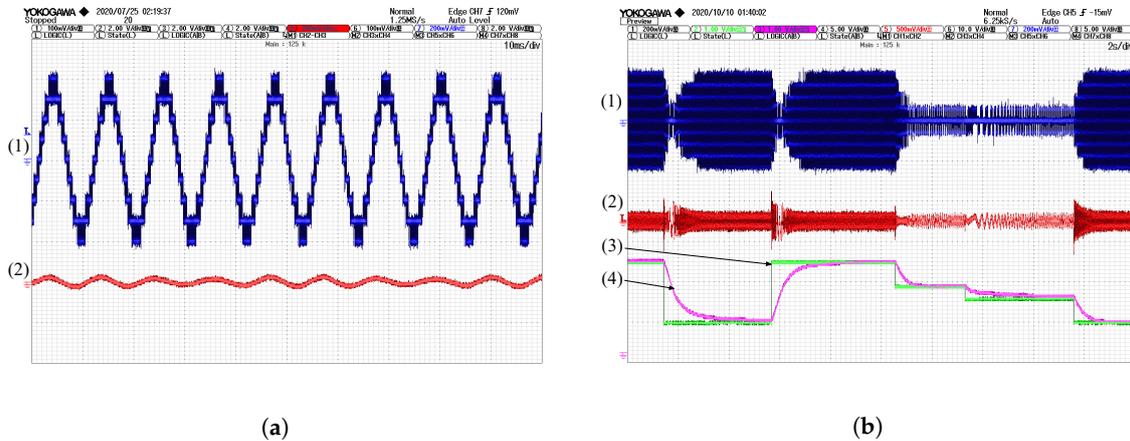
Figure 17. Experimental result for the 9-level inverter: (**a**) (**1**) Phase voltage (y-axis: 20 V/div), (**2**) phase current (y-axis: 2 A/div). (**b**) (**1**) Phase voltage (y-axis: 20 V/div), (**2**) phase current (2 A/div), (**3**) speed reference (y-axis: 1820 RPM/div), (**4**) speed feedback (y-axis: 1820 RPM/div).

(**a**)   (**b**)
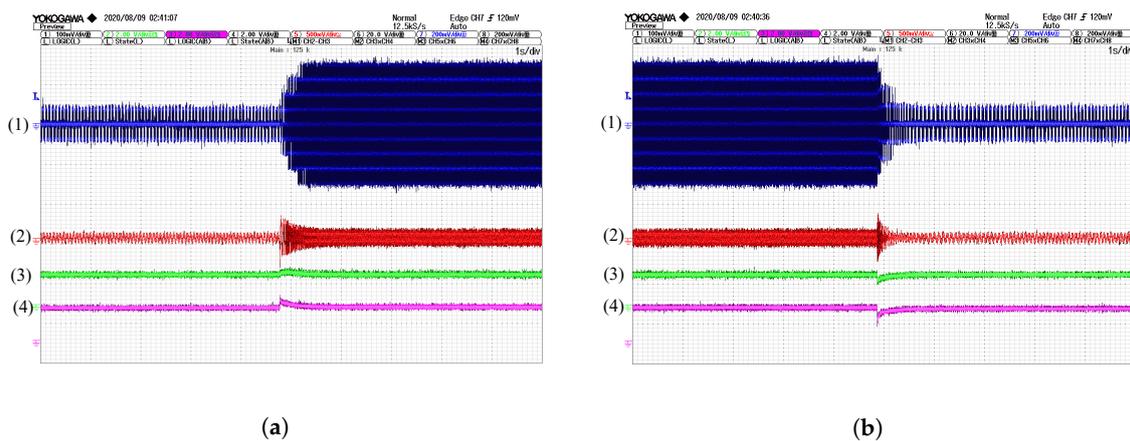
Figure 18. Experimental result for the 9-level inverter: (**a**) (**1**) Phase voltage (y-axis: 20 V/div), (**2**) phase current (y-axis: 5 A/div), (**3**) i_d (y-axis: A/div), (**4**) i_q (y-axis: A/div). (**b**) (**1**) Phase voltage (y-axis: 20 V/div), (**2**) phase current (y-axis: 5 A/div), (**3**) i_d (y-axis: A/div), (**4**) i_q (y-axis: A/div).

(**a**)   (**b**)
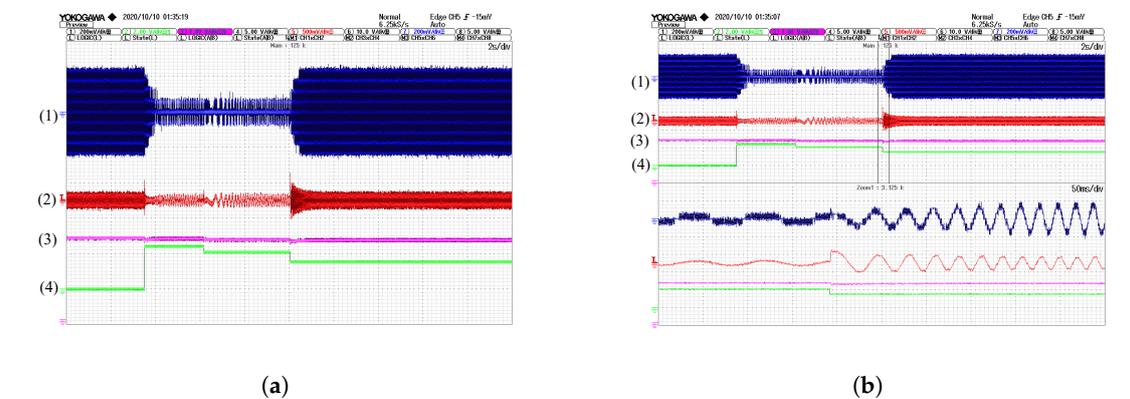
Figure 19. Experimental result when speed is varied for the 9-level inverter: (**a**) (**1**) Phase voltage (y-axis: 20 V/div), (**2**) phase current (y-axis: 5 A/div), (**3**) torque (y-axis: Nms), (**4**) speed reference (y-axis: 3600 RPM/div). (**b**) (**1**) Phase voltage (y-axis: 20 V/div), (**2**) phase current (y-axis: 5 A/div), (**3**) torque (y-axis: Nm), (**4**) speed reference (y-axis: 3600 RPM/div).
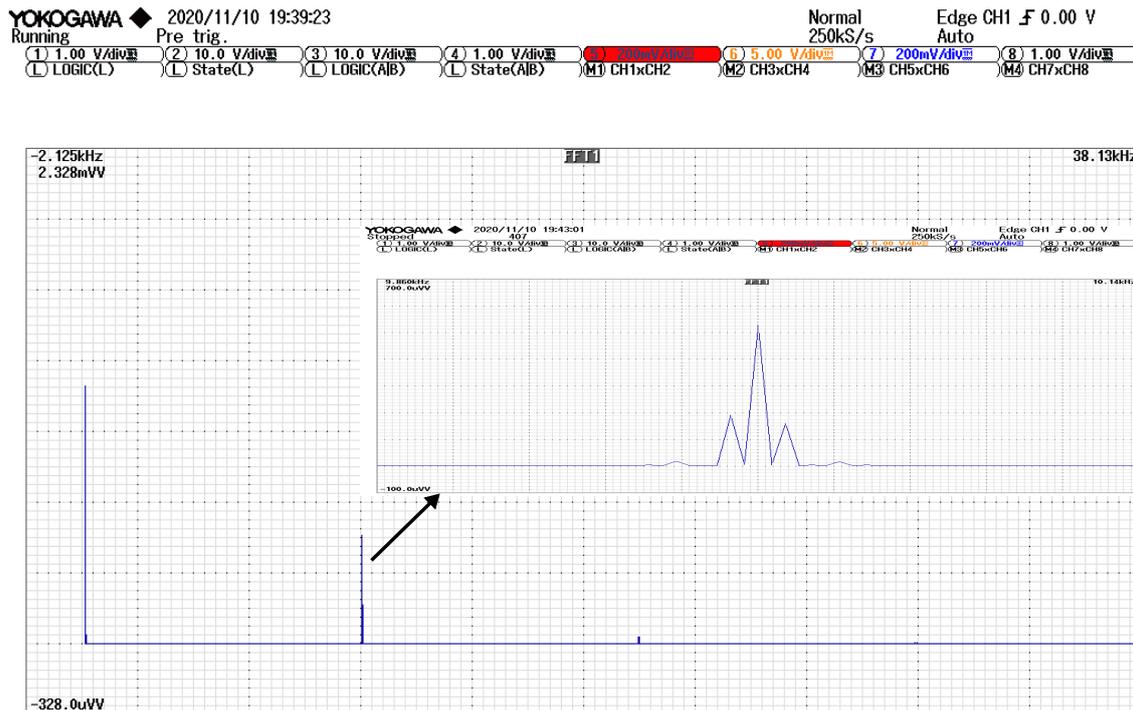
Figure 20. Experimental harmonic spectrum of phase voltage for the 9-level inverter.

5. Conclusions

The growth of FEA applications implies the development of large scale capability power converters. In this paper, a CHB 9-level inverter feeding PMSM for FEA applications has been proposed. It has been shown that the THD% reduces as the number of levels are increased, in turn reducing dv/dt. DC-link voltage is shared between the H-bridge modules as number of level increases, consequently it is possible to use low rated devices. The torque ripple is also reduced in comparison to TLI; the efficiency and the life of the motor are also improved. The adopted prototype of the multi-level converter developed by DigiPower can be used with high power motors and with multi-phase machines and in fault tolerant configurations. Experimental results have been presented to validate the theoretical analysis.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

PE	Power electronics
MLI	Multilevel inverter
FEA	Full electric aircraft
CHB	Cascaded H-bridge
THD	Total harmonic distortion

MI   Modulation index
PMSM   Permanent magnet synchronous motor
P I   Proportional integral

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