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A Genetic-Algorithm-Based DC Current Minimization Scheme for Transformless Grid-Connected Photovoltaic Inverters

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Abstract: Transformerless grid-connected inverters are of great industrial value in photovoltaic power generation. However, the direct current (DC) induced into the inverter's output degrades the power quality of the grid. Recently, a back-propagation neural work proportional–integral–derivative (BP-PID) scheme has proven helpful in solving this problem. However, this scheme can be improved by reducing the suppressing time and overshoot. A genetic algorithm (GA)-based DC current minimization scheme, namely the genetic-algorithm-based BP-PID (GA-BP-PID) scheme, was established in this study. In this scheme, GA was used off-line to optimize the initial weights within the BP neural network. Subsequently, the optimal weight was applied to the online DC current suppression process. Compared with the BP-PID scheme, the proposed scheme can reduce the suppressing time by 59% and restrain the overshoot. A prototype of the proposed scheme was implemented and tested on experimental hardware as a proof of concept. The results of the scheme were verified using a three-phase inverter experiment. The novel GA-PB-PID scheme proposed in this study was proven efficient in reducing the suppressing time and overshoot.

Keywords: DC current; grid-connected inverter; genetic algorithm; back-propagation neural network

1. Introduction

Due to their high efficiency and small geometry, transformerless grid-connected inverters are widely used in the field of photovoltaic power generation [1,2]. Ideally, only the alternating current (AC) is contained in the output of the grid-connected inverter. However, several issues may induce direct current (DC) into the output: (1) asymmetries in the switching behavior of power semiconductor devices, (2) the existing DC current in the grid and unbalanced grid-voltage, (3) the non-parity pulse width modulation (PWN) duty-ration of the gate drivers, (4) turn-on/off delays of the device, and (5) DC current from current detecting errors [3,4]. A tiny DC current injection can cause saturation and reduce the lifetime of distribution transformers in the grid. Consequently, problems such as degradation of power quality, higher energy loss, line-frequency power ripples, and overheating issues will occur. This may lead to unnecessary economic losses. Therefore, it is important to suppress the DC current as fast as possible, so the hazards caused by the DC current can be minimized.

Many countries and non-government organizations have established strict standards to inhibit DC current injection into the grid [5]. There have been several prior efforts to suppress the DC current based on a transformerless grid-connected inverter. The solutions for DC current suppression can be

classified into four schemes: (1) DC current suppression inverters [6–11]; (2) detection and compensation methods [3,12–15]; (3) methods using AC capacitors to block DC-current [14,16,17]; and (4) methods deploying a low-frequency isolation transformer as the inverter output [11,12,16,18]. An adaptive controller scheme, the back-propagation (BP) neural network proportional–integral–derivative (PID) controller scheme, is one possible detection and compensation method. Compared with the schemes using isolation transformers, AC capacitors, or virtual capacitors, the BP-PID scheme is the most direct and efficient suppressing scheme and also uses the simplest current sensor. Moreover, the BP-PID scheme can adaptively adjust the parameters of the PID controller. Thus, it shows better suppressing performance than traditional PID controller schemes. However, this scheme can still be improved by reducing its suppressing time and overshoot.

It is noteworthy that a BP neural network will generate the PID parameters to suppress DC current in an iterative process. The subsequent weight will be generated based on the initial weights. This means that selecting proper initial weights can improve the performance of the BP-PID scheme. Therefore, it is important to select a suitable initial BP neural network to suppress the DC current.

To achieve this purpose, the influence of the BP neural network's weight in the DC current suppressing process was analyzed. A novel DC suppression scheme, the genetic-algorithm (GA)-based BP-PID controller scheme (the GA-BP-PID scheme), is proposed. The GA is employed to optimize the weight of the neural network off-line within the BP-PID scheme. Then, the optimal weight is applied to the BP-PID controller for the on-line operating process. Based on the simulation process, the GA-BP-PID scheme shows better performance in the DC current suppression process than the BP-PID scheme and can efficiently reduce the suppressing time and overshoot.

The contributions of this paper are summarized as follows:

(1) We analyze the influence of the weight within back propagation (BP) neural network on the DC current suppression process.
(2) A novel DC current suppression genetic-algorithm-based BP-PID controller scheme, named GA-BP-PID, is established.
(3) We verify the performance of the GA-BP-PID scheme based on the experimental setup. The results show that the proposed scheme can efficiently reduce the suppressing time and overshoot.

This paper is organized as follows. Section 2 offers the methodology, which briefly introduces the topology of the inductive-capacitive-inductive (LCL)-type three-phase grid-connected inverter and BP-PID control scheme. Then, we discuss the influence of the BP neural network's initial weights on the suppression results. After that, we introduce the GA program and implementation process. Section 3 provides the simulation and results. Section 4 presents the experimental setup and results. Lastly, Section 5 provides the conclusion.

2. Methodology

The BP-PID scheme has proven helpful in suppressing DC current based on the LCL-type three-phase grid-connected inverter. Several recent scientific studies on power grid show that receding robust optimization instead of classical optimization is a viable technique to deal with uncertainty of parameters [19–21]. The BP neural network can automatically regulate the coefficients of the PID controller based on the dynamic DC current. The weights, especially the initial weights within the BP neural network, will influence the parameters of the PID controller. Thus, it is important to select proper initial weights for the BP-PID scheme. In this paper, the GA-BP-PID scheme is proposed to obtain the optimal initial weights in order to improve the suppressing performance of the BP-PID controller. This scheme can be divided into two parts, an off-line part and an on-line part, as shown in Figure 1.

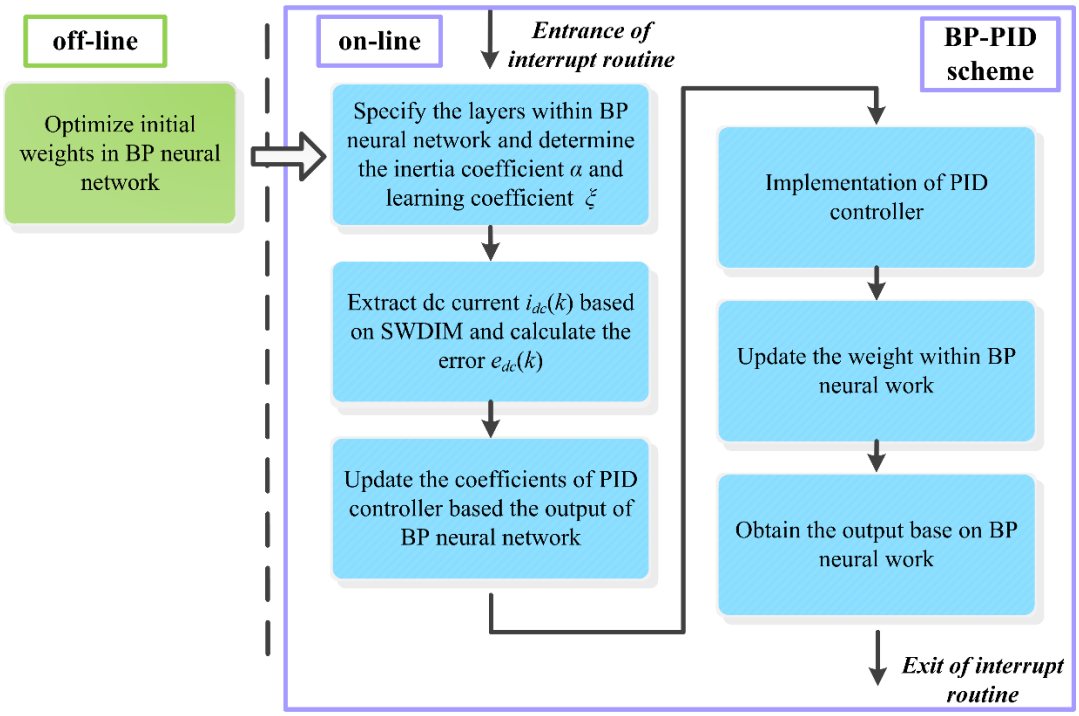
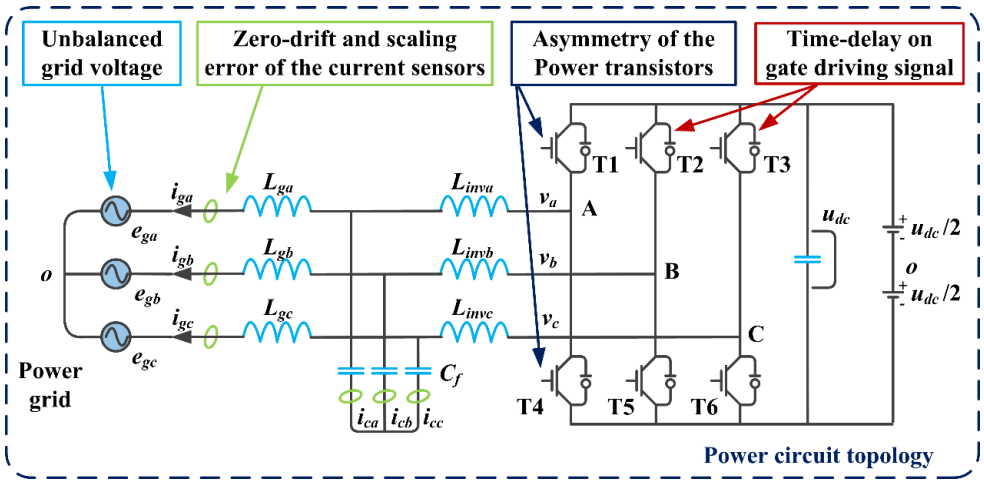


Figure 1. Flow chart of the genetic-algorithm-based back propagation neural network proportional–integral–derivative controller (GA-BP-PID) scheme for both the on-line and off-line regions. The BP-PID controller is only shown for the on-line region.

In the off-line part, GA optimizes the initial weights within the BP neural network. Then, the optimal weights are applied to the on-line part. Correspondingly, the optimal weights will be applied to the BP-PID scheme, and the suppressing process will operate based on them.

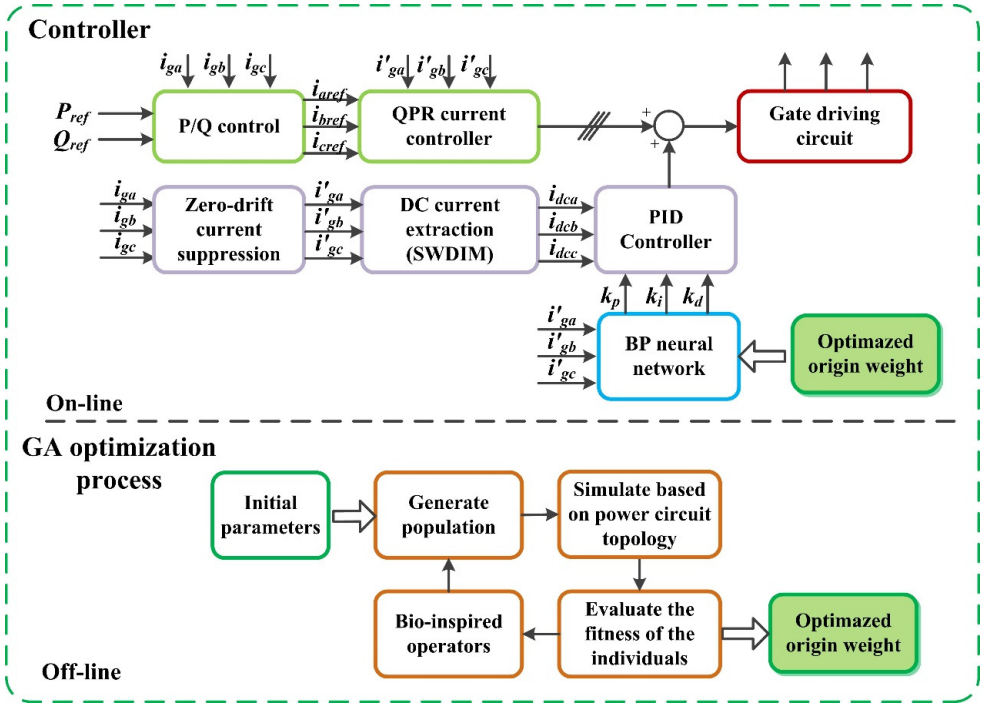
2.1. Topology of the inductive-capacitive-inductive (LCL)-Type Three-Phase Grid-Connected Inverter

The A P/Q control scheme of the three-phase photovoltaic inverter is shown in Figure 2. The three-phase voltage-source two-level inverter and LCL filter are employed to connect the photovoltaic array and the grid. An LCL filter with a star connection is applied in this study.



(a)

Figure 2. *Cont.*



(**b**)

Figure 2. Block diagram of the proposed direct current (DC) suppression scheme. (**a**) Power circuit topology of the inductive-capacitive-inductive (LCL) filter. (**b**) Block diagram of the controller.

In Figure 2, v_a, v_b, and v_c are the inverter-side output voltages. i_{ga}, $i_{gb,}$ and i_{gc} are the grid currents of each phase. i_{aref}, i_{bref}, and i_{cref} are the reference currents. L_{inva}, L_{invb}, and L_{invc} are the inverter-side inductance. L_{ga}, L_{gb}, and L_{gc} are the grid-side inductance. e_{ga}, e_{gb}, and e_{gc} are the three-phase grid voltages. u_{dc} is the DC bus voltage. The sliding window double-integration method (SWDIM) was used to extract the grid current.

2.2. Back Propagation Neural Network Proportional–Integral–Derivative (BP-PID) Control Scheme

In a conventional DC current suppression scheme, the controller parameters are fixed. These fixed parameters are not suitable for dynamic references. Unsuitable parameter specifications will sometimes cause the system to become unstable. Thus, it is important to select suitable parameters for the scheme. However, the selection process can entail a great deal of trial and error.

A BP-PID control scheme is developed to solve this problem [3,22]. The block diagram of this scheme is shown in Figure 1. This scheme can efficiently regulate the coefficients of the PID controller. Thus, it can effectively suppress the DC current and reduce the total harmonic distortions in the grid current.

The BP-PID control procedure entails four steps. Firstly, decide on the initial weight coefficients within the BP network and determine the inertia and learning coefficients of the BP controller. Secondly, extract the DC current and calculate the DC current error. Thirdly, update the parameters of the PID controller based on the BP network. Lastly, update the weight coefficient within the BP network and regulate the on-line parameters. A flow chart of the BP-PID controller is shown in Figure 1.

2.3. The Influence of the Initial Weights within the BP Neural Network on Direct Current (DC) Suppression

The initial weights within the BP neural network can affect the efficiency adjustment of the PID parameters. An improper weight may lead to several problems, such as an increase in the suppressing time, overshoot, and divergence. Therefore, it is necessary to develop a novel scheme to select a

suitable weight. A three-layer BP neural network is presented as an example. The variables within the BP-PID scheme are shown in Table 1.

Table 1. The variables within the BP-PID scheme.

Symbol	Parameter
$\omega_{in,k}$	The kth iterated weights between the input layer and hidden layer
$\omega_{out,k}$	The kth iterated weights between the hidden layer and output layer
ξ_k	Learning coefficient
α_k	Inertia coefficient
Δ_k	Change of DC current
ih_k	lengths of the adjustment for $\omega_{in,k}$
oh_k	lengths of the adjustment for $\omega_{out,k}$

The weights between the neural network layers can be calculated as described below:

$$\omega_{in,k} = \omega_{in,k-1} - \xi_k(1-\alpha_k)\cdot\Delta_k\cdot ih_k + \alpha_k(\omega_{in,k-1} - \omega_{in,k-2}) \tag{1}$$

$$\omega_{out,k} = \omega_{out,k-1} - \xi_k(1-\alpha_k)\cdot\Delta_k\cdot oh_k + \alpha_k\cdot(\omega_{out,k-1} - \omega_{out,k-2}) \tag{2}$$

where $\omega_{in,0}$ and $\omega_{out,0}$ are preset constants, and $\omega_{in,1}$ and $\omega_{out,1}$ can be obtained as

$$\omega_{in,1} = \omega_{in,0} - \xi_1(1-\alpha_1)\cdot\Delta_1\cdot ih_1 \tag{3}$$

$$\omega_{out,1} = \omega_{out,0} - \xi_1(1-\alpha_1)\cdot\Delta_1\cdot oh_1 \tag{4}$$

where ξ is learning coefficient. α is inertia coefficient. Δ describes the change in the DC current, and ih and oh are the step lengths of the adjustment.

Move $\omega_{in,k-1}$ in (1) and $\omega_{out,k-1}$ in (2) to the left-hand side, and the iterative function can be rewritten as (5) and (6):

$$\omega_{in,k} - \omega_{in,k-1} = \alpha_k(\omega_{in,k-1} - \omega_{in,k-2}) - H_{in,k} \tag{5}$$

$$\omega_{out,k} - \omega_{out,k-1} = \alpha_k(\omega_{out,k-1} - \omega_{out,k-2}) - H_{out,k} \tag{6}$$

where

$$H_{in,k} = \xi_k(1-\alpha_k)\cdot\Delta_k\cdot ih_k \tag{7}$$

$$H_{out,k} = \xi_k(1-\alpha_k)\cdot\Delta_k\cdot oh_k \tag{8}$$

Then, define $f_{in}(k) = \omega_{in,k} - \omega_{in,k-1}$, and Equation (9) can be obtained based on (5):

$$f_{in}(k) = \alpha_k f_{in}(k-1) - H_{in,k} \tag{9}$$

By expanding $f_{in}(k-1)$ and re-inserting it into (9), $f_{in}(k)$ can be expressed as (10):

$$f_{in,k} = \prod_{i=1}^{k-1}\alpha_{k+1-i} f_{in,1} - H_{in,k} - \sum_{i=1}^{k-2}(H_{in,k-i}\cdot\prod_{j=1}^{i}\alpha_{k+1-j}) \tag{10}$$

Define $G_{in,k} = H_{in,k} + \sum_{i=1}^{k-2}(H_{in,k-i}\cdot\prod_{j=1}^{i}\alpha_{k+1-j})$. Then, (10) can be rewritten as:

$$f_{in,k} = \prod_{i=1}^{k-1}\alpha_{k+1-i}\cdot f_{in,1} - G_{in,k} \tag{11}$$

Thus,

$$\sum_{i=1}^{k} f_{in,i} = \sum_{i=1}^{k} \prod_{j=1}^{i-1} \alpha_{i+1-j} \cdot f_{in,1} - \sum_{i=1}^{k} G_{in,i} \tag{12}$$

Expand the left-hand side of Equation (12) to yield,

$$\omega_{in,k} - \omega_{in,1} = \sum_{i=1}^{k} \prod_{j=1}^{i-1} \alpha_{k+1-j} \cdot (\omega_{in,1} - \omega_{in,0}) - \sum_{i=1}^{k} G_{in,i} \tag{13}$$

Based on (3), $\omega_{in,1}$ can be shown as,

$$\omega_{in,1} = \omega_{in,0} - H_{in,1} \tag{14}$$

Move (14) into (13), and the kth weight between the input layer and hidden layer $\omega_{in,k}$ can be described as below:

$$\omega_{in,k} = \omega_{in,0} - (1 + \sum_{i=1}^{k} \prod_{j=1}^{i-1} \alpha_{i+1-j}) \cdot H_{in,1} - \sum_{i=1}^{k} G_{in,i} \tag{15}$$

Similarly, the kth weight between the hidden layer and output layer $\omega_{out,k}$ is determined by

$$\omega_{out,k} = \omega_{out,0} - (1 + \sum_{i=1}^{k} \prod_{j=1}^{i-1} \alpha_{i+1-j}) \cdot H_{in,1} - \sum_{i=1}^{k} G_{in,i} \tag{16}$$

Using (15) as an example, the right-hand terms can be separated into two parts, $\omega_{in,0}$ and $-(1 + \sum_{i=1}^{k-1} \prod_{j=1}^{i} \alpha_{k+1-j}) \cdot H_{in,1} - \sum_{i=1}^{k-1} G_{in,i}$, where the second term is related to learning speed ξ_k and α_k. This means that $\omega_{in,k}$ is the kth accumulated adjustment of the original value, $\omega_{in,0}$. Therefore, this adaptive scheme can improve the suppression time based on adjusting the learning speed, as shown in the previous attempts. Moreover, selecting proper initial weights close to the ideal weight can also improve the suppression performance.

2.4. Genetic Algorithm (GA)-BP-PID Scheme

The GA is widely used to solve optimal problems because of its excellent optimization efficiency and global search capabilities. The GA imitates nature's selection process and obtains the optimal solution based on several bio-inspired operators, such as selection, crossover, and mutation. After an iterative calculation, the optimal result can be obtained. In this study, the GA toolbox based on MATLAB [23] is employed to optimize the weights within the BP neural network.

In this study, the aim of the optimization problem is to find a group of initial weights that can minimize the suppression time and overshoot. This means that the optimization process should shorten the suppression time as much as possible and limit the amplitude of the overshoot. The objective function of this multi-objective optimization problem can be described as below:

$$F(X) = c_1 \cdot F_t(X) + c_2 \cdot F_{os}(X) \tag{17}$$

where

$$F_t(X) = T(X)/T(R) \tag{18}$$

$$F_{os}(X) = \begin{cases} A_{os}(X)/C, & where\ A_{os}(X) > C \\ 0\ , & otherwise \end{cases} \tag{19}$$

The optimization problem is to minimize the objective function $F(X)$:

$$\min F(X) \tag{20}$$

s.t.

$$X_{ij} \in [R_l, R_u] \tag{21}$$

where X is the individual potential solution of the GA program, and X_{ij} is a weight between two nodes in different layers, which is a variable vector containing the weights for both the input layer to the hidden layer and the hidden layer to the output layer. The number of the weight depends on the number of layers and nodes within the BP neural network. $F(X)$ is the total fitness value, while c_1 and c_2 are the weight coefficients. F_t (X) and $F_{os}(X)$ are the evaluation of suppression time and overshoot, respectively. $T(X)$ is the suppression time based on a variable vector. Similarly, $T(R)$ indicates reference time consumption and is set as 0.1 s in this problem. $F_{os}(X)$ is a piecewise function to evaluate the overshoot. $A_{os}(X)$ is the maximum amplitude of the overshoot. C is a constant, and R_l and R_u are the upper and lower bounds of the weight. In this paper, the weight coefficients are set as $c_1 = 1$, $c_2 = 1$; constant C is set as $C = 20$ mA, and the upper and lower bounds are set as $R_l = -5$, $R_u = 5$.

There are four major steps within the GA optimization progress, as presented in Figure 3. In the first step, the parameters within the optimization progress are initialized, such as population size, maximum generation, population, bio-inspired operators, etc. In the second step, each individual of the population will be transformed into a matrix form. These matrixes will be applied to the simulation models of the LCL-type three-phase grid-connected inverter. Then, the Simulink software will be used for the simulation process. In the third step, after the simulation work, the suppression time and maximum amplitude are extracted, and the total fitness value $F(X)$ can be calculated. In the last step, individuals will be assessed based on their fitness values, and bio-inspired operators will be used to adjust their values. Iterating steps 2–4 can obtain the individual with the best fitness—that is, the optimal solution. A flow chart of the GA-BP-PID controller is shown in Figure 2.

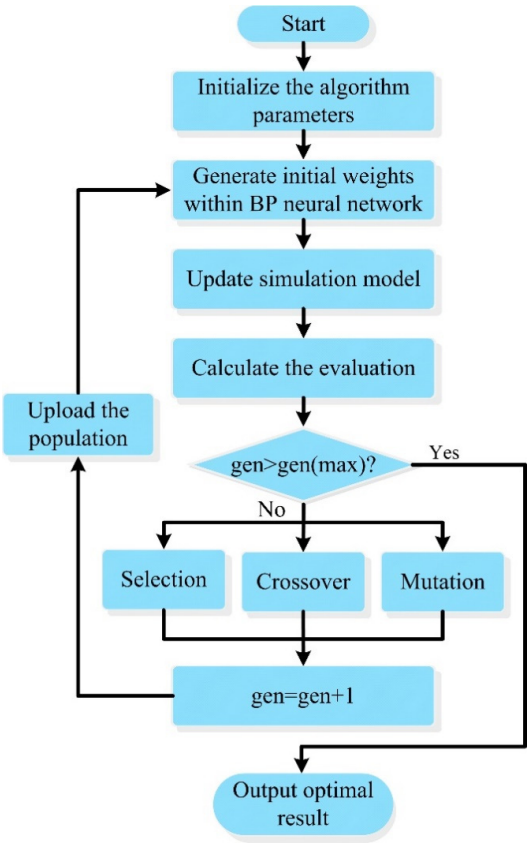


Figure 3. Flow chart of the genetic algorithm program.

3. Simulation Results

3.1. Simulation Parameters

Simulink software was employed to validate the performance of the proposed scheme. A simulation model base on the topology of an LCL-type three-phase grid-connected inverter, as shown in Figure 2, was established. The parameters of the LCL-type three-phase grid-connected inverter are shown in Table 2.

Table 2. The parameters of the LCL-type three-phase grid-connected inverter.

Parameter	Symbol	Value
Rated Power	P_e	2 kW
Grid Line Voltage	u_{AB} u_{BC} u_{CA}	380 V
DC Bus Voltage	U_{dc}	700 V
DC Capacitance	C	3400 μF
Grid Frequency	F	50 Hz
Grid Resistance	r_g	0 Ω
Grid Inductance	L_g	1 mH
Switching Frequency	f_{sw}	10 kHz
Inverter Side Inductance	L_{inv}	2 mH
Inverter Side Resistance	r_{inv}	0 Ω

3.2. GA Optimization Result

A GA program was used for the simulation process. This program generates the weight for the BP neural network. This weight will be transferred into the BP controller of each phase through three constant blocks. The parameters used in the GA program are designed based on the number of variables and the optimization problem [24,25]. The values of these parameters are shown in Table 3.

Table 3. The parameters in the genetic algorithm (GA) program.

Parameter	Value
Max Generation	250
Number of Individual	200
Mutation Rate	0.7
Generation Gap	0.85

The objective function used in this optimization problem are the same as those used in Section 2.4. The minimum objective value in each generation is shown in Figure 4. This figure shows that the minimum objective value decreased rapidly before the first 100 generations and remained steady after 200 generations.

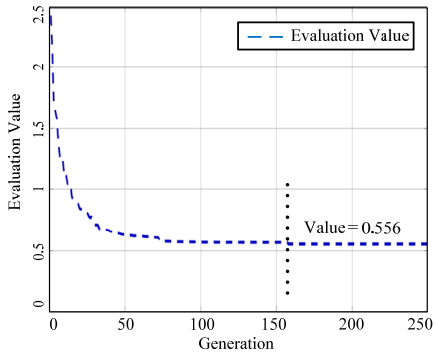


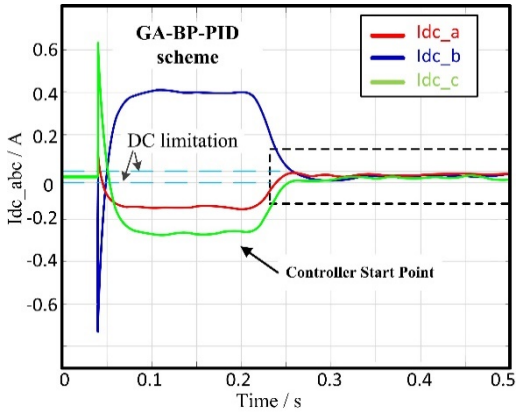
Figure 4. The minimum objective value in each generation.

In this study, a BP neural network with three layers was employed to establish the PID controller. There are four nodes in the input layer, five nodes in the hidden layer, and three nodes in the output layer. This means that the weight between the input layer and the hidden layer is a 4×5 matrix, while another 5×3 matrix is used for the weight between the hidden layer and the output layer. The BP neural network can iteratively generate the parameters of the controller, as described in Section 2.2.

A computer equipped with an Intel(R) Core(TM) i7-2600 CPU was used for the calculations. The frequency of the CPU was 3.40 GHz, and the computer's memory was 8 GB. This computer takes about 40 seconds to accomplish one simulation process. Parallel computation with four threads is induced for the simulation process and cost about 5 days for the entire optimization process.

3.3. Comparison with BP-PID Control

To verify the effectiveness of the proposed scheme, the suppression results of the proposed scheme are compared with those of the BP-PID scheme. During the simulation process, the initial amplitudes of the DC current were set as −0.15 A, 0.4 A, and −0.25 A in phase-A, B, and C, respectively. The active power was P_{ref} = 1.8 kW, and the reactive power was Q_{ref} = 0 kW. The sliding window double integration method (SWDIM) was induced to extract the grid current. The simulation comparisons are shown in Figure 5.



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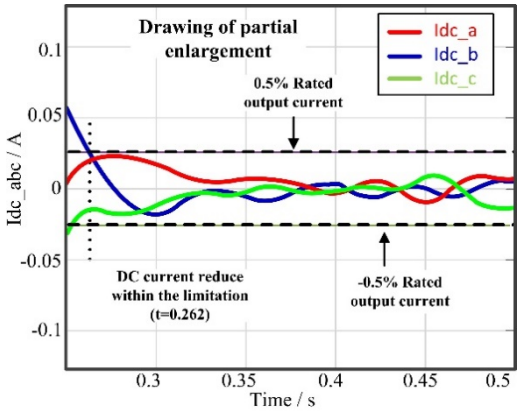

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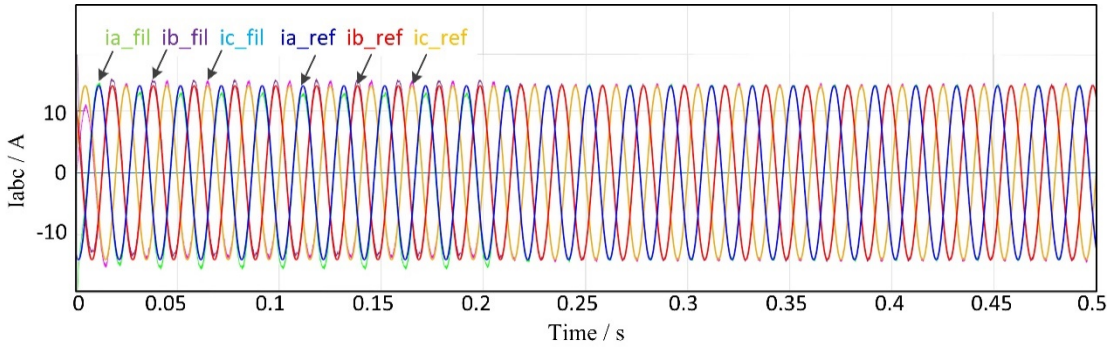
Figure 5. *Cont.*



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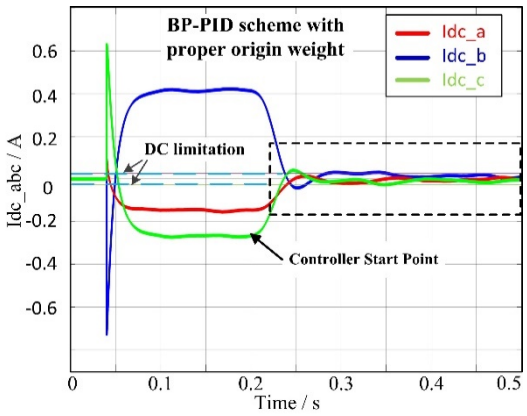

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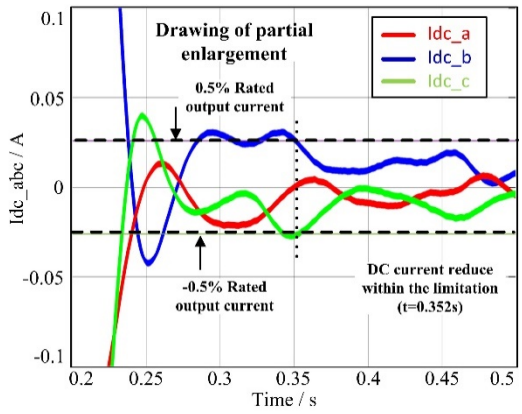

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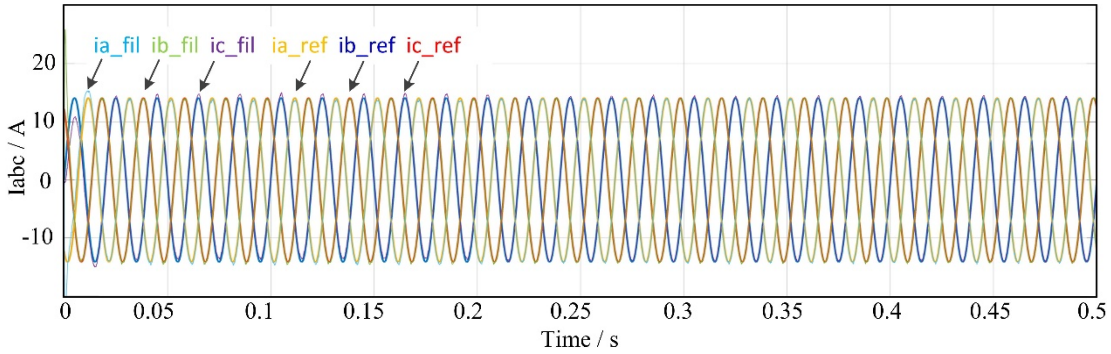
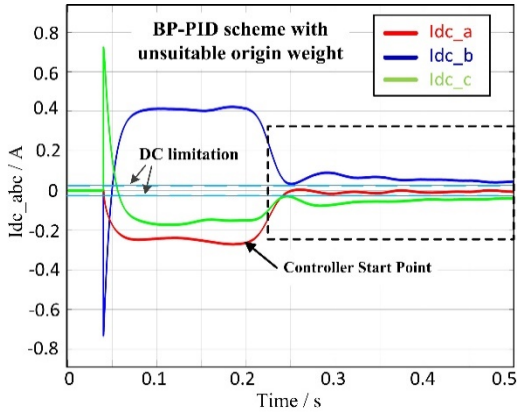


(**f**)

Figure 5. *Cont.*



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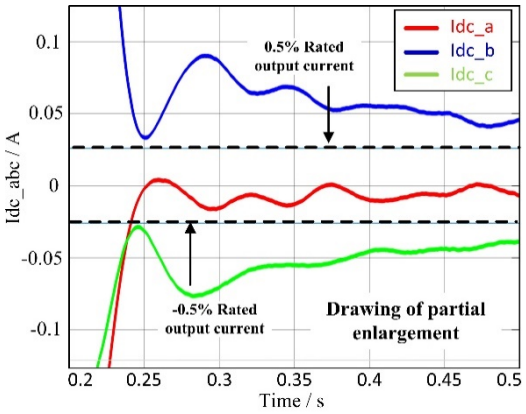
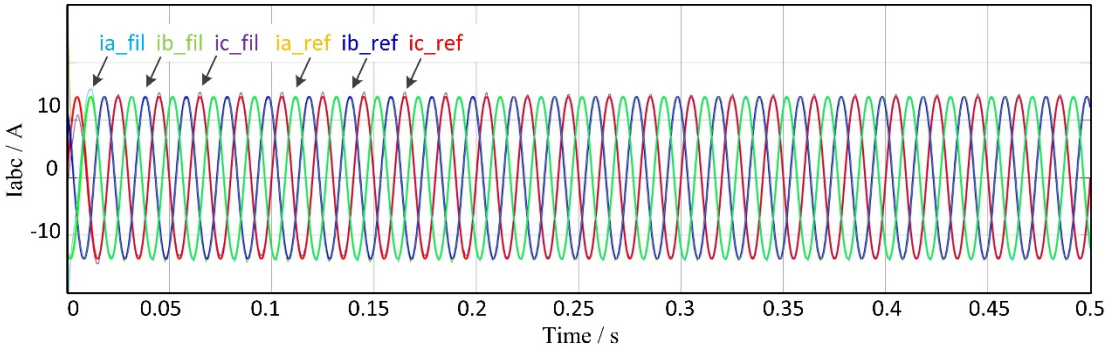


(**h**)



(**i**)

Figure 5. Comparison of the BP-PID schemes with different initial weights in the BP neural network. (**a**) The waveforms of the DC current based on the GA-BP-PID scheme. (**b**) A drawing of the partial enlargement of the dotted line in (a). (**c**) The grid current based on the GA-BP-PID scheme. Similarly, (**d**,**e**,**f**) show the waveforms of the DC current, a drawing of the partial enlargement, and the grid current based on the BP-PID scheme using the reference weight, respectively. (**g**,**h**,**i**) show the waveforms of the DC current, a drawing of the partial enlargement, and the grid current based on the BP-PID scheme using improper weights, respectively.

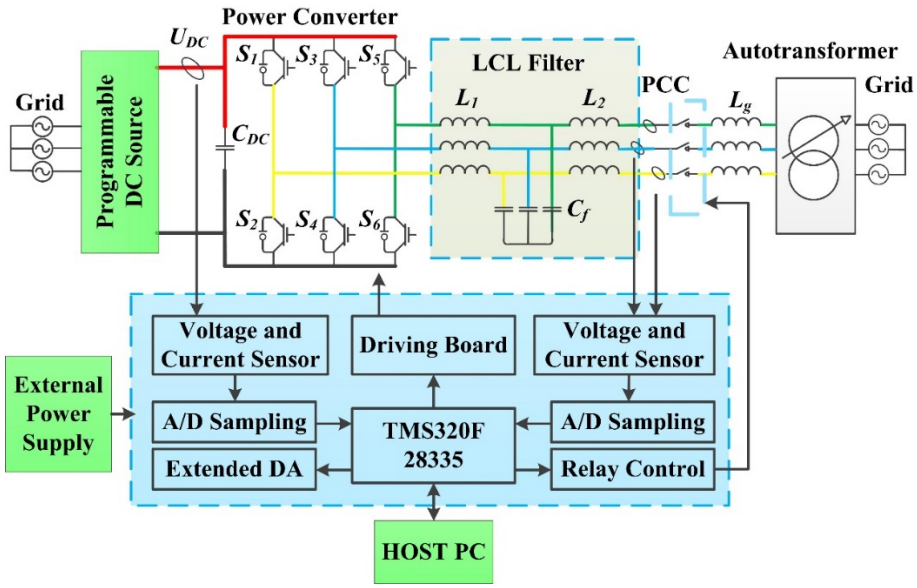
The simulation process can be divided into three stages. Firstly, before 0.04 s, SWDIM uses two periods as a time-delay. Thus, the DC current is equal to zero in this period. Secondly, between 0.04 s and 0.2 s, the DC currents of each phase can be extracted by SWDIM. The DC currents were approximated as −0.15 A, 0.4 A, and −0.25 A. Thirdly, after 0.2 s, the suppression scheme was

implemented. The proposed scheme spent 0.062 s on suppressing the DC current, where the optimal initial weights of the BP neural network were applied. This process cost 0.152 s for the BP-PID scheme, where the same initial weights of the BP network was used, as shown in the reference. Lastly, the suppression process did not finish in 0.5 s, as unsuitable initial weights were applied. GA-BP-PID reduced the suppressing time by 59%. The maximum amplitude of overshoot by the GA-BP-PID control almost vanished. However, this amplitude remains in the result of the BP-PID scheme and is beyond the DC limitations. This result demonstrates that the GA-BP-PID scheme has better performance in suppressing both consumption and overshoot.

4. Experimental Results

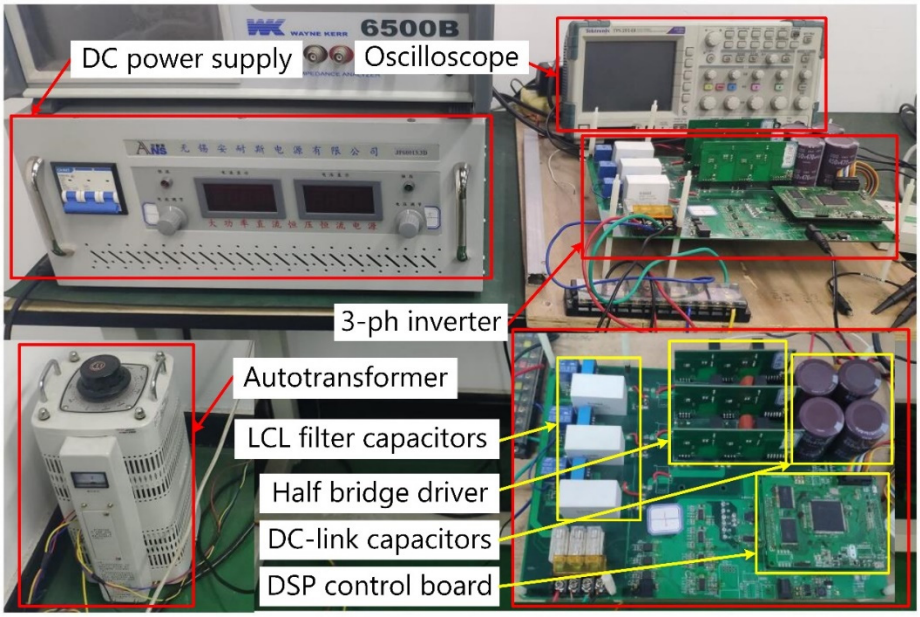
4.1. Hardware Setup

In order to verify the proposed DC current minimization scheme, a 2 kVA three-phase transformer-less grid-connected inverter was built, as shown in Figure 6. The parameters of the hardware are given in Table 4. Power transistors (IRFP460C 500 V/20 A), which can minimize on-state resistance, were applied in the system. These transistors offer stand high-energy pulses in the avalanche and commutation mode and provide excellent switching performance. The switching frequency of the inverter is 10 kHz. A 32-bit floating-point TMS320F28335 DSP was used to perform complicated mathematical calculations and fast control algorithm implementations. To increase the calculation speed, the proposed control algorithm was implemented in the RAM zone of the memory. The direct memory access (DMA) operation method of the microprocessor was introduced to the system, as well. DMA can achieve fast data transmission, and the ADC sampling time can be correspondingly reduced. The experimental results indicate that the total-time the proposed algorithm takes is about 100 µs. Between the inverter output and the grid, a small Hall current sensor was introduced to measure the dc current to the grid. A low-pass filter was employed to filter the voltage of the shunt resistor. The cut-off of the filter was 2 Hz, and the fundamental frequency can be suppressed. A four-channel oscilloscope, TDS2010B (Tektronix, Beaverton, OR, US), was implemented to measure the DC component voltage.



(**a**)

Figure 6. *Cont.*



(**b**)

Figure 6. Experimental hardware of three-phase grid-connected inverter. (**a**) Block diagram of the hardware in the experiment. (**b**) Experimental platform of the grid-connected inverter system.

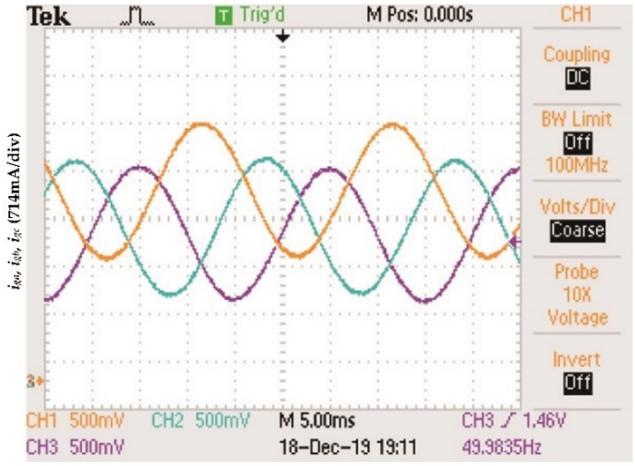
Table 4. Parameters in the experiment.

Parameter	Symbol	Values
Rated power	P_e	2 kW
Grid frequency	f_g	50 Hz
Line-to-line voltage	e_g	16 Vac
DC-link capacitance	C_{dc}	3 mF
Filter capacitance	C_f	2.2 μF
Inverter-side inductance	L_{inv}	2 mH
Grid-side inductance	L_g	1 mH
Switching frequency	f_s	10 kHz
DC-link voltage	V_{dc}	60 V_{ac}

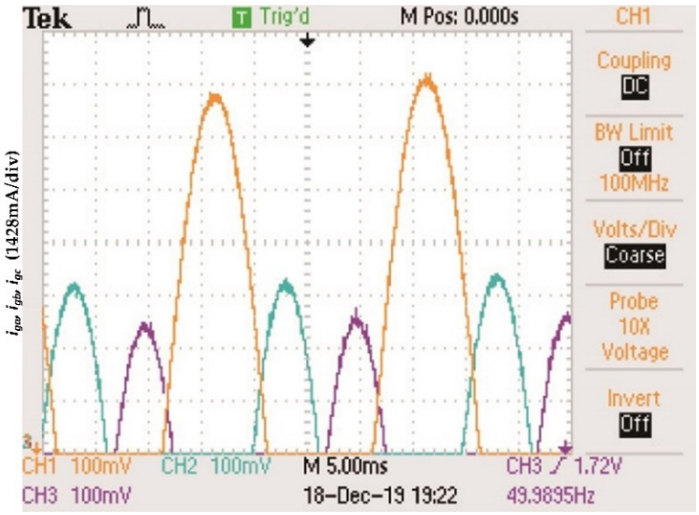
4.2. Experimental Results

To validate the effectiveness of the proposed DC current suppressing scheme, a DC current was superposed on the reference current. The grid-side inductance would also have DC current via the closed-loop control. Then, the proposed control scheme was operated to verify the performance of DC current minimization. The experimental results are shown below.

The waveform of the inverter-side current is shown in Figure 7. The grid reference current is 1 A, and the DC component biases for i_{aref}, $i_{bref,}$ and i_{cref} are superposed on the reference current as −0.15, 0.4, and −0.25A, respectively. The reference current of the d-axis in the rotating coordinates is given by i_{dref} = 1−A. The DC current can be determined from the three-phase currents. The peak values of the three-phase grid current reference are i_{ga} = 0.86 A, i_{gb} = 1.38 A, and i_{gc} = 0.76 A, respectively.



(**a**)



(**b**)

Figure 7. Waveforms of the grid current with DC current at different current references without suppression control. (**a**) i_{ref} = 1 A. (**b**) Zoom-in detail of Figure 6a.

The grid current with the DC current minimization control using the GA-BP-PID scheme is shown in Figure 8. The reference current of the d-axis is given by i_{dref} = 1 A. The peak values of the three-phase grid currents are i_{ga} = 1.003 A, i_{gb} = 0.999 A, and i_{gc} = 1.001 A, respectively. In this way, the grid current becomes more symmetrical, and the DC component is effectively minimized.

The transient response of the grid current is shown in Figure 9. Both schemes can suppress the DC current. However, the GA-BP-PID scheme spends about 0.065 s on the suppressing process, while BP-PID costs 0.16 s under the same conditions. Meanwhile, there is no obvious overshoot in the GA-BP-PID scheme. The GA-BP-PID can reduce suppressing time by about 59% compared to the BP-PID scheme. Moreover, compared with the virtual capacitor-based DC current suppression scheme for a grid-connected inverter, the BP-PID scheme spends about 0.070 s on the suppressing process [15]. Although the proposed scheme and the virtual capacitor-based method spend similar amounts of time on the suppressing process, the GA-BP-PID scheme is more direct and simpler than the virtual capacitor-based method.

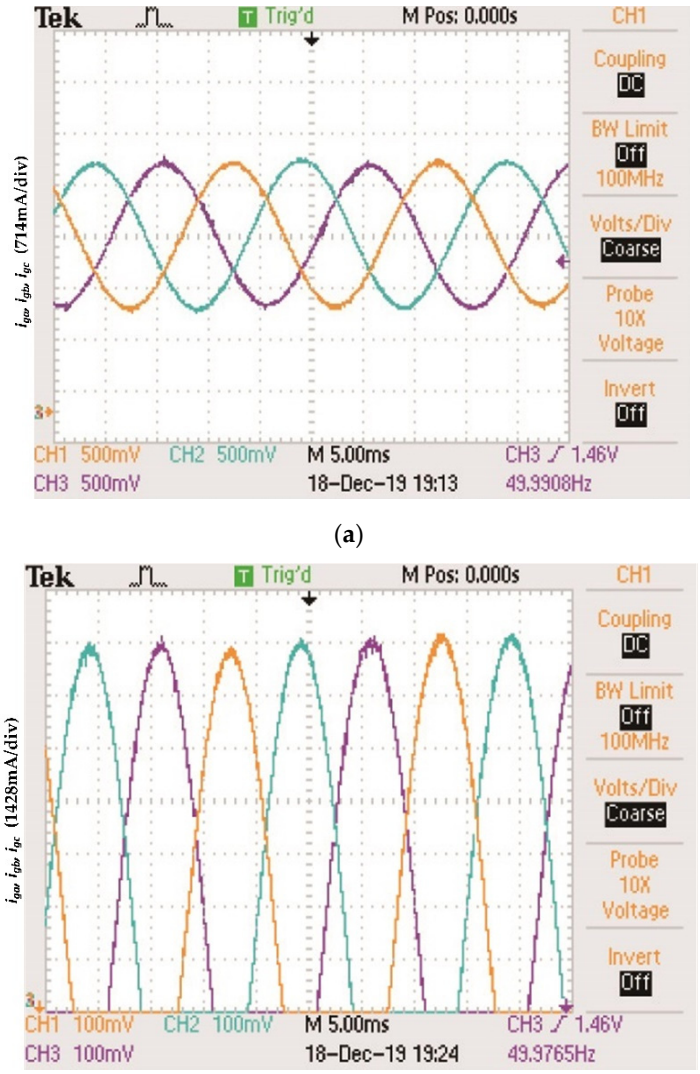


Figure 8. Waveforms of the grid current with the dc current at different current reference with the proposed scheme. (**a**) i_{dref} = 1 A. (**b**) Zoom-in detail of Figure 8a.

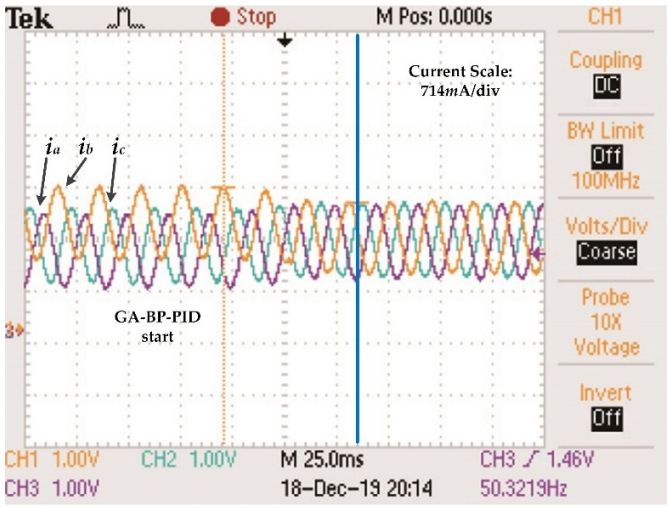
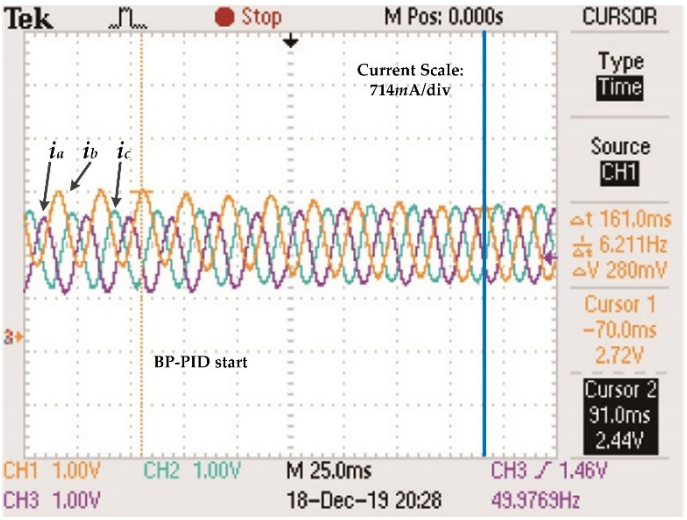


Figure 9. *Cont*.



(**b**)

Figure 9. Waveforms of the grid current. (**a**) Transient response of the grid current based on the GA-BP-PID scheme. (**b**) Transient response of the grid current based on the BP-PID scheme.

5. Conclusions

In this paper, the influence of weights within the BP-PID scheme on the suppression of DC current was analyzed. The initial weights affect subsequent weights via the iteration process. This means that the initial weights will affect the efficiency of the suppressing scheme. A proper weight within the BP neural network can reduce the suppressing time and overshoot.

Based on the analyzed results, a novel GA-based DC current minimization scheme called GA-BP-PID was established. Firstly, GA optimizes the initial weights of the BP neural network off-line. Then, the optimal weight is adopted in the on-line DC current suppression process.

A three-phase inverter system was constructed to verify the proposed scheme. Both of the simulation models and the experimental system were thus established. In the simulation program, the initial amplitude of the DC current is set as −0.15 A, 0.4 A, and −0.25 A in phases A, B, and C, respectively. The active power was P_{ref} = 1.8kW, and the reactive power was Q_{ref} = 0kW. SWDIM was induced to extract the grid current. The GA-BP-PID scheme can significantly improve the suppressing performance compared to the BP-PID scheme. Under the GA-BP-PID scheme, the suppressing time reduced from 0.152 s to 0.062 s; thus, 59% of the suppressing time can be reduced, and the overshoot can be restrained.

The experimental result also verifies the proposed scheme. The grid reference current is 1 A, and the DC component biases for i_{aref}, $i_{bref,}$ and i_{cref} are superposed on the reference current as –0.15 A, 0.4, and –0.25 A, respectively. GA-BP-PID spends about 0.065 s on the suppressing process, and its BP-PID cost about 0.16 s. Compared with the result, GA-BP-PID reduced about 59% of the suppressing time. Meanwhile, the overshoot was also restrained. These results show that the GA-BP-PID scheme can improve the performance of the BP-PID scheme.

However, in this study, the influence of the neural network's structure on the optimizing process was not discussed. Furthermore, genetic algorithms obtain optimal solutions through iterative populations. Thus, these algorithms can spend a long time on the optimizing process, making it difficult to achieve an online optimization process. Therefore, a rapid optimization method should be considered in future works.

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References

1. Carli, R.; Dotoli, M. Decentralized Control for Residential Energy Management of a Smart Users' Microgrid with Renewable Energy Exchange. *J. Autom. Sin.* **2019**, *6*, 641–656. [CrossRef]
2. Vázquez, N.; Sánchez, C.M.; Vázquez, E.; Lesso, R. A Three Port Converter for Renewable Energy Applications. In Proceedings of the 2011 IEEE International Symposium on Industrial Electronics, Gdansk, Poland, 27–30 June 2011; pp. 1735–1740.
3. Long, B.; Huang, L.; Sun, H.; Chen, Y.; Victor, F.; Chong, K.T. An intelligent dc current minimization method for transformerless grid-connected photovoltaic inverters. *ISA Trans.* **2019**, *88*, 268–279. [CrossRef] [PubMed]
4. Long, B.; Zhang, M.; Liao, Y.; Huang, L.; Chong, K.T. An Overview of DC Component Generation, Detection and Suppression for Grid-Connected Converter Systems. *IEEE Access.* **2019**, *7*, 110426–110438. [CrossRef]
5. IEEE. IEEE recommended practice for utility interface of photovoltaic (PV) systems. *IEEE Std.* **2000**. [CrossRef]
6. Buticchi, G.; Lorenzani, E.; Franceschini, G. A DC Offset Current Compensation Strategy in Transformerless Grid-Connected Power Converters. *IEEE Trans. Power Deliv.* **2011**, *26*, 2743–2751. [CrossRef]
7. Zhou, L.; Yang, B.; Guo, K.; Li, H.X.; Zhang, Z.M. The progress and development trend of the DC injection issue in PV grid-connected system. *Power Syst. Prot. Control.* **2012**, *40*, 147–155.
8. Soeiro, T.B.; Vancu, F.; Kolar, J.W. Hybrid Active Third-Harmonic Current Injection Mains Interface Concept for DC Distribution Systems. *IEEE Trans. Power Electron.* **2013**, *28*, 7–13. [CrossRef]
9. He, G.; Xu, D.; Chen, M. A Novel Control Strategy of Suppressing DC Current Injection to the Grid for Single-Phase PV Inverter. *IEEE Trans. Power Electron.* **2015**, *30*, 1266–1274. [CrossRef]
10. Berba, F.; Atkinson, D.; Armstrong, M. Matthew Armstrong. Minimisation of DC current component in transformerless Grid-connected PV inverter application. In Proceedings of the 2011 10th International Conference on Environment and Electrical Engineering, Rome, Italy, 8–11 May 2011; pp. 1–4.
11. Baocheng, W.; Xiaoqiang, G.; Herong, G.; Qiang, M.; Weiyang, W. Real-time DC injection measurement technique for transformerless PV systems. In Proceedings of the 2nd International Symposium on Power Electronics for Distributed Generation Systems, Hefei, China, 16–18 June 2010; pp. 980–983.
12. Zhang, T.; He, G.; Chen, M.; Xu, D. A novel control strategy to suppress DC current injection to the grid for three-phase PV inverter. In Proceedings of the 2014 International Power Electronics Conference (IPEC-Hiroshima 2014-ECCE ASIA), Hiroshima, Japan, 18–21 May 2014; pp. 485–492.
13. Guo, X.Q.; San, G.C.; Shen, H.; Wu, W.Y. Injection Suppression for Three-phase PV Grid-connected Inverter. *Power Electron.* **2013**, *3*, 65–66, 72.
14. Gertmar, L.; Karlsson, P.; Samuelsson, O. On DC Injection to AC Grids from Distributed Generation. In Proceedings of the 2005 European Conference on Power Electronics and Applications, Dresden, Germany, 11–14 September 2005; p. 10.
15. Chen, M.; Xu, D.; Zhang, T.; Shi, K.; He, G.; Rajashekara, K. A Novel DC Current Injection Suppression Method for Three-Phase Grid-Connected Inverter Without the Isolation Transformer. *IEEE Trans. Ind. Electron.* **2018**, *65*, 8656–8666. [CrossRef]
16. Carrasco, J.M.; Franquelo, L.G.; Bialasiewicz, J.T.; Galvan, E.; PortilloGuisado, R.C.; Prats, M.A.M.; Leon, J.I.; Moreno-Alfonso, N. Power-electronic systems for the grid integration of renewable energy sources: A survey. *IEEE Trans Ind Electron.* **2006**, *53*, 1002–1016. [CrossRef]
17. Long, B.; Wang, W.; Huang, L.; Chen, Y.; Li, F.; Sun, H.; Li, H. Design and implementation of a virtual capacitor based DC current suppression method for grid-connected inverters. *ISA Trans.* **2019**. [CrossRef] [PubMed]
18. Farag, B.; David, A.; Matthew, A. A review of minimisation of output DC current component methods in single-phase grid-connected inverters PV applications. In Proceedings of the 2012 2nd International Symposium On Environment Friendly Energies And Applications, Newcastle upon Tyne, UK, 25–27 June 2012; pp. 296–301.

19. Giraldo, J.S.; Castrillon, J.A.; Juan, C.L.; Rider, M.J.; Castro, C.A. Microgrids energy management using robust convex programming. *IEEE Trans. Smart Grid* **2018**, *10*, 4520–4530. [CrossRef]
20. Hosseini, S.M.; Carli, R.; Dotoli, M. A Residential Demand-Side Management Strategy under Nonlinear Pricing Based on Robust Model Predictive Control. In Proceedings of the 2019 IEEE International Conference on Systems, Man and Cybernetics (SMC), Bari, Italy, 6–9 October 2019; pp. 3243–3248.
21. Hosseini, S.M.; Carli, R.; Dotoli, M. Robust Day-ahead Energy Scheduling of a Smart Residential User under Uncertainty. In Proceedings of the 2019 18th European Control Conference (ECC), Naples, Italy, 25–28 June 2019; pp. 935–940.
22. Bo, L.; Huang, L.; Dai, Y.; Lu, Y.; To Chong, K. Mitigation of DC Components Using Adaptive BP-PID Control in Transformless Three-Phase Grid-Connected Inverters. *Energies* **2018**, *11*, 2047. [CrossRef]
23. Chipperfield, A.; Fleming, P.; Pohlheim, H.; Fonseca, C. A Genetic Algorithm Toolbox for Matlab. In Proceedings of the Tenth International Conference on Systems Engineering (ICSE), Coventry, UK, 6–8 September 1994; pp. 200–207.
24. Andrew, M.; Patnaik, L.M. Genetic Algorithms: A Survey. *Computer* **1994**, *27*, 17–26.
25. Sivanandam, S.N.; Deepa, S.N. *Introduction to Genetic Algorithms*; Springer: Berlin/Heidelberg, Germany, 2008; pp. 15–37.