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An Impedance Network-Based Three Level Quasi Neutral Point Clamped Inverter with High Voltage Gain

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Abstract: Due to the impediments of voltage source inverter and current source inverter, Z-Source Inverter (ZSI) has become notorious for better power quality in low and medium power applications. Several modifications are proposed for impedance source in the form of Quasi Z-Source Inverter (QZSI) and Neutral Point Clamped Z-Source Inverter (NPCZSI). However, due to the discontinuity of the source current, NPCZSI is not suitable for some applications, i.e., fuel cell, UPS, and hybrid electric vehicles. Although in later advancements, source current becomes continuous in multilevel QZSI, low voltage gain, higher shoot-through duty ratio, lesser availability of modulation index, and higher voltage stress across switches are still an obstacle in NPCZSI. In this research work, a three-level high voltage gain Neutral Point Clamped Inverter (NPCI) that gives three-level AC output in a single stage, is proposed to boost up the DC voltage at the desired level. At the same time, it detains all the merits of previous topologies of three-level NPCZSI/QZSI. Simulations have been done in the MATLAB/Simulink environment to show the effectiveness of the proposed inverter topology.

Keywords: Neutral Point Clamped Z-Source Inverter (NPCZSI); shoot-through duty ratio; modulation index; voltage gain; power quality

1. Introduction

Z-source inverter (ZSI) has the capability for buck/boost operation; this unique feature is not available in a traditional Current Source Inverter (CSI) and Voltage Source Inverter (VSI). Regardless of this unique feature, Z-source inverter has some curtailments such as lower voltage gain, discontinuous current, and high voltage stresses across the switches [1–3]. In the previous literature, several topologies in the form of Quasi Z-Source Inverter (QZSI), Neutral Point Clamped Z-Source Inverter (NPCZSI), and Neutral Point Clamped Quasi Z-Source (NPCQZSI) Inverter were presented to overcome these limitations. For instance, a voltage doubler, in conjunction with an isolation transformer, was utilized in [4] for quasi ZSI for distributed generation applications. Although the topology ensures the continuity in the input current, it offers a limited boosting ability. Theoretical results for four topologies

of QZSI inverter having less element count and simplified control techniques were presented in [5,6]. The topologies ensure a continuous current without including a major advancement in boosting ability and voltage stresses across switches. A traditional ZSI integrated with a bridge rectifier was proposed in [7] for adjustable speed drive applications. A QZSI was proposed in [8] that included two inductors, two capacitors, and one diode in the QZS network. This topology offers continuity in the input current, however, with the same boosting ability as that of the traditional ZSI. To increase the modulation index range with the continuity in current, a switched inductor QZSI was proposed in [9]. No drastic increase in the boost factor of the inverter was observed. By utilizing a predictive control method, a grid-connected closed-loop QZSI topology was introduced [10] that claimed an improvement in the inverter performance with the same boosting ability as that of traditional ZSI and high voltage stresses across switches. Similarly, different ZS networks integrated with VSI and CSI were investigated in [11]. These are indeed different topologies with the same boost factor as that of traditional ZSI. To make a smoother DC input current, a family of embedded ZSI was suggested with the traditional boosting ability and high stresses across switches [12]. In all the aforementioned references, improvement in boosting ability is still a challenge.

In [13,14], a three-level NPCZSI was proposed that deployed the two conventional impedance sources that included four capacitors and four inductors with two separate dc sources. This proposed topology of the inverter provides an additional state (0 V) in the output voltage to yield the staircase waveform and reduces the harmonic distortion in output voltage. Due to the deployment of two separate impedance sources, the design of this topology becomes very bulky; additionally, the voltage gain of the inverter does not increase too much. This limitation was addressed in [15], where a single impedance source was deputed with the NPCI to reduce the cost and volume of the inverter while retaining all the advantages of the previous topology.

To achieve the optimal results from NPCZSI in the form of enhanced output voltage, waveform quality, and boosting ability, a detailed comparison between two modulation techniques, Phase Disposition Sinusoidal Pulse Width Modulation (PDSPWM) and Phase Opposite Disposition Sinusoidal Pulse Width Modulation (PODSPWM) were analyzed in [16]. A continuous model was suggested in [17] to balance the voltage between two capacitors in NPCI. Instead of standard inductors, the use of coupled transformers was introduced in [18] to enhance the voltage gain ability of NPCZSI by adjusting the turns ratio of transformers. It also overcomes the dependence on modulation index, and hence, makes the stresses lower across switches. However, with this topology, a colossal rise in voltage gain is restricted due to the shoot-through duty ratio and turns ratio of coupled transformers affecting each other. Said constraint is addressed in [19] by modifying the impedance network with the deployment of coupled inductors. A Coupled Quasi Z-Source Inverter (CQZSI) is suggested in [20] to diminish the input current ripples. A single-phase five-level hybrid NPCI was proposed in [21], which integrated the NPCI with an H-bridge inverter. The proposed inverter contends the accomplishment to lower the total harmonic distortion (THD) through the Selective Harmonic Elimination (SHE) technique.

An NPCI, with a Z-source, that was composed of two diodes, two inductors, two switches, and two capacitors was suggested in [22] that acquired all the benefits of QZSI and provided the three-level output voltages, but due to its lower voltage gain ability, it was not an appropriate choice where a higher boost was required. In [23], two topologies named Diode Assisted QZSI and Capacitor Assisted QZSI were proposed, which were extendable, but the repetition of a greater number of units increased the size of the inverter and made it bulky. From the invention of ZSI [24], a lot of attempts have been made to ameliorate this topology to accomplish the optimal benefits from it, but a small voltage gain, lower value of modulation index, and higher voltage stress are still present in previous topologies suggested in the literature.

This research work introduces a new topology for ZSI that overcomes the drawbacks such as lower boosting ability, utilization of higher shoot-through duty ratio, lesser availability of modulation index, and higher voltage stresses across switches of the previous topologies. This topology offers a

remarkable boosting ability and provides a high voltage gain by utilizing a lower shoot-through ratio to make available a higher modulation index and keeps the lower stress across switches.

The paper is organized in the following way. The proposed inverter topology is presented in Section 2, with its complete working modes of operation. A detailed mathematical analysis is performed in Section 3. Section 4 covers the PWM technique, and the Boost Control Method applied to the proposed topology. Simulations and results are provided in Section 5, whereas Section 6 presents a detailed comparison with the previous topologies. Section 7 includes the conclusion.

2. The Proposed Inverter Topology

The schematic diagram of the proposed inverter topology, which can enhance the applied DC voltage to the desired level and transform it into a three-phase three-level output, is illustrated in Figure 1. The applied DC voltage can be procured from a DC battery or some other DC source such as a fuel cell or PV applications.

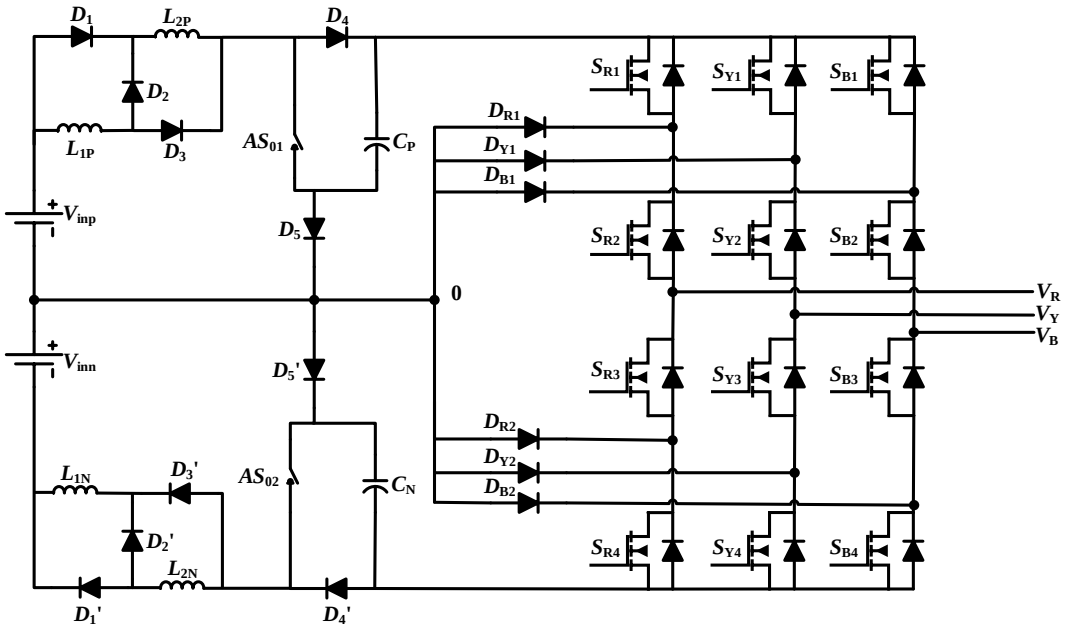


Figure 1. The proposed topology of the inverter.

The inverter is configured with two symmetrical impedance networks, where each network is comprised of two inductors, two capacitors, four diodes, and one active switch to provide the numerous advantages over the conventional inverters. Two alike dc sources are utilized to energize these networks. The conventional NPCI [25] can operate only in two types of states, active-states, and zero-states. However, the proposed inverter includes one more state of operation that is a Shoot Through (ST) state (that allows all switches to turn on at a time).

2.1. Active State

Here, the DC voltage applied to the inverter is exposed to the three-phase AC load after conversion to a three-phase three-level AC, at the desired level. In this mode of operation, $+V_{dc}$ or $-V_{dc}$ voltage appear at the poles of the inverter.

To achieve $+V_{dc}$, diodes D_2 and D_4 operate in the conduction mode and D_1 and D_3 remain in the nonconduction mode; L_{1P} and L_{2P} come in series. DC source V_{inp} and both inductors L_{1P} and L_{2P} of the upper impedance network energize the capacitor C_P. The direction of the current is shown in the equivalent circuit of the active state in Figure 2. In the active state, the current adopts the two paths, one from voltage source V_{inp} to inductor L_{1P}, diode D_2, inductor L_{2P}, diode D_4, and capacitor C_P, and completes its path through D_5. In this path, capacitor C_P is charged by voltage source V_{inp}

and by inductors L_{1P} and L_{2P}, while in the second path, the current approaches to ac load after passing through L_{1P}, D_2, L_{2P}, S_{K1}, S_{K2} (where $K = R, Y, B$) and completes its path through the load to neutral point N and back to V_{inp}.

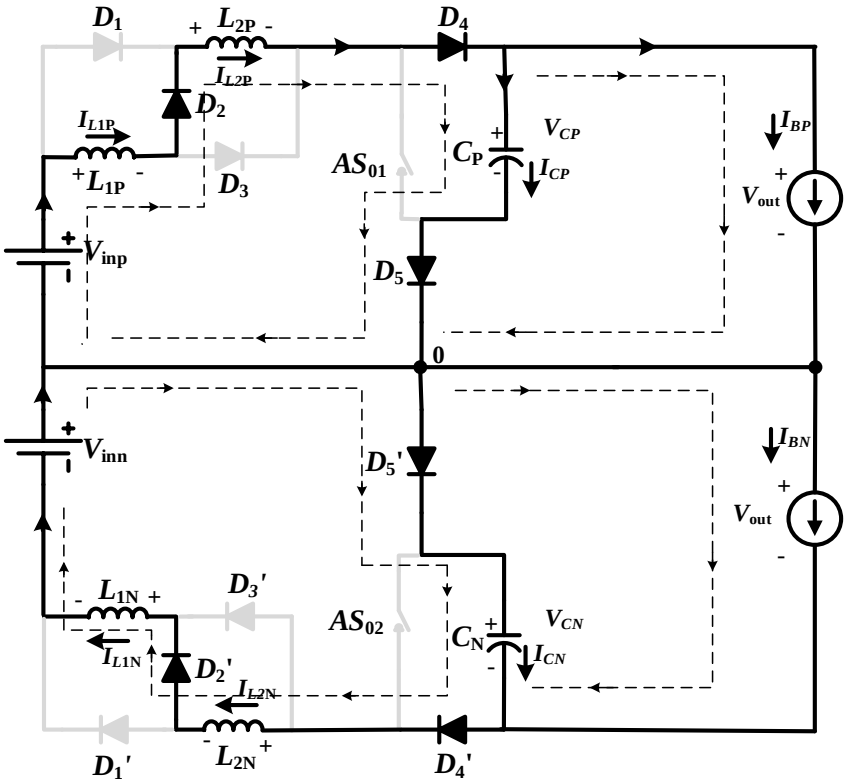


Figure 2. Equivalent circuit for the active state.

To achieve $-V_{dc}$, diodes D_2' and D_4' are in conduction mode, while D_1' and D_3' remain in nonconduction mode. DC source voltage V_{inn} and both inductors L_{1N} and L_{2N} of lower impedance network energize the capacitor C_N. The direction of the flow of current is shown in the equivalent circuit of the active state in Figure 2. In the active state, the current follows the two paths, one from voltage source V_{inn} to capacitor C_N through D_5' and completes its path after passing through inductor L_{2N}, diode D_2', and inductor L_{1N}. In this path, the capacitor is charged by voltage source V_{inn} and by inductors L_{1N} and L_{2N}. In the second path, the current approaches to AC load after passing through S_{K3} and S_{K4} (where $K = R, Y, B$), and completes its path through the inductor L_{2N}, diode D_2', inductor L_{1N}, and back to V_{inn}. In the active state, both active switches (AS_{01} and AS_{02}) remain in off state and play no role.

2.2. Zero-State

During the zero-state of operation, no voltage appears across the load terminals. In the zero-state, two intermediate switches of each leg of the inverter are in on state, whereas the topmost and lowermost switch of each leg of the inverter remains in the off state. During this mode of operation, the diodes D_2 and D_4 are in the conduction mode, while D_1 and D_3 remain in the nonconduction mode. DC source V_{inp} and both inductors L_{1P} and L_{2P} of the upper impedance network energize the capacitor C_P. Similarly, for the lower network, the diodes D_2' and D_4' are in conduction mode, while D_1' and D_3' remain in nonconduction mode and DC source V_{inn} and both inductors L_{1N} and L_{2N} of lower impedance network energize the capacitor C_N.

The direction of the flow of current in the equivalent circuit of zero-state is shown in Figure 3, where it traverses voltage source V_{inp}, inductor L_{1P}, diode D_2, inductor L_{2P}, and capacitor C_P and reaches back to V_{inp} through diode D_4. In this path, capacitor C_P is charged by V_{inp} and by both

inductors L_{1N} and L_{2N}. Similarly, for the lower network capacitor, C_N is charged by V_{inn} and by the combination of L_{1N} and L_{2N}, no power is transferred to load. Like in the active state, both AS_{01} and AS_{02} remain in off state.

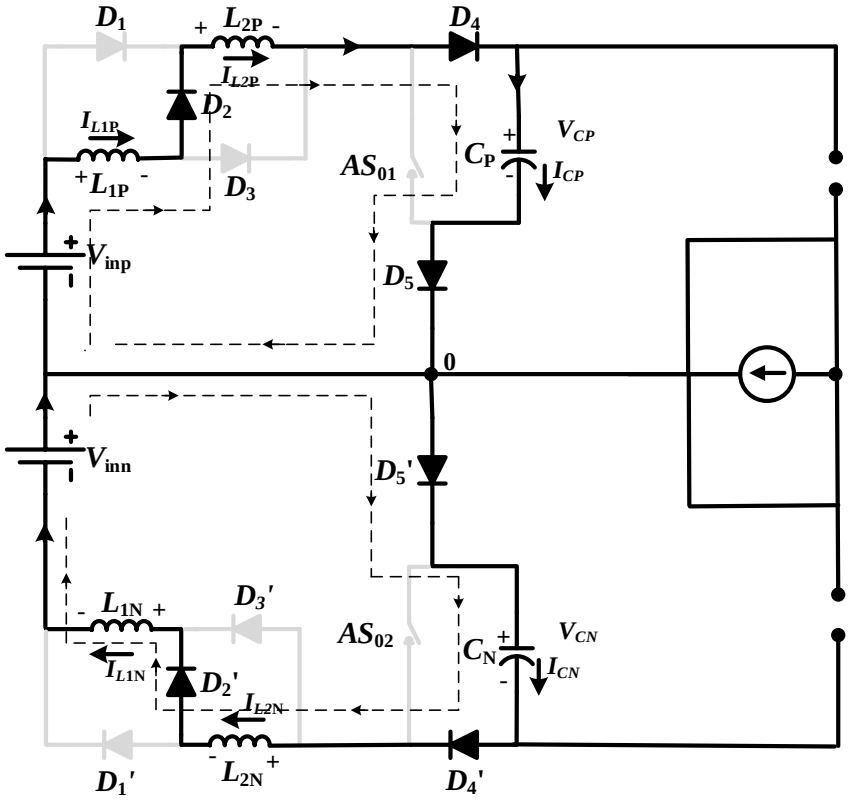


Figure 3. Equivalent circuit for the zero-state.

2.3. Shoot-Through (ST) State

In ST state, active switches, along with all switches of one or more legs of an inverter, go to on state simultaneously, which elicits 0 V across the load (see Figure 4). Seven different approaches that are summarized in Table 1 can be adopted to attain this state.

On closing the active switches, inductors L_{1P} and L_{2P} come in parallel in the upper impedance network and turns diodes D_2, D_4, and D_5 in reverse bias mode. Similarly, L_{1N} and L_{2N} come in parallel in the lower impedance network and configure diodes D_2', D_4', and D_5' in reverse bias mode. In ST state, V_{inp} and capacitor C_P charge inductors L_{1P} and L_{2P}; similarly, in the lower network, V_{inn} and capacitor C_N charge inductors L_{1N} and L_{2N}.

The span of the ST state is limited up to the premises of zero-state and is maximum when it occupies the time duration of the zero-state. This state enables the inverter to perform the buck/boost operation. Thus, by choosing its appropriate value, desired results can be achieved.

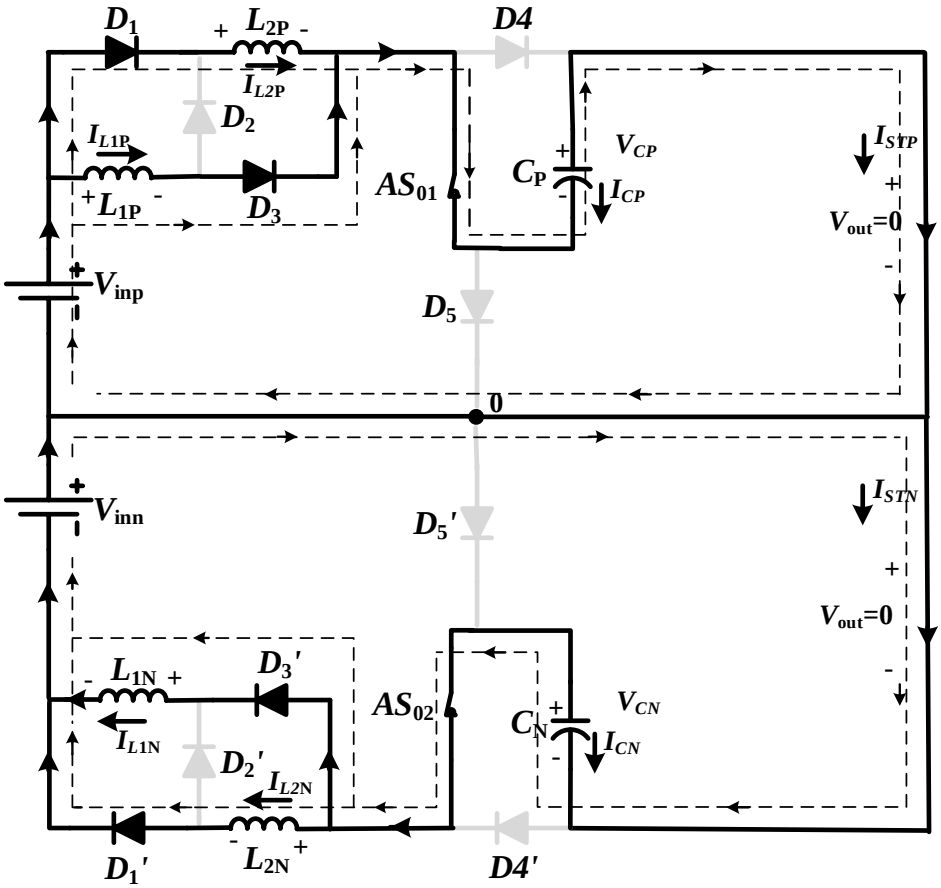


Figure 4. Equivalent circuit for the ST state.

Table 1. Different approaches for ST state.

Sr. No.	ON Switches	OFF Switches
1	S_{R1}, S_{R2}, S_{R3}, S_{R4}, AS_{01}, AS_{02}	S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}
2	S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}, AS_{01}, AS_{02}	S_{R1}, S_{R2}, S_{R3}, S_{R4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}
3	S_{B1}, S_{B2}, S_{B3}, S_{B4}, AS_{01}, AS_{02}	S_{R1}, S_{R2}, S_{R3}, S_{R4}, S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}
4	S_{R1}, S_{R2}, S_{R3}, S_{R4}, S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}, AS_{01}, AS_{02}	S_{B1}, S_{B2}, S_{B3}, S_{B4}
5	S_{R1}, S_{R2}, S_{R3}, S_{R4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}, AS_{01}, AS_{02}	S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}
6	S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}, AS_{01}, AS_{02}	S_{R1}, S_{R2}, S_{R3}, S_{R4}
7	S_{R1}, S_{R2}, S_{R3}, S_{R4}, S_{Y1}, S_{Y2}, S_{Y3}, S_{Y4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}, AS_{01}, AS_{02}	Nil

3. Mathematical Analysis of the Proposed Inverter Topology

In this section, we perform the necessary mathematical calculations for the proposed inverter topology.

3.1. Non-ST-State

Applying the Kirchhoff's Voltage Law (KVL) to Figure 2, the voltage across inductors L_{1P} and L_{2P} are:

$$\begin{cases} V_{\mathrm{L1P}} = V_{\mathrm{inp}} - V_{\mathrm{CP}} - V_{\mathrm{L2P}} \\ V_{\mathrm{L2P}} = V_{\mathrm{inp}} - V_{\mathrm{CP}} - V_{\mathrm{L1P}} \end{cases} \tag{1}$$

where:

$$V_{\mathrm{inp}} = V_{\mathrm{L1P}} + V_{\mathrm{L2P}} + V_{\mathrm{CP}} \tag{2}$$

$$V_{\mathrm{CP}} = V_{\mathrm{out}}$$

To find the inductor and capacitor currents during the non-ST state, apply the Kirchhoff's Current Law (KCL) on upper impedance network:

$$I_{L1P} = I_{L2P} = I_{CP} + I_{BP} \tag{3}$$

$$I_{CP} = I_{L1P} - I_{BP} \tag{4}$$

or:

$$I_{CP} = I_{L2P} - I_{BP} \tag{5}$$

Similarly, for the lower network during the non-ST state:

$$\begin{cases} V_{L1N} = V_{inn} - V_{CN} - V_{L2N} \\ V_{L2N} = V_{inn} - V_{CN} - V_{L1N} \end{cases} \tag{6}$$

where:

$$V_{inn} = V_{L1N} + V_{L2N} + V_{CN} \tag{7}$$

$$V_{out} = V_{CN}$$

Furthermore, the inductor and capacitor currents are:

$$I_{L1N} = I_{L2N} = I_{CN} + I_{BN} \tag{8}$$

$$I_{CN} = I_{L1N} - I_{BN} \tag{9}$$

or:

$$I_{CN} = I_{L2N} - I_{BN} \tag{10}$$

3.2. ST-State

Apply KVL to Figure 4, the voltage across the inductors L_{1P} and L_{2P} are given as:

$$V_{L1P} = V_{L2P} = V_{inp} + V_{CP} \tag{11}$$

$$V_{out} = 0$$

For inductor and capacitor currents during the ST state, apply the KCL on upper impedance network:

$$I_{STP} = I_{L1P} + I_{L2P} = -I_{CP} \tag{12}$$

or:

$$I_{CP} = -(I_{L1P} + I_{L2P}) = -I_{STP} \tag{13}$$

$$V_{L1N} = V_{L2N} = V_{inn} + V_{CN},\ V_{out} = 0 \tag{14}$$

$$I_{STN} = I_{L1N} + I_{L2N} = -I_{CN} \tag{15}$$

or:

$$I_{CN} = -(I_{L1N} + I_{L2N}) = -I_{STN} \tag{16}$$

3.3. Calculations of Current, Voltage, Boost Factor and Gain Factor

As per the Volt-Second Balance Principle (VSBP), the net voltage across the inductor remains zero during a period of one switching cycle. Apply the VSBP at upper impedance network across both inductors L_{1P} and L_{2P} during a complete switching time period T_{osc}:

$$(V_{inp} - V_{CP} - V_{L2P})(1 - D)T_{osc} + (V_{inp} + V_{CP})DT_{osc} = 0 \tag{17}$$

$$(V_{\text{inp}} - V_{\text{CP}} - V_{\text{L1P}})(1-D)T_{\text{osc}} + (V_{\text{inp}} + V_{\text{CP}})DT_{\text{osc}} = 0 \tag{18}$$

Solve (17) to find out the voltage across inductor $L_{2\text{P}}$ during the non-shoot-through state as:

$$\begin{array}{c} V_{\text{L2P}} = \frac{V_{\text{inp}} + V_{\text{CP}}(2D-1)}{(1-D)} \\ = \frac{V_{\text{inp}}}{(1-D)} + \frac{V_{\text{CP}}(2D-1)}{(1-D)} \end{array} \tag{19}$$

Put the above value V_{L2P} into (18):

$$\left(\frac{V_{\text{inp}}}{(1-D)} + \frac{V_{\text{CP}}(2D-1)}{(1-D)}\right)(1-D)T_{\text{osc}} + (V_{\text{inp}} + V_{\text{CP}})DT_{\text{osc}} = 0 \tag{20}$$

By solving (20), the voltage across capacitor C_{P} is given as:

$$V_{\text{CP}} = \frac{V_{\text{inp}}(D+1)}{1-3D} \tag{21}$$

Similarly, apply the VSBP in lower impedance network across inductors $L_{1\text{N}}$ and $L_{2\text{N}}$ during a complete switching time period T_{osc}:

$$(V_{\text{inn}} - V_{\text{CN}} - V_{\text{L2N}})(1-D)T_{\text{osc}} + (V_{\text{inn}} + V_{\text{CN}})DT_{\text{osc}} = 0 \tag{22}$$

$$(V_{\text{inn}} - V_{\text{CN}} - V_{\text{L1N}})(1-D)T_{\text{osc}} + (V_{\text{inn}} + V_{\text{CN}})DT_{\text{osc}} = 0 \tag{23}$$

After solving (22) and (23), the voltage across capacitor C_{N} is given as:

$$V_{\text{CN}} = \frac{V_{\text{inn}}(D+1)}{1-3D} \tag{24}$$

As both the dc input sources are identical $V_{\text{inp}} = V_{inn} = V_{\text{IN}}$, (21) and (24) can be re-written in a general form:

$$V_{\text{CP}} = V_{\text{CN}} = \frac{V_{\text{IN}}(D+1)}{1-3D} \tag{25}$$

As per the Ampere Second Balance Principle (ASBP), the net current through the capacitor remains zero during a period of one switching cycle. Apply the ASBP to capacitor C_{P} in the upper network to find out the current through both inductors $L_{1\text{P}}$ and $L_{2\text{P}}$:

$$(I_{\text{L1P}} - I_{\text{IBP}})(1-D)T_{\text{osc}} - (I_{\text{L1P}} + I_{\text{L2P}})DT_{\text{osc}} = 0 \tag{26}$$

$$(I_{\text{L2P}} - I_{\text{IBP}})(1-D)T_{\text{osc}} - (I_{\text{L1P}} + I_{\text{L2P}})DT_{\text{osc}} = 0 \tag{27}$$

Similarly, for the lower network, apply the ASBP to capacitor C_{N} to find out the current through both inductors $L_{1\text{N}}$ and $L_{2\text{N}}$:

$$(I_{\text{L1N}} - I_{\text{IBN}})(1-D)T_{\text{osc}} - (I_{\text{L1N}} + I_{\text{L2N}})DT_{\text{osc}} = 0 \tag{28}$$

$$(I_{\text{L2N}} - I_{\text{IBN}})(1-D)T_{\text{osc}} - (I_{\text{L1N}} + I_{\text{L2N}})DT_{\text{osc}} = 0 \tag{29}$$

Solve (26) and (27), the average current through $L_{1\text{P}}$ and $L_{2\text{P}}$ is:

$$I_{\text{L1P}} = I_{\text{L2P}} = \frac{(1-D)I_{\text{IBP}}}{(1-3D)} \tag{30}$$

Similarly, the current through inductors L_{1N} and L_{2N} is found as:

$$I_{L1N} = I_{L2N} = \frac{(1-D)I_{IBN}}{(1-3D)} \tag{31}$$

The boost factor B is given as:

$$B = \frac{V_{out}}{V_{inp}} = \frac{V_{CP}}{V_{inp}} = \frac{V_{out}}{V_{inn}} = \frac{V_{CN}}{V_{inn}} \tag{32}$$

or:

$$B = \frac{(D+1)}{1-3D} \tag{33}$$

The overall gain factor G for the proposed inverter topology is given as:

$$G = BM = \frac{(D+1)M}{1-3D} \tag{34}$$

This completes the mathematical calculations for the proposed inverter topology.

4. PWM and Boost Control Techniques

4.1. PWM Signals

The proposed topology is designed for the three-phase three-level inverter; thus, three sine waves with a phase difference of 120 degrees are utilized in the PODSPWM technique [26–30], to generate the Gating Signals (GS) for 12 switches used in the main inverter circuit. The simulation model of the proposed inverter topology is carried out with a 50 Hz frequency for each sinusoidal signal, and the frequency of each triangular signal is kept at 5 kHz. GS for switches in the main inverter circuit is shown in Figure 5.

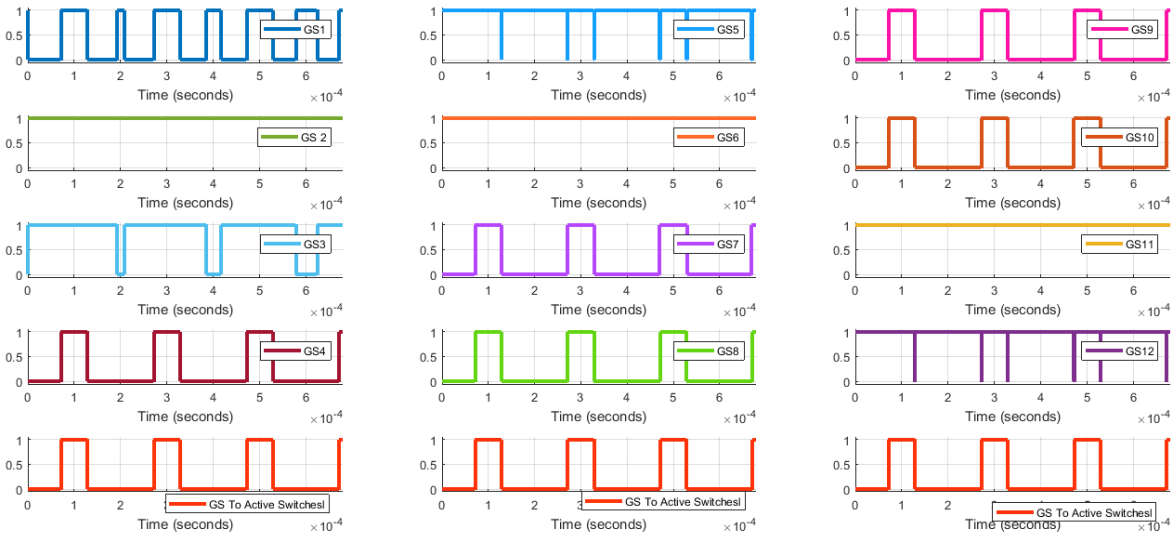


Figure 5. Gating signals for the main inverter circuit.

The GS applied to active switches in the impedance network are illustrated in Figure 6.

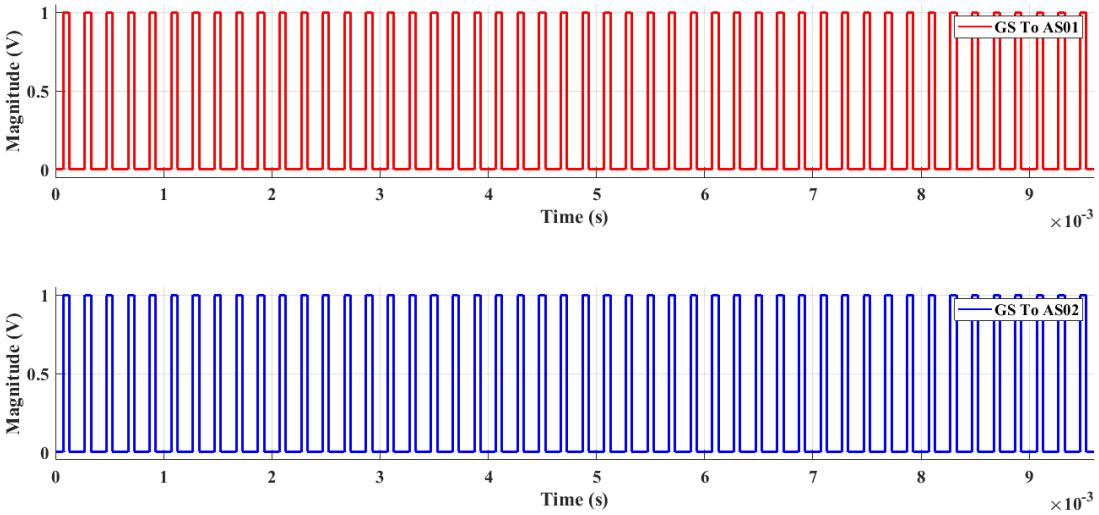


Figure 6. GS to AS_{01} and AS_{02}.

4.2. Maximum Constant Boost Control Method (MCBCM)

Although the Maximum Boost Control Method [31] provides a higher value of G with a smaller value of stress across switches V_s; however, due to diversity in the value of D for each switching cycle, it generates the low-frequency ripples in inductor current, which is not desirable [32]. To overcome this situation, and to achieve a higher value of G at lower values of V_s, MCBCM was introduced to provide a constant value of D by using two envelope signals V_{P} and V_{N}. Here, the third harmonic component with a magnitude of 1/6 of the fundamental component is dumped with the sine waves to enhance the range of M. The value of D is given as [32]:

$$D = \left(\frac{2 - \sqrt{3}M}{2}\right) = 1 - \frac{\sqrt{3}M}{2} \tag{35}$$

The value of M can be increased up to $2/\sqrt{3}$. An increase in the range of M causes a reduction in V_S [32]. Due to the numerous advantages of MCBCM over the other boost control methods, MCBCM with PODSPWM is utilized in the Simulink model. The situation is depicted in Figure 7.

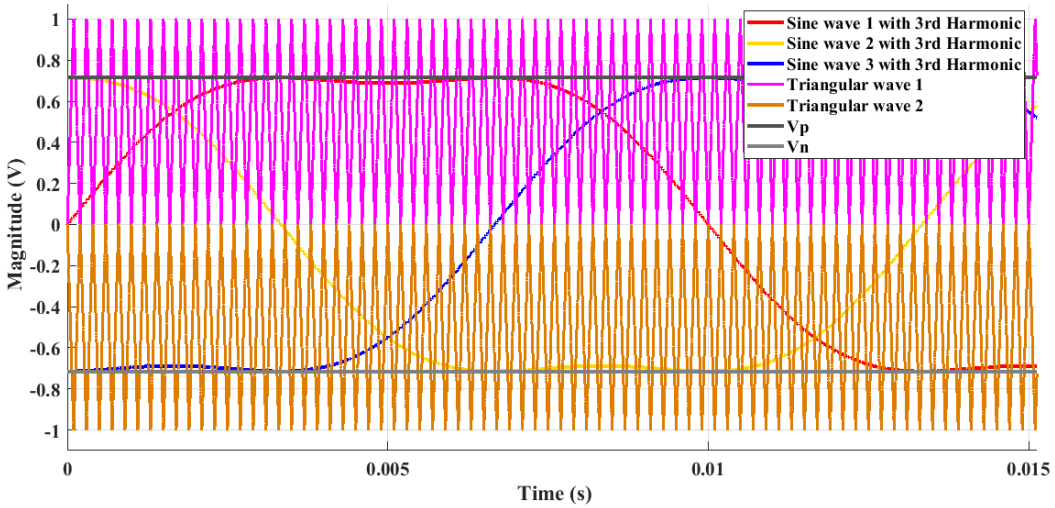


Figure 7. MCBCM with PODSPWM.

The boost factor, overall voltage gain, and stress across the switches for the proposed inverter topology are given as:

$$B = \frac{4 - \sqrt{3}M}{3\sqrt{3}M - 4} \tag{36}$$

$$G = \frac{M(4 - \sqrt{3}M)}{3\sqrt{3}M - 4} \tag{37}$$

$$V_S = BV_{IN} = \frac{(4 - \sqrt{3}M)V_{IN}}{3\sqrt{3}M - 4} \tag{38}$$

5. Simulations Results and Discussion

For solid validation of proposed topology, the inverter is simulated with a detailed switching model in discrete time simulations by using the SimPowerSystems toolbox in MATLAB/Simulink, where the conducting and switching losses are considered for the components used in the impedance network and the main inverter circuit. All the simulation results have a strong agreement with the theoretical results. The details of all components and parameters used in the simulation model for the proposed inverter topology are provided in Tables 2 and 3.

Table 2. Parameters specifications of the proposed inverter topology.

Parameters/Component	Value
Applied DC Voltage	40 V
Capacitor	1000 µF
Inductor	2 mH
Load	250 Ω
Frequency of Reference Signal(s)	50 Hz
Frequency of Carrier Signal(s)	5000 Hz
Modulation Index, M	0.825
Shoot Through Duty Ratio, D	0.2855291
Boost Factor	8.96
Overall Voltage Gain, G	7.392

Table 3. Device parameters in the proposed inverter topology.

Device	Parameter	Value
Diode	Internal Resistance	0.001 Ω
	Forward Voltage Drop	0.7 V
	Snubber Resistance	500 Ω
	Snubber Capacitance	inf
Active Switch	Internal Resistance	0.001 Ω
	Snubber Resistance	1×10^5 Ω
	Snubber Capacitance	inf
IGBT	Internal Resistance	0.01 Ω
	Snubber Resistance	1×10^5 Ω
	Snubber Capacitance	1000 F

The proposed topology outperforms the previous techniques and provides an excellent boosting capacity at a very low ST duty ratio with the high modulation index. Table 4 shows the values of the boosting factor against the different values of the ST duty ratio and modulation index.

Detailed simulation results are presented from Figures 8–13. The simulation model is designed for D = 0.2855291 and M = 0.825, and it offers a boost factor of 8.96, which is the same as the theoretical analysis (see (33)). The proposed inverter provides the 343 V pole voltages against the 40 V DC input voltage. The pole voltages are shown in Figure 8.

Table 4. Boosting ability against different values of *M* and *D*.

ST Duty Ratio (*D*)	Modulation Index (*M*)	Boost Factor (*B*)
0.11	1.0277	1.6567
0.13	1.0046	1.8525
0.15	0.9815	2.0909
0.17	0.9584	2.3878
0.19	0.9353	2.7674
0.21	0.9122	3.2703
0.23	0.8891	3.9677
0.25	0.866	5.0
0.27	0.8429	6.6842
0.2855	0.825	8.96
0.29	0.8198	9.9231
0.31	0.7967	18.7143
0.32	0.7852	33
0.33	0.7736	133

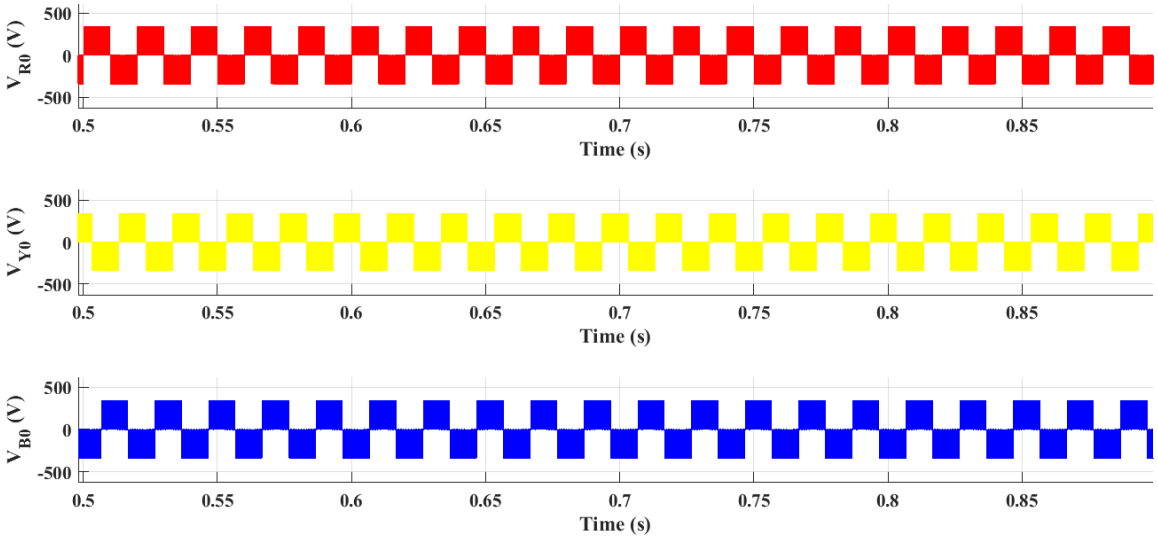


Figure 8. Pole voltage V_{RO}, V_{YO} and V_{BO}.

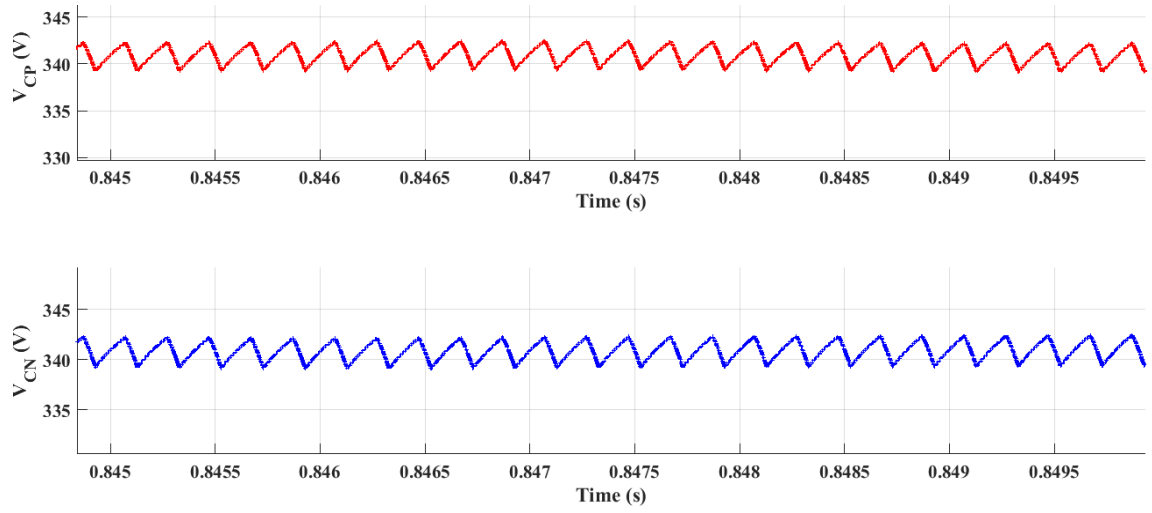


Figure 9. Voltage across capacitors V_{CP} and V_{CN}.

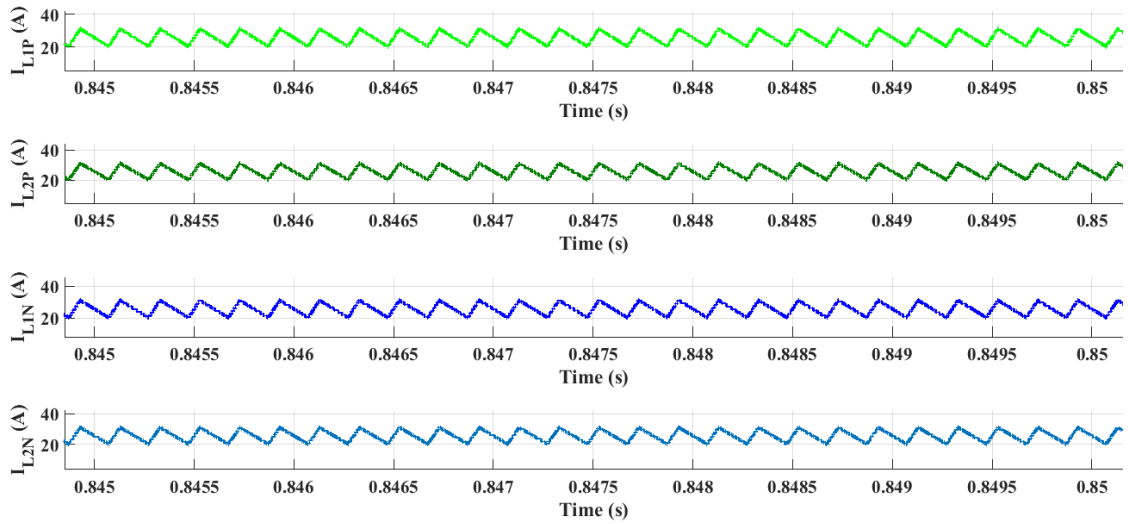


Figure 10. Inductor currents I_{L1P}, I_{L2P}, I_{L1N} and I_{L2N}.

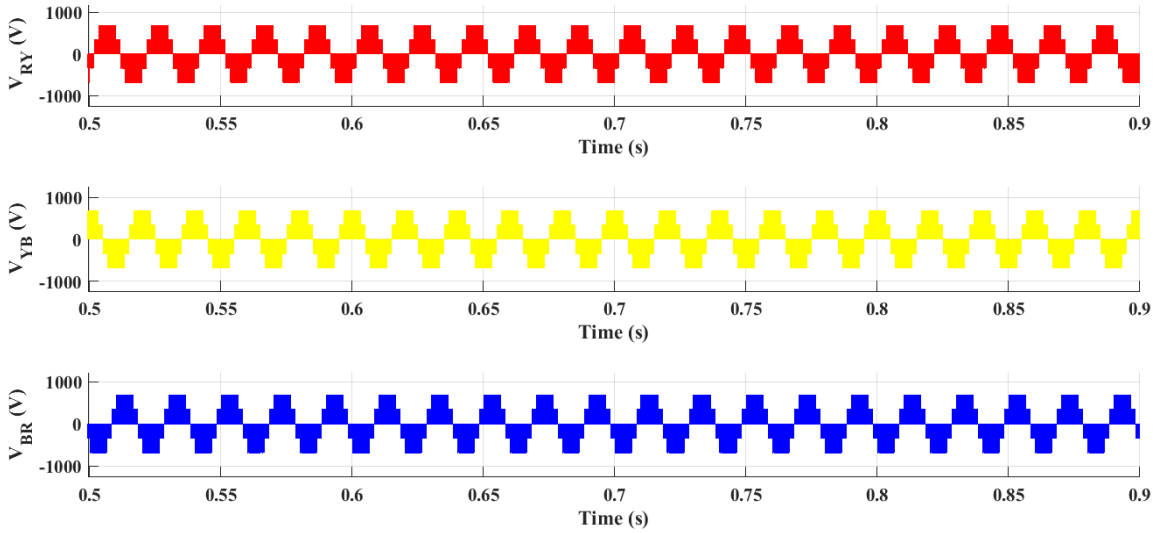


Figure 11. Line voltage V_{RY}, V_{YB}, and V_{BR}.

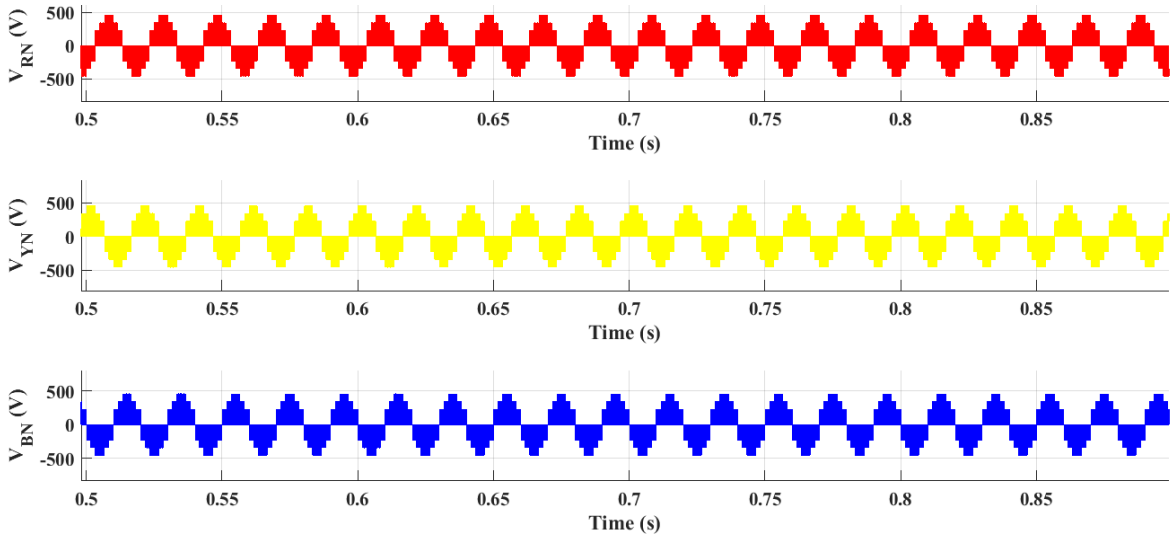


Figure 12. Phase voltage V_{RN}, V_{YN}, and V_{BN}.

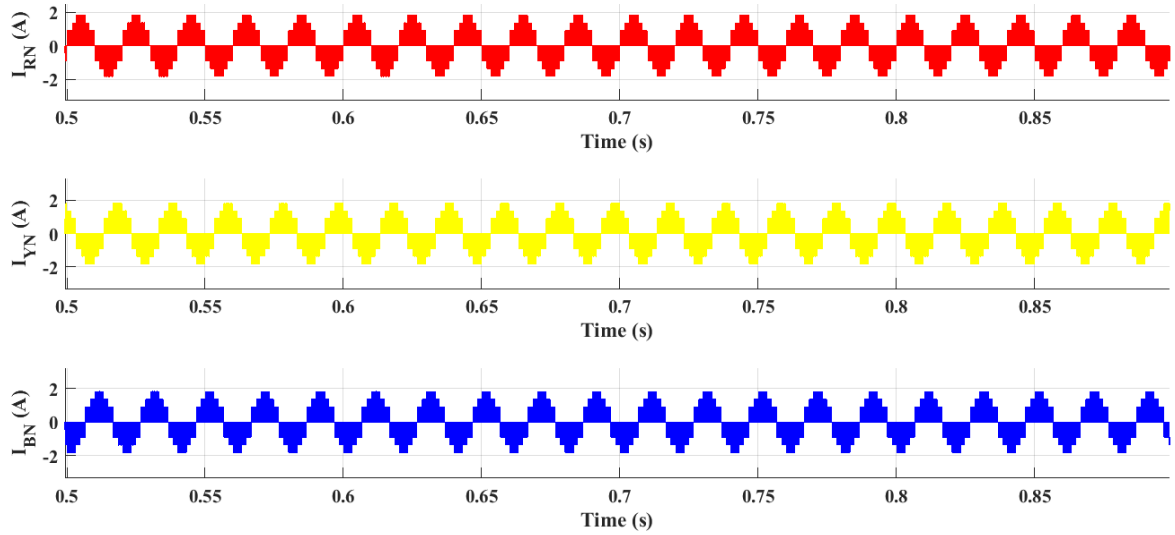


Figure 13. Load currents I_{RN}, I_{YN}, and I_{BN}.

From (21) and (24), the voltage across capacitors V_{CP} and V_{CN} are the same as the pole voltages, having values of 343 V, and the same results are depicted in Figure 9. This ensures the agreement between the mathematically-calculated and simulation results. The voltages across both capacitors are well balanced.

The waveforms for the inductor currents I_{L1P}, I_{L2P}, I_{L1N}, and I_{L2N} are shown in Figure 10.

Line voltage and phase voltage are shown in Figures 11 and 12, respectively. Line voltages are the difference of the pole voltages having a value of 687 V as depicted in the simulation results. Line voltages and phase voltages (the voltages between the phase and neutral points of star-connected load) are interrelated as:

$$\begin{cases} V_{RY} = V_{R0} - V_{Y0} \\ V_{YB} = V_{Y0} - V_{B0} \\ V_{BR} = V_{B0} - V_{R0} \end{cases} \tag{39}$$

$$\begin{cases} V_{RN} = \frac{V_{RY} - V_{YB}}{3} \\ V_{BN} = \frac{V_{BR} - V_{RY}}{3} \\ V_{YN} = \frac{V_{YB} - V_{BR}}{3} \end{cases} \tag{40}$$

A star-connected resistive load having a resistance of 250 Ω per phase is deployed at the output of the inverter. The waveforms of phase currents are shown in Figure 13, that are in-phase with the voltage, thus improving the power quality.

All the simulation results are identical to the theoretical analysis performed for the inverter.

6. Comparison with Previous Topologies

Different parameters, i.e., boosting ability, modulation index, duration of ST duty ratio, and voltage stress across switches, are considered for the comparative analysis purposes to show the effectiveness of the proposed topology. A lot of improvements in the aforementioned parameters offered by the proposed topology are found over the previous topologies.

Figure 14 compares the boost factor versus modulation index for the proposed and the previous topologies, which indicates that the boost factor of the proposed topology is much higher than that of the previous topologies for the same values of modulation index. The proposed inverter is capable of exhibiting higher boosting ability even at larger values of modulation index.

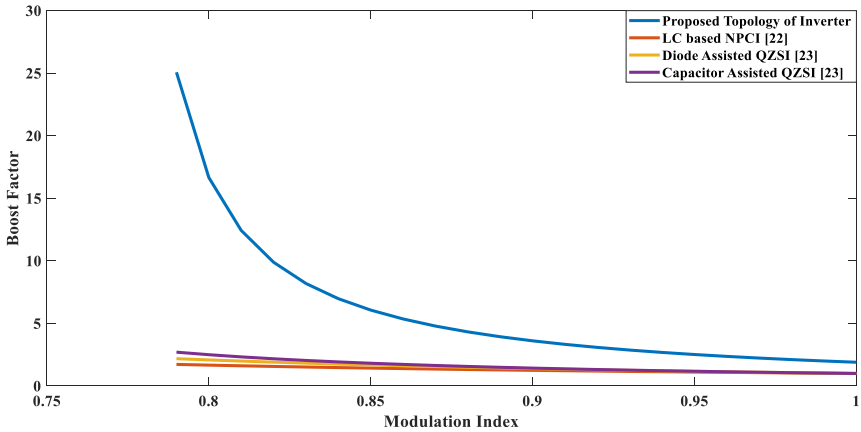


Figure 14. Boost factor versus modulation index.

In addition, the proposed topology is most appropriate to achieve a higher boost factor by utilizing a smaller value of *D* with a wide range of modulation index. Figure 15 shows a relationship of boost factor versus the ST duty ratio for the proposed and the previous topologies. It can be seen that the proposed topology offers better results, even with smaller values of the ST duty ratio. Thus, this topology can be deployed in applications where higher boost is required with a smaller ST duty ratio.

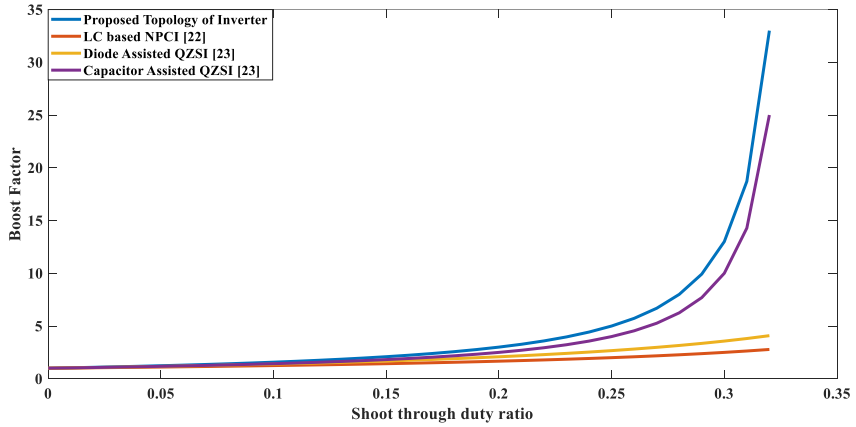


Figure 15. Boost factor versus ST duty ratio.

The proposed topology also shows a remarkable boosting ability with lower voltage stress across the switches. Figure 16 shows a graph between stress across switches and voltage gain, for the proposed topology and the previous topologies, indicating that the proposed topology offers much better results. It enables the availability of higher boost without increasing the stress much. Lowering in switching voltage stresses leads to the reduction of the rating of switches and the size of inverter.

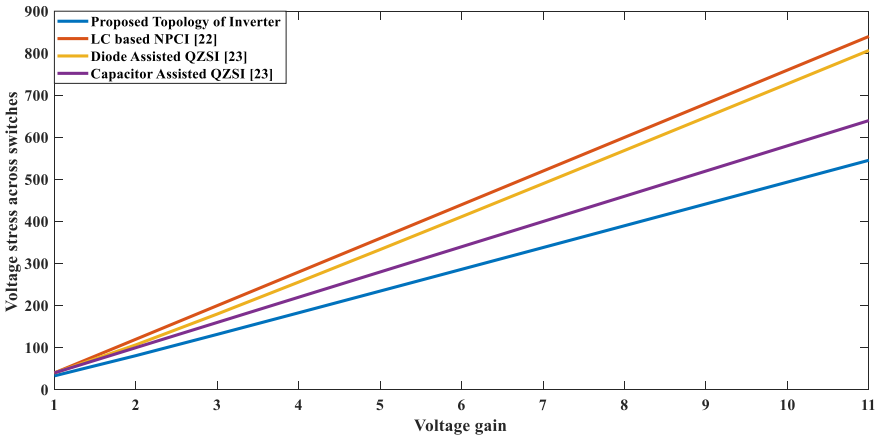


Figure 16. Voltage stress versus gain.

Figure 17 depicts the voltage gain versus the ST duty ratio, which indicates the superiority of proposed topology over the previous topologies in terms of higher voltage gain with lower values of shoot-through duty ratio.

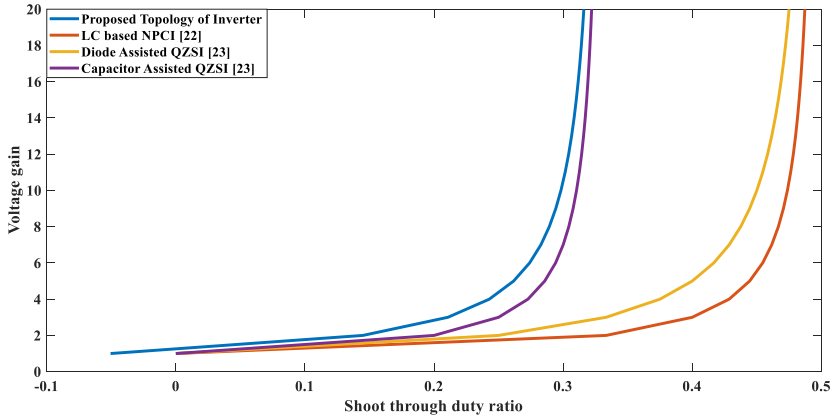


Figure 17. ST duty ratio versus gain.

Figure 18 demonstrates the relationship between boost factor and voltage gain and exhibits that the proposed topology offers the higher voltage gain against the appropriate value of boost factor due to the availability of higher modulation index, whereas, with previous topologies, significantly lower voltage gain can be achieved from the given boost factor. It can be seen from the graph that with the proposed topology, the values of voltage gain are near the corresponding values of the boost factor.

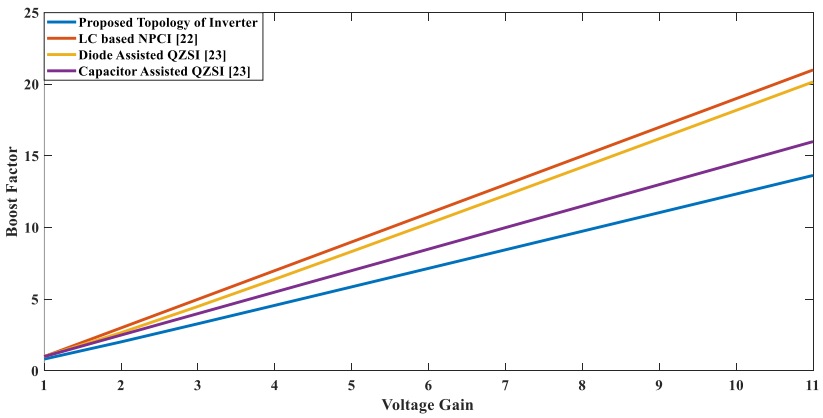


Figure 18. Gain versus boost factor.

In Figure 19, a graph is plotted between BV_{in}/GV_{in} versus the voltage gain, showing clearly that the proposed topology offers better results as compared to previous topologies.

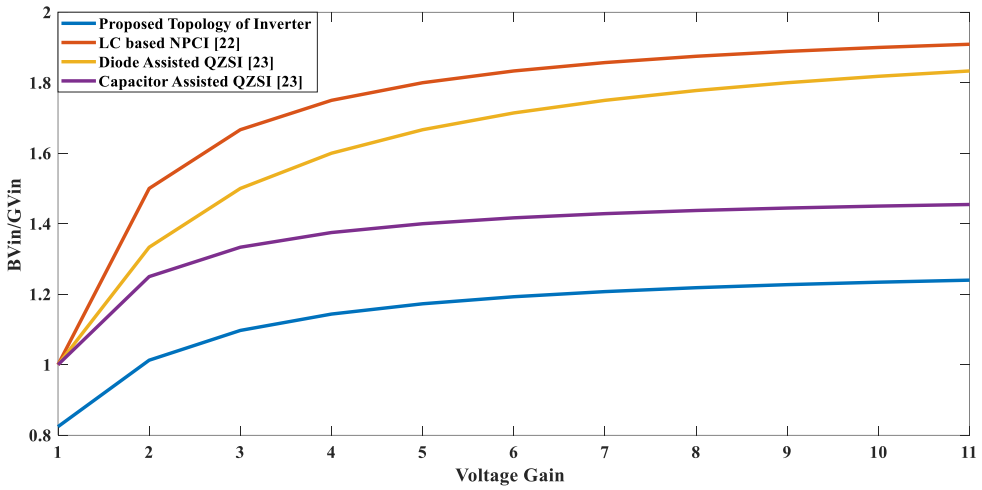


Figure 19. BV_{in}/GV_{in} versus gain.

The simulation results ensure the superiority of the proposed inverter topology over the existing ones. These simulation results can easily be translated into mathematical relations.

In a nutshell, mathematically speaking, a detailed comparison of all such parameters is shown in Table 5. On taking any combination of the input parameters, the output parameters (column 1 of Table 5) are found improved for the proposed topology over the existing ones, just like the simulation results.

Table 5. Comparison with previous topologies.

Parameter	Proposed Inverter Topology	LC-based NPCI [22]	Diode Assisted [23] QZSI	Capacitor Assisted QZSI [23]
Boost Factor	$B = \frac{1+D}{1-3D}$ $B = \frac{4-\sqrt{3}M}{3\sqrt{3}M-4}$ $B = \frac{2\sqrt{3}G}{4-3\sqrt{3}G+\sqrt{27G^2-8\sqrt{3}G+16}}$	$B = \frac{1}{1-2D}$ $B = \frac{1}{2M-1}$ $B = 2G-1$	$B = \frac{1}{1+2D^2-3D}$ $B = \frac{1}{2M^2-M}$ $B = \frac{2G^2}{1+G}$	$B = \frac{1}{1-3D}$ $B = \frac{1}{3M-2}$ $B = \frac{3G-1}{2}$
Voltage Gain	$G = \frac{M(4-\sqrt{3}M)}{3\sqrt{3}M-4}$	$G = \frac{M}{2M-1}$	$G = \frac{1}{2M-1}$	$G = \frac{M}{3M-2}$
Modulation Index	$M = \frac{4-3\sqrt{3}G+\sqrt{27G^2-8\sqrt{3}G+16}}{2\sqrt{3}}$	$M = \frac{G}{2G-1}$	$M = \frac{1+G}{2G}$	$M = \frac{2G}{3G-1}$
Shoot- Through Duty Ratio	$D = \frac{3\sqrt{3}G-\sqrt{27G^2-8\sqrt{3}G+16}}{4}$	$D = \frac{G-1}{2G-1}$	$D = \frac{G-1}{2G}$	$D = \frac{G-1}{3G-1}$
Stress Across Switches	$V_s = \frac{(4-\sqrt{3}M)V_{in}}{3\sqrt{3}M-4}$ $V_s = \left(\frac{2\sqrt{3}G}{4-3\sqrt{3}G+\sqrt{27G^2-8\sqrt{3}G+16}}\right)V_{in}$	$V_s = \frac{V_{in}}{2M-1}$ $V_s = (2G-1)V_{in}$	$V_s = \left(\frac{1}{2M^2-M}\right)V_{in}$ $V_s = \left(\frac{2G^2}{1+G}\right)V_{in}$	$V_s = \left(\frac{1}{3M-2}\right)V_{in}$ $V_s = \left(\frac{3G-1}{2}\right)V_{in}$

Efficiency analysis of the proposed inverter topology is also performed and compared with the previous topologies. Table 6 shows the values of components/parameters used for the analysis. For comparison purposes, they are assumed to be the same for all the topologies. For the simplicity of efficiency analysis, the power losses across the inductors, capacitors, diodes, and active switches (where applicable) due to parasitic resistance of inductors and capacitors, the forward voltage drop of diodes, and on-resistance of active switches are considered.

Table 6. Detail of components/parameters used in the efficiency analysis.

Component/Parameter	Symbol	Value
ESR of Capacitor	R_C	0.08 Ω
DCR of Inductor	R_L	0.07 Ω
On-Resistance of Active Switch	R_S	0.001 Ω
Load Resistance	R_l	250 Ω
Applied DC Voltage	V_{in}	40 V
Voltage Drop Across Diode	V_F	0.7 V

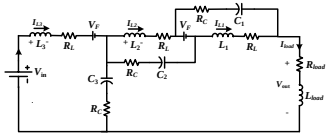
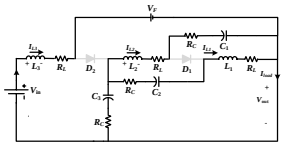
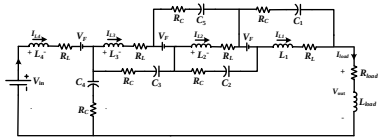
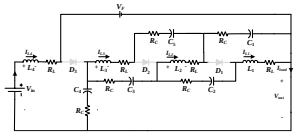
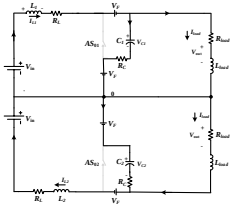
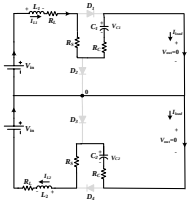
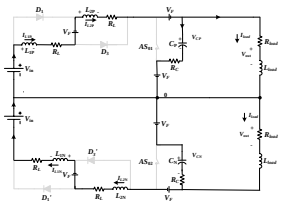
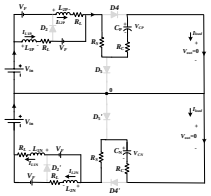
Table 7 shows the equivalent circuits during the NST and ST state of the topologies to be compared. Correspondingly, the power losses that occur across the inductors, capacitors, diodes, and active switches (where applicable) during NST and ST were calculated by utilizing the technique given in [33,34], Expressions of U series (U_1, U_2, U_3, and U_4), V series (V_1, V_2, V_3, and V_4), W series (W_1, W_2, W_3 and W_4), and Z series (Z_3, Z_4) in Table 7 show the power losses across the inductors, capacitors, diodes, and active switches during NST and ST state, respectively.

The efficiency of each topology against the overall voltage gain is computed. As can be observed from Figure 20, efficiency curves of all considered topologies are comparable with one another with a minor difference. The proposed topology offers more than 90% efficiency with a voltage gain of up to 10. With this level of efficiency, it offers several advantages in the form of higher boosting ability, lesser voltage stresses across the switches, lower shoot-through duty ratio, availability of higher modulation index, and improved quality of output waveform by reducing the THD. The reduction in voltage stresses across the switches ensures the utilization of lower rating components/devices even for a higher voltage gain, whereas in the previous topologies, the stresses across the devices drastically increase as the voltage gain increases, as depicted in Figure 16. This situation demands an enormous increase in the rating of components/devices used in previous topologies of the inverter, which leads to a tremendous increase in the cost of components/devices and the size of the inverter, which makes it bulky.

To extend our discussion further, by utilizing Table 5 and Figures 16–20, a detailed comparison of the proposed inverter topology with the previous inverter topologies in terms of overall efficiency, stresses across switches, rating of components/devices, cost, and size is performed and depicted in Figure 21, for a voltage gain of 10 (this voltage is taken as a sample, although the analysis for other values is also true).

It is clear from the comparison that the proposed topology is more feasible for the practical applications as compared to the previous topologies, especially when more voltage gain and boosting ability are required and when cost, size, and lower rating of components are the main concerns. Since the proposed topology belongs to the ZSI family, it finds its applications where all other ZSI are applicable, such as in variable speed drive systems, grid-connected photovoltaic systems, distributed generation systems, hybrid electric vehicles, laminators, conveyor belts, and so on [35–37].

Table 7. Efficiency analysis of various topologies.

Topology	NST State	ST State	Efficiency
Diode Assisted QZSI [23]	 $P_{11} = (1-D)^2(2I_{L1}^2 + I_{L3}^2)R_L + (1-D)(2I_{L1} + I_{L3} - I_{load})V_F$ $+(1-D)^2[2(I_{L1} - I_{load})^2 + (I_{L3} - I_{load})^2]R_C$	 $P_{12} =$ $D^2(2I_{L1}^2 + I_{L3}^2)R_L + D^2 6I_{L1}^2 R_C + DI_{L3}V_F$	$\eta_3 = \frac{V_{out}I_{load}}{P_{33}+P_{34}+V_{out}I_{load}} \times 100\%$ $\eta_1 = \frac{1}{U_1+V_1+W_1+1} \times 100\%$ $U_1 = \frac{R_L\left[\begin{array}{l} 2(1-D)^5 + (1-D)^3 + \\ 2D^2(1-D)^3 + D^2(1-D) \end{array}\right]}{R_i(1-2D)^2}$ $V_1 = \frac{R_C\left[\begin{array}{l} 2(1-D)^5 - 4(1-D)^4(1-2D) + \\ (1-D)^3\left\{3(1-2D)^2 + 6D^2 - 2(1-2D) + 1\right\} \end{array}\right]}{R_i(1-2D)^2}$ $W1 = \frac{V_F}{V_{in}}[2(1-D)^3 + (1-D)^2 + D(1-D)]$
Hybrid Extended Boost QZSI [23]	 $P_{22} = (1-D)^2(3I_{L1}^2 + I_{L4}^2)R_L + 3I_{L1}V_F + (1-D)^2[(I_{L1} - I_{load})^2$ $+(\frac{1-2D}{1-D}I_{L1} - I_{load})^2 + \frac{14D^2I_{L1}^2}{(1-D)^2}]R_C$	 $P_{23} =$ $D^2(3I_{L1}^2 + I_{L4}^2)R_L + 19D^2I_{L1}^2R_C + DI_{L4}V_F$	$\eta_1 = \frac{V_{out}I_{load}}{P_{22}+P_{23}+V_{out}I_{load}} \times 100\%$ $\eta_1 = \frac{1}{U_2+V_2+W_2+1} \times 100\%$ $U_2 = \frac{R_L(1-D)[1+3(1-D)^2][D^2+(1-D)^2]}{R_i(1-3D)^2}$ $V_2 = \frac{38D^2(1-D)^3R_C}{(1-3D)^2R_i}$ $W2 = \frac{V_F}{V_{in}}[(3-2D)(1-D)]$
LC-based NPCI [22]	 $P_{33} = 2(1-D^2)I_L^2R_L + 2(1-D)^2(I_L - I_{load})^2R_C$ $+2(1-D)I_LV_F + 2(1-D)(I_L - I_{load})V_F$	 $P_{34} = 2D^2I_L^2R_L + 2D^2I_L^2R_S + 2D^2I_L^2R_C$	$\eta_3 = \frac{V_{out}I_{load}}{P_{33}+P_{34}+V_{out}I_{load}} \times 100\%$ $\eta_3 = \frac{1}{U_3+V_3+W_3+X_3+1} \times 100\%$ $U_3 = \frac{R_L[2(1-D)^5+2D^2(1-D)^3]}{R_i(1-2D)^2}$ $V_3 = \frac{R_C\left[\begin{array}{l} 2(1-D)^5 + (1-D)^3\left\{2(1-2D)^2 + 2D^2\right\} \\ -4(1-D)^4(1-2D) \end{array}\right]}{R_i(1-2D)^2}$ $W_3 = \frac{V_F}{V_{in}}[4(1-D)^2 - 2(1-D)(1-2D)]$ $X_3 = \frac{R_S[2D^2(1-D)^3]}{R_i(1-2D)^2}$
Proposed Topology of Inverter	 $P_{44} = 4(1-D)^2I_L^2R_L + 2(1-D)^2(I_L - I_{load})^2R_C$ $+4(1-D)I_LV_F + 2(1-D)(I_L - I_{load})V_F$	 $P_{45} = 4D^2I_L^2(R_L + 2R_S + 2R_C) + 4DI_LV_F$	$\eta_4 = \frac{V_{out}I_{load}}{P_{44}+P_{45}+V_{out}I_{load}} \times 100\%$ $\eta_4 = \frac{1}{U_4+V_4+W_4+X_4+1} \times 100\%$ $U_4 = \frac{R_L[4(1-D)^5+4D^2(1-D)^3]}{R_i(1-3D)^2}$ $V_4 = \frac{R_C\left[\begin{array}{l} 2(1-D)^5 + (1-D)^3\left\{2(1-3D)^2 + 8D^2\right\} \\ -2(1-D)^2(1-3D) \end{array}\right]}{R_i(1-3D)^2}$ $W_4 = \frac{V_F[6(1-D)^2-2(1-D)(1-3D)+4D(1-D)]}{V_{in}(1+D)}$ $X_4 = \frac{R_S(8D^2(1-D)^3)}{R_i(1-3D)^2}$

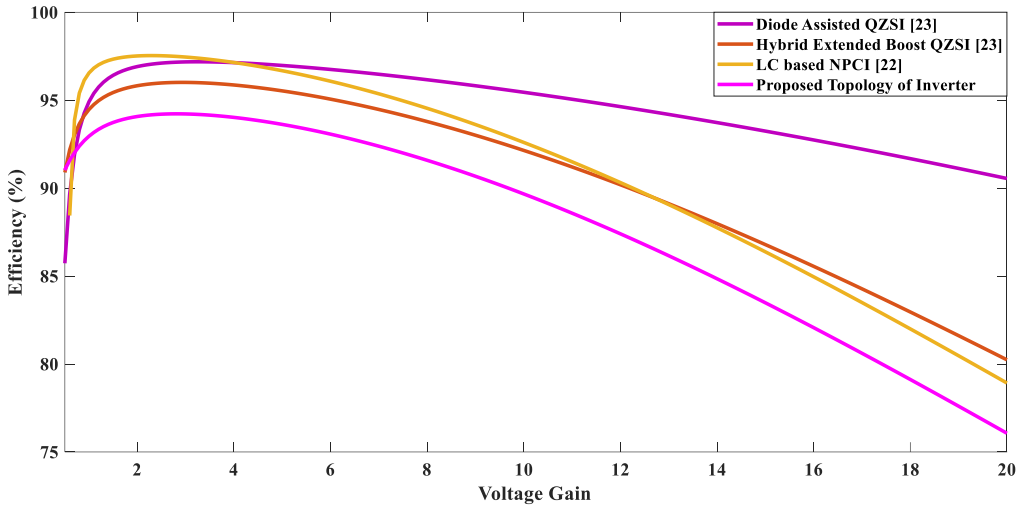


Figure 20. Efficiency versus voltage gain.

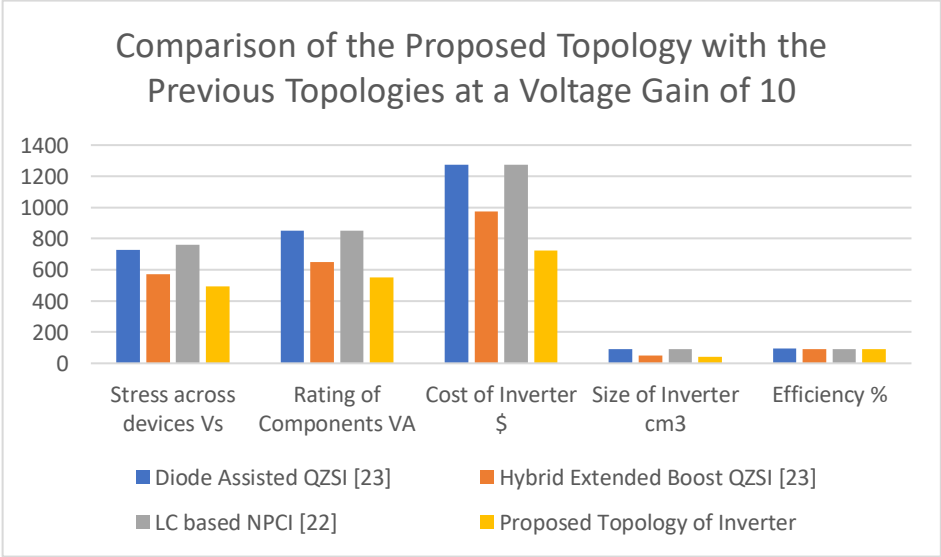


Figure 21. A detailed comparison of the proposed topology with the previous topologies.

7. Conclusions

This research work focused on the development of the three-level high voltage gain NPCI topology to boost up the DC voltage at the desired level and offers the three-level AC output in a single stage. It also detained all the merits of previous topologies of three-level NPCZSI/QZSI, such as continuity in input current and voltage balance across the capacitors. The results validated that the proposed topology ensures the remarkable boosting ability by utilizing the smaller duration of ST state and higher range of modulation index, which enables it to keep the lower stresses across the devices even at higher values of voltage gain; that is the most desirable feature for low voltage applications. The proposed topology has a slightly lower efficiency compared to other topologies; however, it reduces cost and size by utilizing the low rating components at higher voltage gain operations. This unique feature makes it more feasible for practical applications as compared to other topologies that oblige the higher rating components for their operation; this drawback associated with previous topologies not only affects the cost of the inverter but also makes the size of inverter bulky and voluminous.

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References

1. Tang, Y.; Xie, S.; Zhang, C. An improved Z-source inverter. *IEEE Trans. Power Electron.* **2010**, *26*, 3865–3868. [CrossRef]
2. Ding, X.; Qian, Z.; Yang, S.; Cui, B.; Peng, F. A high-performance Z-source inverter operating with small inductor at wide-range load. In Proceedings of the APEC 07-Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 Feburary–1 March 2007; pp. 615–620.
3. Tang, Y.; Xie, S.; Zhang, C.; Xu, Z. Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability. *IEEE Trans. Power Electron.* **2009**, *24*, 409–415. [CrossRef]
4. Vinnikov, D.; Roasto, I.; Jalakas, T. An improved high-power DC/DC Converter for distributed power generation. In Proceedings of the 2009 10th International Conference on Electrical Power Quality and Utilisation, Lodz, Poland, 15–17 September 2009; pp. 1–6.
5. Anderson, J.; Peng, F.Z. A class of quasi-Z-source inverters. In Proceedings of the 2008 IEEE Industry Applications Society Annual Meeting, Edmonton, AB, Canada, 5–9 October 2008; pp. 1–7.
6. Anderson, J.; Peng, F.Z. Four quasi-Z-source inverters. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 2743–2749.
7. Peng, F.Z.; Yuan, X.; Fang, X.; Qian, Z. Z-source inverter for adjustable speed drives. *IEEE Power Electron. Lett.* **2003**, *1*, 33–35. [CrossRef]
8. Li, Y.; Anderson, J.; Peng, F.Z.; Liu, D. Quasi-Z-source inverter for photovoltaic power generation systems. In Proceedings of the 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC, USA, 15–19 February 2009; pp. 918–924.
9. Ismeil, M.A.; Kouzou, A.; Kennel, R.; Abu-Rub, H.; Orabi, M. A new switched-inductor quasi-Z-source inverter topology. In Proceedings of the 2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad, Serbia, 4–6 September 2012; pp. DS3d.2-1–DS3d.2-6.
10. Mosa, M.; Abu-Rub, H.; Rodríguez, J. High performance predictive control applied to three phase grid connected Quasi-Z-Source Inverter. In Proceedings of the IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–13 November 2013; pp. 5812–5817.
11. Loh, P.C.; Gao, F.; Blaabjerg, F.; Goh, A.L. Buck-boost impedance networks. In Proceedings of the 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark, 2–5 September 2007; pp. 1–10.
12. Loh, P.C.; Gao, F.; Blaabjerg, F. Embedded EZ-source inverters. *IEEE Trans. Ind. Appl.* **2009**, *46*, 256–267.
13. Loh, P.C.; Gao, F.; Blaabjerg, F.; Feng, S.Y.C.; Soon, K.N.J. Pulsewidth-Modulated $ Z $-Source Neutral-Point-Clamped Inverter. *IEEE Trans. Ind. Appl.* **2007**, *43*, 1295–1308. [CrossRef]
14. Loh, P.C.; Blaabjerg, F.; Wong, C.P. Comparative evaluation of pulse-width modulation strategies for Z-source neutral-point-clamped inverter. In Proceedings of the 2006 37th IEEE Power Electronics Specialists Conference, Jeju, Korea, 18–22 June 2006; pp. 1–7.
15. Loh, P.C.; Lim, S.W.; Gao, F.; Blaabjerg, F. Three-level Z-source inverters using a single LC impedance network. *IEEE Trans. Power Electron.* **2007**, *22*, 706–711. [CrossRef]
16. Loh, P.C.; Gao, F.; Blaabjerg, F.; Lim, S.W. Operational analysis and modulation control of three-level Z-source inverters with enhanced output waveform quality. *IEEE Trans. Power Electron.* **2009**, *24*, 1767–1775. [CrossRef]
17. Maheshwari, R.; Munk-Nielsen, S.; Busquets-Monge, S. Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors. *IEEE Trans. Ind. Electron.* **2012**, *60*, 1861–1871. [CrossRef]
18. Mo, W.; Loh, P.C.; Blaabjerg, F.; Wang, P. Trans-Z-source and Γ-Z-source neutral-point-clamped inverters. *IET Power Electron.* **2014**, *8*, 371–377. [CrossRef]
19. Wang, X.; Liu, H.; Li, Y. A novel coupled inductor Z-source three-level inverter. *IEICE Electron. Express* **2017**, *14*. [CrossRef]

20. Battiston, A.; Miliani, E.-H.; Pierfederici, S.; Meibody-Tabar, F. A novel quasi-Z-source inverter topology with special coupled inductors for input current ripples cancellation. *IEEE Trans. Power Electron.* **2015**, *31*, 2409–2416. [CrossRef]
21. Yahya, A.; Waqar, T.; Husain, N.; Ali, S.M.U. Hybrid Multilevel Topology Based High Power Quality Inverter. In Proceedings of the APEC'98 Thirteenth Annual Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 15–19 February 1998.
22. Sahoo, M.; Keerthipati, S. A three-level LC-switching-based voltage boost NPC inverter. *IEEE Trans. Ind. Electron.* **2016**, *64*, 2876–2883. [CrossRef]
23. Gajanayake, C.J.; Luo, F.L.; Gooi, H.B.; So, P.L.; Siow, L.K. Extended-boost $ Z $-source inverters. *IEEE Trans. Power Electron.* **2010**, *25*, 2642–2652. [CrossRef]
24. Peng, F.Z. Z-Source Inverter. *IEEE Trans. Ind. Appl.* **2003**, *39*. [CrossRef]
25. Nabae, A.; Takahashi, I.; Akagi, H. A new neutral-point-clamped PWM inverter. *IEEE Trans. Ind. Appl.* **1981**, *5*, 518–523. [CrossRef]
26. McGrath, B.P.; Holmes, D.G. Multicarrier PWM strategies for multilevel inverters. *IEEE Trans. Ind. Electron.* **2002**, *49*, 858–867. [CrossRef]
27. Rathore, S.; Kirar, M.K.; Bhardwaj, S.K. Simulation of cascaded H-bridge multilevel inverter using PD, POD, APOD techniques. *Electr. Comput. Eng. Int. J. ECIJ* **2015**, *4*, 27–41. [CrossRef]
28. Haskar Reddy, V.N.; Babu, C.S.; Suresh, K. Advanced Modulating Techniques for Diode Clamped Multilevel Inverter Fed Induction Motor. *ARPN J. Eng. Appl. Sci.* **2011**, *6*, 90–99.
29. Colak, I.; Kabalci, E.; Bayindir, R. Review of multilevel voltage source inverter topologies and control schemes. *Energy Convers. Manag.* **2011**, *52*, 1114–1128. [CrossRef]
30. McGrath, B.P.; Holmes, D.G. A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters. In Proceedings of the 2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No. 00CH37018), Galway, Ireland, 23 June 2000; Volume 2, pp. 674–679.
31. Peng, F.Z.; Shen, M.; Qian, Z. Maximum boost control of the Z-source inverter. *IEEE Trans. Power Electron.* **2005**, *20*, 833–838. [CrossRef]
32. Shen, M.; Wang, J.; Joseph, A.; Peng, F.Z.; Tolbert, L.M.; Adams, D.J. Constant boost control of the Z-source inverter to minimize current ripple and voltage stress. *IEEE Trans. Ind. Appl.* **2006**, *42*, 770–778. [CrossRef]
33. Pan, L. LZ-source inverter. *IEEE Trans. Power Electron.* **2014**, *29*, 6534–6543. [CrossRef]
34. Zhu, X.; Zhang, B.; Qiu, D. Enhanced boost quasi-Z-source inverters with active switched-inductor boost network. *IET Power Electron.* **2018**, *11*, 1774–1787. [CrossRef]
35. Rodriguez, J.; Lai, J.-S.; Peng, F.Z. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
36. Peng, F.Z.; Joseph, A.; Wang, J.; Shen, M.; Chen, L.; Pan, Z.; Ortiz-Rivera, E.; Huang, Y. Z-source inverter for motor drives. *IEEE Trans. Power Electron.* **2005**, *20*, 857–863. [CrossRef]
37. Khlebnikov, A.S.; Kharitonov, S.A. Application of the Z-source converter for aircraft power generation systems. In Proceedings of the 2008 9th International Workshop and Tutorials on Electron Devices and Materials, Novosibirsk, Russia, 1–5 July 2008; pp. 211–215.