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Fabrication and Characterization of Cu₂ZnSnSe₄ Thin-Film Solar Cells using a Single-Stage Co-Evaporation Method: Effects of Film Growth Temperatures on Device Performances

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Abstract: Kesterite-structured Cu₂ZnSnSe₄ (CZTSe) is considered as one of the Earth-abundant and non-toxic photovoltaic materials. CZTSe films have been prepared using a single-step co-evaporation method at a relatively low temperature (i.e., below 500 °C). Due to the volatile nature of tin-selenide, the control over substrate temperature (i.e., growth temperature) is very important in terms of the deposition of high-quality CZTSe films. In this regard, the effects of growth temperatures on the CZTSe film morphology were investigated. The suitable temperature range to deposit CZTSe films with Cu-poor and Zn-rich compositions was 380–480 °C. As the temperature increased, the surface roughness of the CZTSe film decreased, which could improve p/n junction properties and associated device performances. Particularly, according to capacitance-voltage (C-V) and derived-level capacitance profiling (DLCP) measurements, the density of interfacial defects of CZTSe film grown at 480 °C showed the lowest value, of the order of $\sim 3 \times 10^{15}$ cm⁻³. Regardless of applied growth temperatures, the formation of a MoSe₂ layer was rarely observed, since the growth temperature was not high enough to have a reaction between Mo back contact layers and CZTSe absorber layers. As a result, the photovoltaic (PV) device with CZTSe film grown at 480 °C yielded the best power conversion efficiency of 6.47%. It is evident that the control over film growth temperature is a critical factor for obtaining high-quality CZTSe film prepared by one-step process.

Keywords: earth-abundant; kesterite structure; CZTSe; growth temperature

1. Introduction

Climate changes induced by increased emission of greenhouse gases have become a global issue in the past decades. Currently, solar energy is recognized as one of the most promising options to address the issue [1,2]. Various photovoltaic (PV) solar cell technologies are currently being developed in three formats: (1) crystalline silicon (c-Si)-based, (2) thin film-based, and (3) emerging material-based technologies [3,4]. Even though the global PV market share of thin-film PV modules based on CdTe, Cu(In,Ga)Se₂ (CIGS), and a-Si solar cells is currently only less than 5%, while the c-Si-based market far

Energies **2020**, *13*, 1316 2 of 10

exceeds a 90% share of the market [5], it is obvious that the market will noticeably grow according to technology and industry trends in the near future. It is worth noting here that the CIGS solar cell is the only technology that has recently increased its market share among the aforementioned thin film technologies [5,6]. If Earth-abundant materials can be successfully applied into the absorber layer, replacing In and Ga elements in a CIGS system for a stable and high-efficiency solar cell, it will be even more meaningful for fabrication cost reduction and PV deployment expansion [7]. The Cu₂ZnSn(S,Se)₄ (CZTSSe) compound family is a potential source of materials among numerous Earth-abundant element-based compounds that have been intensively explored for PV application [8–10]. Since the IBM research group opened up a novel deposition method (i.e., hydrazine-based solution process), a power conversion efficiency (PCE) record of 12.6% has been attained for a CZTSSe device [11]. However, there has been no further improvement in the device's efficiency, and so far it has been hard to scale up the device size, even if the solution process is cost effective. In terms of uniform and large-area CZTSSe film deposition, the vacuum-based processes are more suitable as a scalable method. In this respect, DGIST has reported 11.3% PCE using sputter-deposition of a precursor followed by post-annealing (denoted as a two-step process) [12]. National renewable energy laboratory (NREL) has achieved the PCE of 9.15% for a Cu₂ZnSnSe₄ (CZTSe)-based PV device using a co-evaporation method (denoted as a one-step process) [13]. Given that, among currently available processes, a one-step process is the simplest way to produce CZTSSe absorbers, it may be considered as a feasible method for commercializing CZTSSe solar cells. Nevertheless, details on the growth of co-evaporated CZTSSe films and the optimization of devices have not been studied systemically. Presumably, the difficulty in obtaining high-quality CZTSSe films could be associated with the volatile nature of Sn-Se compounds and the narrow phase stability zone of the CZTSSe material system [14–16].

In this work, the effects of growth temperature on the morphological, structural, and electrical properties of CZTSe films prepared by a single-step co-evaporation method were investigated. The desirable temperature range to deposit high-quality CZTSe films with Cu-poor and Zn-rich compositions was found. At the optimal temperature (480 °C), the surface roughness of CZTSe films was decreased, leading to a reduction in the densities of bulk and interfacial defects. According to derived-level capacitance profiling (DLCP) measurement, the estimated carrier density of the CZTSe film is in the range of $\sim 1 \times 10^{16}$ cm⁻³. As a result, the best CZTSe-based solar cell yielded the PCE of 6.47%. This suggests that the control over film growth temperature is an important factor for obtaining a high-quality CZTSe film prepared by the single-step process.

2. Experimental Details

The back electrode was prepared by depositing the molybdenum (Mo) on the 5×5 cm² soda-lime glass (SLG) with a 700 nm thickness using a direct-current magnetron spurting. A bilayer approach for the deposition of Mo on soda-lime glass (SLG) was adopted with a 280-nm-thick bottom layer at a high processing pressure for better adhesion and a 420-nm-thick top layer at a low pressure for a low resistivity.

The growth of CZTSe absorber films on Mo/SLG substrates was carried out by single-stage co-evaporation technique. CZTSe films were prepared on Mo-coated SLG substrates in a manner previously described [17]. Note that the co-evaporator was also used to deposit a pure sulfur CZTS film. CZTSe films were deposited at various growth temperatures by using four effusion cells for Cu, Zn, Sn, and Se elements. The growth temperature during film deposition was adjusted from 380 to 480 °C. A film with approximately 1 μ m thickness was produced by a 90-min deposition process. When the substrate temperature was cooled down naturally, Zn, Sn, and Se elements were additionally supplied while the shutter of the Cu source was closed. The purpose of adopting the abovementioned conditions is to suppress Se vacancies in the film as well as the decomposition of the CZTSe film at relatively high temperature [18,19]. The entire temperature profile for the CZTSe film deposition is given as shown in Figure 1.

Energies 2020, 13, 1316 3 of 10

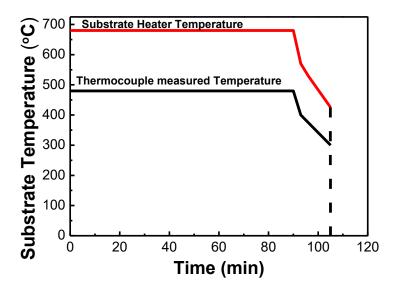


Figure 1. Growth temperature profile for Cu₂ZnSnSe₄ (CZTSe) film deposition.

The typical device structure for high-efficiency CIGS and CZTSSe PVs was employed throughout the studies [17,20]. A 60-nm-thick CdS buffer layer (n-type) was deposited on the CZTSe/Mo/SLG by using chemical bath deposition (CBD). The thickness of the CdS buffer layer was monitored via quartz crystal microbalance (QCM). For the window layer, an intrinsic zinc oxide with a 50 nm thickness and Al-doped zinc oxide with a 350 nm thickness were deposited by using a radio-frequency magnetron spurting on the CdS/CZTSe/Mo/SLG. Finally, the Al front grid was prepared by a thermal evaporator. The device area was 0.44 cm².

The structural characterizations for CZTSe films were performed using an X-ray diffractometer (Rigaku D/Max-2500, Japan) and Raman spectroscopy (N8 NEOS SENTERRA, USA). To verify the film microstructure, scanning electron microscope (SEM) images were taken using a Hitachi S-4700 filed-emission SEM, Japan. Energy-dispersive X-ray spectroscopy (EDS) connected to SEM equipment was used at an accelerating voltage of 20 KeV to estimate the chemical composition of CZTSe films. Current-voltage measurements were carried out using a McScience K201-LAB 50, South Korea under AM 1.5G illumination with an intensity of 100 mW/cm². The spectral responses were measured using a McScience K3100, South Korea. A calibrated Si solar cell was used as a reference for the device measurement. To estimate the carrier density of CZTSe film, both capacitance-voltage (C-V) and derived-level capacitance profiling (DLCP) were performed using a precision LCR meter (Agilent 4284A, USA) at 300 K.

3. Results and Discussion

The CZTSe films were grown at various temperatures ranging from 350 to 530 °C to determine a suitable growth temperature range for high-quality CZTSe films. As seen in Figure 2a,b, when the growth temperature was set to 530 °C, a continuous film was not formed. The CZTSe films grown below 480 °C showed compact and continuous morphologies, even if few voids were formed. Actually, there was no significant change in the grain sizes. However, as seen in Figure 2i,j, when the growth temperature was less than 350 °C, the ratio of (Zn)/(Sn) concentrations was more than 2 and that of (Cu)/((Zn)+(Sn)) was lower than 0.6, which are values outside of the optimal composition ranges (e.g., for the CZTSSe-based record device, $(Cu)/((Zn)+(Sn))\sim0.8$ and $(Zn)/(Sn)\sim1.1$ [11]. Given that high-quality films possess compact and large-grained morphologies with suitable Cu-poor and Zn-rich compositions, the required growth temperatures to enable device-quality CZTSe films prepared by one-step method seem to be in the temperature range of 380~480 °C, as depicted in Figure 2c,h. The poor film coverage with island grains and unfavorable chemical composition could be associated with the high volatility of Sn-Se compounds during CZTSe film deposition [21,22]. Moreover, it was

Energies 2020, 13, 1316 4 of 10

observed that as the growth temperature was increased from 380 to 480 $^{\circ}$ C, the surface roughness of the CZTSe films was reduced. The smoother surface could lead to an improvement in p/n junction properties and associated device performance.

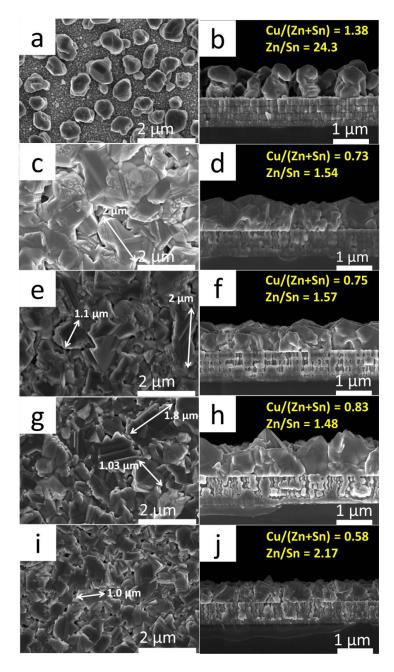


Figure 2. SEM surface and cross-sectional images of $Cu_2(Zn,Sn)Se_4$ films prepared at various growth temperatures: (**a**,**b**) 550 °C, (**c**,**d**) 480 °C, (**e**,**f**) 440 °C, (**g**,**h**) 380 °C, and (**i**,**j**) 330 °C.

To investigate the formation of secondary phases and the single-phase nature of CZTSe films, X-ray diffraction patterns of CZTSe films grown at various growth temperatures were measured, as shown in Figure 3. Regardless of various applied growth temperatures, all XRD peaks were assigned to the phase of CZTSe material (JCPDS No. 52-0868) and the films were observed to have (112)-preferred-orientation. This indicates that no secondary phases in the CZTSe films were observed. Nevertheless, the presence of secondary phases, such as ZnSe and Cu₂SnSe₃, in the films cannot be ruled out [23–26]. As seen in Figure 3b, the (112) peak was shifted toward a higher XRD diffraction

Energies **2020**, *13*, 1316 5 of 10

angle when the film was deposited at the higher growth temperature. Such a peak shift seems to be related to the incorporation of sulfur residue from the co-evaporation chamber, since the co-evaporator was used to deposit pure CZTS sulfide and the vaporizing temperature of sulfur is very low.

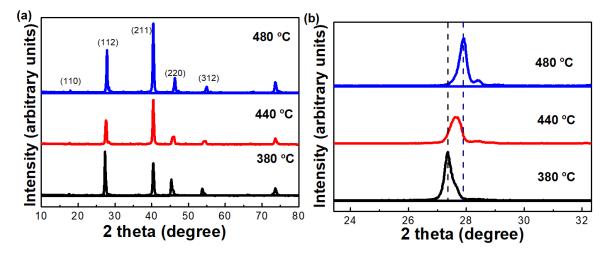


Figure 3. (a) XRD patterns of CZTSe films prepared at various temperatures ranging from 380 to 480 °C and (b) magnified view of the XRD (112) peak of CZTSe films.

To identify the formation of the secondary phases and impacts of various growth temperatures on CZTSe film, Raman scattering measurement was performed at room temperature with a 532 nm laser excitation. In literature, the A1 mode Raman peak of CZTSe and CZTS is located at $194-197 \, \mathrm{cm}^{-1}$ and $322-327 \, \mathrm{cm}^{-1}$, respectively [27–32]. Thus, as seen in Figure 4, the primary main peak of the films is assigned to the A1 peak for CZTSe and the second main peak seems to be assigned to the A1 peak for CZTS. Furthermore, the A1 peak for CZTSe films is shifted as a function of growth temperature and the intensity of peak at \sim 324 cm⁻¹ is increased without a peak shift. This observation is consistent with the XRD result, as seen in Figure 3b. In general, high growth temperature could induce a small amount of sulfur incorporation if a small amount of sulfur exists in the chamber. Actually, the incorporation of sulfur can influence the bandgap of CZTSe films and voltage output of PV devices.

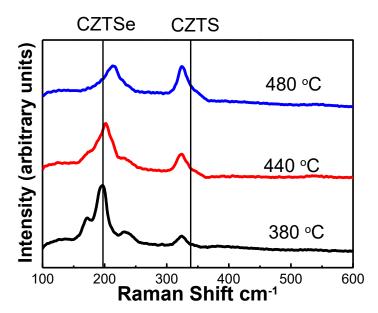


Figure 4. Raman spectra of the CZTSe films prepared at various growth temperatures ranging from 380 to 480 °C.

Energies **2020**, *13*, 1316 6 of 10

To evaluate the PV device performance with CZTSe films grown at various temperatures, the CZTSe film is incorporated as an absorber in the conventional structure for CIGS solar cells, for instance, ITO/i-ZnO window/CdS buffer/absorber/Mo back contact. The current density-voltage (J-V) characteristics of PV devices with a CZTSe film grown at various growth temperatures are shown in Figure 5a. In addition, the photovoltaic parameters measured from the J-V curves are listed in Table 1. Basically, all PV parameters and device efficiencies improved gradually with an increase in the growth temperature for CZTSe film. The device efficiency prepared at the higher growth temperature of 480 °C increased from 1.36% to 6.08% because of the improvement in both shunt resistance and saturated recombination current density (J_0), resulting in reduced $V_{\rm OC}$ deficit (Table 1). Such improvements seem to be associated with the formation of a sturdy p/n junction by the reduction in the film surface roughness, as seen in Figure 2. In addition, the incorporated sulfur can affect device performance, since the cutoff of EQE spectra in the long-wavelength (Figure 5b) is decreased as a function of growth temperature. However, the current best cell is still lower than the highest value of 9.15% for a CZTSe film prepared by one-step method [13].

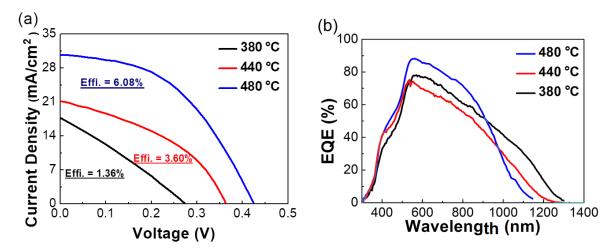


Figure 5. (a) Illuminated J-V curves and (b) EQE spectra for CZTSe films prepared at various growth temperatures ranging from 380 to 480 °C.

Table 1. Summary of photovoltaic parameters of photovoltaic (PV) devices based on the CZTSe films prepared at various growth temperatures. The Voc deficit of $\frac{Eg}{q}$ –Voc was calculated with an estimated bandgap (Eg) from the EQE spectra fitting, as seen in Figure S1. The estimated bandgap (Eg) increased from 1.14 to 1.23 eV as the growth temperature of CZTSe film increased from 380 to 480 °C.

Sample	Effi. (%)	V _{OC} (V)	Jsc (mA/cm ²)	Fill Factor FF (%)	R_{Sh} (Ω)	$\mathbf{R_S}$ (Ω)	A	J ₀ (mA/cm ²)	Voc deficit (mV)
480 °C	6.08	0.425	30.77	46.48	4166.7	2.02	3.11	1.8×10^{-4}	805
440 °C	3.60	0.363	22.84	43.47	109.9	1.98	1.34	3.9×10^{-3}	827
380 °C	1.36	0.274	17.71	28.15	45.23	2.11	3.77	1.4×10^{-3}	873

To understand defect properties of CZTSe PV devices, CV and DLCP measurements were performed. By fitting the CV and DLCP data (Figure S2a,c), various information such as free carriers, interface, and bulk defect densities were estimated and summarized, as seen in Table 2. They indicate that the density of interfacial defect was decreased, showing less than <10¹⁶ cm³ as the growth temperature increased, while the density of bulk defects for all PV devices remained at a similar level.

Energies **2020**, 13, 1316 7 of 10

Additionally, the depletion width of the CZTSe film grown at $480\,^{\circ}$ C was relatively larger than one of films grown at the lower temperatures. Consequently, this means that interface recombination was more dominant compared to bulk recombination and may be related to surface roughness.

Table 2. Summary of the results derived from the CV and DLCP measurement of CZTSe PV devices.
$(N_A: Free carrier density, N_{IF}: Interface defect density, N_B: Bulk defect density).$

Sample	N _A (cm ³)	N _{IF} (cm ³)	N _B (cm ³)	Depletion Width (nm)
480 °C	1.0×10^{16}	3.0×10^{15}	1.6×10^{16}	119
440 °C	9.2×10^{16}	2.2×10^{16}	3.7×10^{16}	64.7
380 °C	5.6×10^{16}	1.5×10^{17}	1.3×10^{16}	70.5

Figure 6 shows that when MgF₂ anti-reflection coating with a 100 nm thickness was applied, the device efficiency was slightly increased from 6.04% to 6.47% due to an increase in the spectral response at long wavelength, as shown in Figure 6b. Further studies may be needed to gain deeper insights into defect passivation by post-deposition treatment of alkali elements (e.g., Na, K, Rb, and Cs) [33–35]. Additionally, in order to increase the spectral response at the short wavelength region, a Zn(O,S) buffer layer can be considered as a wide bandgap and Cd-free material [36–38].

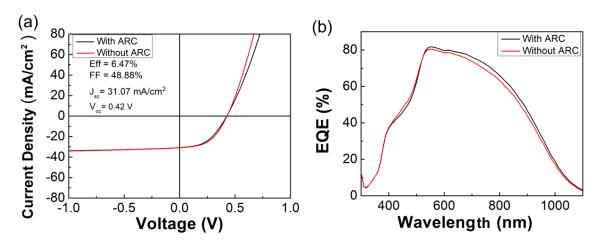


Figure 6. (a) Illuminated J-V curves and (b) EQE spectra for CZTSe films grown at 480 °C with and without anti-reflection coating (ARC).

4. Conclusions

Earth-abundant $Cu_2ZnSnSe_4$ films were deposited on Mo-coated SLG substrates by using a single-stage co-evaporation method. The films were grown at various growth temperatures to determine a suitable growth temperature range for high-quality CZTSe films. When the films were grown at 380~480 °C, XRD and Raman data indicate that all films adopted a kesterite structure with *I-4* space group without observation of secondary phase formation. Most of all, the surface roughness of the CZTSe film grown at the higher temperature of 480 °C was significantly decreased. As a result, the PV device efficiency was increased up to 6.47%, since both shunt resistance and saturated recombination current density were improved, leading to a reduction in the Voc deficit. According to C-V and DLCP measurements, the increase in the open circuit voltage of the device is consistent with a reduction in the density of interfacial defects. Overall, our results suggest that control over film growth temperature is a critical factor for obtaining high-quality CZTSe film prepared by one-step process. Moreover, alkali post-deposition treatment may enable improved device efficiency through defect passivation. By using a wider bandgap buffer layer (e.g., Zn(O,S)), spectral responses in the short

Energies **2020**, 13, 1316 8 of 10

wavelength region could be enhanced. Overall, such technologies may offer a pathway to higher device efficiency.

Supplementary Materials: Supplementary materials to this article can be found online at: http://www.mdpi.com/1996-1073/13/6/1316/s1.

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Conflicts of Interest: The authors declare no conflict of interest.

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Energies **2020**, 13, 1316

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