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Control Design and Experimental Validation of a HB-NPC as a Shunt Active Power Filter

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Abstract: This work presents the design of a control law based on the average model of a shunt active power filter considering an H-bridge neutral point clamped topology and its experimental validation. Therefore, the proposed controller is formed by three control loops, namely current (inner), regulation (outer), and balance control loops. The current loop aims to compensate both the displacement power factor and the harmonic distortion produced by nonlinear loads connected to the point of common coupling. To deal with harmonic current distortion, the current loop involves an adaptive mechanism based on a bank of resonant filters tuned at odd harmonics of the fundamental grid frequency. The regulation and balance loops are aimed to maintain the voltage of the capacitors forming the DC-link at a desired constant level. For this, proportional-integral controllers are designed. The design of all three loops considers the average model of the system. The performance of the proposed multi-loop control law is evaluated through numerical results and real-time experimental implementation, both considering a 2 kW academic benchmark with a constant switching frequency of 7 kHz. In order to provide harmonic distortion, a nonlinear load based on an uncontrolled diode bridge rectifier is considered. Additionally, step-load changes from 0.5 kW to 1 kW are considered for the nonlinear load. As a result, a suitable current tracking, voltage regulation, and balance are observed despite parametric uncertainties, load variations, and harmonic distortion. As a consequence, in steady state, simulation results indicate that the compensated grid current THD is 1.75%; meanwhile, the nonlinear load current THD is 52.5%. Experimental results indicate that the compensated grid current THD is 2.32%; meanwhile, the nonlinear load current THD is 53.8%.

Keywords: harmonic compensation; multilevel converter; model based control

1. Introduction

The ever increasing connection of non-linear loads (NLL) to the grid has produced power quality problems in sensitive electrical distribution systems. In particular, these NLL enlarge the reactive power and harmonic components circulating in electrical grids, which, in turn, lead to several issues, such as voltage waveform distortions, overheating of distribution transformers, electromagnetic interference, and inefficient distribution of energy, among others. Currently, modern electrical systems are adopting the concept of smart grids, which allows dealing in a more appropriate way with the high penetration of renewable energy (solar, wind, biomass energy, etc.) and multiple electronic loads.

However, the need for energy quality compensators is still imperative [1]. Shunt active power filters (SAPF) represent a viable alternative to attenuate the adverse effects caused by NLL [2,3]. SAPF can compensate both the harmonics generated by NLL and the reactive power produced by non-resistive linear loads to ensure a power factor (PF) close to unity according to international power quality standards, such as IEEE-519 [4]. Therefore, the use of SAPF entails a significant increase in the overall efficiency of the system and leads to reduced energy consumption costs.

The typical structure of an SAPF consists of a voltage source inverter (VSI), which converts the type of electrical energy and serves as a coupling between the grid and the DC-link. The DC-link in the SAPF is made of capacitors, large enough to store energy to compensate transient current peaks throughout the operation of the system. An output filter is generally used as the coupling impedance between the VSI and the grid at the point of common coupling (PCC) to reduce the current switching ripple. Many VSI topologies used in SAPF applications have been studied. In particular, multilevel converters have demonstrated better characteristics when compared to traditional two-level conventional topologies [2]. Mainly, multilevel inverters are able to produce higher quality voltage and current waveforms. Furthermore, in multilevel inverters, the voltage across the switching devices is lower, which implies low electric stress on power semiconductors and a reduction of switching losses, keeping high efficiency. For instance, the five level HB-NPC topology has shown efficiency greater than 96% for photovoltaic applications [5].

In particular, the neutral point clamped (NPC) [6–8], full H-bridge [9], and flying capacitor [10], which are three-level power converter topologies, have been used as the VSI in SAPF applications. Five-level inverters, namely five-level (one-leg) NPC [11,12], H-bridge NPC (HB-NPC) [13,14], and cascade full-bridge topologies [15], have also been used as SAPF. Five-level inverters are able to generate an AC output voltage waveform with smaller switching ripple as compared to three-level inverters. They also provide lower common-mode voltage, lower harmonic distortion, and lower electromagnetic interference [6,16,17]. For instance, in [18], a cascade H-bridge (CHB) based multilevel converter was used as a static VAR compensator (STATCOM) in a wind farm. Additionally, a CHB-based SAPF using single-phase toroidal core transformers in cascaded configuration was presented in [19], which allowed the system to operate with a single DC-link capacitor. Furthermore, a detailed comparison of multilevel topologies' characteristics and their applications were presented in [20,21].

In the last few years, research related to the control design for different topologies used in SAPF applications has been carried out extensively as well. For instance, the work in [8] presented a control design for a three-level NPC as an SAPF. Here, the control method aimed to solve the current tracking problem and provided damping to the three order output filter. In [11,12], fuzzy logic control solutions were presented to solve the current tracking problem in a five-level NPC converter. In [22], a three-phase VSI connected to the PCC was used as an SAPF. In this case, the NLL was represented by an electric vehicle supplied by a photovoltaic system, which was controlled by a neuro-fuzzy inference system in combination with an MPPT scheme. In [23], a combination of a neural network control strategy plus a bandless hysteresis controller was proposed for a switched capacitor used as an SAPF. However, due to the nonlinear nature of the system, this control technique produced variable switching frequency, leading to undesirable resonance effects in grid-tied power electronics converters [24]. In [25], a proportional-integral (PI) iterative controller was proposed for a shunt hybrid power filter. In [26], a modified multifrequency passivity-based control (PBC) strategy was proposed for an SAPF based on a T-Type inverter topology. The modification consisted of the introduction of a PI regulator into the coupling loop of the conventional PBC. In [3], a model-based sliding-mode control (SMC) was proposed for a three-phase full-bridge shunt active power filter. The solution consisted of a Kalman filter structure to estimate the variables used to generate the switching surfaces. Nevertheless, a major drawback of SMC is the oscillations, also referred to as chattering, which are produced due to the switching time delay and the unknown dynamics of the system. As a consequence, SMC presents

low control precision and unstable switching frequency in power electronics applications interacting with the electrical grid [27].

However, multilevel inverters exhibit also certain drawbacks. For instance, the control design becomes more challenging than in conventional three-level topologies. In fact, most multilevel power converters require an extra control strategy to guarantee that each capacitor in the topology maintains a specific voltage level. This is referred to as the voltage balancing loop, which gets more involved for higher levels and may represent a considerable additional computational cost. For instance, the work in [28] described in detail the modeling and control design for a three-level half-bridge NPC converter used as an SAPF, whereas, in [29], a control scheme for the cascaded H-bridge topology was proposed. In [30], a predictive current control scheme for an SAPF was presented. In [13,14], also predictive current control schemes were proposed for single-phase NPC power converters as an SAPF. In [14], a single-objective predictive control method was proposed for a single-phase SAPF based on a three-level NPC converter. Here, the control scheme aimed to compensate the reactive power and harmonic distortion without using weighting factors as the cost function. In [10], a novel finite control state set model predictive control was proposed for a flying capacitor topology operating as an SAPF. However, an issue for the implementation of predictive control techniques is the tuning for a reliable weighting factor, which is a complex optimization challenge in active power filtering applications [14]. Moreover, the absence of a modulating signal produces a varying switching frequency due to the limited number of valid switching states generating large current and voltage ripples [31].

This paper presents the modeling process and control design of an SAPF based on a five-level HB-NPC topology. This topology is composed of the bridge connection of two NPC branches, which provides five output voltage levels. The controller includes a control law capable of compensating reactive and harmonic currents. As the DC-link is split and composed of two capacitors, the controller also includes two additional voltage loops, namely voltage balance and regulation control loops to control the DC-link.

The contributions of this work towards shunt active power filtering are as follows:

- The design of a multi-loop controller for SAPF based on a five-level HB-NPC topology, which considers a time scale separation between current and voltage dynamics. The last yields three independent control loops, i.e., current tracking loop, voltage regulation loop, and voltage balance loop for PF correction and harmonic mitigation.
- The proposed control scheme does not depend on system parameters' knowledge; therefore, a robust behavior against grid uncertain parameters, output filter uncertain parameters, current harmonic distortion, and load variations is exhibited.
- According to the best of the authors knowledge, there is no similar work in the literature regarding the experimental validation of the proposed control scheme applied to a five-level HB-NPC topology for an SAPF of 2 kW academic prototype with a constant switching frequency of 7 kHz.

The rest of the paper is organized as follows: In Section 2, the model of the system is obtained, and the control objectives together with the main assumptions are presented. Section 3 details the design of the three control loops, and numerical results are presented as well. Section 4.2 shows experimental results to evaluate the performance of the closed-loop system. Finally, Section 5 provides some concluding remarks about the present work.

2. System Description

Figure 1 depicts the five-level HB-NPC (5L-HB-NPC) topology used as an SAPF, which is connected in parallel to the NLL. The grid voltage is represented by v_G, which supplies both the NLL and the SAPF, and has a fundamental frequency given by ω. The grid impedance is represented by the series connection of L_G and R_G. Hence, the voltage at the PCC is given by:

$$v_{\text{PCC}} = v_G - L_G \dot{i}_G - R_G i_G. \tag{1}$$

The SAPF is coupled to the PCC through an L_F filter (R_F represents the filter parasitic resistance). Notice that, to generate a multilevel output voltage, it is necessary to store enough energy in both DC-link capacitors C_1 and C_2. In other words, it is necessary to maintain a DC-link voltage level high enough to allow the reconstruction of a required VSI output voltage, also referred to as the injected voltage. The VSI output voltage must dominate the grid voltage amplitude to allow the appropriate injection of current towards the grid. Moreover, it is mandatory to guarantee that all capacitors in the DC-bus have a balanced voltage to avoid asymmetries on the reconstructed injected voltage. This fact will be detailed later in the control objectives' definition.

As shown in Figure 1, the 5L-HB-NPC consists of two branches of conventional three-level NPC converters connected in an H-bridge configuration. Every switch of the topology is represented by S_n ($n \in \{1,2,3,4,5,6,7,8\}$). The topology involves four diodes to gain access from the mid-point of the DC-link to the VSI output voltage to produce the null states. The permissible outputs for the converter are summarized in Table 1, where the value o one represents the ON state, whilst the value of zero represents the OFF state at the corresponding switch. The inverter output voltage is represented by e_{AF}, which takes values from a discrete set of possible voltage levels, i.e., $e_{AF} \in \{v_{C1}, v_{C2}, (v_{C1}+v_{C2}), 0, -(v_{C1}+v_{C2}), -v_{C1}, -v_{C2}\}$.

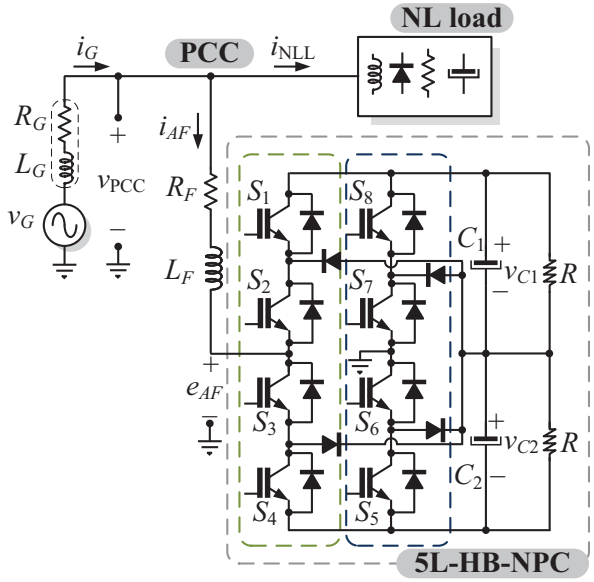


Figure 1. Single-phase SAPF based on a 5L-HB-NPC topology.

Table 1. Switching states of the 5L-HB-NPC.

State	δ_1	δ_2	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	e_{AF} (V)
1	1	−1	1	1	0	0	1	1	0	0	$v_{C1}+v_{C2}$
2	1	0	1	1	0	0	0	1	1	0	$+v_{C1}$
3	0	−1	0	1	1	0	1	1	0	0	$+v_{C2}$
4	0	0	0	0	1	1	1	1	0	0	0
5	0	0	0	1	1	0	0	1	1	0	0
6	0	0	1	1	0	0	0	0	1	1	0
7	0	1	0	1	1	0	0	0	1	1	$-v_{C1}$
8	−1	0	0	0	1	1	0	1	1	0	$-v_{C2}$
9	−1	1	0	0	1	1	0	0	1	1	$-(v_{C1}+v_{C2})$

To simplify the modeling process, an equivalent circuit that represents a simplification of the power converter operation is obtained following the guidelines presented in [32] and is shown in Figure 2, where the switches are replaced by two equivalent single pole triple throw switches. Notice that δ_1 and δ_2 represent switching functions taking values in the discrete set $\{-1, 0, 1\}$. Table 1 relates the switch positions combinations to the equivalent switching functions δ_1 and δ_2. Out of this equivalence, the following expression of the control signal e_{AF} in terms of the switching functions δ_1 and δ_2 and the DC capacitor voltage levels can be obtained:

$$e_{AF} = \frac{1}{2}(\delta_1 - \delta_2)(v_{C1} + v_{C2}) + \frac{1}{2}({\delta_1}^2 - {\delta_2}^2)(v_{C1} - v_{C2}). \tag{2}$$

As stated in the power electronics literature [33], the model SAPF based on the 5L-HB-NPC can be obtained by direct application of Kirchhoff's current and voltage laws, on the equivalent circuit of Figure 2, which yields:

$$\begin{aligned}
(L_F + L_G)\dot{x}_G &= -(R_G + R_F)x_G - e_{AF} + L_F\dot{i}_{\text{NLL}} + R_F i_{\text{NLL}} + v_G, && (3)\\
C\dot{x}_R &= u_a(x_G - i_{\text{NLL}}) - \frac{x_R}{R}, && (4)\\
C\dot{x}_B &= u_a u_b(x_G - i_{\text{NLL}}) - \frac{x_B}{R}, && (5)\\
e_{AF} &= \frac{x_R u_a}{2} + \frac{x_B u_a u_b}{2}, && (6)\\
u_a &\triangleq \delta_1 - \delta_2, && (7)\\
u_b &\triangleq \delta_1 + \delta_2, && (8)
\end{aligned}$$

where $x_G \triangleq i_G$, $x_R \triangleq (v_{C1} + v_{C2})$, and $x_B \triangleq (v_{C1} - v_{C2})$. The nonlinear current generated by the NLL is represented by i_{NLL}. Notice that the state x_R provides a measure of the capacitor voltage regulation, while the state x_B represents the capacitor voltage difference at the DC-link, i.e., the voltage balance. The output inductive filter is represented by L_F. The DC-link is formed by two bulky capacitors C_1 and C_2 with the same capacitance value, i.e., $C_1 = C_2 = C$. Notice that the resistive term R is considered a system parameter and represents the typical resistance used for safety reasons to discharge the DC-link capacitors in maintenance works [34]. Notice also that this resistor is commonly of a high value above tens of kilo ohms and may provide a small damping effect on the system. On the other hand, the voltage at the PCC v_{PCC} is an available signal to be measured.

For control design purposes, an average model of the system is considered instead. For this, the switching signals δ_1 and δ_2 are replaced by the corresponding duty ratios d_1 and d_2, which abide by the continuous range $[-1, 1]$. That is, in the above model, only the definitions of u_a and u_b are modified as follows:

$$u_a \triangleq d_1 - d_2, \;\; u_b \triangleq d_1 + d_2. \tag{9}$$

which, in principle, makes e_{AF} a continuous signal and smooths the dynamics of all three states x_G, x_R, and x_B. Notice that the duty cycles can be recovered from (9) as follows:

$$d_1 = \frac{1}{2}(u_a + u_b), \;\; d_2 = \frac{1}{2}(u_b - u_a). \tag{10}$$

The usage of averaged models for control design is a widely-accepted practice and is supported by the fact that the switching frequency of the power converter is at least 10 times higher than the bandwidth of the closed-loop system dynamics.

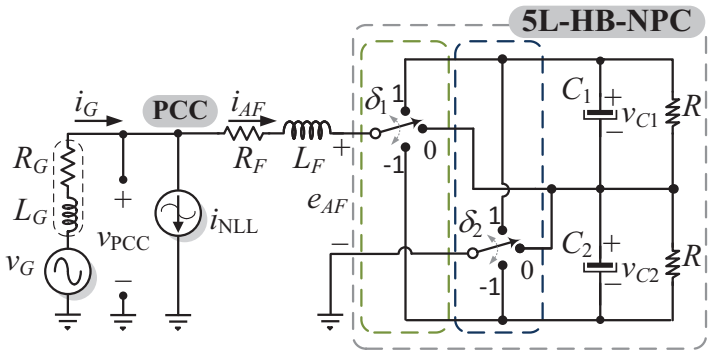


Figure 2. Equivalent diagram of the SAPF based on the 5L-HB-NPC topology with the switching functions δ_1 and δ_2.

Based on the system model (3)–(8), the following three control objectives can be stated, namely current tracking, voltage balance, and voltage regulation objectives:

O1. Current tracking objective: An inner (current) control loop is designed to guarantee tracking of the state x_G towards a desired reference x_G^*, i.e., (Without loss of generality, time dependency is only explicitly used in (11) and (13)–(15). Throughout the paper, time dependency is omitted for simplicity.):

$$\lim_{t\to\infty} x_G(t) = x_G^*(t), \tag{11}$$

where the current reference is calculated as:

$$x_G^* = \frac{p^\star}{v_{\text{PCC,RMS}}^2} v_{\text{PCC},1}, \tag{12}$$

where $v_{\text{PCC},1}$ is the fundamental component of v_{PCC} and $v_{\text{PCC,RMS}}$ its RMS value. In practice, v_{PCC} may be polluted by harmonic distortion, and thus, it is preferred to construct the current reference $x_G^\star(t)$ in terms of the fundamental component. Signal $v_{\text{PCC},1}$ can be obtained from an external filter or with a phase-locked loop (PLL) scheme [35]. The term $p^\star$ represents the active power reference of the system, which modulates the amplitude of the grid current. The scalar term $p^\star$ is obtained from the outer (regulation voltage) control loop, as will be explained later.

O2. Voltage regulation objective: An outer (regulation voltage) loop is designed to maintain (on average) the DC-link voltage regulated to a desired constant value V_{DC}. In particular, this control objective is expressed as:

$$\lim_{t\to\infty} \langle x_R \rangle_0(t) = V_{\text{DC}}, \tag{13}$$

where $\langle x_R \rangle_0$ represents the DC component of x_R and is used to address the average of x_R, which is extracted using the following averaging function:

$$\langle x_R \rangle_0(t) = \frac{1}{T} \int_{t-T}^{t} x_R(\tau) d\tau, \tag{14}$$

where T represents the fundamental period of the disturbance signal; in this case, a second order harmonic of the fundamental is expected, and thus, $T = \pi/\omega$ can be proposed.

As an outcome of this control loop, the power reference $p^\star$ is obtained. The regulation objective must guarantee that the DC-Link stores enough energy to allow the appropriate injection of the

compensating (reactive and harmonic) current to the PCC.

O3. Voltage balance objective: A balance loop is designed to guarantee that capacitors C_1 and C_2, in the DC-bus, achieve the same voltage level. This avoids asymmetries on the reconstructed injected voltage and guarantees a safe operation of the capacitors. Equivalently, the balance objective is reached if the difference of the capacitor voltages x_B goes to zero, that is,

$$\lim_{t\to\infty} x_B(t) = 0. \tag{15}$$

Additional to the control objectives above defined, the following assumptions are formulated based on the physical construction of the system. These assumption allow, in principle, decoupling the model of the system into three separated dynamics, which permits a simplified analysis and design of the control scheme and establishing the parameter tuning rules.

A1. The inductor current dynamics is faster than the voltage dynamics (in the closed loop). Furthermore, the voltage balance dynamics is considered faster than the voltage regulation dynamics (in the closed loop). Hence, the controller design procedure can be divided into three independent loops' design (one loop for each dynamics). This is commonly referred to as the decoupling assumption and is based on the singular perturbation theory and analysis [36], i.e., a time scale separation.

A2. The fundamental frequency of the grid voltage $\omega = 2\pi f_G$ is a known constant.

A3. The i_{NLL}, as well as the v_{PCC} are periodic signals (may be perturbed by harmonic disturbances) with a fundamental frequency ω, and thus, they can be described by Fourier series as follows:

$$v_{\text{PCC}} = \sum_{h\in H_G} \boldsymbol{\Psi}_h^\top \mathbf{V}_{P,h} \ , \ i_{\text{NLL}} = \sum_{h\in H_G} \boldsymbol{\Psi}_h^\top \mathbf{I}_{NL,h},$$

$$\boldsymbol{\Psi}_h = \begin{pmatrix} \cos h\omega t \\ \sin h\omega t \end{pmatrix}, \ \mathbf{V}_{P,h} = \begin{pmatrix} V_{P,h}^r \\ V_{P,h}^i \end{pmatrix},$$

$$\mathbf{I}_{NL,h} = \begin{pmatrix} I_{NL,h}^r \\ I_{NL,h}^i \end{pmatrix},$$

where $\mathbf{V}_{P,h}$ and $\mathbf{I}_{NL,h}$ are the vectors of unknown harmonic coefficients. Normally, for single-phase systems, such a harmonic distortion is only comprised of odd harmonics, i.e., harmonics in the set $H_G = \{1, 3, 5, \ldots\}$.

A4. The system parameters L_F, C, and R are considered positive unknown constants or may vary slowly due to the aging effect.

3. Controller Design

Based on Assumption A1, the system can be split into three dynamics, each accompanied by its corresponding controller design. The design is thus performed in three separated loops referred to as the current tracking loop, voltage balance loop, and voltage regulation loop, which are explained in detail next.

3.1. Current Tracking Loop

The system current dynamics is described by Subsystem (3), where signal e_{AF} has become a continuous signal after the averaging argumentation, i.e., after replacing the switching signals δ_1 and δ_2 by the corresponding duty ratios d_1 and d_2, as above explained

The new e_{AF} can be seen as a filtered version of the generated VSI output voltage. However, e_{AF} represents the actual control input of Subsystem (3), and thus, it becomes the reference voltage to be reconstructed by the VSI.

Notice that e_{AF} in (6) is comprised of two terms. First is the term $\varepsilon_{AF} = x_R u_a/2$, which is designed to solve the current tracking issue, i.e., to produce the appropriate injected current. Second is the term $x_B u_a u_b/2$, which is a vanishing term, i.e., it equals zero in the steady state after the voltage balance is reached.

Rewriting the current dynamics (3) in terms of the increments yields the following system referred to as the error model:

$$(L_F + L_G)\dot{\tilde{x}}_G = -R_P\tilde{x}_G - \varepsilon_{AF} + \phi_H - \frac{x_B u_a u_b}{2} - L_G\dot{x}_G^* - R_P x_G^* + v_G, \tag{16}$$

$$\varepsilon_{AF} = x_R u_a/2, \tag{17}$$

where $\tilde{x}_G \triangleq (x_G - x_G^*)$ is the error (or increment) of the grid current, i.e., the feedback state; ε_{AF} is the non-vanishing part of e_{AF}; the term $\frac{x_B u_a u_b}{2}$ is considered as a vanishing perturbation; $R_P \triangleq R_F + R_G$ is an unknown positive lumping the parasitic resistances of the system; and ϕ_H is a term where periodic signals are collected as follows:

$$\phi_H = L_F\dot{i}_{\text{NLL}} + R_F i_{\text{NLL}} + L_F\dot{x}_G^* - R_F x_G^*.$$

Subsequently, based on Assumption A3, the term ϕ_H contains similar harmonic contents as the NLL.

Based on the error model (16) and the periodic properties of term ϕ_H above described, the following control law is proposed:

$$\varepsilon_{AF} = v_{\text{PCC}} + k_C\tilde{x}_G + \hat{\phi}_H. \tag{18}$$

The proposed control law in (18) is comprised of three terms. First, a feedforward term v_{PCC} is added to alleviate the exogenous perturbation produced by the effect of the grid impedance. Second, a proportional term, associated with proportional gain $k_C > 0$, is included to add damping to the system. Third, a harmonic compensation term $\hat{\phi}_H$ is included to cope with the harmonic term ϕ_H considered as a perturbation. The design of this latter follows the ideas in [34], which appealed to the internal model principle [37].

Subsystem (16) in the closed loop with the proposed control law (18) yields the following error model:

$$L_F\dot{\tilde{x}}_G = -(k_C + R_P)\tilde{x}_G + \tilde{\phi}_H - \frac{x_B u_a u_b}{2}, \tag{19}$$

where $\tilde{\phi}_H$ is designed as described in [34], which consists of a bank of second-order harmonic oscillators, i.e., a bank of resonant filters tuned at odd harmonics of the fundamental frequency. The control law (18) can be written as:

$$\varepsilon_{AF} = v_{\text{PCC}} + k_C\tilde{x}_G + \sum_{h\in H_G}\frac{2\lambda_h s}{s^2 + h^2\omega_h^2}\tilde{x}_G, \tag{20}$$

where $\lambda_h > 0$ is the gain of the h-th oscillator tuned at the $h\omega$-th harmonic.

Notice that the design of the current tracking loop neglects the vanishing perturbation $x_B u_a u_b/2$ appearing in (16). This is based on the fact that the balance loop, to be described next, guarantees

$x_B \to 0$, while u_a and u_b are bounded by construction and relatively small, and thus, the product yields a relatively small amount.

Based on the structure of (17), it is proposed to calculate the auxiliary control variable u_a, which is necessary to recuperate the duty cycles d_1 and d_2 according to (10), as follows:

$$u_a = \frac{2\varepsilon_{AF}}{x_R}. \tag{21}$$

3.2. Regulation and Balance Control Loops

The design of the voltage balance and regulation loops appeals to the decoupling Assumption A1. This is guaranteed if a suitable design of the physical system and selection of the adequate control parameters is performed. As a consequence, the current dynamics reach the steady state faster than the rest of the system. Therefore, it is assumed that $x_G = x_G^*$ in a relatively short time, which means that $\tilde{x}_G = 0$ and $\varepsilon_{AF} = v_{\text{PCC}}$.

3.2.1. Voltage Balance Control Loop

The design of the voltage balance loop considers Subsystem (5) evaluated at the steady state value of the control input (21) above described and subject to the restriction $x_G = x_G^*$. The dynamics of the voltage balance can thus be rewritten as follows:

$$C\dot{x}_B = \frac{2u_b}{x_R}\left(p^\star - P_L\right) - \frac{x_3}{R}. \tag{22}$$

This is a first-order system (22) with control input u_b affected by a constant term. The term $p^\star \triangleq \langle x_G^* v_{\text{PCC}} \rangle_0$ is calculated at the regulation loop to be explained later, while the term $i_{\text{NLL}} v_{\text{PCC}} \triangleq P_L$ represents the load consumed power. Hence, the power term $(p^\star - P_L)$ coincides with the power losses of the system collected in the term R, i.e., $p^\star - P_L \cong 2V_{\text{DC}}^2/R$. In fact, a more convenient representation for (22) is the following:

$$C\dot{x}_B = u_b\frac{4V_{\text{DC}}}{R} - \frac{x_3}{R}. \tag{23}$$

Based on the structure of (23), the following control law is proposed to guarantee voltage balance. It consists of a proportional plus an integral controller:

$$u_b = -(k_{pB}x_B + k_{iB}\chi_B) \tag{24}$$

$$\dot{\chi}_B = x_B, \tag{25}$$

where k_{pB} is a proportional gain and k_{iB} is an integral gain of the proposed PI controller; χ_B is an auxiliary variable to realize the integral part.

The auxiliary control signal u_b together with u_a above calculated in the current tracking loop are necessary to recuperate the duty cycles d_1 and d_2 according to (10).

3.2.2. Voltage Regulation Control Loop

The voltage regulation loop aims to guarantee that the DC-link is charged to a desired V_{DC} voltage level well above the grid voltage peak value. This is a necessary condition to allow proper compensation of harmonic distortion and reactive power, as above explained. The design of the voltage regulation control loop considers Subsystem (4). The decoupling assumption A1 is also considered, out of which the control signal ε_{AF} in (18) has reached its steady state value. Therefore, the voltage regulation dynamics are simplified as follows:

$$C\dot{z}_R = 2v_{\text{PCC}}(x_G^* - i_L) - \frac{2z_R}{R}, \tag{26}$$

where the following transformation to the new state variable z_R has been used:

$$z_R \triangleq \frac{x_R^2}{2}. \tag{27}$$

After this variable transformation, the voltage regulation objective (O2) changes to guarantee regulation of the new variable z_R towards a desired reference $\frac{V_{\mathrm{DC}}^2}{2}$. Expressing Subsystem (26) in terms of increments of the new variable z_R yields the following system:

$$\frac{C}{2}\dot{\tilde{z}}_R = p^\star - P_L - \frac{\tilde{z}_R}{R}, \tag{28}$$

where the error $\tilde{z}_R$ is defined as:

$$\tilde{z}_R \triangleq z_R - \frac{V_{\mathrm{DC}}^2}{2},$$

and the term $p^\star$ is used only to consider the DC component of the product $x_G^* v_{\mathrm{PCC}}$, that is $p^\star \triangleq \langle x_G^* v_{\mathrm{PCC}} \rangle_0$. Notice that $p^\star$ acts as the control input in the system (28).

Based on the structure of the system (28), the following modified PI control law is proposed to guarantee voltage regulation (on average):

$$\begin{aligned} p^\star &= -(k_{iR}\zeta_R + k_{pR}\chi_R), \\ \dot{\zeta}_R &= \tilde{z}_R, \\ \tau_R \dot{\chi}_R &= \tilde{z}_R - \chi_R, \end{aligned} \tag{29}$$

where $k_{pR} > 0$ is the proportional gain and $k_{iR} > 0$ is the integral gain. Notice that, in the proposed modified PI controller (29), the proportional term includes a first-order low-pass filter with a time constant given by τ_R. This modification of the PI controller avoids the reinjection of the ripple present in z_R towards $p^\star$. The block diagram of the overall proposed scheme is presented in Figure 3. Notice that the resulting control scheme makes use of two PI controller at voltage loops in combination with a proportional plus a bank of resonant filters at the current loop. The overall scheme can be easily implemented in a digital signal processor.

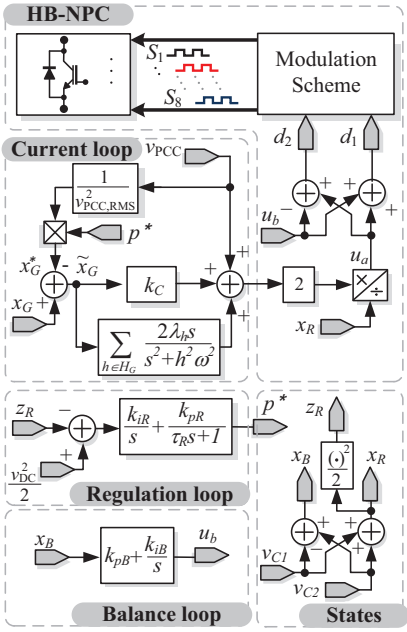


Figure 3. Block diagram of the proposed controller.

3.3. Tuning Guidelines

In what follows, tuning rules for the parameters of the proposed controller are presented to guarantee a desired closed-loop performance. These guidelines are based on the average model of the system, the control objectives, and the assumptions for the controller design.

3.3.1. Tuning Guidelines: Current Tracking Loop

As mentioned above, to guarantee the stability of the current tracking loop and the convergence of the tracking error x_G to zero, it suffices to select $k_C > 0$. However, to guarantee certain performance, it is still necessary to find certain boundaries as described next.

Consider the closed-loop dynamics of the current subsystem (19), which can also be expressed as:

$$L_F \dot{\tilde{x}}_G + k_C \tilde{x}_G = \tilde{\phi}_H, \tag{30}$$

where $\tilde{\phi}_H \triangleq \hat{\phi}_H - \phi_H$ represents the harmonic disturbance estimation error. Note that the bandwidth of (30) is given by $\omega_{BWx_G} = k_C/L_F$. Thereby, if ω_{BWx_G} is limited to be at most $1/10$ of the sampling frequency $2\pi f_s$, then k_C must fulfill:

$$k_C \leq \frac{\pi L_F f_s}{5}. \tag{31}$$

3.3.2. Tuning Guidelines: Voltage Balance Loop

The tuning of parameters k_{pB} and k_{iB} of the voltage balance loop is based on Subsystem (22), which can be rewritten as follows:

$$C\dot{x}_B = -\frac{4V_{\mathrm{DC}}}{R}(k_{pB}x_B + k_{iB}\chi_B) - \frac{x_3}{R}. \tag{32}$$

Its characteristic polynomial is given by:

$$P_B(s) = s^2 + \frac{2k_{pB}+1}{RC}s + \frac{2k_{iB}}{RC}. \tag{33}$$

For this second-order system, the natural oscillation frequency and the damping factor are given by:

$$\omega_{nB} = \sqrt{\frac{2k_{iB}}{RC}}, \tag{34}$$

$$\chi = \frac{2k_{pB}+1}{2\sqrt{k_{iB}RC}}. \tag{35}$$

By assuming that $\omega RC \gg 10$ and considering a critically damped response, then parameters k_{pB} and k_{iB} can be tuned according to:

$$k_{iB} \leq \frac{\omega^2 RC}{50}, \quad k_{pB} \geq \frac{2\sqrt{2}\omega RC}{10}. \tag{36}$$

3.3.3. Tuning Guidelines: Voltage Regulation Loop

The tuning of k_{pR}, k_{iR}, and τ_R considers the closed-loop subsystem (29), which can be rewritten as:

$$\begin{aligned} \frac{C}{2}\dot{\tilde{z}}_R &= -k_{pR}\chi_R - k_{iR}\zeta_R - \frac{z_R}{R} - \frac{V_{\mathrm{DC}}^2}{2}, \\ \dot{\zeta}_R &= \tilde{z}_R, \\ \tau_R\dot{\chi}_R &= \tilde{z}_R - \chi_R, \end{aligned} \tag{37}$$

where ζ_R is a state variable associated with the integral action and χ_R is the state associated with the LPFmodification. It is a common practice to select $\tau_R \ll 1/(2\omega)$, where ω is the fundamental frequency. Hence, the effect of the pole located at $-1/\tau_R$ can be neglected from Subsystem (37), which is then reduced to a second order system. The characteristic polynomial of this reduced system is given by:

$$P_R(s) = s^2 + \frac{2k_{pR}+2}{RC}s + \frac{2k_{iR}}{RC}, \tag{38}$$

where the damping factor and the natural oscillation frequency can be obtained as:

$$\varsigma = \frac{Rk_{pR}+1}{R\sqrt{k_{iR}C}}, \tag{39}$$

$$\omega_{nR} = \sqrt{\frac{2k_{iR}}{C}}. \tag{40}$$

If the damping factor is restricted to $\varsigma \geq 1/\sqrt{2}$, then the bandwidth dynamics of the voltage regulation must comply with $\omega_{BWx_R} \leq \omega_{nR}$. Furthermore, in agreement with the time-scale separation assumption, the condition $\omega_{BWx_R} \ll \omega_{BWx_G}$ must hold. Moreover, to avoid the effect of the second harmonic fluctuation, ω_{x_R} can be further restricted to $\omega/5$. Thus, the parameters can be selected according to:

$$k_{iR} \leq \frac{\omega^2 C}{10}, \quad k_{pR} \geq \frac{\omega C}{200}, \tag{41}$$

where it has been assumed that $\omega RC \gg 20$.

4. Numerical and Experimental Results

In this section, numerical and experimental results are given in order to assess the performance of the proposed control law. For the experimental results, R_F, L_G, and R_G were unknown parameters. However, the controller was capable of dealing with these uncertainties.

4.1. Numerical Results

Numerical simulation results considering the system of Figure 4 are displayed in this part. For this purpose, PSCAD software was employed. The system parameters of the SAPF are shown in Table 2, and the controller parameters are depicted in Table 3.

Table 2. System parameters.

SAPF		**NLL-L**		**NLL-H**	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
v_{PCC}	127 V_{RMS} at 60 Hz	R_{NL1}	85 Ω	R_{NL2}	100 Ω
L_F	3 mH	C_{NL1}	45 µF	C_{NL2}	45 µF
$C_1 = C_2$	1880 µF	R_{L1}	75 Ω	R_{L2}	100 Ω
f_{sw}	7 kHz	L_{L1}	8 mH	L_{L2}	7 mH
R	40 kΩ				
R_{st}	100 Ω				

Table 3. Controller parameters.

Tracking Loop	Regulation Loop	Balance Loop
$k_C = 20$	$k_{iR} = 0.016$	$k_{iB} = 0.0008$
$\lambda_1 = 300$	$k_{pR} = 0.035$	$k_{pB} = 0.01$
$\lambda_3 = 700$	$\tau_R = 60$	
$\lambda_5 = 1450$	$V_{DC} = 220$	
$\lambda_7 = 800$		
$\lambda_9 = 80$		
$\lambda_{11} = 60$		
$\lambda_{13} = 60$		

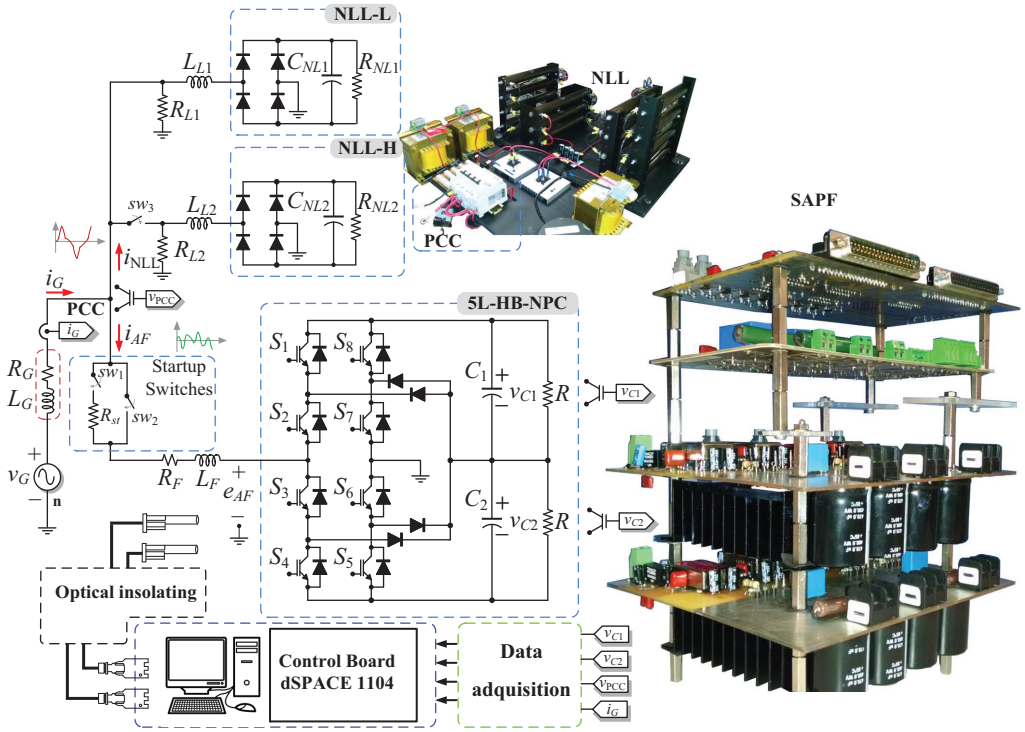


Figure 4. Experimental setup of the 5L-HB-NPC as the SAPF.

The steady state responses of the voltage at the PCC v_{PCC}, the grid current i_G, the current demanded by the NLL i_{NLL}, and the current injected by the SAPF i_{AF} are shown in Figure 5. Notice that, despite the load current i_{NLL} being highly distorted, the proposed control law was able to compensate the grid current i_G to the desired sinusoidal waveform and in phase with the voltage at PCC v_{PCC}; where i_{AF} is the quadrature current provided by the SAPF to compensate the nonlinear current i_{NLL}. Note also that the THD of i_G had a value of 1.75%, while the current consumed by the NLL i_{NLL} presented a THD of 52.5%.

Figure 6 shows the steady state responses of the voltage v_{PCC}, the fundamental component of the voltage at the PCC $v_{\mathrm{PCC},1}$, the compensated current i_G, and the VSI output voltage e_{AF}. At this point, it is worth mentioning that the grid current i_G was constructed using the fundamental component of the grid voltage $v_{\mathrm{PCC},1}$ to avoid the harmonics re-injection through the current reference of the current control loop. The computation of the current reference using $v_{\mathrm{PCC},1}$ guaranteed that the proposed control law was able to compensate the grid current i_G to a sinusoidal signal and in phase with the grid voltage v_{PCC}. Notice that $v_{\mathrm{PCC},1}$ was obtained by using a band-pass filter as in [28] or by using an extra phase-locked loop algorithm [35]. The five-level output voltage of the multilevel converter e_{AF} is also shown in this figure.

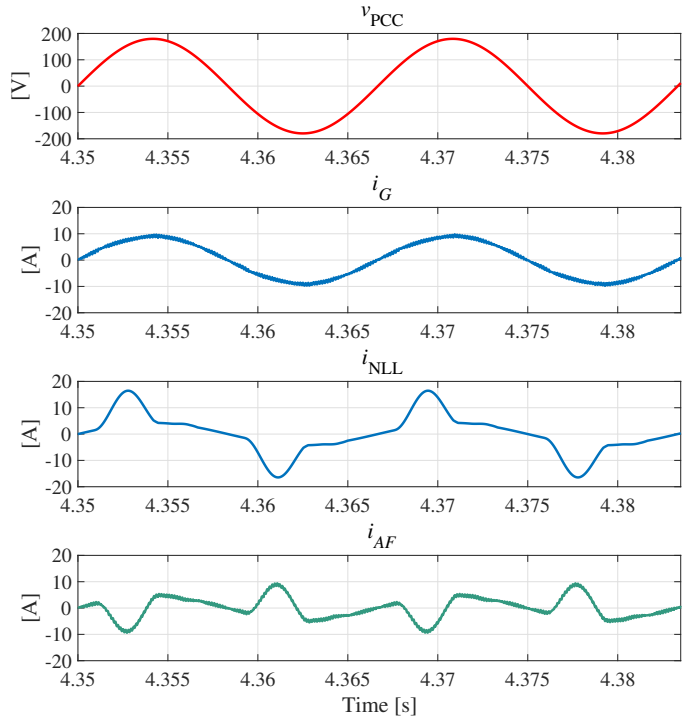


Figure 5. Steady state responses of the voltage at the PCC v_{PCC}, the line current i_G, the current consumed by the NLL i_{NLL}, and the injected current i_{AF}.

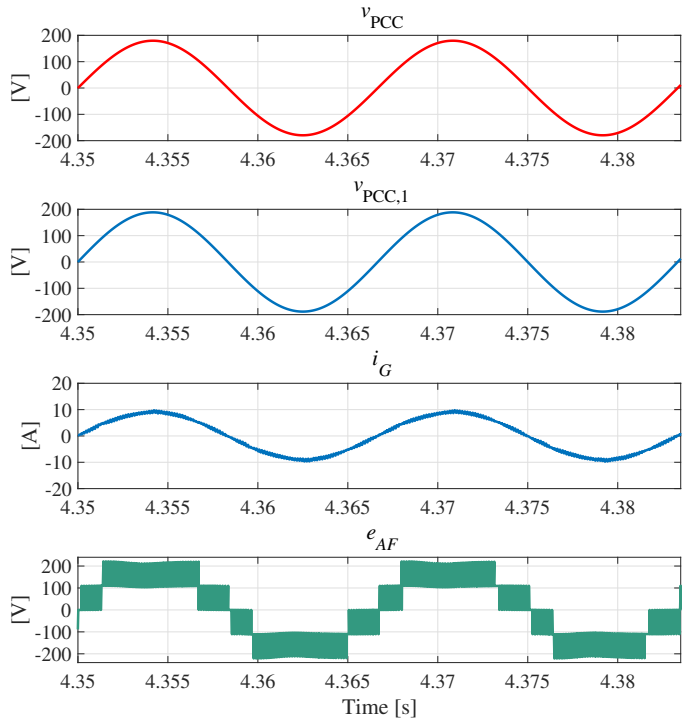


Figure 6. Steady state responses of the grid voltage v_{PCC}, the fundamental component of the grid voltage $v_{PCC,1}$, the line current i_G, and the multilevel output voltage of the inverter e_{AF}.

The transient responses of the voltage across each capacitor of the DC-Link v_{C1}, v_{C2}, the sum of the capacitors voltage x_R, and the power reference calculated in the regulation loop p^* during a step change in the NLL are presented in Figure 7. It can be noted that during the change in the power demand, the voltage regulation loop was capable of maintaining the voltage on each capacitor of the DC-Link v_{C1}, v_{C2} at the desired value of 110 V each, after a smooth transient. Moreover, in Figure 8, it is possible to observe that the difference between v_{C1} and v_{C2} was zero on average, which demonstrated the effectiveness of the voltage balance loop facing the changes in the power demand. Furthermore, the current tracking loop exhibited a smooth waveform transition during the power demand, increasing or decreasing the amplitude of i_G as required.

Figure 9 shows the transient responses of the grid current i_G, the current consumed by the NLL i_{NLL}, and the current injected from the SAPF i_{AF} during a change of power at the NLL. Note that the waveforms of i_G and i_{AF} did not present any undesirable overshoot during the load changes.

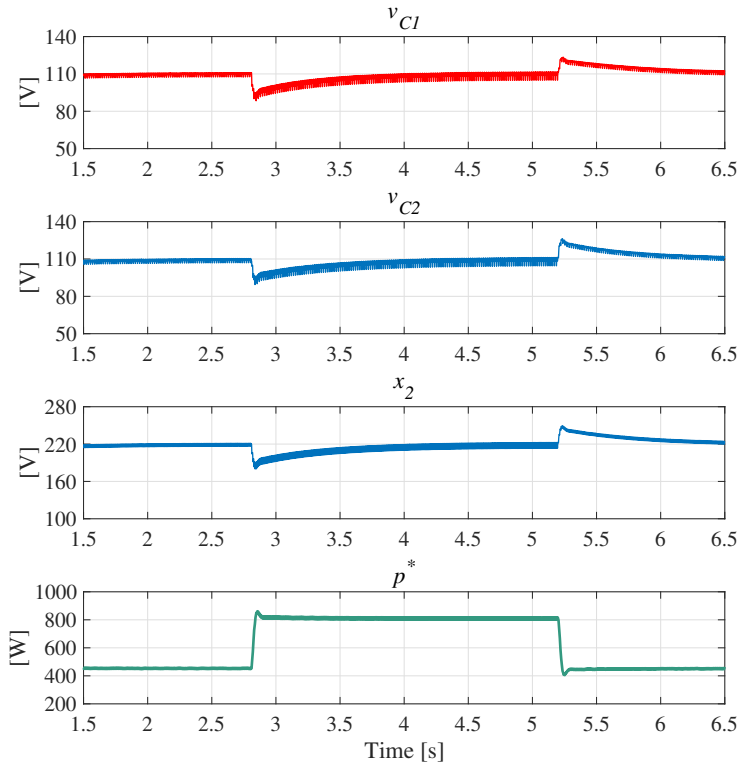


Figure 7. Transient responses of the voltage across each capacitor of the DC-Link v_{C1}, v_{C2}, the sum of the capacitors voltage x_2, and the power reference calculated in the regulation loop p^* during a load change.

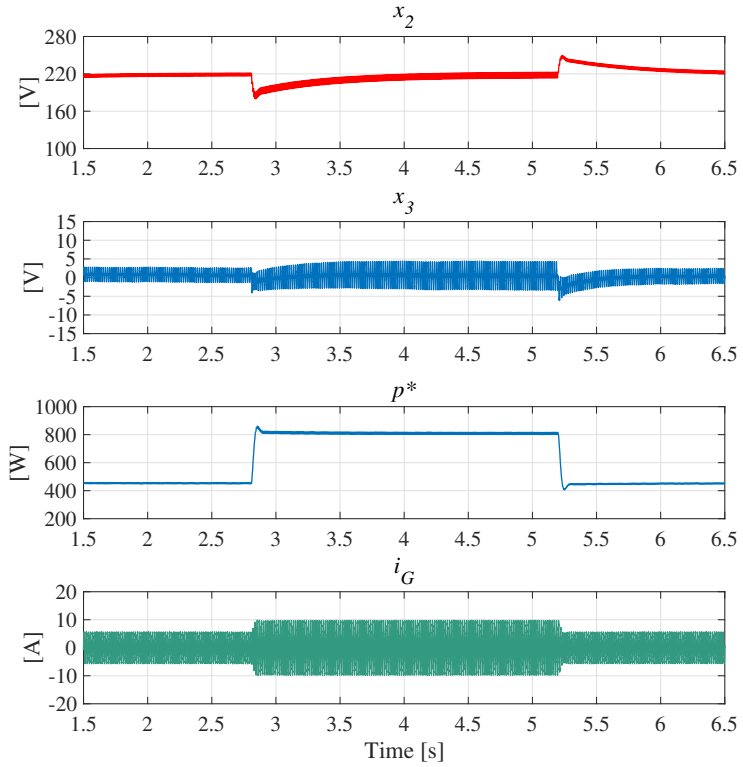
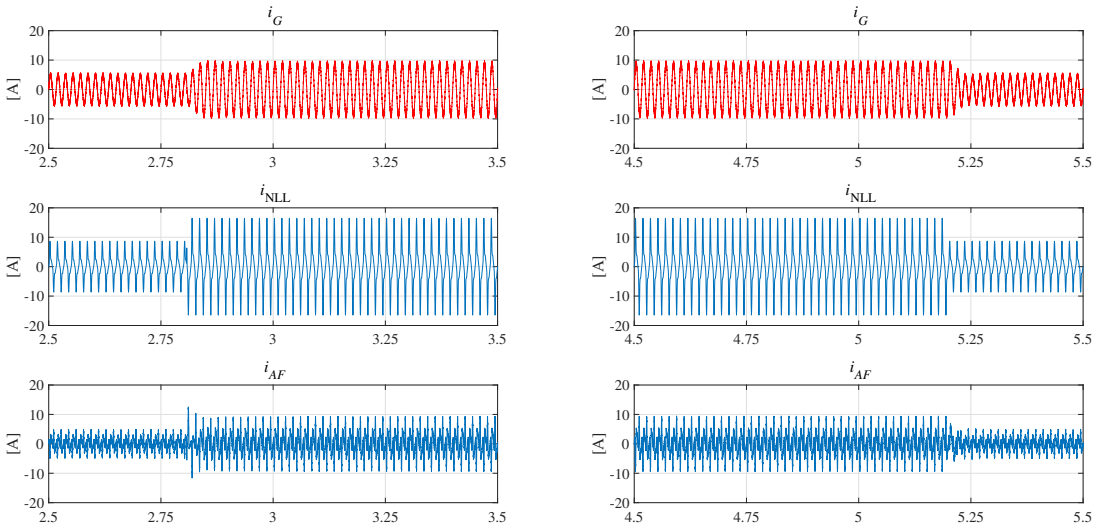


Figure 8. Transient responses of the sum of the capacitors voltages x_2, the difference of the capacitors voltages x_3, the power reference p^*, and the line current i_G during a load change.



(**a**) (**b**)

Figure 9. Transient responses of the line current i_G, the current consumed by the NLL i_{NLL}, and the current injected by the SAPF i_{APF}, during a change of the power demanded by the NLL: (**a**) from low to high load and (**b**) from high to low load.

In order to further evaluate the performance of the proposed control law, an RLload connected to the output of the uncontrolled bridge rectifier was considered for evaluation. In this case and only for this numerical evaluation case, the electrical NLL consisted of a single-phase uncontrolled rectifier (NLL-H in Figure 4) with $R_{L2} = 100\ \Omega$, $R_{NL2} = 15\ \Omega$ and $L_{L2} = 12$ mH, considering two different sizes of inductive output filters $L_F = 2$ mH in Figure 10a and was reduced to $L_F = 1$ mH in Figure 10b. Therefore, in Figure 10a, the steady state responses of the voltage at the point of common coupling v_{PCC}, the grid current i_G, the current demanded by the NLL i_{NLL}, and the current injected by the SAPF i_{AF} are presented. Despite the connection of a different NLL, the controller was capable of achieving an almost sinusoidal current i_G. Nevertheless, a slight deviation appeared as small peaks during the load current zero-crossing on the compensated grid current i_G. This fact occurred given that the slope of NLL was close to 90º, which was produced by the bulky inductance of NLL, and the size of the output filter helped to eliminate the switching frequency, conversely limiting the current compensation capacity in pronounced slopes. Note that the current deformation was able to be alleviated if a small output inductance was placed as in Figure 10b, but the switching ripple increased. Notice also that the total compensation of this spike was not possible given the well-known limitations imposed by the output filter ($\Delta i_{AF}/\Delta t$). On the other hand, the grid current i_G was in phase with the voltage at the PCC v_{PCC} in both cases, which proved the benefits of the controller for power quality improvement despite the NLL loads connected at the PCC. For Figure 10a, the THD of the compensated grid current i_G was 1.49%; meanwhile, for NLL current i_{NLL}, the THD was 17.1%. On the other hand, for the compensated grid current i_G of Figure 10b, the THD was 1.1%; meanwhile, the THD of the NLL i_{NLL} stayed at the same value of 17.1%. Notice that the THD of the compensated grid current i_G in both cases reached values less than 5%.

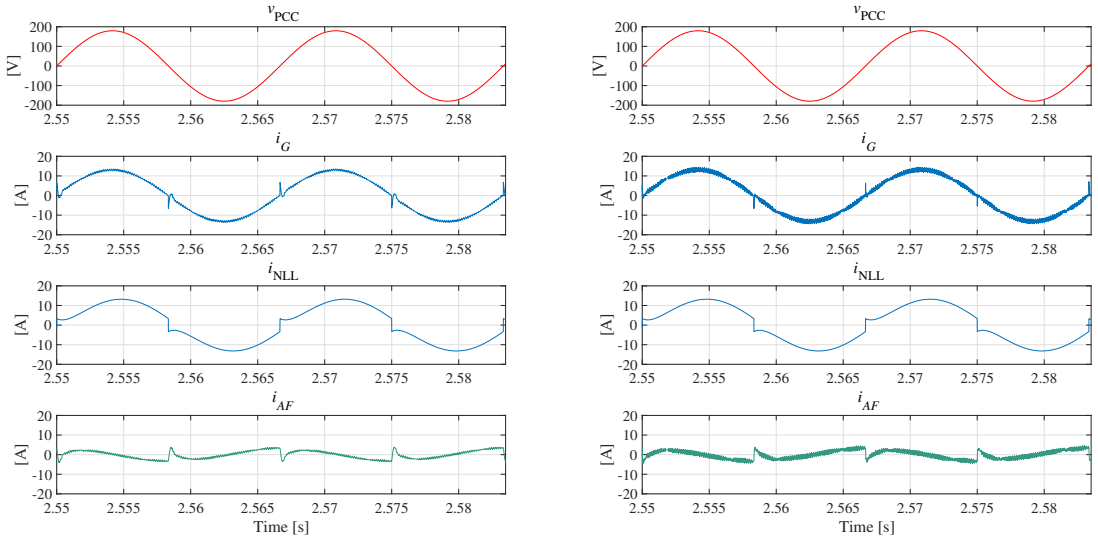


Figure 10. Steady state responses of the voltage at the PCC v_{PCC}, the compensated line current i_G, the current consumed by the NLL i_{NLL} with RLload, and the injected current i_{AF} with the inductive output filter of (**a**) $L_F = 3$ mH and (**b**) $L_F = 1$ mH.

4.2. Experimental Results

The performance of the SAPF based on the 5L-HB-NPC inverter under the proposed controller was experimentally tested in a 2 kW prototype with a constant switching frequency of 7 kHz. The 5L-HB-NPC as an SAPF was implemented as shown in Figure 4. The system parameters for the academic prototype are summarized in Table 2. As depicted in Figure 4, the SAPF was connected to the PCC to compensate the nonlinear currents produced by the NLL. The i_{NLL} was produced by

a pair of NLLs, which were implemented as uncontrolled diode bridge rectifiers feeding an RCload composed of a resistor R_{NLn}, a capacitor C_{NLn}, and an input inductance L_Ln. Furthermore, a linear resistor R_Ln was connected at the input of each NLL to increment the power demand. The combination of these load produced a distorted current referred as i_{NLL} to be compensated by the SAPF. Notice that $n = 1, 2$ was used to refer to the fixed low nonlinear load (NLL-L) or the switched high nonlinear load (NLL-H). The system parameters of the SAPF are summarized in Table 2. The SAPF was implemented using the discrete semiconductors IRG4PC40FD as IGBT switching elements and the semiconductor MUR3060WT as a clamped diode. The control law was implemented in a dSPACE 1104 control board. The parameters of the controller were tuned according to the above guidelines and are listed in Table 3. The current sensor was CLN-50, and the voltage sensors were LV25P.

Figure 11 shows the steady state responses (measured at the PCC) of the voltage v_{PCC}, the grid current i_G, the current consumed by the NLL i_{NLL}, and the injected current i_{AF} from the SAPF. Notice that the voltage at the PCC presented harmonic distortion. Nevertheless, the grid current i_G showed an almost pure sinusoidal waveform in phase with the voltage waveform despite the NLL connected to the PCC. This came from the fact that the fundamental component of v_{PCC} was used as a basis to construct the current reference. This corroborated the tracking of the grid current i_G towards its sinusoidal reference.

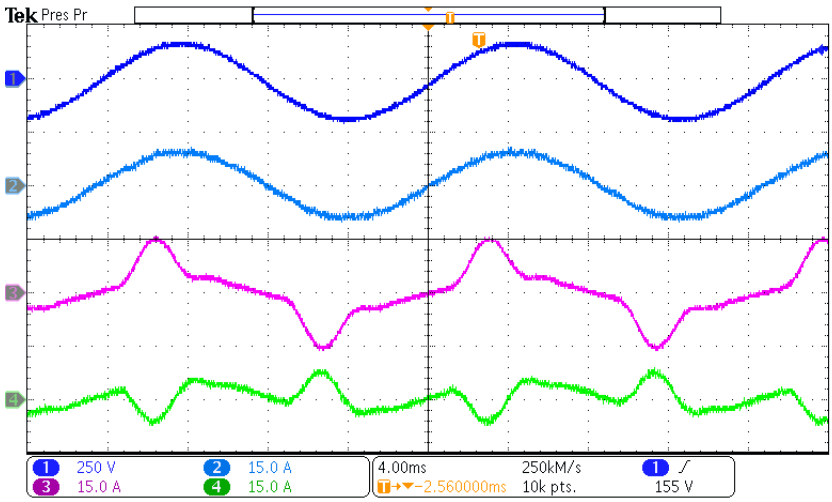


Figure 11. Steady state responses at the PCC after the current compensation process of: (CH1) the voltage v_{PCC} (y-axis 250 V/div); (CH2) the grid current i_G (y-axis 15 A/div); (CH3) the current consumed by the NLL i_{NLL} (y-axis 15 A/div); and the injected current i_{AF} (y-axis 15 A/div, x-axis 4 ms/div).

The steady state responses at the PCC of the voltage v_{PCC} and the estimation of its fundamental component $v_{\text{PCC},1}$ together with their corresponding frequency spectra are depicted in Figure 12. Notice that the signal v_{PCC} contained harmonic distortion, that is some odd harmonics components were present. Nevertheless, the fundamental component estimate $v_{\text{PCC},1}$ did not show any harmonic distortion. This was crucial in the proposed controller as $v_{\text{PCC},1}$ was used in the construction of the current reference according to (12).

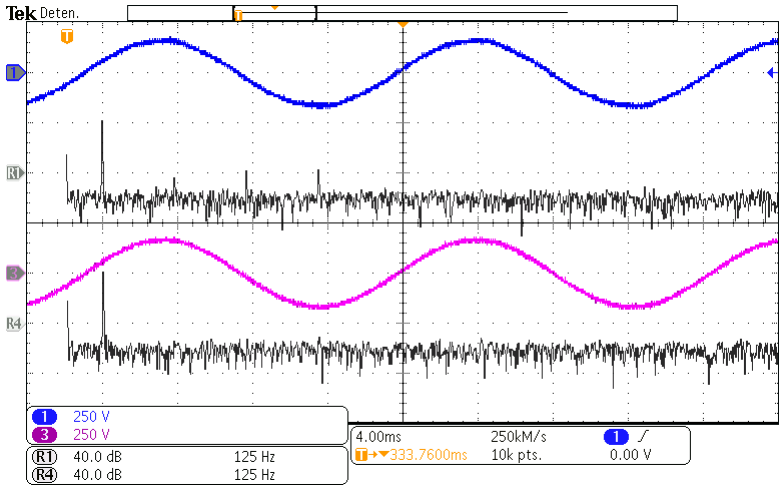


Figure 12. Steady state responses at the PCC of: (CH1) the voltage v_{PCC} (y-axis 250 V/div, x-axis 4 ms/div); (R1) the frequency spectra of v_{PCC} (y-axis 40 dB/div, x-axis 125 Hz/div); (CH3) the fundamental component estimate of the grid voltage $v_{\mathrm{PCC},1}$ (y-axis 250 V/div, x-axis 4 ms/div); and (R4) the frequency spectra of $v_{\mathrm{PCC},1}$ (y-axis 40 dB/div, x-axis 125 Hz/div).

Figure 13 shows the steady state responses of the grid voltage v_{PCC}, the fundamental component estimate of the grid voltage $v_{\mathrm{PCC},1}$, the grid current i_G, and the multilevel output voltage generated by the VSI e_{AF}. It can be observed that all signals were in phase, in particular the grid current i_G and the voltage v_{PCC}. Furthermore, it can be observed that the injected voltage e_{AF} exhibited five levels, as expected.

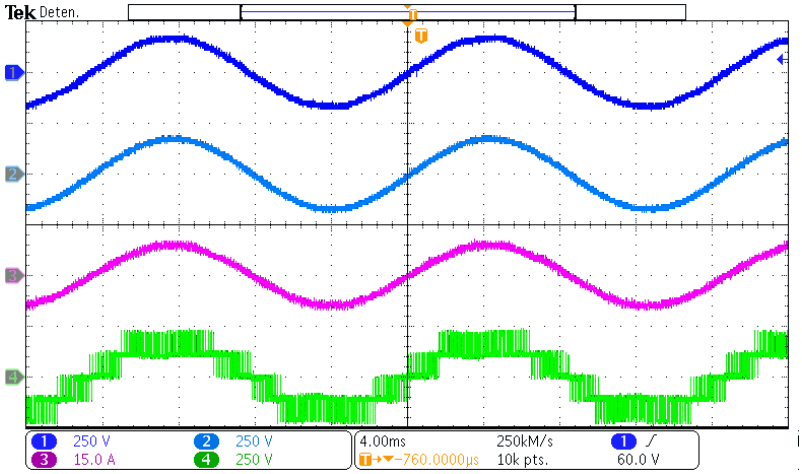


Figure 13. Steady state responses of: (CH1) the grid voltage v_{PCC} (y-axis 250V/div); (CH2) the fundamental component estimate of the grid voltage $v_{\mathrm{PCC},1}$ (y-axis 250V/div); (CH3) the line current i_G (y-axis 15 A/div); and (CH4) the multilevel output voltage generated by the VSI e_{AF} (y-axis 250 V/div).

Figure 14 shows the transient responses of v_{C1}, v_{C2}, x_2, and p^* after i_{NLL} stepwise changes. Notice that the voltage on capacitors v_{C1} and v_{C2} was maintained at the desired reference after a short transient produced by the step changes in the power demanded by the NLL. This corroborated the effectiveness of the voltage regulation loop.

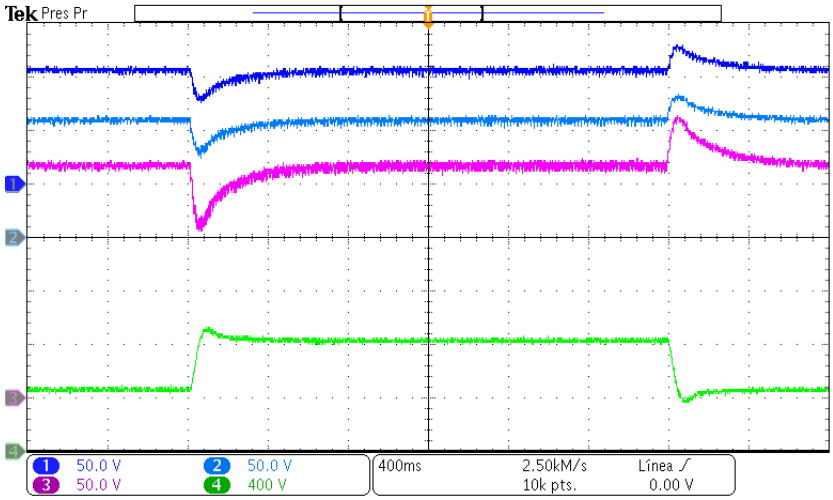


Figure 14. Transient responses during NLL stepwise changes of: (CH1) the capacitor voltage v_{C1} (y-axis 50 V/div); (CH2) the capacitor voltage v_{C2} (y-axis 50 V/div); (CH3) the sum of the capacitors voltages x_2 (y-axis 50 V/div); and (CH4) the power reference p^* calculated in the regulation loop (y-axis 400 W/div).

To evaluate the current and voltage dynamical response of the system variables, Figure 15 shows transient responses under the proposed controller during stepwise changes on the power demand $p^\star$. Notice that the sum of the capacitor voltages x_R was regulated to the desired value despite the changes in the power demand. Moreover, it was observed that the capacitor voltage difference, represented by x_B, was maintained at zero (in average) and exhibited almost imperceptible transients. This corroborated that the controller guaranteed the voltage balance while keeping the capacitor voltages at a reference of 220 V_{DC}. Note also that the grid current i_G increased proportional to the power demanded by the system, and the envelope did not exhibit any overshoot during the transients.

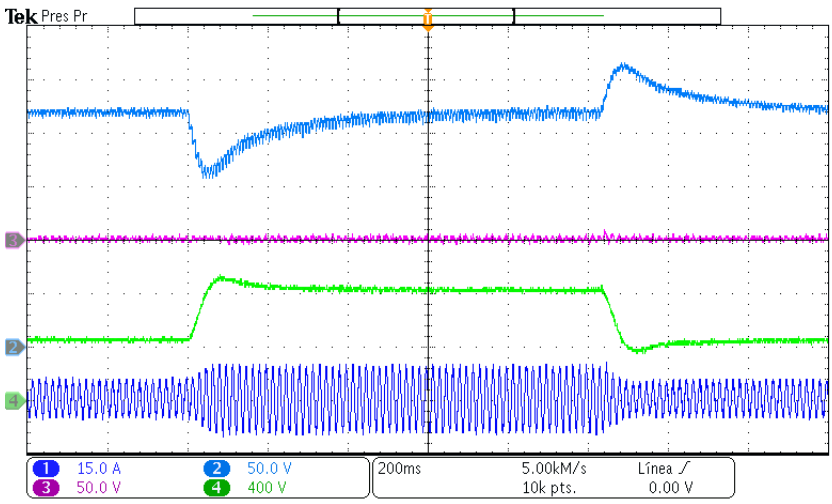
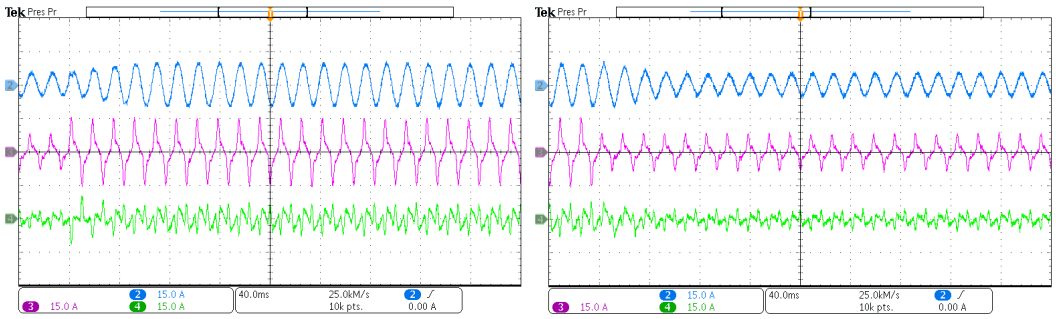


Figure 15. Transient responses during NLL stepwise changes of: (CH1) the sum of the capacitor voltage x_2 (y-axis 50 V/div); (CH2) the difference of the capacitors voltages x_3 (y-axis 50 V/div); (CH3) the power reference p^* calculated in the regulation loop (y-axis 50 V/div); and (CH4) the grid current i_G.

Figure 16 shows the transient responses, during a change of the power demanded by the NLL, of the grid current i_G, the current consumed by the NLL i_{NLL}, and the current injected by the SAPF i_{AF}.

Notice that, during the stepwise changes on the power demand, the current i_G exhibited a fast and smooth response without any overshoot.



(**a**) (**b**)

Figure 16. Transient responses, during a change in the power demanded by the NLL, of: (CH2) the grid current i_G; (CH3) the current consumed by the NLL i_{NLL}; and (CH4) the current injected by the SAPF i_{AF}: (**a**) from low to high load and (**b**) from high to low load (y-axis 15 A/div, x-axis 40 ms/div in all cases).

Figure 17 depicts the steady-state responses of the grid current i_G and the current consumed by the NLL i_{NLL}, together with their corresponding frequency spectra. Notice that the grid current i_G had a quasi-sinusoidal waveform with a THD of 2.32%, while the demanded current by the NLL i_{NLL} had a THD of 53.8%. This represented a noticeable power quality improvement. This was also corroborated by comparing the frequency spectra. Notice that, despite the harmonic pollution observed in the frequency spectra of i_{NLL}, the grid current i_G did not exhibit a perceivable harmonic distortion.

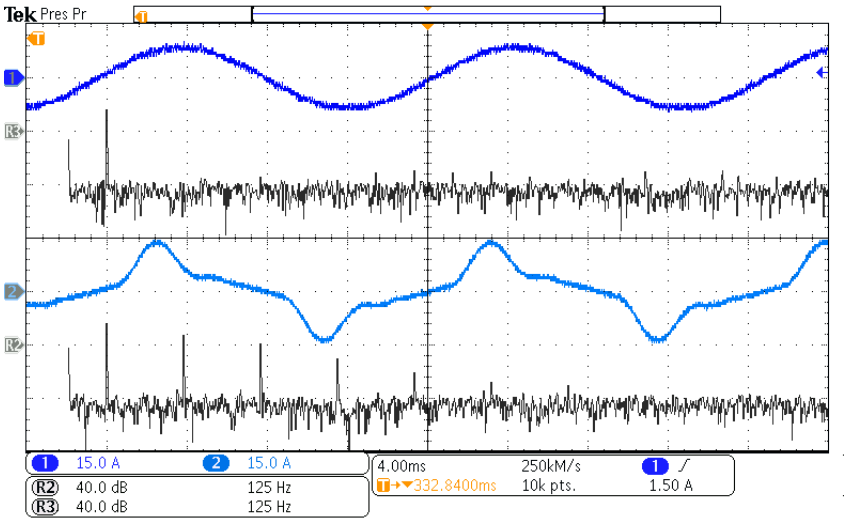


Figure 17. Steady state responses of: (CH1) the grid current i_G (y-axis 15 A/div, x-axis 4 ms/div); (R2) the frequency spectra of i_G (y-axis 40 dB/div, x-axis 125 Hz/div); (CH2) the current consumed by the NLL i_{NLL} (y-axis 15 A/div, x-axis 4 ms/div); and (R3) the frequency spectra of i_{NLL} (y-axis 40 dB/div, x-axis 125 Hz/div).

5. Concluding Remarks

In this work, a control law for a shunt active power filter based on the five-level full-bridge NPC multilevel topology was presented. The control law comprised three control loops aimed to guarantee the control objectives of grid current tracking, DC-link voltage balance, and DC-link voltage regulation. The resulting control law was designed appealing to a dynamics decoupling assumption.

This assumption simplified enormously the control design as it was split into three independent control loops referred to as current, balance, and regulation loops. The current control loop resulted in a combination of a proportional controller aimed to provide damping to the system and a bank of resonant filters aimed to compensate reactive power and harmonic distortion. Regarding the balance and regulation control loops, PI controllers were obtained in each case. In particular, the PI controller of the regulation control loop involved a slight modification, which consisted of the introduction of a low pass filter in the proportional gain to limit the bandwidth of the overall loop. This consideration alleviated the effects and propagation of the unavoidable second harmonics fluctuation in the DC-link voltage produced by the rectification process. Finally, the control law was evaluated in an experimental 2 kW setup of the shunt active power filter based on the five-level full-bridge NPC multilevel topology. The experimental results showed that the active power filter under the proposed controller was able to guarantee an operation with a power factor close to unity and a grid current with less than 5% THD.

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Abbreviations

The following abbreviations and symbols are used in this manuscript:

5L-HB-NPC	Five-level H-bridge neutral point clamped
NLL	Nonlinear loads
SAPF	Shunt active power filter
PF	Power factor
VSI	Voltage source inverter
PCC	Point of common coupling
THD	Total harmonic distortion
PLL	Phase locked loop
RMS	Root mean square
v_G	Grid voltage
ω	Grid fundamental frequency
L_G	Grid inductance
R_G	Grid resistance
v_{PPC}	Voltage at point of common coupling
$i_G = x_G$,	Grid current
L_F	Filter inductance
R_F	Parasitic filter resistance
$C_1 = C_2 = C$	DC-link capacitors
S_1,...,S_8	Converter switches
i_{AF}	Filter current
i_{NLL}	Nonlinear load current
e_{AF}	VSI output voltage
v_{C1}, v_{C2}	Capacitors' C_1 and C_2 voltages, respectively
δ_1, δ_2	Switching functions
d_1, d_2	Duty ratios
$x_R = v_{C1} + v_{C2}$	Voltage regulation state variable
$x_B = v_{C1} - v_{C2}$	Voltage balance state variable
u_a, u_b	Control signals

R	Capacitors' discharge resistance
x_G^*	Grid current reference
$p^\star$	Active power reference
$v_{\text{PPC,RMS}}$	RMS voltage of v_{PPC}
$v_{\text{PPC,1}}$	Fundamental component of v_{PPC}
V_{DC}	Desired constant value for the DC-link
$\langle x_R \rangle_0(t)$	Average value of x_R
T	Fundamental period of averaging function
f_G	Fundamental frequency of grid voltage
$\mathbf{V}_{P,h}$, $\mathbf{I}_{NL,h}$	Vectors of unknown harmonic coefficients.
$\mathbf{\Psi}_h$	Fourier trigonometric vector
$\tilde{x}_G$	Grid current error variable
ϵ_{AF}	Vanishing part of e_{AF}
$R_P = R_G + R_F$	Parasitic resistance
ϕ_H	Sum of periodic signals
k_C	Proportional gain
$\hat{\phi}_H$	Harmonic compensation term
$\tilde{\phi}_H$	Harmonic compensation error
λ_h	Gain of the h-th oscillator
P_L	Demanded load power
k_{pB}, k_{iB}	Proportional and integral gains of the balance loop.
χ_B	Balance loop integral variable
z_R, $\tilde{z}_R$	Transformation variable and error variable
k_{iR}, k_{pR}	Integral and proportional gains of regulation loop
τ_R	Low-pass filter time constant
ζ_R, $\dot{\chi}_R$	Regulation loop integral variable and low-pass filter state
ω_{BWx_G}	Bandwidth of the closed-loop current subsystem
ω_{nB}, χ	Natural oscillation frequency and damping factor of the balance loop
ω_{nR}, ς	Natural oscillation frequency and damping factor of the regulation loop
ω_{BWx_R}	Bandwidth of the closed-loop voltage regulation subsystem

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