# Overview and Comparative Assessment of Single-Phase Power Converter Topologies of Inductive Wireless Charging Systems

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**Abstract:** The acquisition of inductive power transfer (IPT) technology in commercial electric vehicles (EVs) alleviates the inherent burdens of high cost, limited driving range, and long charging time. In EV wireless charging systems using IPT, power electronic converters play a vital role to reduce the size and cost, as well as to maximize the efficiency of the overall system. Over the past years, significant research studies have been conducted by researchers to improve the performance of power conversion systems including the power converter topologies and control schemes. This paper aims to provide an overview of the existing state-of-the-art of power converter topologies for IPT systems in EV charging applications. In this paper, the widely adopted power conversion topologies for IPT systems are selected and their performance is compared in terms of input power factor, input current distortion, current stress, voltage stress, power losses on the converter, and cost. The single-stage matrix converter based IPT systems advantageously adopt the sinusoidal ripple current (SRC) charging technique to remove the intermediate DC-link capacitors, which improves system efficiency, power density and reduces cost. Finally, technical considerations and future opportunities of power converters in EV wireless charging applications are discussed.

**Keywords:** AC–AC converters; battery chargers; electric vehicles; power conversion harmonics; wireless power transmission

## 1. Introduction

The electrification of transportation has been considered as a promising solution to tackle greenhouse gas emissions and fossil fuel depletion. To boost the market share of electric vehicles (EVs), their inherent issues such as limited driving range, long charging time, and costly and cumbersome energy storage systems should be resolved. Wireless charging technology can mitigate the aforementioned issues [1–10]. Wireless power transfer (WPT) enabling transferring energy from a source to a load without electrical contact has been extensively studied and successfully demonstrated using various techniques, namely, acoustic power transfer (APT) [11,12], radio frequency power transfer (RFPT) [13,14], optical power transfer (OPT) [15,16], capacitive power transfer (CPT) [17], and inductive power transfer (IPT) [18]. However, it is well demonstrated from the literature that the IPT technology is the most suitable for EV charging applications where the power requirement is form few to several kW, and the air gap varies from a few centimeters to a few meters [5]. Particularly, researchers and engineers have fitted the outcomes of the IPT to EV battery charging applications with various commercial products and standards [19]. The IPT chargers offer with several benefits such as

safety, convenience, flexibility, weather immunity, and the possibility of range extension and battery volume reduction [1,8,10,20,21]. The wireless chargers can be deployed in residential garages, and office/service/shopping center parking lots for static wireless charging [22], or they can be placed at bus stops, taxi ranks, and traffic lights to implement quasi-dynamic wireless charging [23]. Moreover, dynamic wireless charging systems can be installed on the roads to constantly charge the EVs, in turn, to extend the driving range and reduce the battery volume of the vehicles [24–26].

　　　Essentially, an IPT charging system comprises an inductive coupling coil pair, compensation networks, primary converters to generate high-frequency inputs, and a secondary rectifier to convert AC to DC current to charge the battery. In the IPT charging systems, power electronic converters make a significant contribution to the size and cost, and efficiency of the overall system. Typically, dual-stage conversion (AC–DC–AC) systems have been employed to excite the IPT systems, as shown in Figure 1a. The dual-stage converter topologies are intensively studied and widely used in industry [27–29]. The main advantage of these topologies is that each conversion stage can be separately designed and controlled to optimize specific performance indices. However, the presence of multiple conversion stages and a bulk DC-link capacitor increases the cost, size, and weight of the system. In recent years, the use of matrix converters (MCs) for feeding the IPT systems has drawn increasing attention [30–38]. MCs enable direct conversion of low-frequency AC inputs (50–60 Hz) to high-frequency outputs (up to 85 kHz) without any intermediate conversion stage; therefore, they enhance the system performance in terms of power density, reliability, and cost [32,39]. The single-phase matrix converter-based IPT systems remove the DC-link energy storage elements in the primary side to absorb double line frequency ripple, thus it appears on the battery side. Sinusoidal ripple current (SRC) charging technique reported in [40–45] allows batteries to be charged by double line frequency (100 or 120 Hz) current with minor side effects on their performance. Therefore, matrix converter-based IPT systems can use the sinusoidal charging technique advantageously and remove the intermediate DC-link capacitor. The single-stage EV IPT charging system using MCs is illustrated in Figure 1b.



(a)



(b)
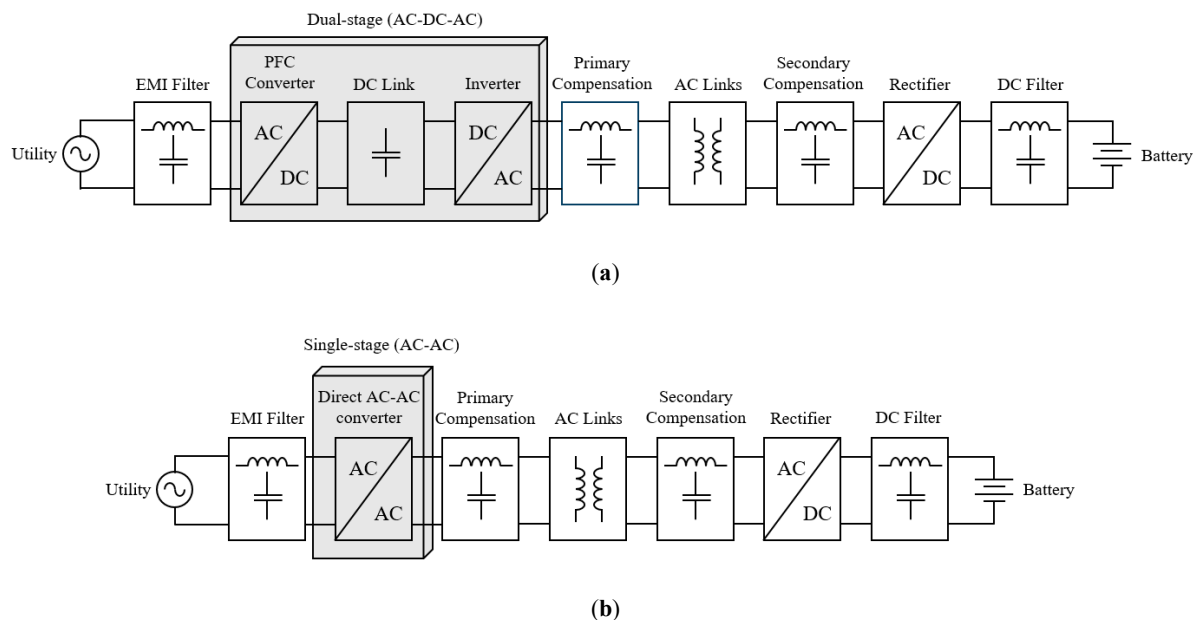
**Figure 1.** Configuration of electric vehicle (EV) inductive power transfer (IPT) systems with (**a**) dual-stage power conversion and (**b**) single-stage power conversion. PFC, power factor correction; EMI, electromagnetic interference.

　　　This paper aims to provide an extensive overview of single-phase power conversion topologies employed in static wireless charging. Then, a comprehensive performance comparison between the conventional dual-stage (power factor correction (PFC) and full-bridge voltage source inverter (VSI))

and single-stage topologies including the buck-derived full-bridge (FB)MC and boost-derived FBMC in the IPT EV charging application is presented. The comparison involves the input power factor, input current distortion, power losses, switching stress, and normalized cost, while taking into account the requirements of Standard J2954 [19] established by the Society of Automotive Engineers (SAE). The Standard SAE J2954 defines acceptable criteria for interoperability, electromagnetic compatibility, electromagnetic field (EMF), minimum performance, safety, and testing for wireless charging of light-duty electric vehicles. Table 1 shows the power classes, operating frequency, and efficiency performance targets of the WPT systems defined in the SAE J2954. As can been seen, four wireless power transfer (WPT) classes are defined based on the maximum input volt-amp (VA) drawn from the grid by the primary side or ground assembly (GA) electronics. The input real power depends on the input power factor, while the output power depends on the efficiency of the system. The SAE J2954 specifies that WPT systems should be operated at a single nominal frequency of 85 kHz. However, for WPT systems using frequency control to compensate operating variations, their operating frequency must be tuned in the band of 81.38 to 90.00 kHz. Finally, the improvement opportunities for each of the IPT charging topologies are discussed in this paper.

**Table 1.** Wireless power transfer (WPT) power classification for light-duty electric vehicles—SAE J2954.

| WPT Levels | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Maximum AC input power (kVA) | 3.7 | 7.7 | 11 | 22 |
| Minimum target efficiency at nominal alignment (%) | >85 | >85 | >85 | To be defined (TBD) |
| Minimum target efficiency at offset position (%) | >80 | >80 | >80 | TBD |
| Operating frequency (kHz) | | | 81.38–90 (typical 85) | |

## 2. Power Converter Topologies for Inductive Wireless Charging

In this section, an overview of front-end converter topologies for WPT applications is provided. They can be classified into two groups, namely dual-stage and single-stage based on the power conversion stages. The classification of single-phase converter topologies for IPT systems is shown in Figure 2.
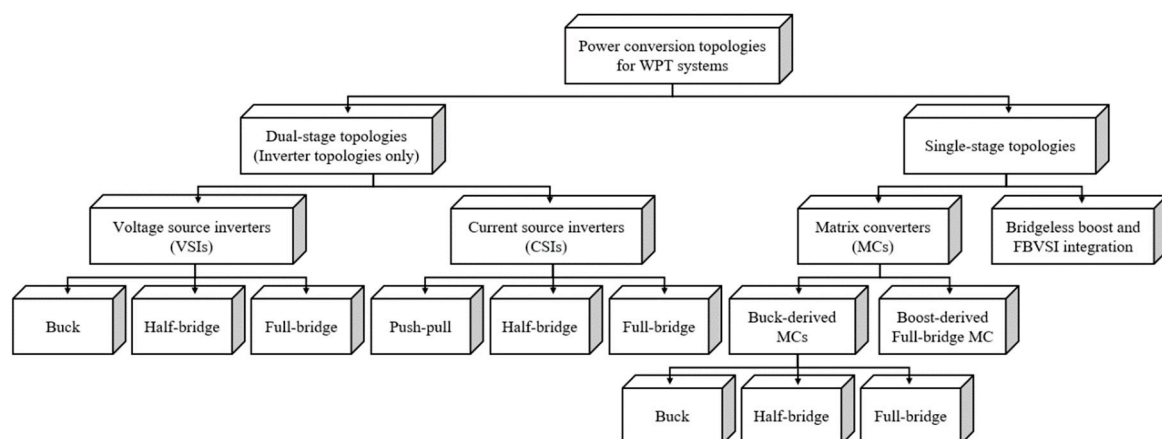


**Figure 2.** Classification of front-end converter topologies for IPT applications. FB, full-bridge; WPT, wireless power transfer.

### 2.1. Dual-Stage Power Conversion

A front-end AC–DC converter is used to convert the supply AC voltage to an intermediate DC-link voltage and to shape the input current for both PFC and harmonic reduction. A comprehensive review for the PFC rectifiers is presented in [46,47]. For the inversion stage, a current-source inverter (CSI) or a VSI can be employed.

Two CSI topologies commonly used in IPT systems are push-pull, half-bridge [48–53], and full-bridge [54,55]. Figure 3a–c shows the configuration of CSIs. The requirement of blocking diodes and bulky inductors that increases the size and cost of the whole IPT system is one of the major drawbacks of the CSIs. A single parallel compensating capacitor in the primary circuit is normally used with CSIs; however, the inverter switches suffer high voltage stress in high-power applications [48,50,52,54]. In order to overcome this drawback, a parallel-series *CC* compensation circuit is introduced in [53,55]. The CSIs combined with the parallel-series *CC* compensation circuit mitigates current and voltage stress on inverter switches and harmonic contents in primary coil current.
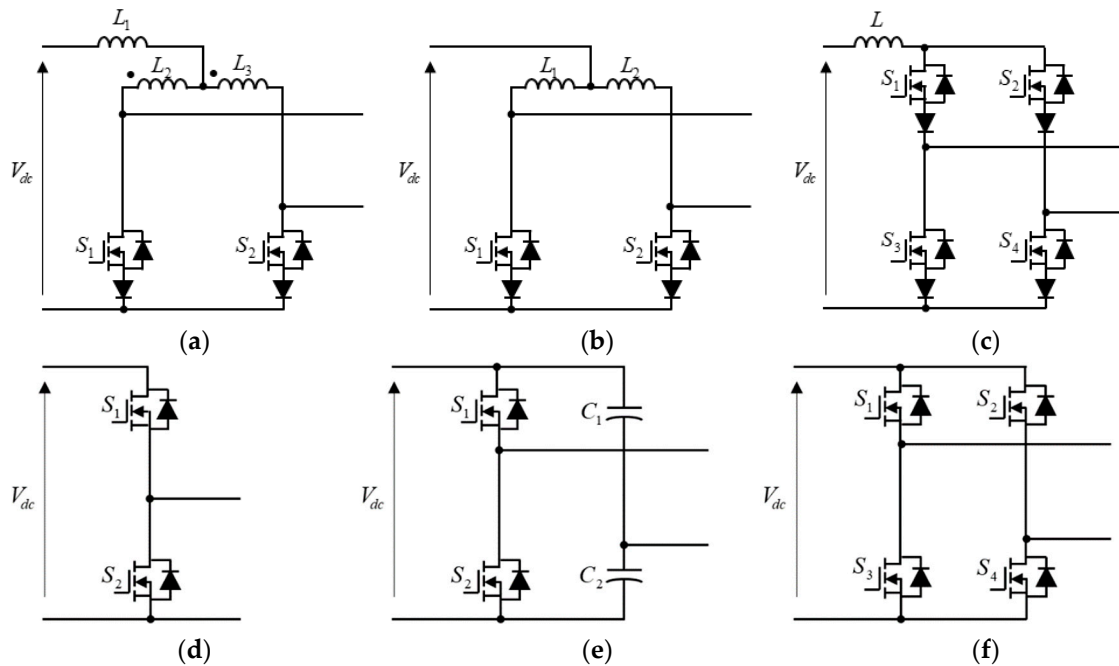


**Figure 3.** Inverter topologies: (**a**) push-pull, (**b**) half-bridge CSI, (**c**) full-bridge CSI, (**d**) buck, (**e**) half-bridge VSI, and (**f**) full-bridge VSI.

For VSI topologies, buck, half-bridge, and full-bridge topologies shown in Figure 3d–f can be used in the IPT systems, and they are compatible with single capacitor series, *LCL*, and *LCCL* compensation networks [1,21,56–66]. The series compensation is simple and cost-effective. However, under light load conditions or in the absence of the receiver, the system experiences severe instability [67,68]. *LCL* or *LCCL* tanks overcome these issues and have a high tolerance to coil misalignments [68]. However, a significant amount of lower-order harmonics in the output current of the VSIs connected with *LCL* and *LCCL* compensation circuits deviates zero-phase-angle operation of the inverters, increasing their switching losses [69]. Moreover, the inductors in *LCL* and *LCCL* compensation circuits must be designed precisely as the effective power transfer capability is highly sensitive to the inductance value [57,61]. Figure 4 shows the compatibility of the inverter types and primary compensation circuits of the IPT systems. Table 2 shows the comparison of the inverter topologies regarding the component requirement. It can be seen that the CSIs require more components than the VSIs.
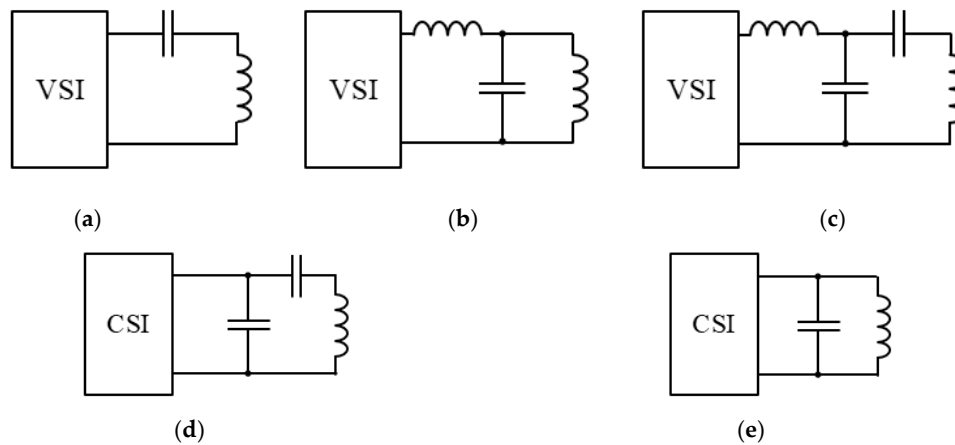
**Figure 4.** Compatibility between inverter types and primary compensation circuits in IPT systems. (**a**) Series *C*, (**b**) *LCL*, (**c**) *LCCL*, (**d**) parallel *C*, and (**e**) parallel-series *CC*.
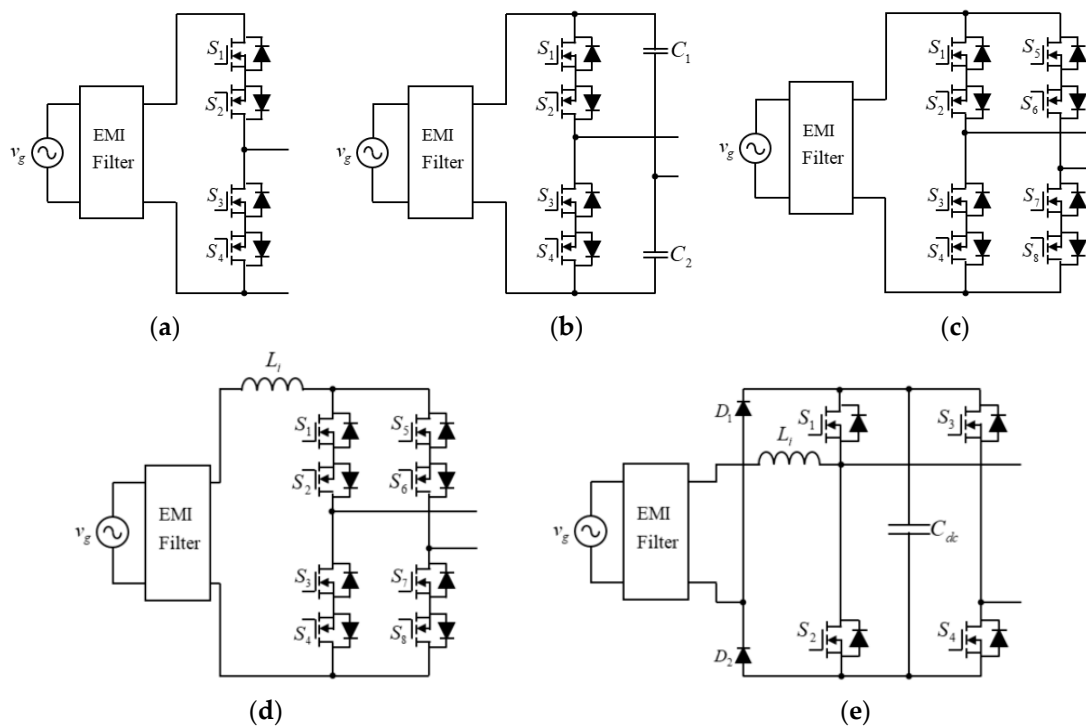


**Figure 5.** Single-stage conversion topologies: (**a**) buck matrix converter, (**b**) half-bridge matrix converter, (**c**) full-bridge matrix converter, (**d**) boost-derived matrix converter, and (**e**) bridgeless boost converter.

**Table 2.** Power conversion topologies and control schemes of the inductive power transfer (IPT) systems.

| Power Conversion Topologies | | Figure | Component Requirement | | Control Schemes |
|---|---|---|---|---|---|
| | | | Switches | Passive Components | |
| Dual-stage (excluding front-end PFC stage) | Current-source push-pull | Figure 3a | 2 reverse blocking | 1 inductor, 1 phase-splitting transformer | • Variable switching frequency<br>• DC-link voltage control<br>• Secondary-side control<br>• Dual-side control |
| | Current-source half-bridge | Figure 3b | 2 reverse blocking | 2 inductors | |
| | Current-source full-bridge | Figure 3c | 4 reverse blocking | 1 inductor | • Variable switching frequency<br>• DC-link voltage control<br>• Pulse width modulation (phase-shift control)<br>• Secondary-side control<br>• Dual-side control |
| | Voltage-source buck | Figure 3d | 2 reverse conducting | None | • Discrete energy injection<br>• Variable switching frequency<br>• DC-link voltage control<br>• Pulse width modulation (duty cycle control)<br>• Secondary-side control<br>• Dual-side control |
| | Voltage-source half-bridge | Figure 3e | 2 reverse conducting | 2 capacitors | |
| | Voltage-source full-bridge | Figure 3f | 4 reverse conducting | None | • Discrete energy injection<br>• Variable switching frequency<br>• DC-link voltage control<br>• Pulse width modulation (phase-shift control)<br>• Secondary-side control<br>• Dual-side control |
| Single-stage | Buck MC | Figure 5a | 2 bidirectional | None | • Discrete energy injection<br>• Pulse width modulation (duty cycle control)<br>• Secondary-side control<br>• Dual-side control |
| | Half-bridge MC | Figure 5b | 2 bidirectional | 2 capacitors | |
| | Full-bridge MC | Figure 5c | 4 bidirectional | None | • Discrete energy injection<br>• Pulse width modulation (phase-shift control)<br>• Secondary-side control<br>• Dual-side control |
| | Boost-derived full-bridge MC | Figure 5e | 4 bidirectional | 1 inductor | • Pulse width modulation<br>• Secondary-side control<br>• Dual-side control |
| | Bridgeless boost | Figure 5f | 2 diodes, 4 reverse conducting | 1 inductor, 1 capacitor | • Pulse width modulation<br>• Secondary-side control<br>• Dual-side control |

### 2.2. Single-Stage AC–AC Conversion

Matrix converters (MCs) are considered as a prominent candidate for powering the WPT systems with only single-stage power conversion. Several MCs including buck [36,37], half-bridge [30,31], and full-bridge [35] have been introduced to IPT applications in the literature. All MCs reported in [30,31,35–37] have a buck-derived configuration, as shown in Figure 5a–c, thus line-current regulation is compromised. In EV charging application, if a highly nonlinear diode-bridge rectifier is used at the battery side, there will be severe line current distortion and power factor deterioration, as explained in [70]. In [35], a secondary active full-bridge rectifier whose phase shift angle follows the line-voltage waveform is used to shape the line current. In this topology, the primary and secondary converters must be controlled synchronously in every switching cycle, which increases the implementation complexity.

In order to overcome the above issue, a boost-derived full-bridge MC (FBMC) compatible with a primary parallel-series *CC* compensation network is proposed in [38]. The proposed converter topology is able to shape the line current and regulate power flow through two control loops, which are similar to those of a conventional boost converter. In [39], a single-stage topology integrating bridgeless boost PFC converter and full-bridge VSI is proposed for IPT applications. The converter is operated in discontinuous conduction mode, thereby, the line current control loop is eliminated. However, in discontinuous conduction mode (DCM), the converter incurs more current stress, losses, and electromagnetic interference (EMI) problems, which is not suitable for high-power applications. Figure 5d and e show the configuration of boost-derived FBMC and bridgeless boost PFC converter in IPT systems.

## 3. Power Control Schemes

Figure 6 shows the classification of power control schemes for IPT systems. Power control in IPT systems can be implemented on the primary side, secondary side, or both sides. The secondary side control is suitable for the IPT applications where multiple secondary coils are coupled to a single primary coil. In these applications, the frequency and the magnitude of primary current are fixed, and the power flow is controlled on the secondary side by an active rectifier or a back-end DC–DC converter illustrated in Figure 6 for each secondary coil [30,58,59,71–74]. These topologies are normally employed in long-power track systems where a constant track current is required to power independent secondary coils.
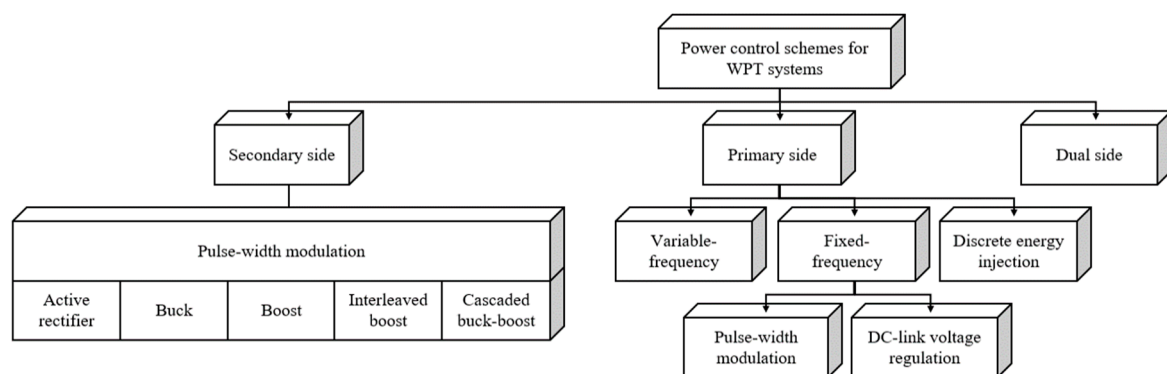
**Figure 6.** Classification of power control schemes for IPT applications.

However, in charging applications where only one a secondary coil is coupled to a primary coil and keeping the secondary-side configuration as simple as possible is a priority, the primary side control is selected. The primary side control can be divided into three groups: fixed frequency, variable frequency, and discrete energy injection. In fixed frequency control, the switching frequency of the inverter is kept at a constant value, which is slightly different from the primary resonant frequency to offer soft-switching operation. In order to control the power flow, the phase (phase shift control) or

the duty cycle of the inverter switches is varied [75,76]. This allows the inverters to produce output voltage/current with variable pulse width. The other way to regulate the power flow with the fixed switching frequency is controlling the input DC voltage of the inverter using a front-end DC–DC converter [48]. For the variable switching frequency control scheme, the duty cycle of the gating signals is maintained constant at 50% and the switching frequency is varied to regulate the output power [49]. However, if the operating frequency is largely different from the resonant frequency, the resonant tank will incur a large circulating current, causing an efficiency drop in the overall system owing to large losses in switches and the coils. Moreover, the bifurcation phenomenon must be carefully considered in this control technique [77]. In [36], a discrete energy injection control is used for the matrix buck converter in order to control the magnitude of the primary current. The control technique reduces the switching frequency and enables soft switching. However, the zero-crossing detection of primary high-frequency current that is required to ensure the converter to be operated in zero current switching (ZCS) conditions is an implementation challenge. Moreover, current sag occurs during the zero-crossing of its single-phase input voltage, which degrades the average power transferred. The dual-side control is suitable for bidirectional IPT systems where power flow can be regulated in both directions by controlling the duty cycle of the primary and secondary converters and the phase-shift between them [56,57,78]. Table 2 shows the compatibility of power conversion topologies and control schemes of the IPT applications.

## 4. Performance Comparison and Discussion

In this section, the performance of a conventional dual-stage topology and two potential single-stage topologies including buck- and boost-derived FBMCs are compared regarding input power quality, current stress, voltage stress, power losses, and cost.

### 4.1. Design Considerations

The conventional dual-stage IPT charging system is illustrated in Figure 7a. At the front end, a conventional boost rectifier is used to shape the grid current and maintain a constant DC voltage $V_{dc}$ across DC-link capacitor $C_i$. As a bulky and costly inductor is required for the CSIs, an FBVSI is the most common choice at the primary side to generate a high-frequency voltage ($v_p$) feeding the primary coil. A series-series (SS) compensation topology is used because it is simple and cost-effective, and its primary compensation is independent of the coupling coefficient and load. Moreover, the efficiency of SS compensation is high even at a low coupling coefficient [68,79]. In order to maximize the power transfer capabilities and minimize the VA rating of the primary inverter, the resonant circuits at both sides of the coupling are usually tuned to the same resonant frequency ($\omega_0$) equal to the switching frequency of the inverter.

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \tag{1}$$

where $L_p$ and $L_s$ are primary and secondary coil self-inductances, respectively, and $C_p$ and $C_s$ are primary and secondary tuning capacitors, respectively.

Power regulation is conducted using the phase-shift control at the primary inverter side. Considering an ideal IPT system operating at the resonance frequency ($\omega_0$), power transferred from the primary to the secondary side can be given by

$$P_o = \frac{8 V_{dc} V_b}{\pi^2 \omega_0 M} \sin \pi D_p \tag{2}$$

where $D_p$ is the duty cycle of the primary voltage ($v_p$) and $M$ is the mutual inductance and can be calculated as

$$M = k \sqrt{L_p L_s} \tag{3}$$
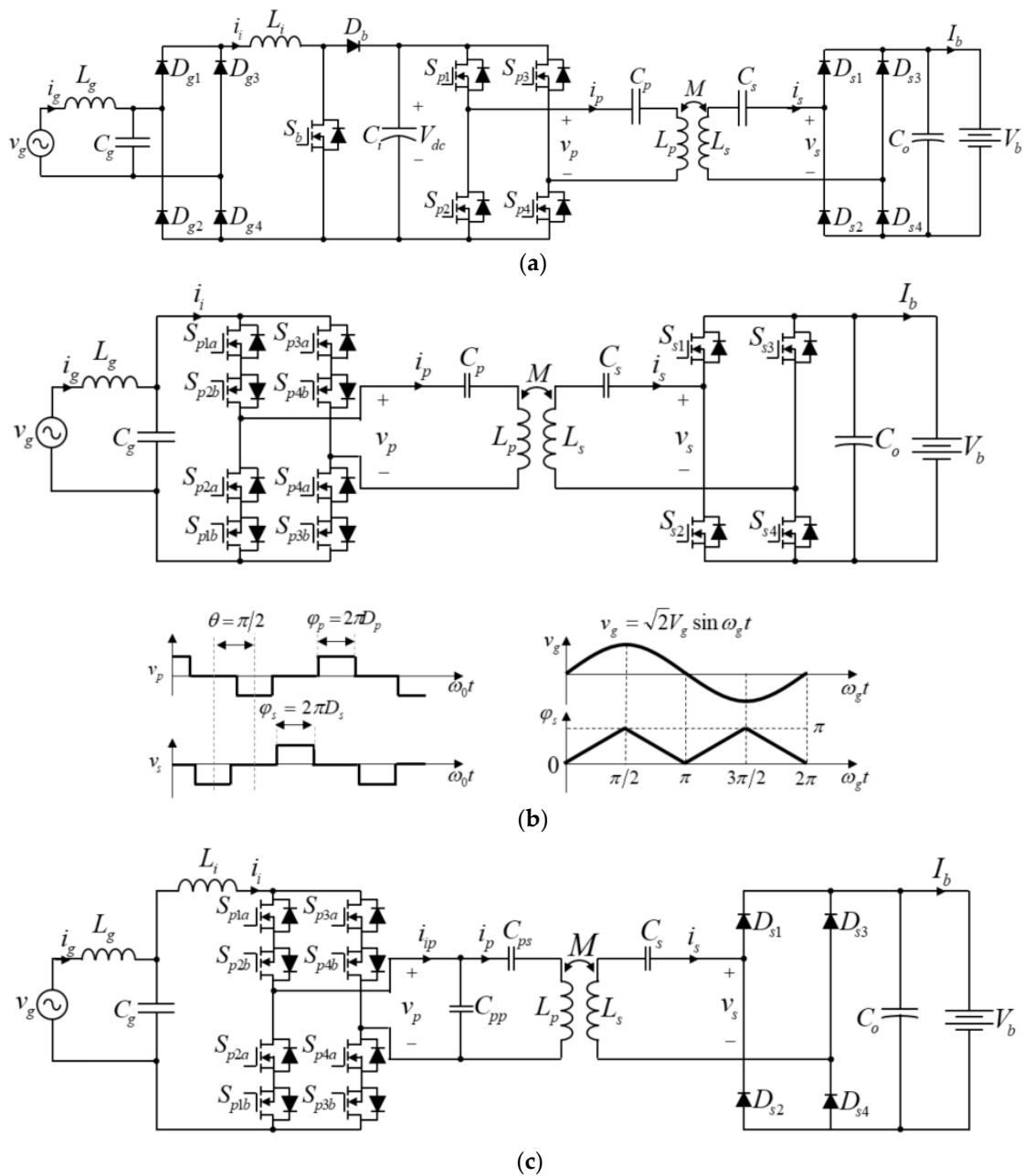
**Figure 7.** IPT charging system fed by (**a**) dual-stage power converter (PFC and full-bridge VSI), (**b**) buck-derived FBMC, and (**c**) boost-derived FBMC.

In EV wireless charging applications, the coupling coefficient *k* may be in the range of 0.1–0.3. In a dual-stage topology, the major drawback is low power density owing to multiple conversion stages and a bulky DC-link capacitor. The reduction of the number of power conversion stages can be obtained using MCs. Figure 7b shows the IPT charging system using a buck-derived FBMC. The FBMC constituted by four bidirectional switches can directly convert low frequency (50–60 Hz) grid voltage to resonant frequency (85 kHz) voltage feeding the inductive coil. During the positive half cycle of the grid voltage $v_g$, switches $S_{pnb}$ (*n* = 1, 2, 3, 4) are turned on and switches $S_{pna}$ are the phase-shift pulse-width modulation (PWM) strategy. Otherwise, during the negative half-cycle, the switches $S_{pna}$ are kept on and switches $S_{pnb}$ are controlled by the phase-shift PWM strategy.

An active rectifier is employed in the battery side for shaping the input current. The primary and secondary converters are synchronized in every switching cycle so that primary voltage $v_p$ is 90°

lagging with secondary voltage $v_s$, and the duty cycle of the secondary voltage is controlled following grid voltage waveform to correct input current, as shown in Figure 7b. The power transferred is controlled by adjusting the duty cycle of the primary voltage.

$$P_o = \frac{4\sqrt{2}V_g V_b}{\pi^2 \omega_0 M} \sin \pi D_p \tag{4}$$

where $V_g$ is the root mean square (RMS) value of the grid voltage.

Although the buck-derived FBMC-based IPT charging system removes the intermediate conversion stage, high-frequency communication is required to synchronize the PWM patterns of the primary and secondary converters in every switching cycle, which increases the control complexity. The boost-derived MC can solve the above issue. It is capable of correcting the grid current and regulating power flow through two control loops, which are similar to those of a conventional boost converter. Figure 7c shows an IPT topology fed by a boost-derived FBMC [38]. On the primary side, parallel-series *CC* compensation is used to reduce voltage stress on the MC switches. The tuning capacitor $C_{ps}$ is selected so as to limit the maximum peak of $v_p$ across the converter switches. It is desirable to restrict $v_p$ to 0.5~0.7 of the rating voltage of the switches [48]. The switching scheme and controller design for the boost-derived full-bridge matrix converter are described in [38]. Tables 3 and 4 show the passive component design and the switching stresses of the converter components.

**Table 3.** Passive component design. FB, full-bridge.

| Topologies | Components | Parameters | |
|---|---|---|---|
| Dual-stage [80] | Boost inductor $L_i$ | Inductance $L_i = \frac{1}{\%\Delta I_i} \frac{V_g^2}{P_{o(\max)} f_s}\left(1 - \frac{\sqrt{2}V_g}{V_{dc}}\right)$ | Peak current $\hat{I}_{Li} = \sqrt{2}\frac{P_o}{V_g} + \frac{\Delta I_i}{2}$ |
| | Boost capacitor $C_i$ | Capacitance $C_i = \frac{1}{\%\Delta V_{dc}} \frac{P_o}{\omega_g V_{dc}^2}$ | Peak voltage $\hat{V}_{Ci} = V_{dc} + \frac{\Delta V_{dc}}{2}$ |
| | Compensation capacitors $C_p$ and $C_s$ | Capacitance $C_p = \frac{1}{\omega_0^2 L_p}$ $C_s = \frac{1}{\omega_0^2 L_s}$ | Peak voltage $\hat{V}_{Cp} = \frac{4V_b}{\pi\omega_0^2 C_p M}$ $\hat{V}_{Cs} = \frac{4V_{dc}}{\pi\omega_0^2 C_s M}$ |
| Buck-derived FB MC [81,82] | Compensation capacitors $C_p$ and $C_s$ | Capacitance $C_p = \frac{1}{\omega_0^2 L_p}$ $C_s = \frac{1}{\omega_0^2 L_s}$ | Peak voltage $\hat{V}_{Cp} = \frac{4V_b}{\pi\omega_0^2 C_p M}$ $\hat{V}_{Cs} = \frac{4\sqrt{2}V_g}{\pi\omega_0^2 C_s M}$ |
| Boost-derived FB MC [38] | Boost inductor $L_i$ | Inductance $L_i = \frac{\sqrt{2}V_g}{2\Delta I_i f_s}$ | Peak current $\hat{I}_{Li} = \frac{\sqrt{2}P_o}{V_g} + \frac{\Delta I_i}{2}$ |
| | Compensation capacitors $C_{pp}$, $C_{ps}$, and $C_s$ **Note:** $C_{ps}$ is designed to limit the peak of primary voltage $v_p$, which is the voltage stress on MC switches. | Capacitance $C_s = \frac{1}{\omega_0^2 L_s}$ $C_{pp} = \frac{L_p - \frac{1}{\omega_0^2 C_{ps}}}{\frac{\omega_0^4 M^4}{R_{oeq}^2} + \omega_0^2\left(L_p - \frac{1}{\omega_0^2 C_{ps}}\right)^2}$ | Peak voltage $\hat{V}_{Cs} = \frac{\pi P_o}{\omega_0 C_s V_b}$ $\hat{V}_{Cpp} = \hat{V}_p = \sqrt{\left(\frac{4V_b}{\pi M}\right)^2\left(L_p - \frac{1}{\omega_0^2 C_{ps}}\right)^2 + \left(\frac{\pi\omega_0 M P_o}{V_b}\right)^2}$ $\hat{V}_{Cps} = \frac{4V_b}{\pi\omega_0^2 C_{ps} M}$ |

**Table 4.** Stress on switching devices.

| Topologies | Components | Current Stress | Voltage Stress |
|---|---|---|---|
| Dual-stage | Boost switch $S_b$ and diode $D_b$ | Peak current $\hat{I}_{Sb} = \hat{I}_{Db} = \frac{\sqrt{2}P_o}{V_g} + \frac{\Delta I_i}{2}$ | Break down voltage $\hat{V}_{Sb} = \hat{V}_{Db} > V_{dc} + \frac{\Delta V_{dc}}{2}$ |
| | Primary inverter switches $S_{pn}$ ($n = 1, 2, 3, 4$) | Peak current $\hat{I}_{Spn} = \frac{4V_b}{\pi\omega_0 M}$ | Break down voltage $\hat{V}_{Spn} > V_{dc} + \frac{\Delta V_{dc}}{2}$ |
| | Secondary rectifier diodes $D_{sn}$ ($n = 1, 2, 3, 4$) | Peak current $\hat{I}_{Dsn} = \frac{4V_{dc}}{\pi\omega_0 M}$ | Break down voltage $\hat{V}_{Dsn} > V_b$ |
| Buck-derived FB MC | Primary inverter switches $S_{pnx}$ ($n = 1, 2, 3, 4$ and $x = a, b$) | Peak current $\hat{I}_{Spnx} = \frac{4V_b}{\pi\omega_0 M}$ | Break down voltage $\hat{V}_{Spnx} > \sqrt{2}V_g$ |
| | Secondary rectifier switches $S_{sn}$ ($n = 1, 2, 3, 4$) | Peak current $\hat{I}_{Ssn} = \frac{4\sqrt{2}V_g}{\pi\omega_0 M}$ | Break down voltage $\hat{V}_{Ssn} > V_b$ |
| Boost-derived FB MC | Primary inverter switches $S_{pnx}$ ($n = 1, 2, 3, 4$ and $x = a, b$) | Peak current $\hat{I}_{Spnx} > \frac{\sqrt{2}P_o}{V_g} + \frac{\Delta I_i}{2}$ | Break down voltage $\hat{V}_{Spnx} > \hat{V}_p$ |
| | Secondary rectifier diodes $D_{sn}$ ($n = 1, 2, 3, 4$) | Peak current $\hat{I}_{Dsn} > \frac{\pi P_o}{V_b}$ | Break down voltage $\hat{V}_{Dsn} > V_b$ |

## 4.2. Performance Comparison

In this section, the performance of IPT configurations is compared in terms of input power factor, input current distortion, current stress, voltage stress, power losses on converters, and normalized cost. The IPT charging systems are designed in compliance with the level 1 (WPT1) of static wireless charging standard for light-duty vehicles provided in SAE J2954 technical information report [19] with power rating $P_o$ = 3.3 kW, operating frequency $f_s$ = 85 kHz, grid voltage $V_g$ = 208 V, and battery voltage $V_b$ = 300–400 V. The parameters of the charging system with each type of power conversion configuration are shown in Table 5. All the components are designed based on Tables 3 and 4. The selection of components is based on their maximum current and voltage stresses. Note that available discrete Rohm SiC MOSFETs and Schottky diodes are considered for all power conversion topologies. Moreover, *LC* filters are used as interfaces between the grid and the charging systems to limit current harmonic injection owing to the switching power converters. The *LC* filters are designed based on the spectrum analysis of the input current waveforms ($i_i$). The details of the selected components for different power conversion stages are listed in Table 6.

Figure 8 shows the typical waveforms of IPT charging systems with different power supply topologies. It can be seen that the absence of DC-link energy storage in MC-based topologies causes a double line frequency fluctuation in transferred power. This results in a fluctuating charging current as shown in Figure 8b and c. As reported in [40–44,83,84], batteries can be charged by double line frequency (100 or 120 Hz) current with negligible side effects on their performance.

**Table 5.** Specifications of IPT charging systems.

| Topologies | Parameter | Symbol | Value | Unit |
|---|---|---|---|---|
| Dual-stage | Primary, secondary, mutual inductance | $L_p, L_s, M$ | 356, 328, 65 | μH |
| | Compensation capacitors | $C_p, C_s$ | 10, 11 | nF |
| | Boost inductor | $L_i$ | 0.215 | mH |
| | DC-bus capacitor | $C_i$ | 1540 | μF |
| | DC-bus voltage | $V_{dc}$ | 400 | V |
| | Grid inductor | $L_g$ | 0.215 | mH |
| | Grid capacitor | $C_g$ | 0.78 | μF |
| | Output capacitor | $C_o$ | 500 | μF |
| Buck-derived FBMC | Primary, secondary, mutual inductance | $L_p, L_s, M$ | 111, 111, 24 | μH |
| | Compensation capacitors | $C_p, C_s$ | 32, 32 | nF |
| | Grid inductor | $L_g$ | 0.215 | mH |
| | Grid capacitor | $C_g$ | 0.78 | μF |
| | Output capacitor | $C_o$ | 500 | μF |
| Boost-derived FBMC | Primary, secondary, mutual inductance | $L_p, L_s, M$ | 111, 111, 24 | μH |
| | Compensation capacitors | $C_{ps}, C_{pp}, C_s$ | 43, 115, 32 | nF |
| | Boost inductor | $L_i$ | 0.215 | mH |
| | Grid inductor | $L_g$ | 0.036 | mH |
| | Grid capacitor | $C_g$ | 0.136 | μF |
| | Output capacitor | $C_o$ | 500 | μF |

**Table 6.** Main components of power conversion stages.

| Topologies | Components | Symbol | Part Number | Quantity |
|---|---|---|---|---|
| Dual-stage | Front-end rectifier diodes | $D_{gn}$ * | SCS240AE2C-ND | 4 |
| | Boost diode | $D_b$ | SCS240AE2C-ND | 1 |
| | Boost switch | $S_b$ | SCT3060ALGC11-ND | 1 |
| | Primary inverter switches | $S_{pn}$ * | SCT3120ALHRC11-ND | 4 |
| | Secondary rectifier diodes | $D_{sn}$ * | SCS230AE2HRC-ND | 4 |
| | Boost inductor | $L_i$ | HF5712-561M-25AH | 2 parallel |
| | DC-bus capacitor | $C_i$ | LGN2X221MELC50 | 7 parallel |
| | Grid inductor | $L_g$ | HF5712-561M-25AH | 2 parallel |
| | Grid capacitor | $C_g$ | B32656T7394K000 | 2 parallel |
| Buck-derived FBMC | Primary MC switches | $S_{pna}, S_{pnb}$ * | SCT3030ALGC11-ND | 8 |
| | Secondary rectifier diodes | $S_{sn}$ * | SCT3060ALGC11-ND | 4 |
| | Grid inductor | $L_g$ | HF5712-561M-25AH | 2 parallel |
| | Grid capacitor | $C_g$ | B32656T7394K000 | 2 parallel |
| Boost-derived FBMC | Primary MC switches | $S_{pna}, S_{pnb}$ * | SCT2080KEC-ND | 8 |
| | Secondary rectifier diodes | $D_{sn}$ * | SCS240AE2C-ND | 4 |
| | Boost inductor | $L_i$ | HF5712-561M-25AH | 2 parallel |
| | Grid inductor | $L_g$ | HF467-980M-25AV | 2 parallel |
| | Grid capacitor | $C_g$ | B32654A1683K000 | 2 parallel |

*$n$ = 1, 2, 3, 4.
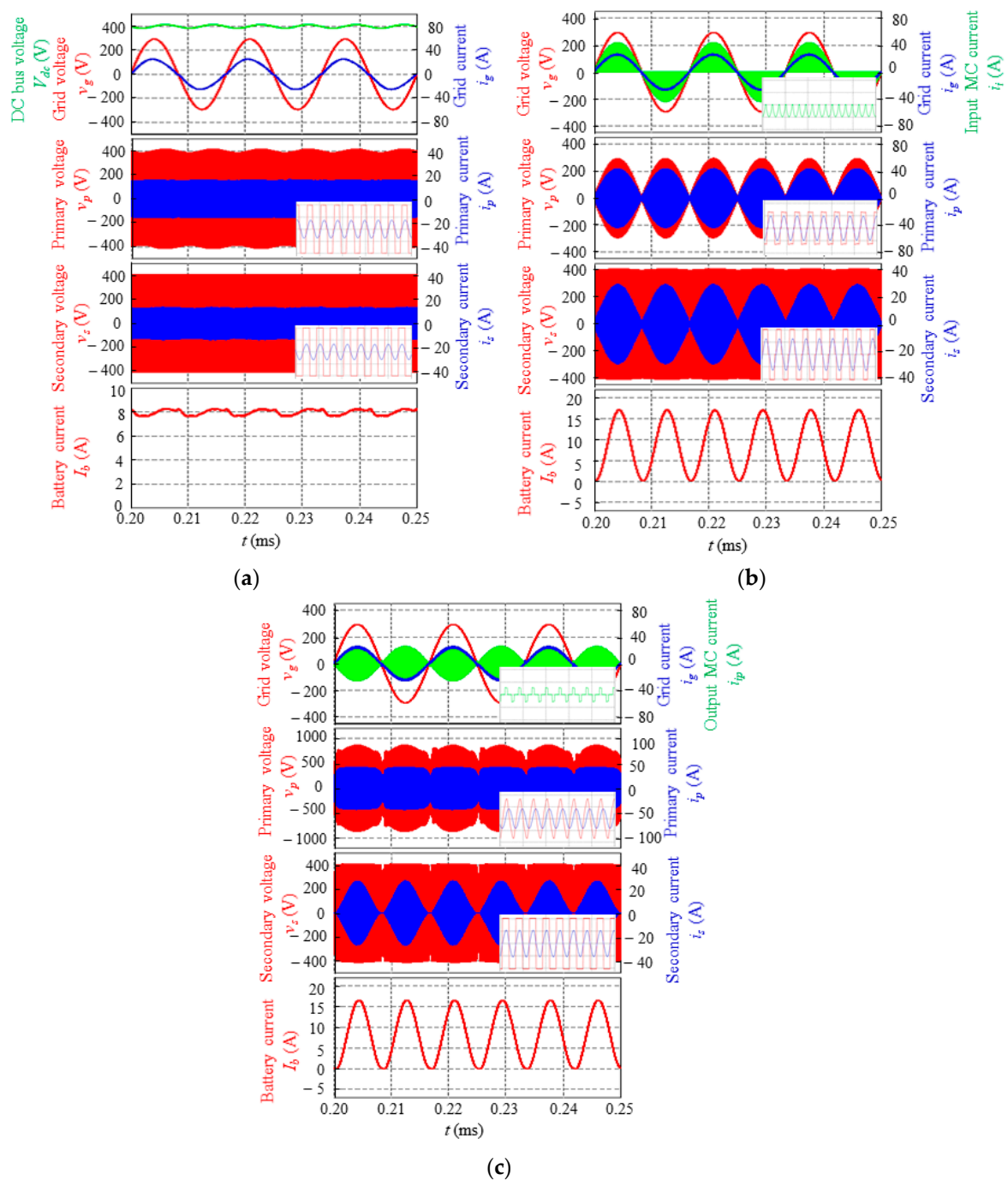
**Figure 8.** Simulation waveforms of IPT charging systems fed by (**a**) dual-stage power converter (PFC and full-bridge VSI), (**b**) buck-derived FBMC, and (**c**) boost-derived FBMC.

### 4.2.1. Input Power Factor and Input Current Distortion

An EV charger must ensure a good grid power quality with a high power factor and low current distortion. All three topologies provide sinusoidal grid currents with the power factor of 0.99. Figure 9a shows total harmonic distortion (THD) of the grid current under different load conditions (20%, 50%, and 100% of load). It can be seen that the three topologies can be preferred in order of boost-derived FBMC, dual-stage converter, and buck-derived FBMC, regarding grid current distortion. Despite having the identical input *LC* filter, the buck-derived FBMC injects higher current harmonics to the grid than dual-stage topology, because its input current is discontinuous. The boost-derived FBMC has

the continuous input current with ripple frequency at a twofold switching frequency, thereby gaining the significant harmonic reduction of grid current with a smaller input filter.
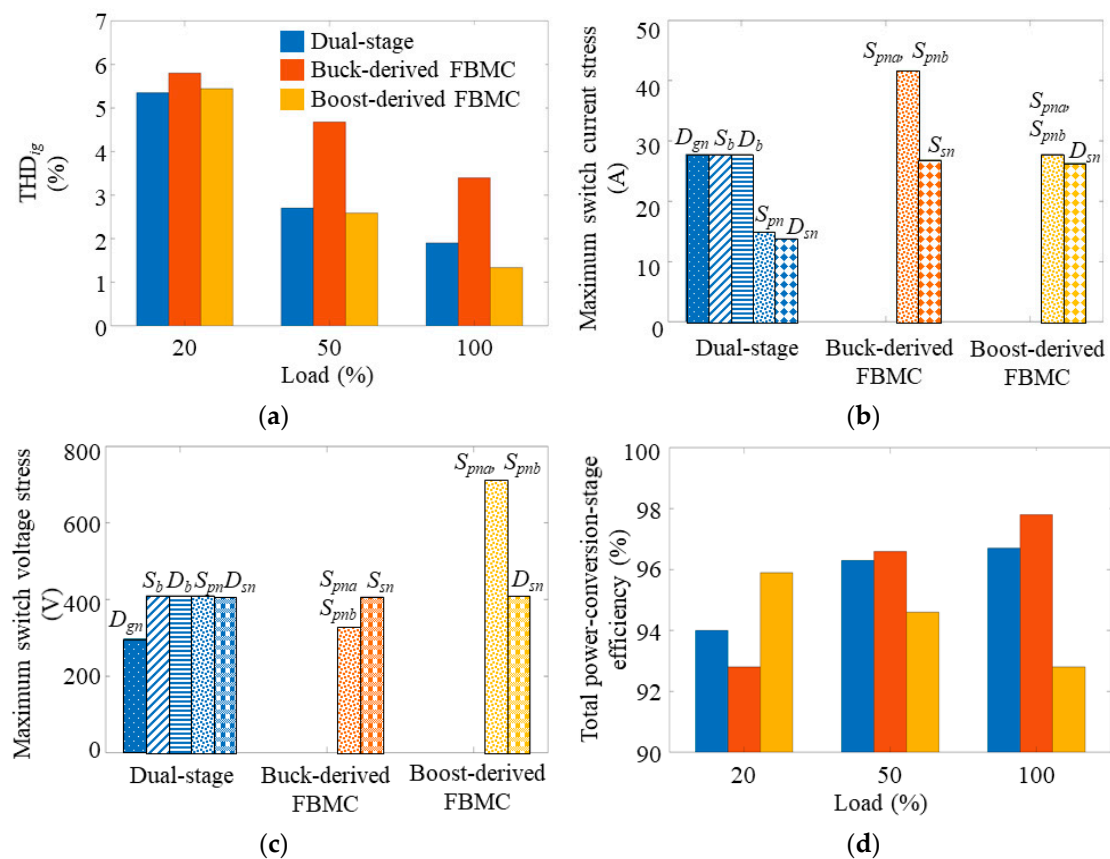


**Figure 9.** Performance comparison of three IPT charging systems: (**a**) grid current total harmonic distortion (THD), (**b**) switch current stress, (**c**) switch voltage stress, and (**d**) power-conversion-stage efficiency.

### 4.2.2. Switching Stress

Figure 9b and c show the maximum current and voltage stress on the converter switches. Although the parallel-series *CC* compensation is used, the switches of boost-derived FBMC still suffer from high voltage stress. The buck-derived FBMC is characterized by low switch voltage stress (grid voltage peak) and high switch current stress. The dual-stage topology exhibits the lowest switch current stress in the primary inverter and secondary rectifier.

### 4.2.3. Efficiency and Loss Distribution

The losses on the conversion stages of each system are simulated and analyzed using the thermal modules in PSIM simulation. The efficiency of the power conversion stages of each system versus various output power is illustrated in Figure 9d. It is clear that the efficiency of the buck-derived FBMC system is the highest (almost 98%) at full load conditions, but it decreases gradually to 93% at the light load conditions. In contrast, the efficiency of the boost-derived FBMC system steadily increases from 92.5% to 96% when the load decreases from 100% to 20%. The dual-stage system maintains fairly high efficiency (94~96.5%) in a wide load range.

The detailed loss distribution of the three systems is shown in Figure 10. It can be observed that the conduction losses of primary converters dominate the total losses of power conversion stages. In the dual-stage system, the conduction losses of the front-end rectifier and the primary inverter are the

two major parts. For the single-stage systems, the conduction losses of matrix converters contribute to the largest proportions (>60%).
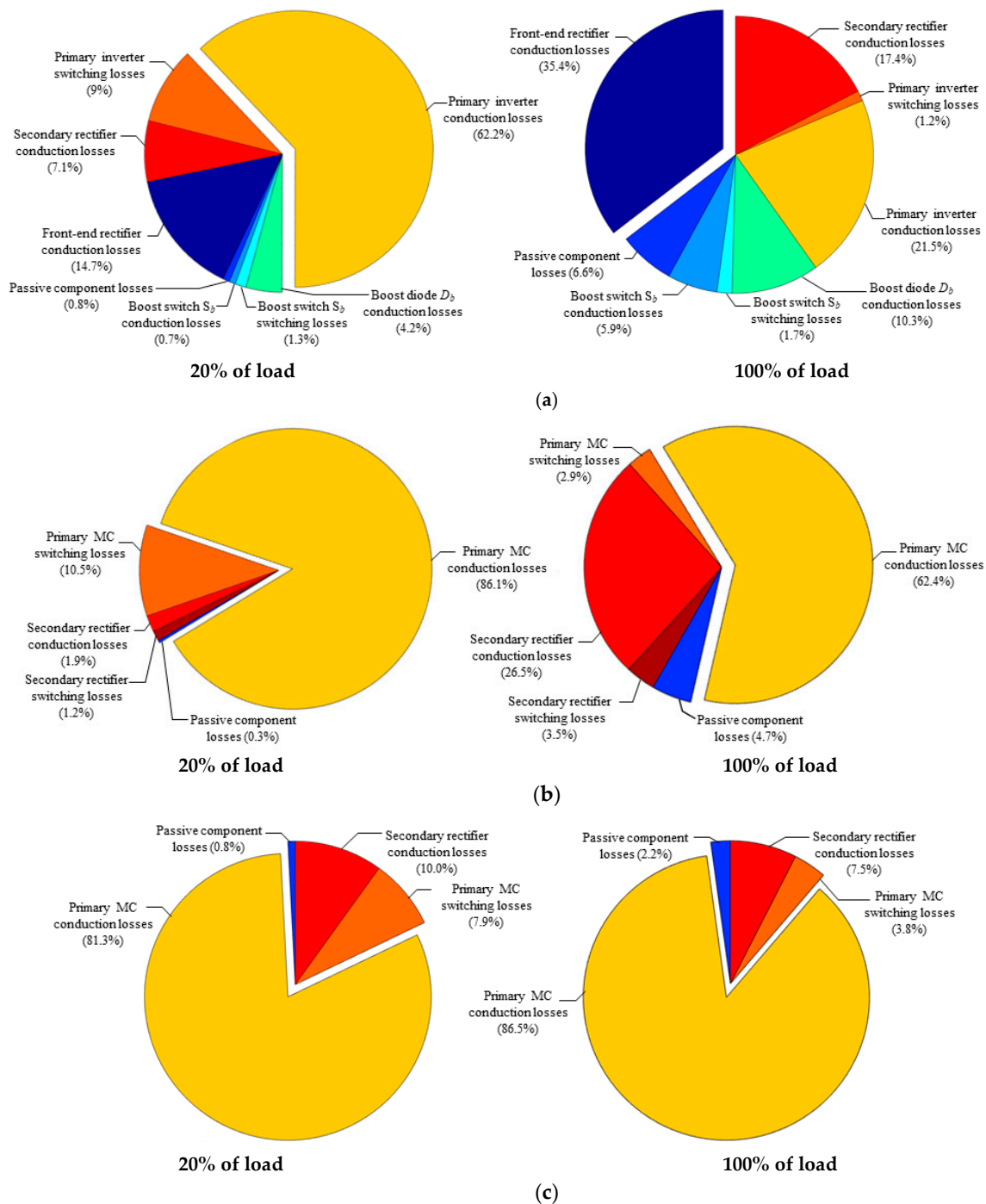


**Figure 10.** Loss distribution: (**a**) dual-stage topology, (**b**) buck-derived FBMC, and (**c**) boost-derived FBMC.

### 4.2.4. Cost

Cost is also an important quantity to evaluate the performance of a power converter. The cost structure of each charging system excluding inductive coupling coils and compensation networks is illustrated in Figure 11. The costs of the power conversion stages are calculated based on the component cost provided in Table 7. In order to simplify the cost analysis, the auxiliary cost including

printed circuit board (PCB) cost, cooling system cost, and housing cost is assumed to be 10% of the power converter cost. Note that MOSFETs are driven by isolated gate drivers, and MOSFETs having common-source connection utilize a common gate driver power supply to reduce the system cost. This shows that the cost of single-stage systems is lower than that of the dual-stage counterpart. The buck-derived FBMC system is the most cost-effective solution, as it presents 8.4% less cost than the dual-stage system. It is found that the costs of the passive components dominate in the dual-stage system, whereas the semiconductor devices of matrix converters occupy the largest portions in the total cost of the single-stage systems.
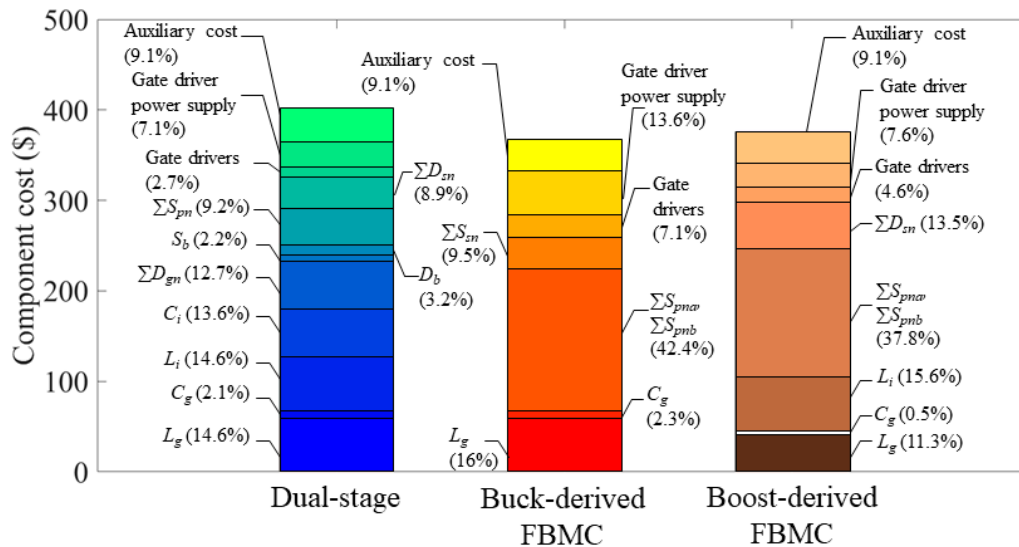


**Figure 11.** Component cost structure of the charging system excluding inductive coupling coils and compensation networks.

**Table 7.** Cost of components.

| Components | Manufacturer Part Number | Rating | Unit Cost ($) |
|---|---|---|---|
| Diode | SCS230AE2HRC-ND | 650 V/30 A | 8.97 |
| | SCS240AE2C-ND | 650 V/40 A | 12.75 |
| MOSFET | SCT3120ALHRC11-ND | 650 V/21 A | 9.27 |
| | SCT3060ALGC11-ND | 650 V/39 A | 8.74 |
| | SCT3030ALGC11-ND | 650 V/70 A | 19.46 |
| | SCT2080KEC-ND | 1200 V/40 A | 17.77 |
| Gate driver IC | UCC5390SCD | N/A | 2.16 |
| Gate driver supply | R12P21503D | +15 V/−3 V/2 W | 7.11 |
| Inductor | HF467-980M-25AV | 25 A/72 μH | 21.15 |
| | HF5712-561M-25AH | 25 A/430 μH | 29.25 |
| Capacitor | LGN2X221MELC50 (Electrolytic) | 600 V/220 μF | 7.78 |
| | B32656T7394K000 (Film) | 500 V/0.39 μF | 4.23 |
| | B32654A1683K000 | 500 V/0.068 μF | 1.01 |

*4.3. Discussions*

From the above analysis, it can be observed that the three IPT charging systems have their own advantages and disadvantages. A comparison summary of the three IPT charging systems is shown in Figure 12, where performance indices are presented in a scale range from 1 (worst) to 3 (best). In order to evaluate the efficiencies of the three systems, their average values under all load conditions are considered. The switching stresses are assessed based on the product of the maximum current

and voltage stresses. Figure 12 shows that the buck-derived FBMC surpasses the other counterparts with the advantages of high efficiency, cost reduction and possible power density improvement due to less component count, while the boost-derived FBMC has the greatest input current quality due to the feature of the continuous input current with ripple frequency at a twice switching frequency. The conventional dual-stage topology has the lowest stress on switching devices, and its efficiency maintains a comparable high level over wide load range. Moreover, the dual-stage converter topology is highly matured in terms of manufacturability and control as it has been developed by many manufacturers and widely used in the industry. Also, this topology allows each converter stage to be separately designed and optimized.
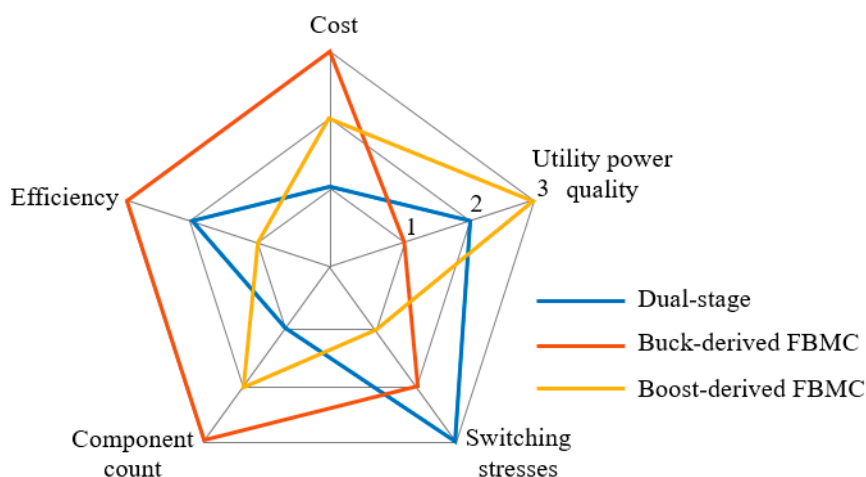


**Figure 12.** Comparison summary of the dual-stage and single-stage IPT charging systems.

## 5. Future Trends and Opportunities

Over the past decade, there have been significant developments in power converter topologies and control schemes for EV IPT charging. One of the important challenges is the design of high-frequency power converters for IPT to meet future requirements. Still, there is a lot of scope for further improvements to enhance the performance in terms of efficiency, power density, scalability, and reliability to promote the IPT-based systems for EV charging. Reducing power losses in power conversion from the source to the input of the coil is a vital factor in improving efficiency. One of such initiatives is to develop advanced soft-switching modulation techniques for the existing converter topologies and new reduced-switch-count converter topologies to reduce switching losses. This is expected to improve the thermal design and power density of the overall system. Several soft-switching control schemes have been reported in the literature. Generally, they can be divided into three groups: with auxiliary DC-DC converters [85–87], with variable resonant networks [88,89], and with active inverter/rectifier control [59,90–92]. However, the proposed control schemes require extra DC-DC converters or resonant components, or have an operation range limitation and high control complexity.

Direct power conversion topologies such as matrix converters can be one of the possible candidates with the elimination of life-limited bulky DC capacitors employing enhanced charging techniques like SRC charging. Another important performance enhancement is employing wide bandgap devices in the existing converter topologies or development of advanced topologies, which can operate at higher switching frequencies with low switching losses [93]. This can boost the performance of power converters in the wireless charging applications [94]. The application of gallium nitride (GaN) in IPT systems has opened up a new scope in improvement in power transfer and power density. These devices have a low voltage drop, ability to operate at the higher switching frequency, and comparatively lower thermal generation during operation, which allows for passive cooling to increase the converter power density and cost-effectiveness [95]. However, some challenges regarding the manufacturing process, packaging with higher current ratings, the gate driver design, device characterization, busbar

layout, thermal management, and reliability need to be addressed. Therefore, much more research initiatives in the aforementioned issues could decide the power density of the converter. In addition, employing the GaN devices allows an increase in switching frequencies even at higher current standards, which improves the performance of WPT, such as transfer distance extension, higher tolerance to coil misalignment, and passive component size reduction. Furthermore, the magnetic integration can be used to integrate magnetic components of power converters, compensation networks, and coupling coils, in turn, to enhance using higher flux density material to reduce the system size and losses. One of the possible ways is the utilization of advanced materials and nanotechnology to reduce the size and weight of passive components.

In the recent days, modular power converters with fault-tolerance are demanded due to industrial requirements such as flexibility in assembly, manufacturing process, scalability and reduced mean time to failure (MTTF). Some of the possible potential candidates are multiphase parallel inverter [96], modular multilevel converter [97], parallel IPT power supply topologies [98] and extreme fast charging architectures [99] to improve the output power capability and fault tolerance for WPT systems, which can open up more research in developing advanced power topologies and fault-tolerant control schemes. Other stimulating research areas for developing technology are bidirectional power flow, integration with hybrid energy storage systems and multiple energy sources [100]. However, these areas are still under research that further attention and investigation for developing advanced multi-port converter topologies and newly advanced control schemes must comply with future charging standards to promote IPT systems for EV charging applications.

## 6. Conclusions

This paper presents an extensive overview of power conversion topologies and control schemes for IPT-based EV charging applications. The design considerations and performance evaluation of the conventional dual-stage topology and two potential single-stage topologies including buck- and boost-derived FBMCs were discussed. It is concluded that the conventional dual-stage topology has the lowest stress on switching devices, and the boost-derived FBMC provides the greatest input current quality. On the other hand, the superiorities of the buck-derived FBMC over the other topologies are high efficiency, low component count and cost. However, further investigation on IPT-based charging systems is needed including scalability to higher power levels, adoption of soft-switching technology, fault-tolerability technology, active power decoupling methods, magnetic integration, green energy based-IPT systems, multi-mode operation systems, wide bandgap device technology, high-performance advanced and non-invasive control schemes. With the continual improvements and the aforementioned advancements, IPT-based systems will definitely increase the availability and economic viability of the EVs in the near future.

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