Adaptive On-Time Buck Converter with Wave Tracking Reference Control for Output Regulation Accuracy

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Abstract: A ripple-based constant on-time (RBCOT) buck converter with a virtual inductor current ripple (VICR) control can relax the stability constraint of large equivalent series resistance (ESR) at an output capacitor, but output regulation accuracy deteriorates due to the issue with output DC offset. Thus, this paper proposes a wave tracking reference (WTR) control to improve converter stability with low ESR and concurrently eliminate output DC offset on the regulated output voltage. Moreover, an adaptive on-time (AOT) circuit is presented to suppress the switching frequency variation with load current changes in continuous conduction mode. A prototype chip was fabricated in 0.35 μm CMOS technology for validation. The measurement results demonstrate that the maximum output DC offset is 4.1 mV and the output voltage ripple is as small as 3 mV. Furthermore, the switching frequency variation with the AOT circuit is 11 kHz when load current changes from 50 mA to 500 mA, and the measured maximum efficiency is 90.9% for the maximum output power of 900 mW.

Keywords: constant on-time; output DC offset; efficiency; buck converter

1. Introduction

With the rapid development of the Internet of things (IoT), high-performance power management integrated circuits are in great demand. Since small size, low cost, and long service time are desired for consumer electronics, the properties of DC–DC switching converters should meet the requirements such as minimal number of external components, high conversion efficiency, and small chip area of their control circuits. The peak current mode control is widely used in DC–DC converters due to the advantages of constant switching frequency, input voltage feedforward property, and automatic over-current protection [1]. However, frequency compensation is needed for the peak current mode control to ensure the stability of the DC–DC converter. Not only are compensation components needed but the transient response of the DC–DC converter is also restricted. In recent years, a ripple-based constant on-time (RBCOT) control scheme for buck converters, as shown in Figure 1, has received wide attention because of its simple structure, good light-load efficiency, and fast load transient response [2–7].

Due to low cost, small size, long lifetime, small variation of quality at different frequencies, and high temperature limit, the multilayer ceramic capacitor (MLCC) is widely used in buck converters. However, the RBCOT control requires an output capacitor with large equivalent-series resistance (ESR) to meet stability criteria, whereby the product of the output capacitance and its ESR should be larger than half of the on-time period [8–10]. Thus, the low ESR of an MLCC would cause instability of the RBCOT buck converter. Due to valley voltage operation, the RBCOT buck converter suffers from the DC offset issue on the regulated output voltage [11,12]. The output DC offset is proportional to the output voltage ripple.

To alleviate the instability issue with low ESR of a capacitor, a virtual inductor current ripple (VICR) control method was presented [8–16]. Since the VICR control adds an additional signal of inductor current ripple into the output feedback path, the stability

constraint on large ESR can be relaxed. However, the VICR control enlarges output DC offset due to the additional signal. To fulfill the VICR control, two low-pass filters are needed, as shown in the part B of Section 2 in [8]. The low-pass filters occupy a significant chip area; hence, this method may be inappropriate for integrated circuit design. To reduce the output DC offset issue caused by the VICR control, the pseudowave tracking method is presented [9]. The valley detector is used to sense the valley voltage of the sensed inductor current. Then, through the dual differential amplifier, the output feedback signal becomes the valley voltage of the summation signal. Thus, the output DC offset issue is removed. Nevertheless, an inductor current sensor, a trimming mechanism, and an LPF in valley detector are needed; thus, the design difficulty and silicon area are increased. A current-mode on-time controlled buck converter is presented to solve the low ESR issue [15,16]. However, an error amplifier and off-chip compensation components are required, thereby increasing the size and cost of the converter.
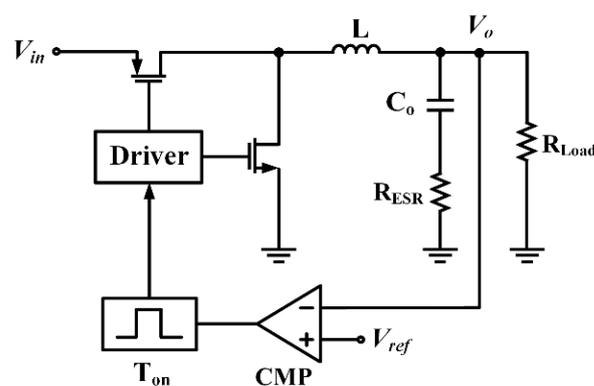
Figure 1. Conventional ripple-based constant on-time (RBCOT) buck converter.

Due to ripple-based control scheme, the RBCOT buck converter is a clock-free architecture. Its switching frequency varies when the input voltage, output voltage, and load current are changed [15,17,18]. This improves the power efficiency of the RBCOT converter at light load, but this control is prone to electromagnetic interference (EMI) issues. Analog circuits such as radiofrequency circuits, digital-to-analog converters, analog-to-digital converters, and audio systems are sensitive to switching frequency interference because frequency variation can degrade their performance. Therefore, switching frequency variation of the RBCOT buck converter is required to be constrained to enhance the system performance. Several previous studies proposed techniques to alleviate the variation of switching frequency. Although a phase-locked loop can be employed in the COT control to lock switching frequency at a predefined value [2,19,20], additional complicated circuits and components are required to increases silicon area and cost. References [15,21] used the information of input voltage and output voltage to adjust on-time period to maintain constant switching frequency. However, switching frequency still varied with different load currents. Moreover, a previous study adopted the output signal of its error amplifier to keep constant switching frequency [16]. Nevertheless, the relationship among the on resistance of the high-side power transistor, direct current resistance (DCR) of the inductor, and two resistances used in a current sensor should be constrained [16]; therefore, the design difficulty is increased. Another method applied a current sensor and load current corrector to revise the on-time period [12], but the reduction in switching frequency variation was insignificant.

This paper proposes a wave tracking reference (WTR) control for the low ESR of an MLCC to improve system stability and concurrently eliminate output DC offset. Since the circuit of the WTR control is implemented in an integrated circuit (IC) without any low-pass filter, trimming mechanism, or off-chip component, the chip area can be reduced with no additional IC pin. Furthermore, an adaptive on-time (AOT) circuit is presented to minimize the switching frequency variation of buck converter in case of load current

changes. The design of the proposed AOT circuit is simple and results in low power consumption. Hence, by employing the VICR control and AOT circuit, the chip area and EMI issue can be reduced significantly while the output regulation accuracy is improved. The remainder of this paper is organized as follows. Section 2 discusses the output DC offset and frequency variation analysis in the RBCOT buck converter. The proposed AOT buck converter with WTR control and the implementation of crucial control circuits are illustrated in Section 3. Section 4 shows the experimental results. Lastly, a conclusion is given in Section 5.

2. Output DC Offset and Frequency Variation Analysis in RBCOT Buck Converter
2.1. DC Offset on Regulated Output Voltage

A schematic of RBCOT buck converter with a VICR control is shown in Figure 2. There are two LPFs in the VICR control. LPF_1 and LPF_2 are used to obtain the inductor current signal V_{sen} and its average value $V_{sen,dc}$, respectively. By performing subtraction, a sensing ripple signal $V_{sen,rip}$ can be obtained. Signal V_{sum} is the summation of $V_{sen,rip}$ and output feedback signal V_{fb}, and it can be expressed as

$$V_{sum} = K_1 V_o + K_2(V_{sen} - V_{sen,dc}),$$ (1)

where K_2 is the gain of the VICR control, and K_1 is the feedback gain. According to the valley voltage operation of the RBCOT control, the valley voltage $V_{sum,valley}$ is shown as

$$V_{sum,valley} = V_{ref} = V_{fb} - \frac{V_{sen,rip}}{2}.$$ (2)
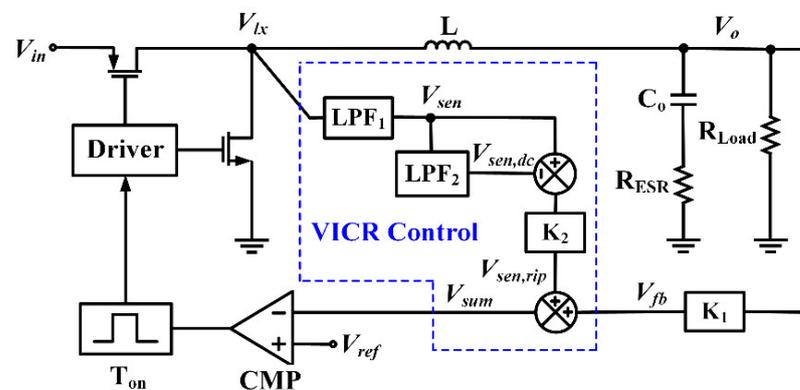
Figure 2. RBCOT buck converter with virtual inductor current ripple (VICR) control.

From Equation (2), V_o can be formulated as follows:

$$V_o = \frac{V_{fb}}{K_1} = \frac{1}{K_1}\left(V_{ref} + \frac{V_{sen,rip}}{2}\right) = \frac{1}{K_1}V_{ref} + V_{offset}.$$ (3)

The output DC offset can be defined as

$$V_{offset} = \frac{V_{sen,rip}}{2K_1} = \frac{K_2(V_{sen} - V_{sen,dc})}{2K_1}.$$ (4)

According to Equation (4), when considering the stability issue, K_2 should be adequately large to obtain a sufficiently large $V_{sen,rip}$, but the regulation accuracy of output voltage deteriorates due to undesired deviation from V_{ref}. Hence, there is a tradeoff between stability and output regulation accuracy. Furthermore, the output DC offset depends on input voltage, output voltage, output inductor, output capacitor, and switching frequency. Reference [8] presented a cancellation circuit to alleviate the output DC offset

issue; however, one LPF, one adder, and one subtractor are required, resulting in a higher chip area.

2.2. Frequency Variation Analysis

To analyze the variation in switching frequency, parasitic resistances are considered in the power stage of buck converter, as shown in Figure 3. The parasitic resistances include on-resistances $R_{N,on}$ and $R_{P,on}$ of power transistors M_N and M_P, respectively, and DC resistance R_{DCR} of the inductor. According to the principle of inductor voltage second balance, when M_P and M_N are turned on, the peak-to-peak inductor current ripple can be formulated as follows:

$$\Delta i_{L,ON} = [V_{in} - I_{Load}(R_{P,on} + R_{DCR}) - V_o]\frac{DT}{L} \text{ when } M_P \text{ is on,} \tag{5}$$

$$\Delta i_{L,OFF} = [-I_{Load}(R_{N,on} + R_{DCR}) - V_o]\frac{(1-D)T}{L} \text{ when } M_N \text{ is on.} \tag{6}$$
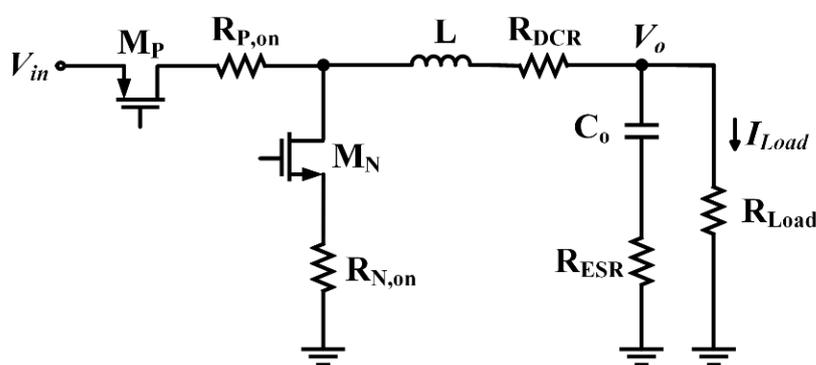
Figure 3. Power stage of buck converter including parasitic resistance.

Equations (5) and (6) show that the voltage across the inductor is affected by the parasitic resistances. In a steady state, the summation of Equations (5) and (6) is equal to zero. Then, the duty cycle can be expressed as

$$D = \frac{V_o + I_{Load}(R_{N,on} + R_{DCR})}{V_{in} + I_{Load}(R_{N,on} - R_{P,on})}. \tag{7}$$

Since switching frequency f_{sw} of buck converter in continuous conduction mode (CCM) is equal to duty cycle divided by turn-on time, f_{sw} can be derived as

$$f_{sw} = \frac{V_o + I_{Load}(R_{N,on} + R_{DCR})}{V_{in} + I_{Load}(R_{N,on} - R_{P,on})} \cdot \frac{1}{T_{ON}}. \tag{8}$$

Equation (8) reveals that f_{sw} suffers from variation under different load currents in CCM even if V_{in} and V_o are fixed. On the other hand, a larger load current requires a higher switching frequency.

3. Adaptive On-Time Buck Converter with the Wave Tracking Reference Control

The block diagram of adaptive on-time (AOT) buck converter with the wave tracking reference (WTR) control is illustrated in Figure 4. To solve the aforementioned issue, the WTR control is proposed to improve converter stability and concurrently eliminate output DC offset. Therefore, the low ESR of an MLCC can be used, and small output voltage ripple in a steady state is achieved in this work. The AOT circuit is employed to suppress the switching frequency variation of the buck converter operating in CCM in case of load current changes.
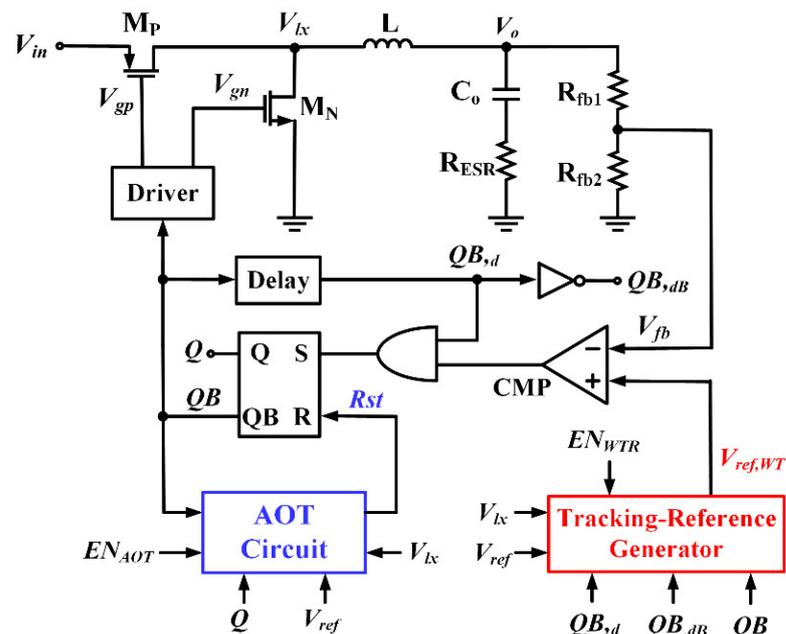
Figure 4. Block diagram of adaptive on-time (AOT) buck converter with wave tracking reference (WTR) control.

The scale-down output feedback signal V_{fb} is compared with the WTR signal $V_{ref,WT}$ produced by the tracking reference generator. When V_{fb} is smaller than $V_{ref,WT}$, the comparator output exists in a high state. At this instant, signal QB_d is in a high state, and terminal S of the SR latch also exists in a high state. Subsequently, power transistors M_P and M_N are turned on and off, respectively, and the on-time period of M_P is determined by the AOT circuit. The gate driver with dead time function is applied to provide sufficient driving capability and prevent shoot-through current. During the on-time period, the inductor current increases. At the end of the on-time period, signal Rst is set to a high state, and then the input voltage V_{in} stops charging the output inductor. When V_{fb} is lower than $V_{ref,WT}$, M_P is turned on again.

3.1. Wave Tracking Reference (WTR) Control

Figures 5 and 6 illustrate the concept of the VICR and WTR controls for the RBCOT buck converter. Assuming the ESR of a capacitor is sufficiently small, the ripple of V_{fb} is ignored. For the VICR control, $V_{sen,rip}$ is added to V_{fb}. Because the average value of $V_{sen,rip}$ is zero, for signal V_{sum}, there is a 0.5 $V_{sen,rip}$ difference between V_{ref} and V_{fb}. Thus, the VICR control causes the output DC offset, as shown in Equation (4). In Figure 6, by subtracting ripple signal $V_{rip,new}$ from the reference signal V_{ref}, system stability of the WTR control can be ensured. When the valley voltage of $V_{rip,new}$ is set to zero, the output DC offset is eliminated due to V_{fb} and V_{ref} being identical. When power transistor M_P is turned on, its on-time period is controlled by the AOT circuit. M_P is turned on again when V_{fb} is lower than $V_{ref,WT}$, and this instant happens during the off-time period. Thus, $V_{rip,new}$ requires information about the inductor current ripple only during the off-time period. As a result, the implementation complexity and power consumption of a sensing circuit can be reduced significantly. From Figure 6, $V_{ref,WT}$ is shown as

$$V_{ref,WT} = V_{ref} - V_{rip,new}. \tag{9}$$

On the basis of the WTR control, the peak voltage $V_{ref,WT,peak}$ is expressed as

$$V_{ref,WT,peak} = V_{ref} = V_{fb}. \tag{10}$$
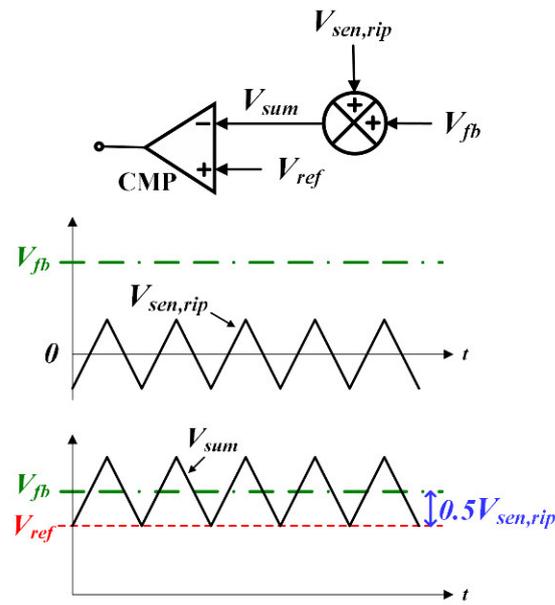
Figure 5. Concept of VICR control.
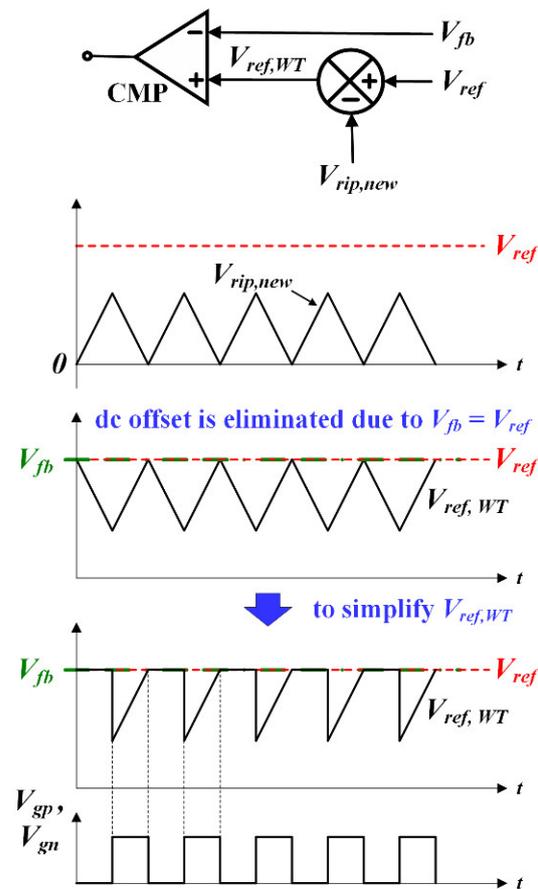
Figure 6. Concept of WTR control.

From Equation (10), the output voltage can be derived as

$$V_o = \frac{1}{K_1} V_{fb} = \frac{1}{K_1} V_{ref}, \tag{11}$$

where $K_1 = R_{fb2}/(R_{fb1} + R_{fb2})$. Similar to the VICR control, $V_{rip,new}$ should be set adequately large to ensure the system stability with WTR control. In contrast, the output DC offset with the WTR control is eliminated because V_{fb} is equal to V_{ref}. As a result, the WTR control can concurrently improve DC accuracy and stability in an AOT controlled buck converter with low ESR.

3.2. Implementation of WTR Control

To implement the WTR control, a tracking reference generator is proposed, and its schematic and operation waveforms are illustrated in Figure 7. When power transistor M_N is turned on, transistor M_{N5} also turns on. During the off-time period, the source voltage of M_{N5} is set to zero due to the negative feedback composed of operational amplifier OP_2 and transistor M_{P6}. Since the gate, source, and drain voltages of M_N and M_{N5} are the same, the sensing current I_{sen} is produced by M_{N5}, and its value is proportional to the aspect ratio of M_{N5} to M_N.
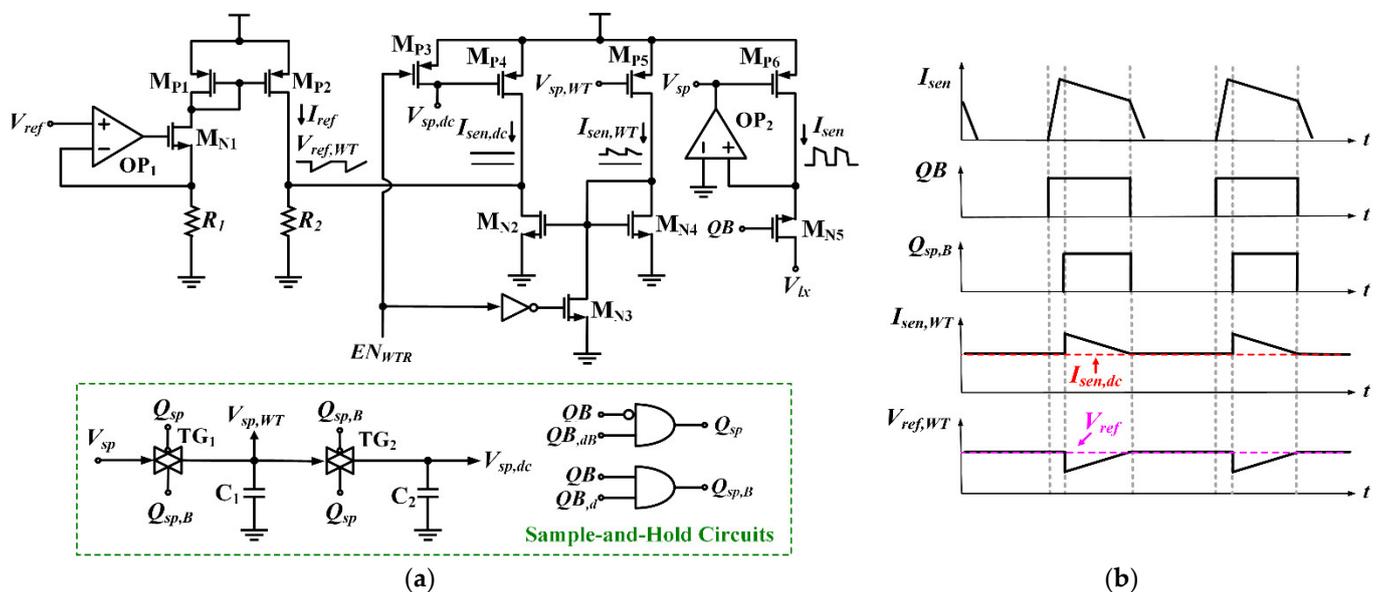
Figure 7. (**a**) Schematic and (**b**) operation waveforms of the tracking reference generator.

To generate a wave tracking current $I_{sen,WT}$ and a DC current $I_{sen,dc}$ from I_{sen}, as shown in Figure 7b, the gate signal V_{sp} of M_{P6} is sent to the two sample-and-hold (S/H) circuits. When signal QB, as shown in Figure 4, changes from a low state to high state, I_{sen} starts from zero. During the rising period, I_{sen} does not reach the right level; thus, two delay signals $QB_{,d}$ and $QB_{,dB}$, as shown in Figure 4, are utilized for appropriate sampling. At the beginning of falling period for I_{sen}, QB is already in a low state; hence, no delay signal is needed. The two S/H circuits are controlled by signals $Q_{sp,B}$ and Q_{sp}, which are generated by QB and the two delay signals $QB_{,d}$ and $QB_{,dB}$. In the S/H circuits, when $Q_{sp,B}$ changes to a high state, transmission gate TG_1 is turned on, and then $V_{sp,WT}$ tracks V_{sp}. TG_1 and TG_2 are turned off and on, respectively, when $Q_{sp,B}$ and Q_{sp} are in a low and high state. Subsequently, a DC level is kept on $V_{sp,WT}$ and $V_{sp,dc}$. $V_{sp,WT}$ and $V_{sp,dc}$ are connected to the gate terminals of M_{P5} and M_{P4}, respectively. Consequently, $I_{sen,WT}$ and $I_{sen,dc}$ are produced, as shown in Figure 7b. $I_{sen,dc}$ is equal to the valley level of $I_{sen,WT}$. By subtracting $I_{sen,dc}$ from $I_{sen,WT}$, the off-time inductor current ripple is generated.

Operational amplifier OP_1, transistor M_{N1}, and resistor R_1 form a voltage-to-current circuit, and the current passing through M_{N1} is equal to V_{ref} divided by R_1. Then, through a current mirror composed of transistors M_{P1} and M_{P2}, a DC current I_{ref} is produced. To

perform current subtraction, transistors M_{N2} and M_{N4} are used. Finally, the WTR signal $V_{ref,WT}$ is realized and can be formulated as

$$V_{ref,WT} = R_2 \left(\frac{V_{ref}}{R_1} + I_{sen,dc} - I_{sen,WT} \right). \tag{12}$$

Since $I_{sen,dc}$ is equal to the valley level of $I_{sen,WT}$ and R_1 and R_2 are the same, the peak voltage $V_{ref,WT,peak}$ and V_{ref} are identical. Thus, the output DC offset is eliminated. Signal EN_{WTR} is adopted to enable or disable the function of WTR control scheme. When EN_{WTR} is in a low state, transistors M_{P3} and M_{N3} are on; hence, the WTR function is disabled and WTR signal $V_{ref,WT}$ is equal to V_{ref}. Otherwise, the WTR function is active. Compared to the VICR control, the WTR control is implemented without any low-pass filter, trimming mechanism, or off-chip components, leading to smaller chip area without an additional IC pin.

3.3. Adaptive On-Time (AOT) Circuit

For the RBCOT control, when the load current increases, the off-time period of power transistor M_P is diminished. Thus, the switching frequency is increased due to the fixed on-time period. To alleviate the variation on switching frequency in CCM in the case of load current changes, the AOT circuit is presented as shown in Figure 8a. The AOT circuit consists of a constant on-time (COT) circuit and a sink current I_2. Since only an additional current I_2 is demanded, the AOT circuit is simple and results in a small silicon area and low power consumption. For the COT circuit, I_1 is maintained constant. When signal QB changes to a low state, transistor M_{N1} and power transistor M_P are turned off and on, respectively, and then I_1 starts to charge capacitor C_1. When voltage V_{con} reaches the reference voltage V_{ref}, signal Rst is in a high state. Subsequently, transistor M_{N1} and power transistor M_P are turned on and off, respectively. Then, C_1 is discharged to zero. Until QB changes to a low state, C_1 is charged again. Hence, a constant on-time period is generated.

    (**a**)   (**b**)
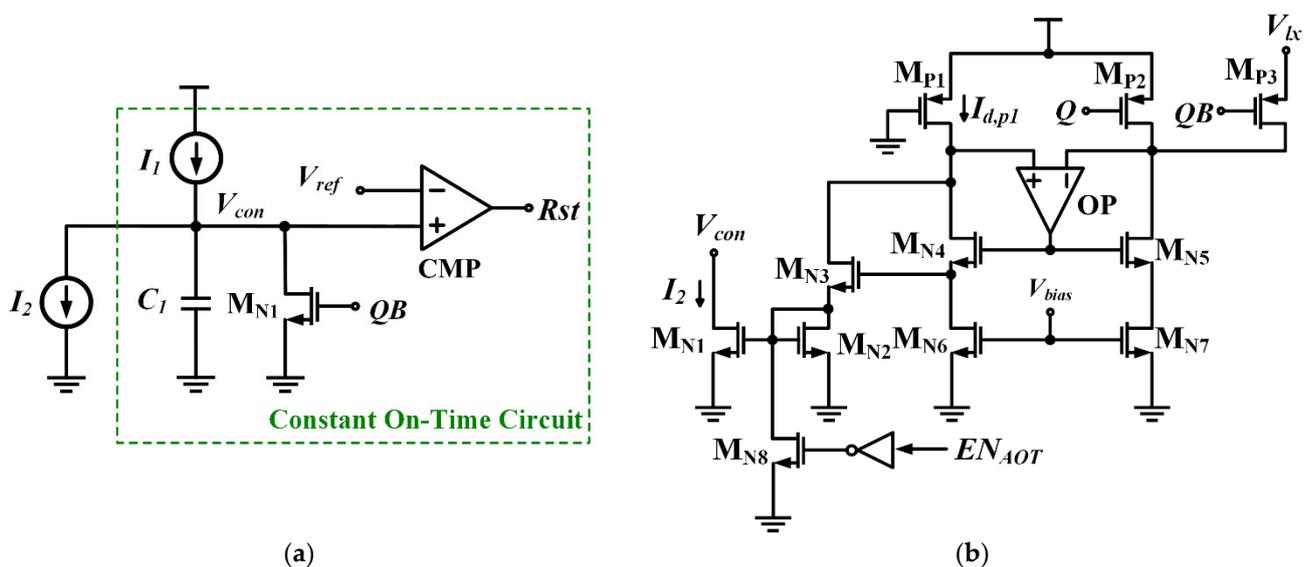
Figure 8. Schematics of (**a**) AOT circuit and (**b**) current I_2.

I_2 is proportional to the load current. When the load current increases, the charging current following through C_1 is decreased, leading to a longer on-time period. As a result, the variation in switching frequency at different load currents is suppressed. The schematic of current I_2 is shown in Figure 8b. When Q and QB are in high and low states, transistors M_{P2} and M_{P3} are off and on, respectively. Through the negative feedback loop, the noninverting pin of operational amplifier OP is equal to voltage V_{lx}. Thus, the gate,

drain, and source voltages of transistor M_{P1} and power transistor M_P are the same, and current $I_{d,p1}$ is proportional to the drain current of M_P. To ensure that most of current $I_{d,p1}$ passes through transistor M_{N3}, the current generated by transistor M_{N6} should be set small. Through transistors M_{N1} and M_{N2}, I_2 is generated. When power transistor M_P is off, transistor M_{P2} is on, and then current $I_{d,p1}$ becomes zero for power saving. When signal EN_{AOT} is in a low state, I_2 becomes zero, and the buck converter operates with COT control. Otherwise, the buck converter operates with AOT function when EN_{AOT} is in a high state.

3.4. Stablility in the WTR Control

Referring to the proposed converter in Figure 4 and the function of tracking reference generator in Figure 7, the equivalent circuit model is shown in Figure 9, which can be processed with a subtraction of two signals: one is from direct current feedback $V_{sen,WT}$, and the other is the sensed DC current information $V_{sen,dc}$ after an LPF. The current sensing gain R_{sen} is equal to kR_2, where k is a value of current mirror and R_2 is the resistance shown in Figure 7. According to the approach in [8,9], the transfer function G_{vr} of reference to output voltage is derived in Equation (13) as the on-time period is small.

$$G_{vr}(s) \approx \frac{v_o}{v_{ref}} = \frac{R_{fb1}+R_{fb2}}{R_{fb2}} \frac{1+sC_oR_{ESR}}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}}$$

$$\text{where } \omega_1 = \frac{\pi}{T_{sw}}, \ Q_1 = \frac{T_{sw}}{\left(\left(1+\frac{R_{sen}}{R_{ESR}}\right)R_{ESR}C_o - \frac{T_{on}}{2}\right)\pi} \tag{13}$$
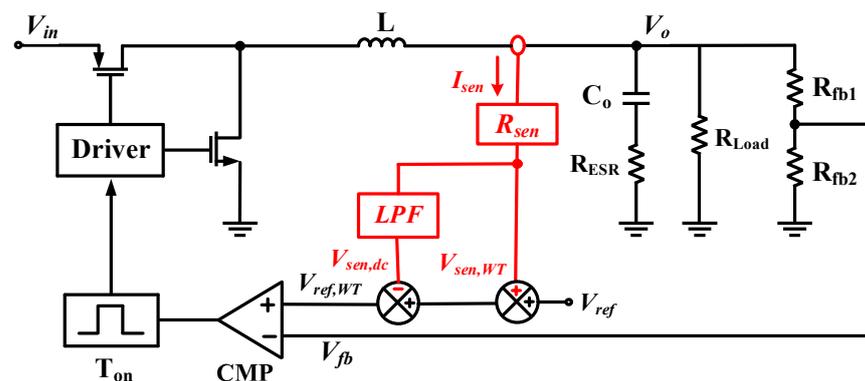
Figure 9. Linear model of the buck converter with WTR control.

To get rid of converter instability, the poles must be on the left-half plane. Thus, Equation (14) is calculated since Q_1 needs to be larger than zero.

$$R_{sen} > \left(\frac{T_{on}}{2R_{ESR}C_o} - 1\right)R_{ESR,eff}. \tag{14}$$

In the WTR control, the external current information equivalently increases the effective value of R_{ESR} by the factor of (R_{sen}/R_{ESR} + 1) to release the stability constraint of large R_{ESR} in a conventional COT converter. Without the WTR control, R_{sen} become zero. Hence, for conventional COT control, the product of the output capacitance and its ESR should be larger than half of the on-time period.

4. Experimental Results

To verify the feasibility of WTR control and AOT circuit, a laboratory prototype of the proposed buck converter was built with an input voltage of 3.3 V, output voltage of 1.8 V, and maximum output current of 500 mA. The output inductance was 6.8 μH and the output capacitor was a 10 μF MLCC with an ESR of 4 mΩ. The proposed buck converter was fabricated with a standard 0.35 μm CMOS process. The chip microphotograph is shown in Figure 10, and its core area was $837 \times 915 \ \mu m^2$. Figure 11 shows the simulated waveforms

of the tracking reference generator. The sensing inductor current I_{sen}, waveform tracking current $I_{sen,WT}$, DC current $I_{sne,dc}$, and WTR signal $V_{ref,WT}$ can be found in Figure 7. When signal EN_{WTR} was in a high state, the tracking reference generator was enabled. It can be noted that current $I_{sen,WT}$ and current $I_{sne,dc}$ were the same during on-time periods. There were spikes in signal $I_{sen,WT}$ due to the operation of the S/H circuits, but these spikes did not affect the WTR control operation. The waveforms coincided with the circuit analysis in Section 3.2.
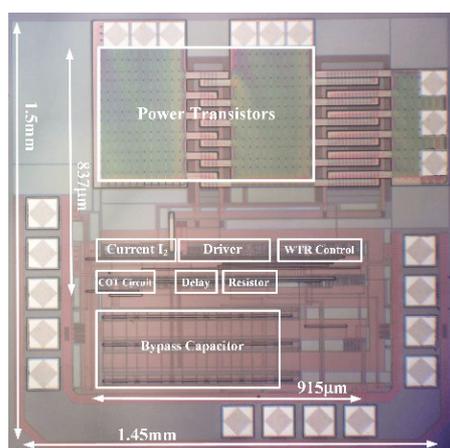
Figure 10. Chip microphotograph.
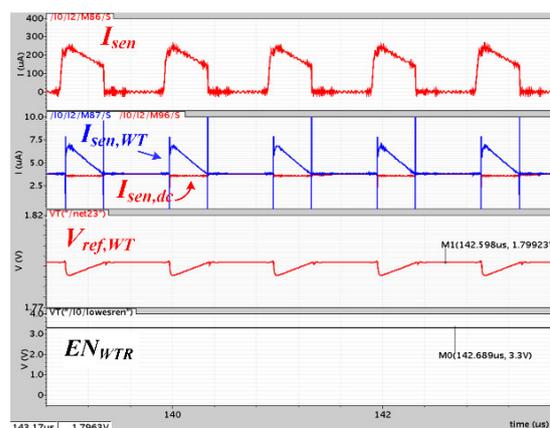
Figure 11. Simulated waveforms of the tracking reference generator.

Figures 12 and 13 show the measured waveforms of the buck converter with the WTR control at load currents of 100 and 500 mA, respectively. The output voltage of the buck converter was kept at 1.8 V, and the output voltage ripple ΔV_o was as small as 3 mV. This means that the WTR control could ensure the stability of the buck converter with ripple base control. Figure 14 plots the measured output DC offset with the proposed control when the load current changed from 50 mA to 500 mA. The maximum DC offset of the proposed converter was 4.1 mV. Figure 15 shows the measured transient waveforms of the proposed buck converter for the load current changing between 450 mA and 50 mA. For a step-down load, the proposed buck converter took 4 μs to resume its regulated value with a transient ripple of 50 mV. Furthermore, the output voltage levels at two different load currents were the same. The recovery time and transient ripple of the buck converter were 9 μs and 100 mV for a step-up load.

(**a**)　　　　　　　　　　　　　　　　(**b**)
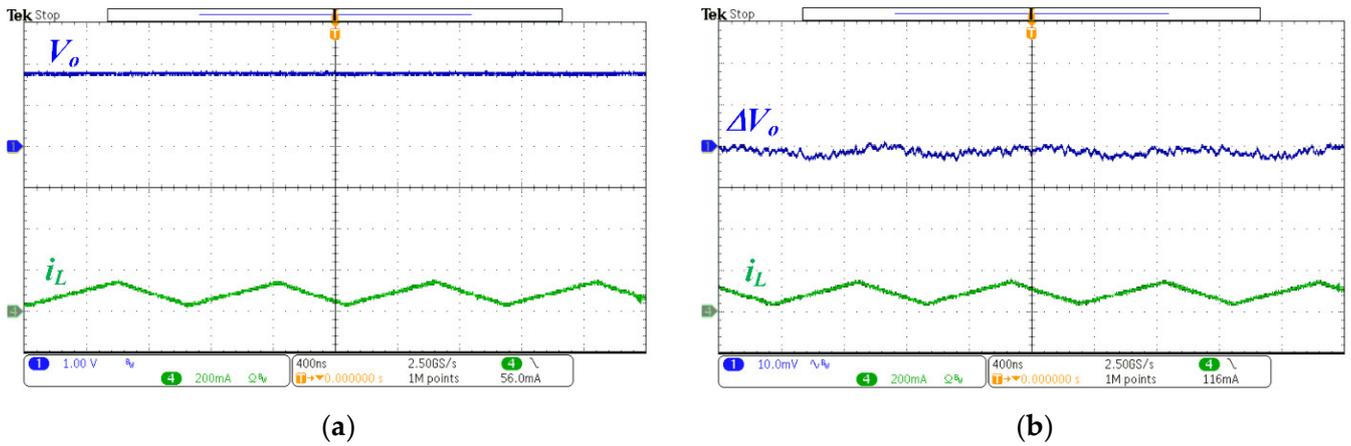
Figure 12. Measured waveforms with WTR control for (**a**) output voltage and (**b**) output voltage ripple at load current of 100 mA.

(**a**)　　　　　　　　　　　　　　　　(**b**)
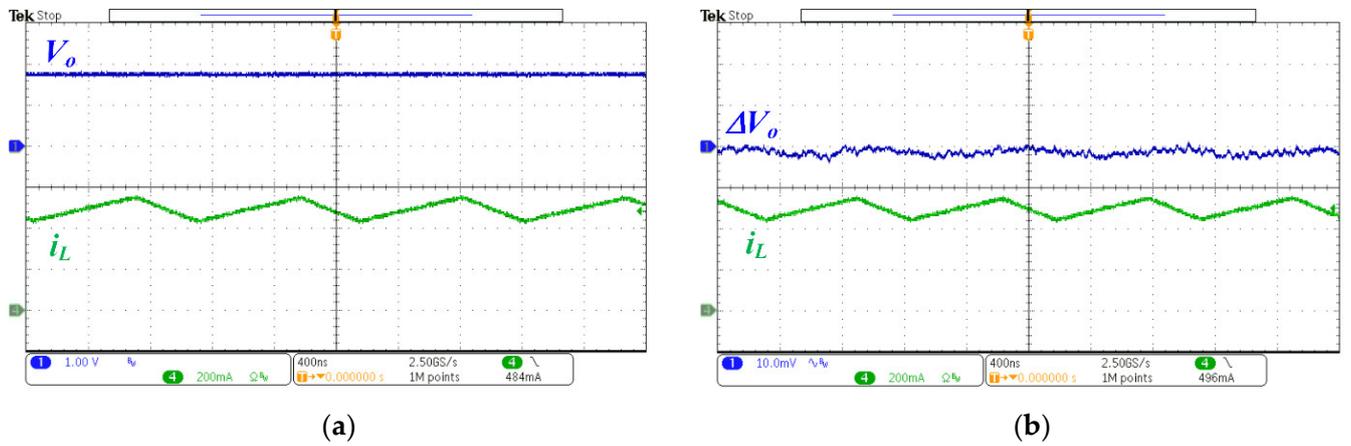
Figure 13. Measured waveforms with WTR control for (**a**) output voltage and (**b**) output voltage ripple at load current of 500 mA.
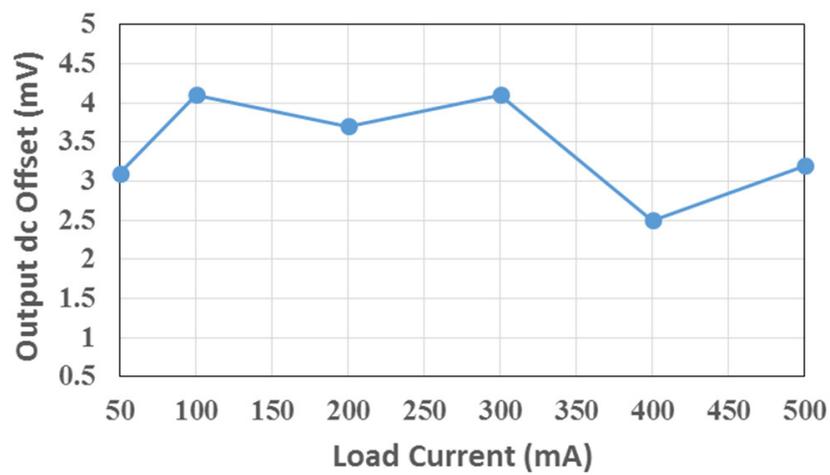
Figure 14. Output DC offset versus different load currents.

(**a**) (**b**)
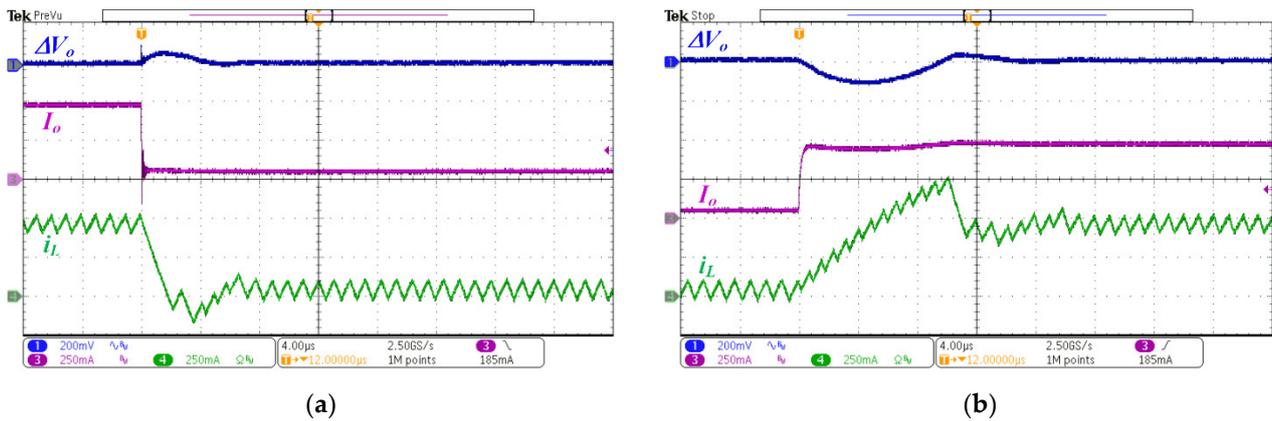
Figure 15. Measured transient waveforms of the proposed buck converter for (**a**) step-down and (**b**) step-up loads.

Figure 16 plots the switching frequency of the buck converter versus load currents without and with AOT function. It can be found that the differences in switching frequency without and with AOT function were about 79 kHz and 11 kHz, respectively. The switching frequency with AOT control was kept approximately constant at different load currents. Figure 17 plots the measured efficiency of the proposed converter when the load current changed from 50 mA to 500 mA. The maximum efficiency of the proposed converter was 90.9% at a load current of 200 mA. A comparison of results with previously proposed on-time controlled buck converters is summarized in Table 1. The performance of f_{sw} variation is indicated by ($\Delta f_{sw}/f_{sw}$) and ($\Delta f_{sw}/\Delta I_{\mathrm{Load}}$). The performance of the proposed buck converter was comparable to those with different control techniques.
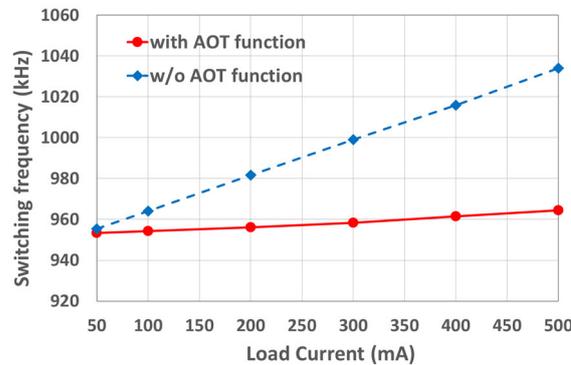
Figure 16. Switching frequency versus different load currents with and without AOT function.
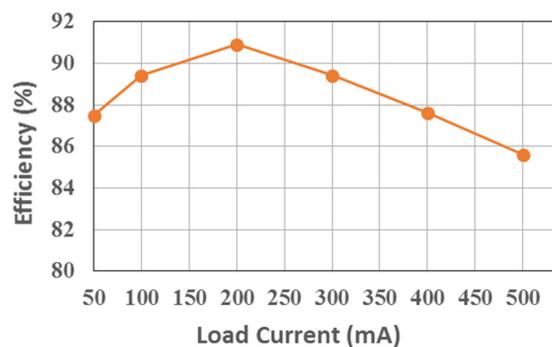
Figure 17. Efficiency versus different load currents.

Table 1. Comparison of reported on-time controlled buck converters.

	[9]	[12]	[16]	[22]	This Work
Control scheme	COT	AOT	AOT	COT	AOT
Process	28 nm	0.18 μm	0.18 μm	0.5 μm	0.35 μm
Input voltage (V)	3.3	3.3	2.7~3.6	12	2.5~3.6
Output voltage (V)	1.05	1.2	1~1.2	1.04	1.8
Inductor (μH)	1	4.7	N/A	2.2	6.8
Capacitor (μF)	4.7	8.9	N/A	88	10
Switch frequency (kHz)	2500	750	100	400	960
Output voltage ripple (mV)	6	1	N/A	8	3
Offset (mV)	4	N/A	N/A	2	4.1
Load transient step (A)	1.4	0.745	0.7	2.8	0.45
Recovery time (μs)	4	3.6	7.8	28	4
Peak efficiency	94%	87%	88.2%	92.3%	90.9%
Switch frequency variation (Δf_{sw}) (kHz)	N/A	84	52	N/A	11
$\Delta f_{sw}/f_{sw}$	N/A	11.2%	5.2%	N/A	1.1%
Load current range (ΔI_{LR})	N/A	0.65 A	0.9 A	N/A	0.45 A
$\Delta f_{sw}/\Delta I_{LR}$ (kHz/A)	N/A	129	57.8	N/A	24.4

5. Conclusions

An RBCOT buck converter with VICR control can relax the stability constraint of a large ESR at the output capacitor, but the output regulation accuracy is degraded due to output DC offset. Moreover, the switching frequency of the RBCOT buck converter varies with load current changes. Therefore, in this paper, WTR control was proposed for MLCC to improve converter stability while eliminating DC offset on the regulated output voltage. The WTR control was implemented without any low-pass filter, trimming mechanism, or off-chip components compared to the VICR control. Since the AOT circuit was utilized to suppress the switching frequency variation in CCM at different load currents, even without clock-controlled circuits, the buck converter operated with a nearly constant switching frequency. The test chip was fabricated in a 0.35 μm CMOS process for validation. The experimental results showed that the maximum output DC offset was 4.1 mV and the output voltage ripple was as small as 3 mV, while the recovery times were 4 μs and 9 μs for step-down and step-up loads. Furthermore, the switching frequency variation was 11 kHz when load current changed from 50 mA to 500 mA, and the measured maximum efficiency was 90.9%.

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